Freescale Semiconductor, Inc.

Application Note AN2048

Emulator Considerations When Designing with the MPC8xx

NCSD Applications
Freescale, Austin, Texas

Introduction

When attaching an emulator to the MPC8xx, some emulator specific considerations are called for. These can in some cases be generic recommendations, but in certain cases will be unique to the emulator you have chosen. In all cases, refer to your specific supplier for their latest requirements.

The following information was provided by the emulator companies noted, and does not constitute an endorsement by Freescale. This information is provided as a warning and convenience to our customer, but in all cases, verify with the emulator supplier you have selected for the most up to date needs they have.

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Applied Micro Systems (AMC)

- When a Applied Microsystems Corporation (AMC) SuperTAP is connected using the mirror or LSA connection method, the SuperTAP uses the JTAG lines and uses the alternate set of DPI control lines. Therefore, JTAG lines are not available.

- When the AMC SuperTAP is connected using the direct chip replacement method, SuperTAP uses the normal DPI lines to control its processor.

- When using the AMC SuperTAP and to avoid conflicts between the DPI and JTAG lines we recommend removing the JTAG lines from the circuit with SuperTAP installed, or making the processor the first device in the scan chain and allow no other device to drive the Transfer Data Out (TDO) signal.

- It may be necessary to isolate the TDI line to prevent the SuperTAP from driving into the target scan chain and confusing other devices downstream.

- It may be necessary to pull the TRST* line to all other devices controlled by the SuperTAP to ground. This should assure a floating TDI signal will not cause false transitions to be clocked into the other devices.

Embedded Support Tools (EST) MPC8xx and EST's VisionICE

VisionICE 10 Pin BDM Support

Reset Configuration Issues:

- Actively drive the DBGC (D9,D10) and DBPC (D11,D12), Hard Reset Configuration bits onto the bus to select the Multifunction I/O pin selection for target and Development Port. The values required to be driven onto these pins are based on the signals that have been routed to the 10 pin BGND connector.

- There are two BDM "Freeze " signal schemes. Motorola's, Option A is recommended by EST but, Option B is also supported for 10-pin BDM functionality. Option B is used as an alternative typically when target design uses PCMCIA Port B to eliminate pin conflicts on the " Freeze " signal. Option B requires that the FRC bit in the SIUMCR = 0.

  Option A: (DBGC=3 DBPC=0 and MPC860 signal names used for example)

Pin 1 = IPB0/IWP0/VFLS0	Pin 2 = /SRESET (unused by EST)
Pin 3 = GND	Pin 4 = DSCK/TCK
Pin 5 = GND	Pin 6 = IP_B1/IWP1/VFLS1
Pin 7 = /HRESET	Pin 8 = DSDI/TDI
Pin 9 = VOD(unused by EST)	Pin 10 = DSDO/TDO

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Option B: (DBGC = 0 or 1 and FRC = 0)

Pin 1 = FRZ//IRQ6	Pin 2 = /SRESET (unused by EST)
Pin 3 = GND	Pin 4 = DSCK
Pin 5 = GND	Pin 6 = FRZ//IRQ6
Pin 7 = /HRESET	Pin 8 = DSDI
Pin 9 = VOD (unused by EST)	Pin 10 = DSDO

- Physically locate the 10 pin connector as close as possible to the processor to minimize trace length and cross coupling of noise onto the BDM signals. Do not run high speed clocks or signals adjacent to the BDM communication signals.

- Ensure that the emulator (10-pin BGND pin 7, /HRESET) is connected directly the /HRESET signal of the processor. This will provide the ability for the emulator to drive and sense the status of / HRESET. The target design should only drive the /HRESET with open collector, open drain type devices. Note: /HRESET should not be tied to /PORESET. (The emulator drives the /HRESET and DSCK to enable BDM operation.)

- To guarantee that JTAG Mode is not accidentally invoked, connect a pull down (~ 10K) resistor on the /TRST signal and a pull-up (~10K) on the TMS signal. When the MPC's development port (BDM) is used, JTAG functionality is disabled. Designs that require both should have a Reset configuration scheme to support the two modes.

VisionICE Event System ,Trace Support (Optional Target Connection)

- The VisionICE Event System requires some of the multifunction MPC860 signals to function in a particular pin configuration modes. This pin configuration will provide detailed information on the processor's code execution when cache is enabled and disabled. Follow the 10-pin BDM recommendations listed previously for Option A plus specific pin assignments.

- The Hard Reset Configuration should actively drive the DBGC and DBPC to specific values. DBGC=3 - Configures the multifunction pins to function as VFLS0, VFLS1, VF0, VF1, VF2, / STS, AT0, AT1, AT2, AT3, OP3. DBPC= 0 - Configures the TCK/DSCK = DSCK, TDO/DSDO = DSDO, TDI/DSDI = DSDI. It's recommended to actively drive ALL signals of the Hard Reset Configuration word since, other physical connections will be made to the Data Bus when using EST's POD.

- The VisionICE Event System requires a processor CLKOUT for tracing Bus Cycles.Verify that the value in the SCCR (Bits 1 and 2) register are not disabling the CLKOUT from the processor.

- An electrically clean CLKOUT signal is required by the VisionICE Event System. The Clockout must be electrically connected to or a direct copy of MPC Clockout.. If re-driven, the Clockout must be generated via low skew zero propagation delay circuit (i.e. PLL Clock Driver). Typically, internal clock speed should be designed (and configured) to match external bus clock speed for optimum Event & Trace functionality. Contact EST for target designs employing split bus speeds.

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General Physical Connection Considerations for EST

- Connection between the VisionICE Event System and the Target's MPC8xx is done in one of two ways. Other than the signals for BDM connection (Option A above.), the emulator also needs direct physical connection to the MPC's external Address, Data and Control pins. This can be accomplished by one of two methods. The first is to socket the MPC8xx processor and connect to the VisionICE to the socket using EST's Target Adapter product. The second and more convenient method is to design EST's recommended 80 pin connectors into the target design, thus eliminating the need for processor socketing. It's best to contact EST for this type of connection prior to designing the Target.

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