Workstation Architecture

by R. Belleville, Mgr. Advanced Design

1. Workstation Requirements and Goals
2. Discussion of alternative approaches
3. The concept of a synchronous multi-tasking processor
4. The Dandelion Workstation
5. The Cub Workstation

Star Workstation Constraints

1. Support large format display (1024x808)

2. Support Ethernet communication

3. Support high performance rigid disks

4. Support Low Speed Electronic Printer

5. Support Mesa Emulation

6. Support a number of slow devices

Star Workstation Design Alternatives

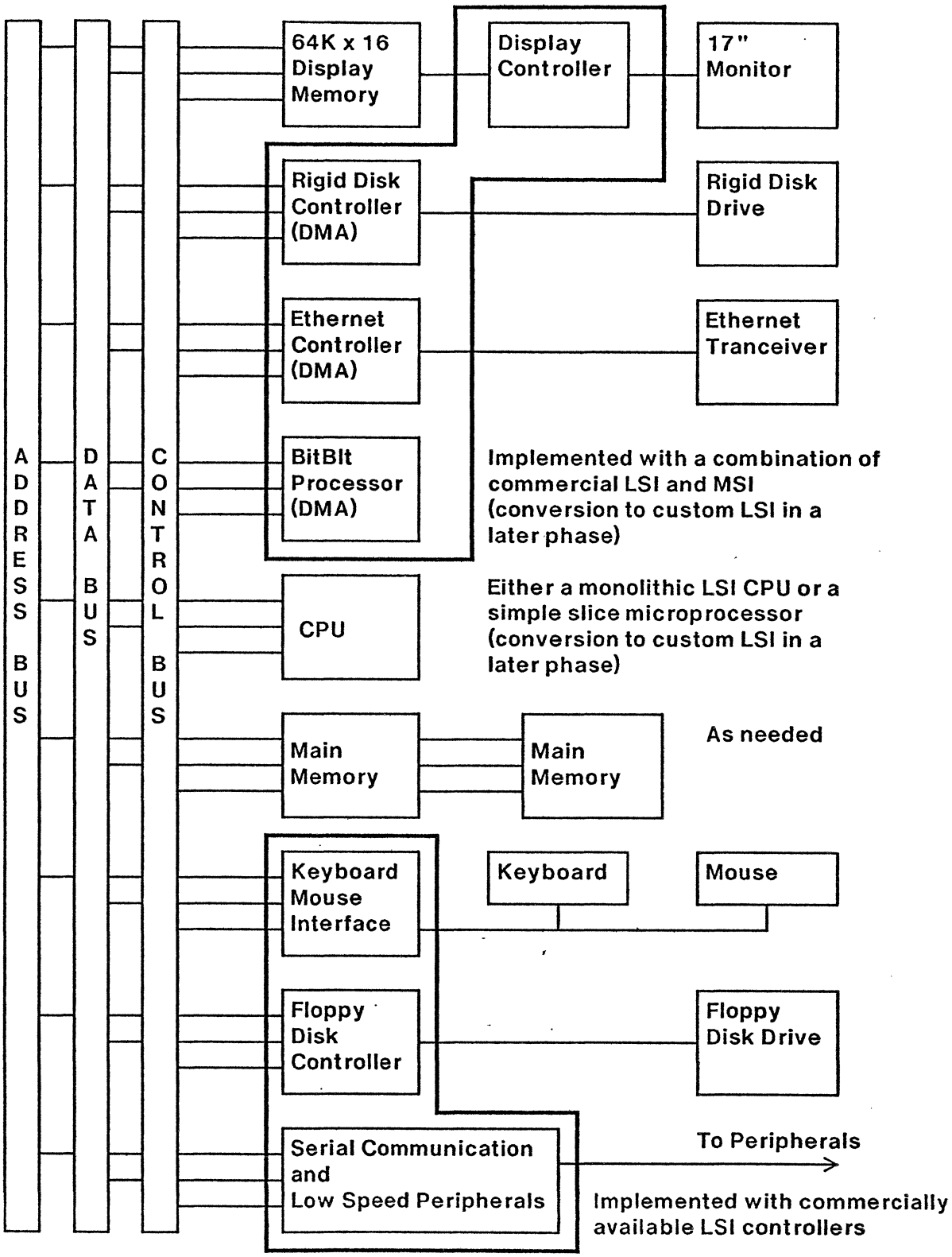
1. Commercial LSI Microprocessors

2. Bus-Organized Distributed Systems

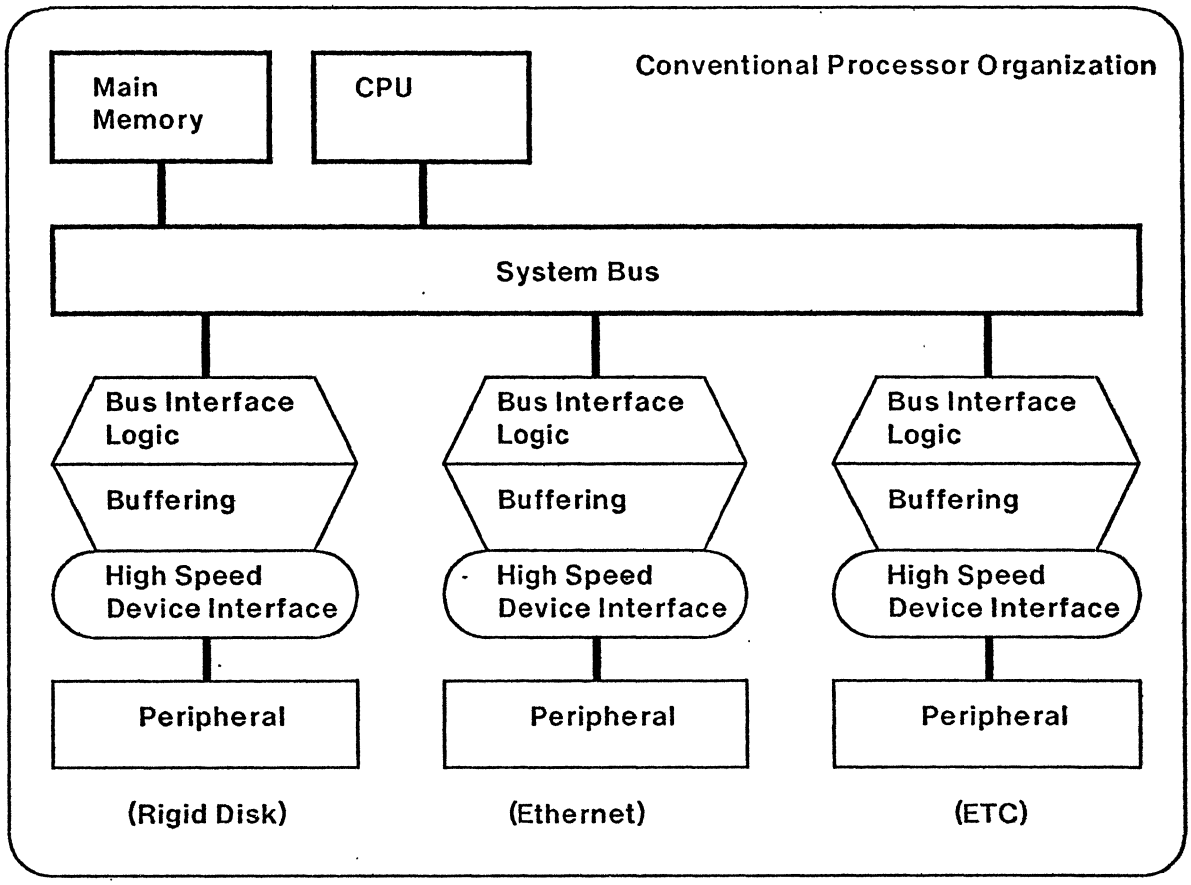
3. Custom LSI

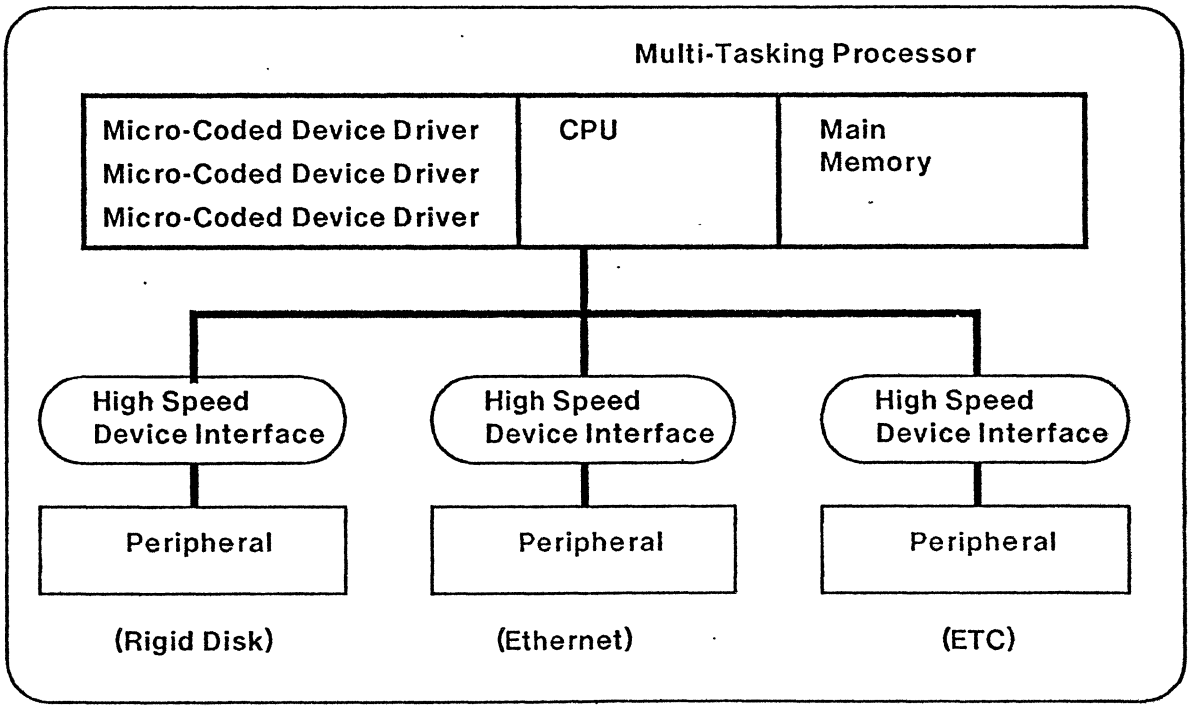
4. Synchronous Multi-Tasking Microprocessors

ws-alternatives.bravo



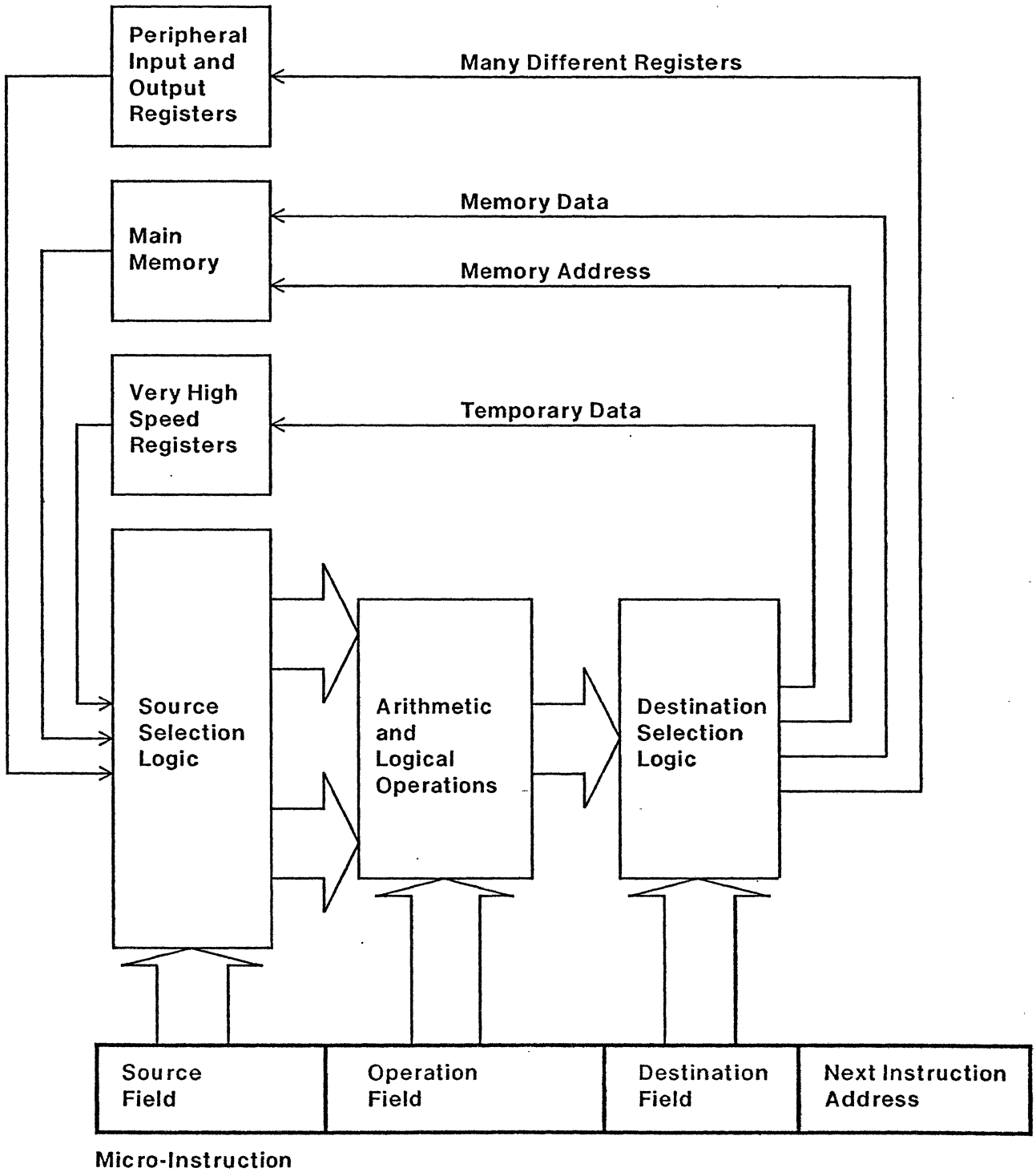
Bus Organized Workstation Microprocessor busorg.sil



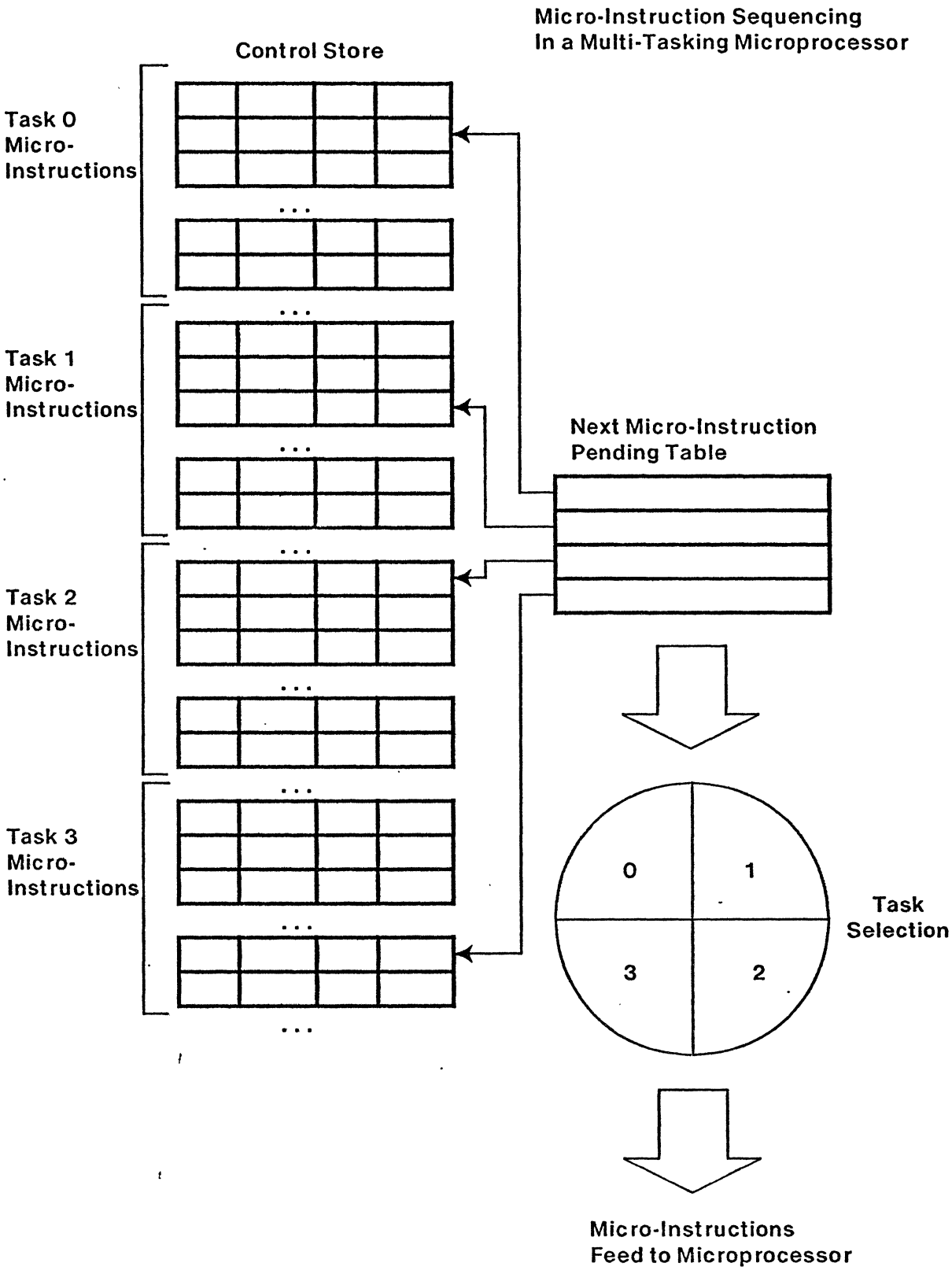


Multi-Tasking.sil

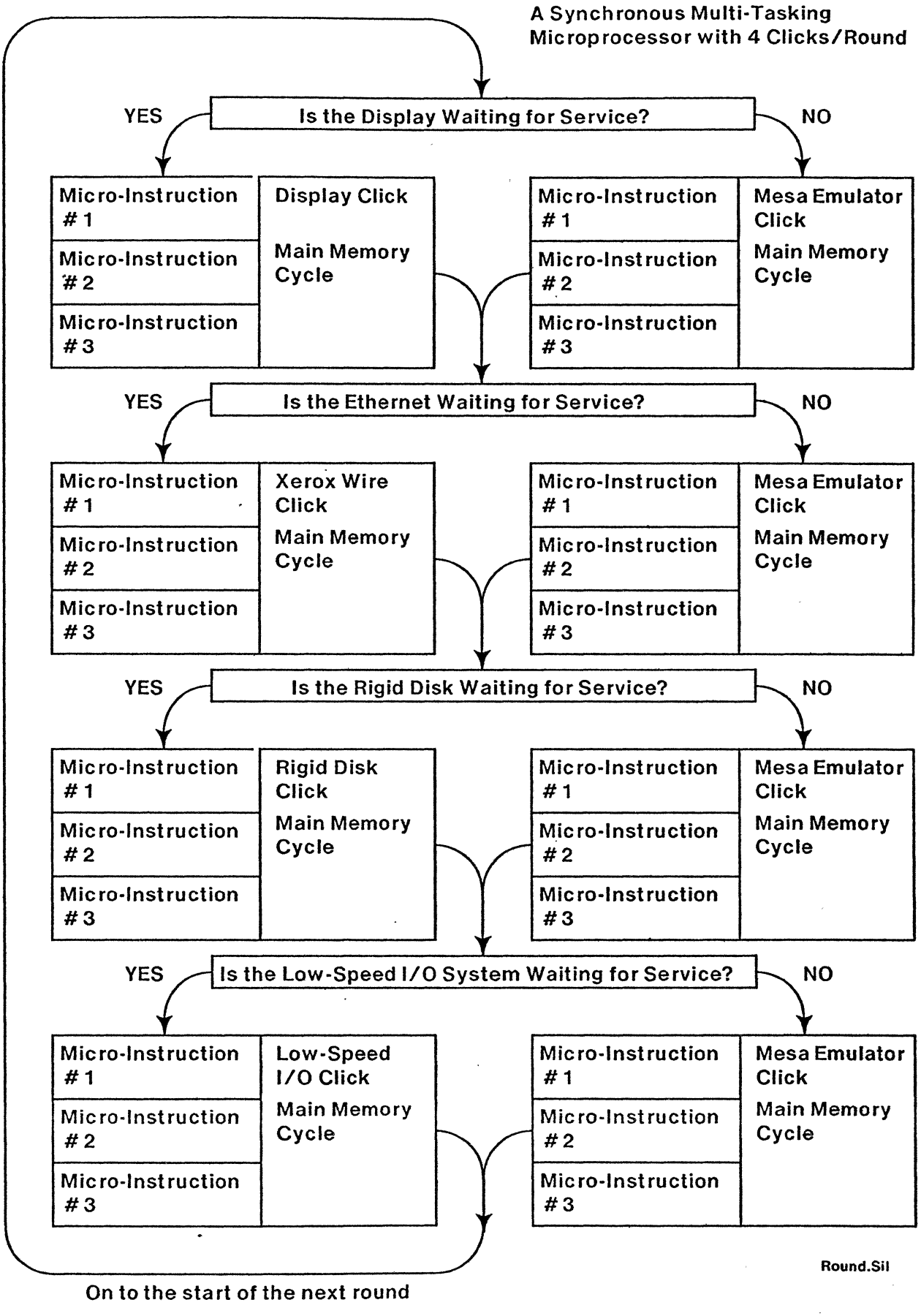
What Effect Micro-Instructions have on Microprocessors



micro-effect.sil



Micro-Sequence.sil


A Synchronous Multi-Tasking
Microprocessor with 4 Clicks/Round
Is the Display Waiting for Service?
YES
NO
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Display Click
Main Memory Cycle
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Mesa Emulator Click
Main Memory Cycle
Is the Ethernet Waiting for Service?
YES
NO
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Xerox Wire Click
Main Memory Cycle
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Mesa Emulator Click
Main Memory Cycle
Is the Rigid Disk Waiting for Service?
YES
NO
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Rigid Disk Click
Main Memory Cycle
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Mesa Emulator Click
Main Memory Cycle
Is the Low-Speed I/O System Waiting for Service?
YES
NO
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Low-Speed I/O Click
Main Memory Cycle
Micro-Instruction #1
Micro-Instruction #2
Micro-Instruction #3
Mesa Emulator Click
Main Memory Cycle
Round.Sil
On to the start of the next round

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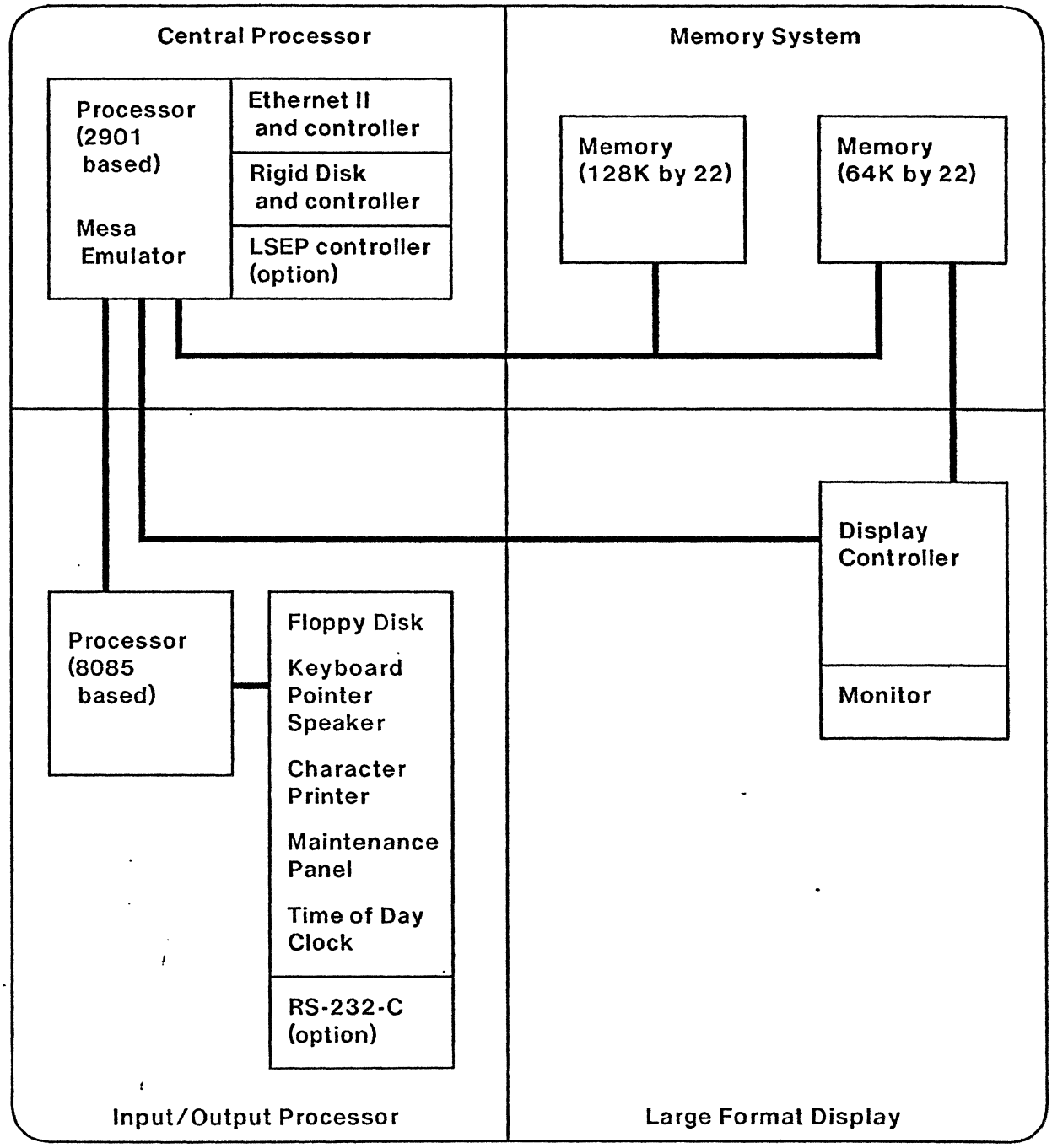
The Dandelion System



February 26, 1980
DandeLion-Block.sil
RLB

Workstation Configuration

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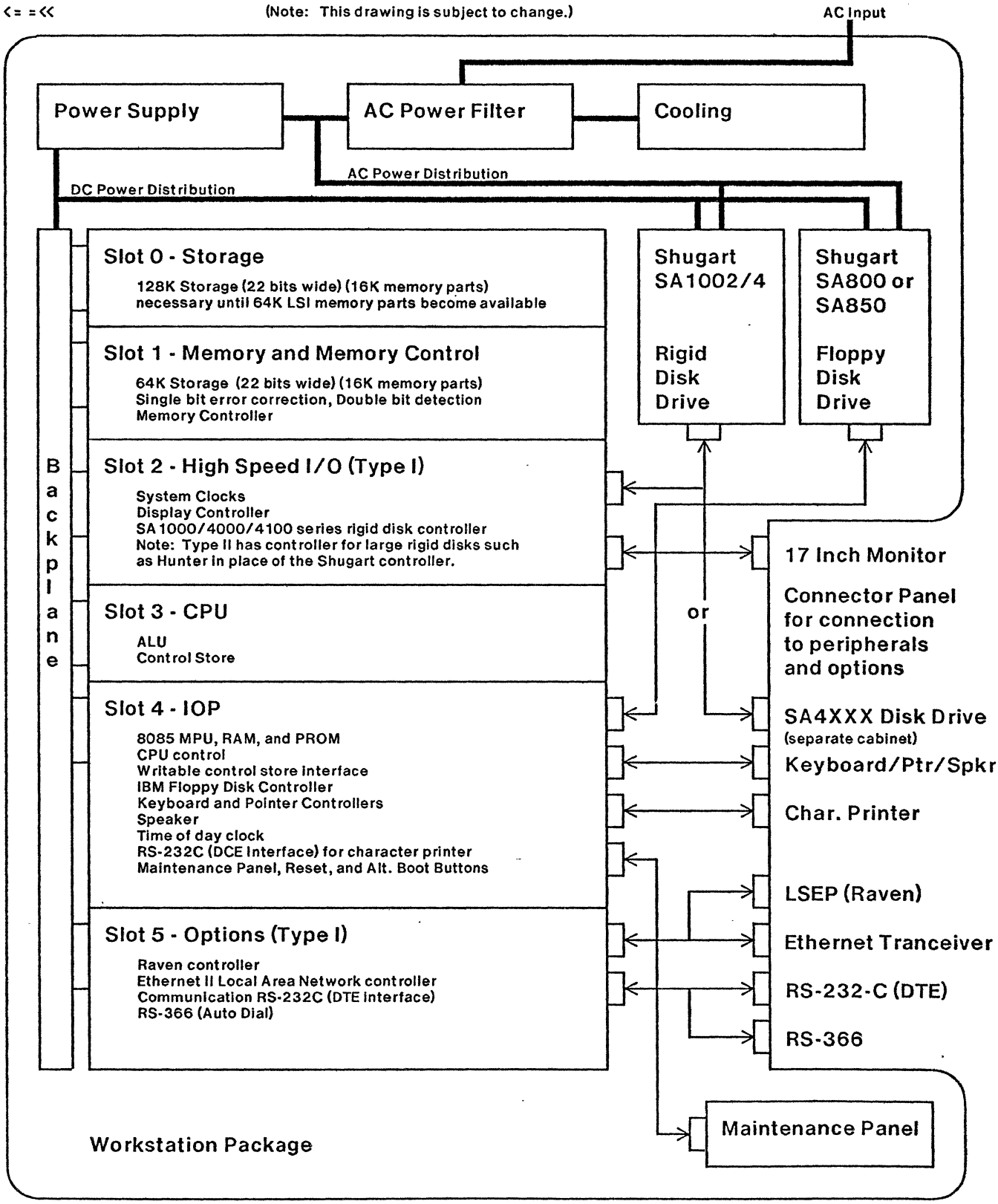
(Note: This drawing is subject to change.)



February 26, 1980
Logic-Configuration.Sil
RLB

Dandelion Chip Count

1. Memory and Memory Control

   Ram 88, Other 70, Total 158

2. 128K Storage

   Ram 176, Other 26, Total 202

3. Central Processor

   Control store 49, Other 118, Total 167

4. Input/Output Processor

   Ram 32, Prom 4, Floppy 27, Kbd 12, Other 88, Total 163

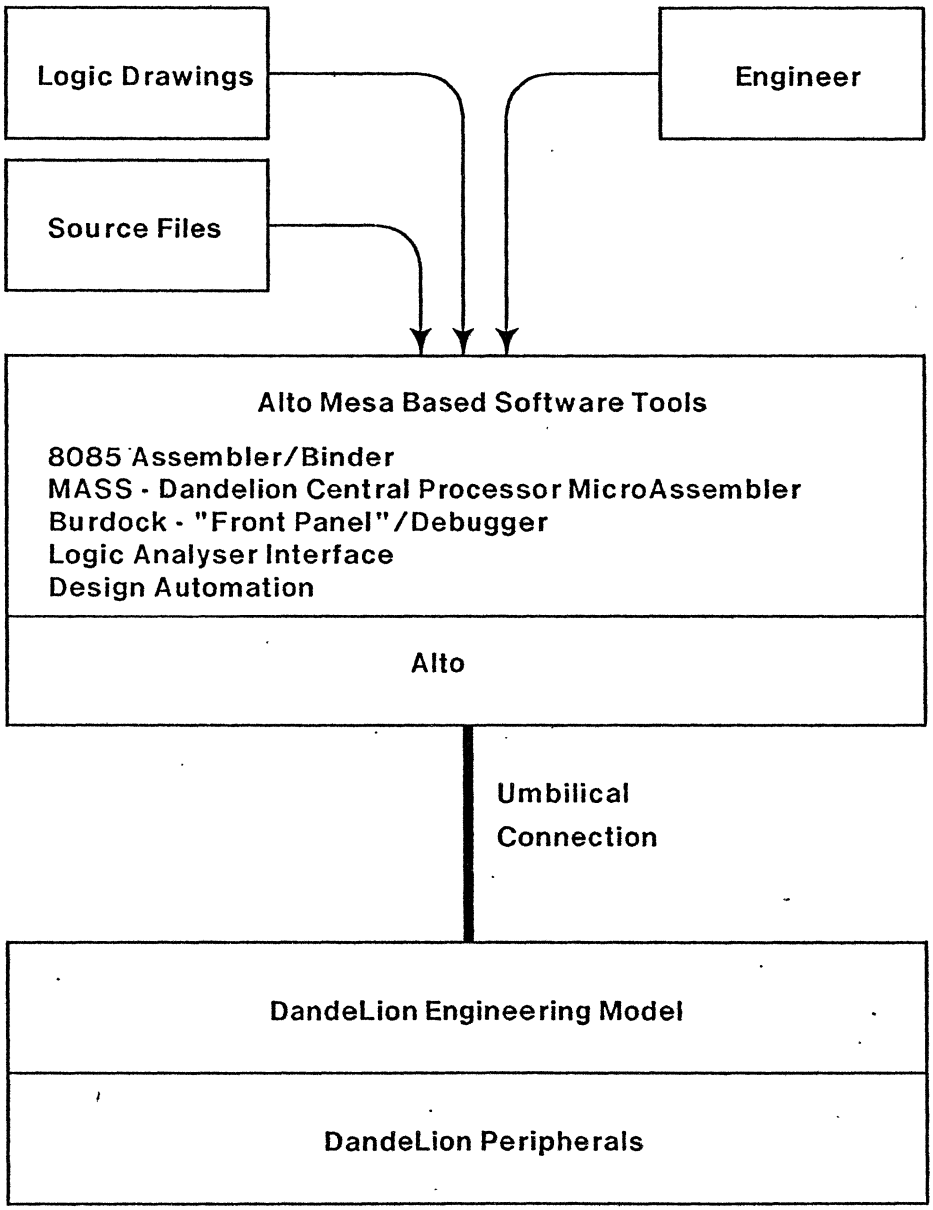
5. High Speed I/O

   Clocks 19, Display 56, Disk 65, Total 140

6. Option Type I

   RS232 & LSEP 39, Ethernet (est) 55, Total 94

Workstation Development Environment



WS-Development.sil

Workstation Design's
Tasks

Bob Garner	**ALU Desgin, Emulator microcode**
Don Charnley	
Ron Crane	**Memory system, Display controller, related microcode**
Dan Davies	**Disk Controllers, Xerox Wire Controller**
Roy Ogus	**Xerox Wire microcode**
Dick Snow	**Development tools environment**
Don Charnley	**Microassembler**
Jim Frandeen	**Micorassembler**
Pat Olmstead	**LSEP interface microcode, printing application w/ Dandelion**
Pitts Jarvis	**LSEP controller**
Roy Ogus	**IOP**
Neil Hansen	**Model building, logics**
Jim Cucinitti	
Jim Peterson	**Diagnostics and Field Service**
Bob Belleville	**Everything else**

The Dandelion Empire

TPM		Hal Lazar/ Hans Scharmann	EL Segundo
Industrial Design		Robin Kincaid/ Claude Hutcheson	Dallas
Package		Dick Hanson & Allen Bell	Dallas
Power Supply		Avi Kandola	EL Segundo
PWBA Manufacture		ED	EL Segundo
Conponent Qual		ED	EL Segundo
Other Engineering Support		ED	EL Segundo
Manufacture		Bill Powers	Dallas
Field Service		Art Johnson	EL Segundo
LSEP	TPM	John Michell	EL Segundo
	ROS	Joe Hruchak et al	Webster
	Engine	John Forester et al	Webster

I am sure there are more I haven't found yet.

dandelion-empire.sil

Workstation Design's
Tasks

Tom Chang	Ethernet support
Don Charnley	Microassembler, Design review
Jim Cucinitti	Memory system mechanization, Tech. Support
Ron Crane	Memory system, Display controller, related microcode
Dan Davies	Disk Controllers
Bob Garner	ALU Desgin, Emulator microcode, Ethernet controller
Neil Hansen	Model building, Tech. Support
Pitts Jarvis	Development tools (Burdock), LSEP controller
Roy Ogus	IOP, IOP software, Maintenance panel
Pat Olmstead	LSEP interface microcode, printing application w/ Dandelion
Dick Snow	Development tools environment
Ken Yamanaka	RS-232 controller
Bob Belleville	Everything else
Kaz Mass	Purchasing / Expedite

wd-tasks.sil
August 7, 1980

Development Time Schedule

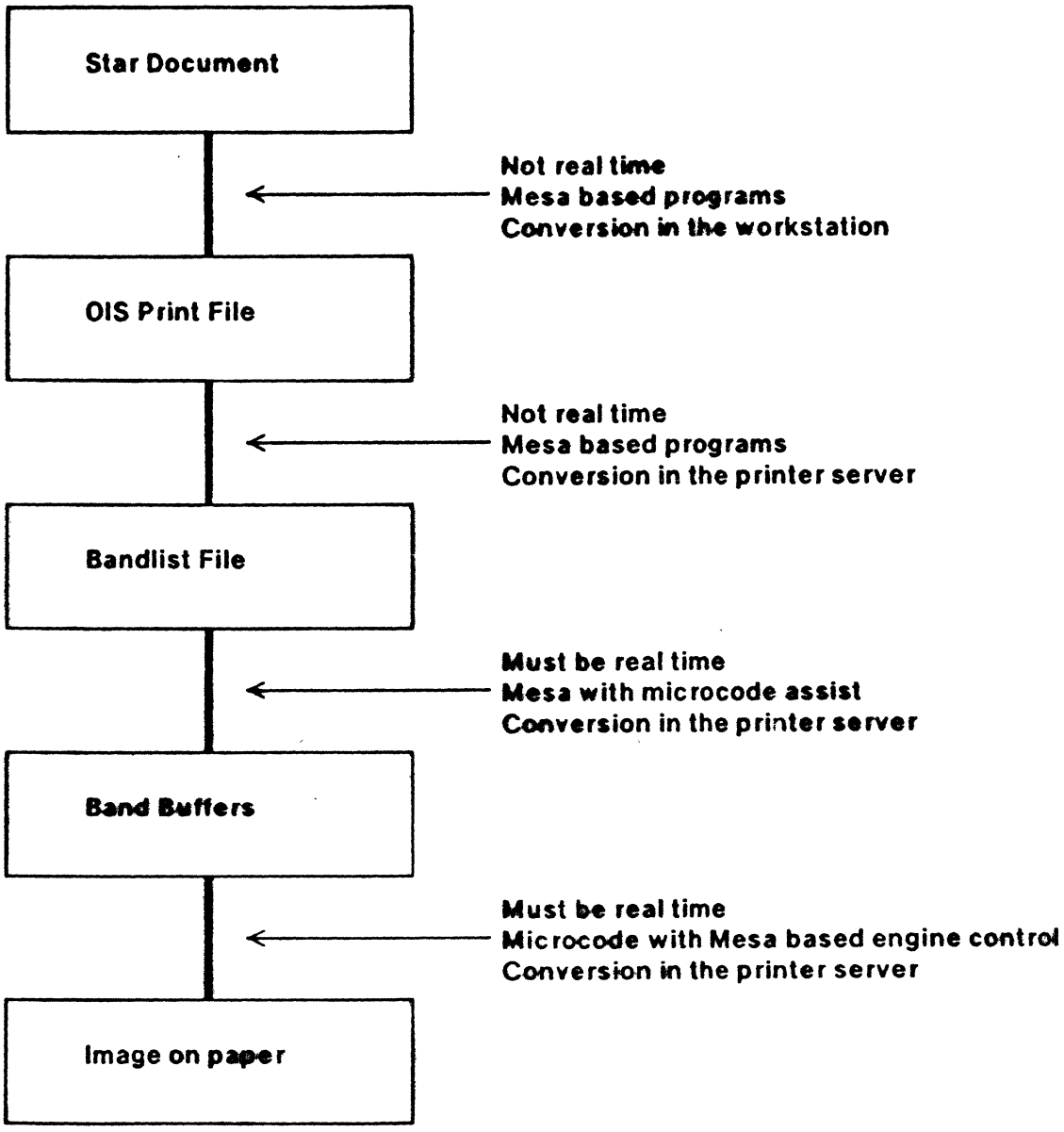
1978	4th Quarter	October Study
1979	1st Quarter	February Study Begin design
	2nd Quarter	IOP up
	3rd Quarter	CP up Tools up
	4th Quarter	Display up Microcode based example programs
1980	1st Quarter	Disks up Logic design to mechanization
	2nd Quarter	Mesa up Some first etch under test
	3rd Quarter	Pilot up 3 EMs up
	4th Quarter	PPMs (6) Servers to field (2?)
1981	1st Quarter	200 machines
	2nd Quarter	
	3rd Quarter	1000 - to 1800 machines
	4th Quarter	

wd-timeline.sil
August 7, 1980

Dandelion/LSEP System Concept

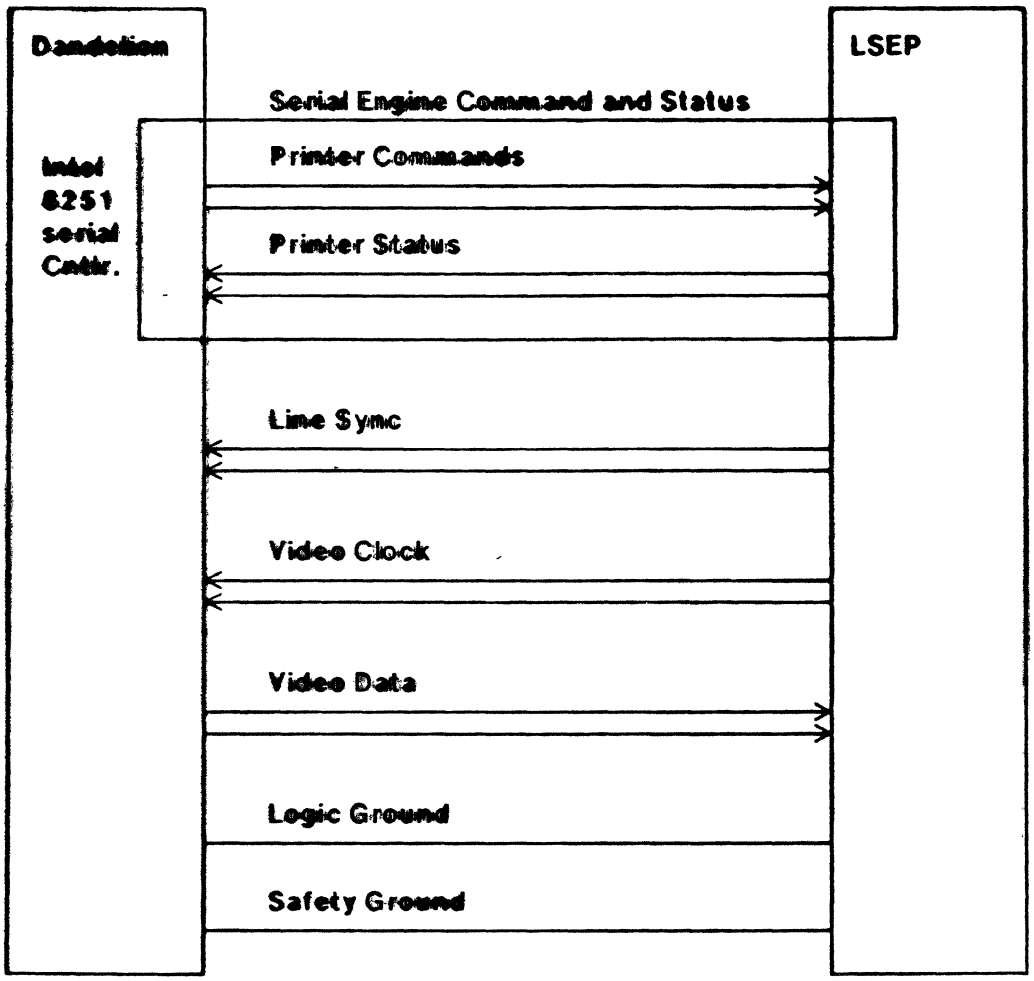
LSEP-Concept.all
RLB 14 Nov 80

1. Minimum hardware
2. Microcode to simulate the "Alto/Orbit"
3. Use whole machine during printing
4. Very limited bandwidth to the printer



Dandelion/LSEP Interface

LSEP-Interface.sil
RLB 14 Nov 80



All are ECL balanced pairs

Receivers are MC10125
Transmitters are MC10124

MSEP should be the same; however, a Page Sync may have to be added to insure page registration.