

ALTOII MEMORY

ADDRESS MAPPING

The mapping of addresses to memory chips can be altered by the setting of the "memory configuration switch". This switch is located at the top of the backplane of the AltoII. If the switch is in the alternate position, the first and second 32K portions of memory are exchanged.

The AltoII memory system is organized around 32-bit doublewords. Stored along with each doubleword is 6 bits of Hamming code and a Parity bit for a total of 39 bits:

bits 0-15	even data word
bits 16-31	odd data word
bits 32-37	Hamming code
bit 38	Parity bit

Things are further complicated by the fact that two types of memory chips are used: 16K chips in machines with extended memory and 4K chips for all others.

The bits in a 1-word deep slice of memory are called a group. A group contains 4K or 16K doublewords, depending on the chip type. The bits of a group on a single board are called a subgroup. Thus a subgroup contains 10 of the 40 bits in a group. There are 8 subgroups on a memory board. Subgroups are numbered from the high 3 bits of the address: for 4K chips this means MAR[0-2]; for 16K chips (i.e., an Alto with extended memory) this means BANK.MAR[0]:

Subgroup	Chip Positions	
7	81-90	
6	71-80	
5	61-70	
4	51-60	
3	41-50	
2	31-40	
1	21-30	
0	11-20	Nearest the edge connector

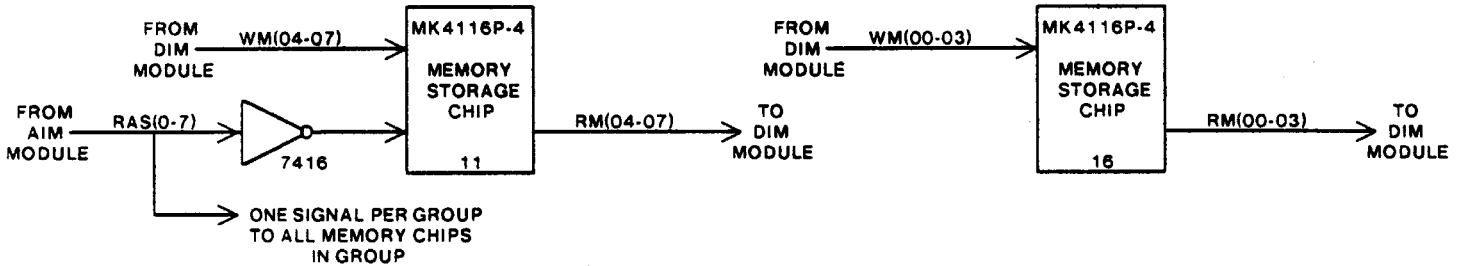
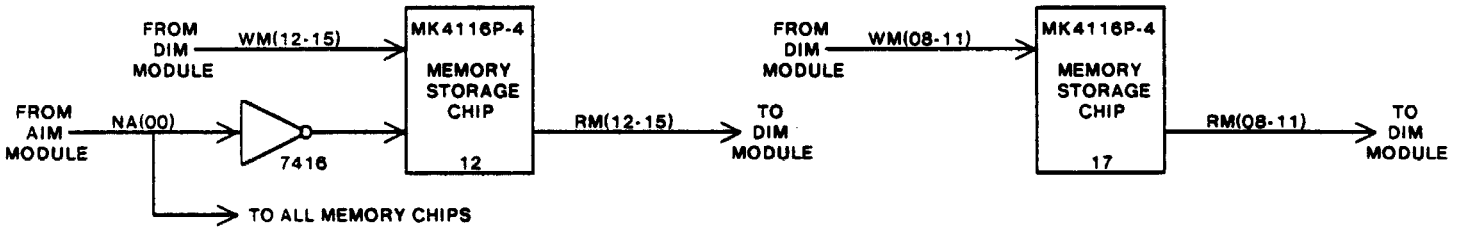
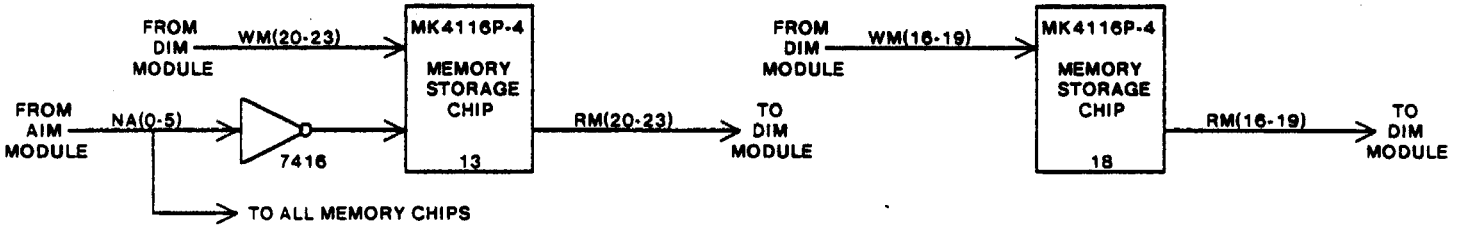
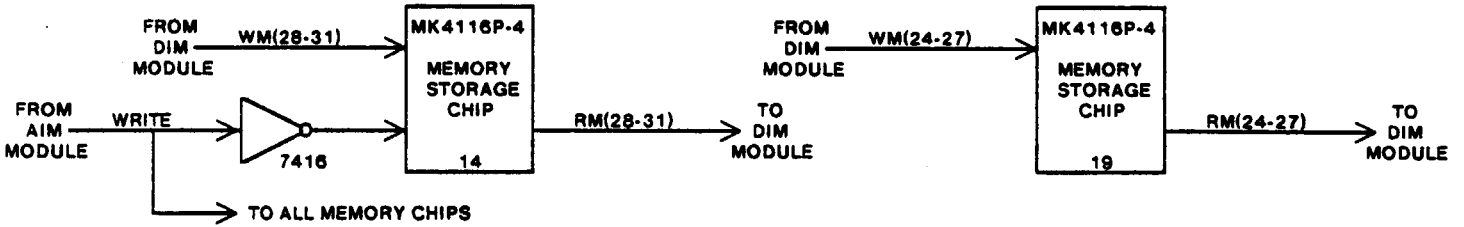
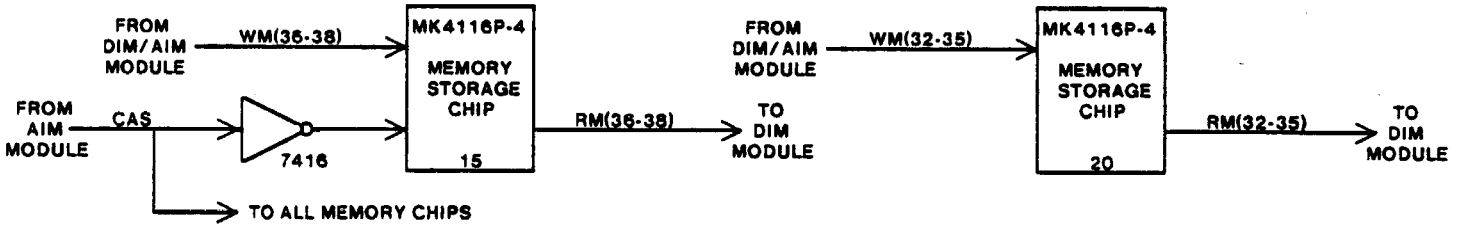
The location of the bits in group 0 is:

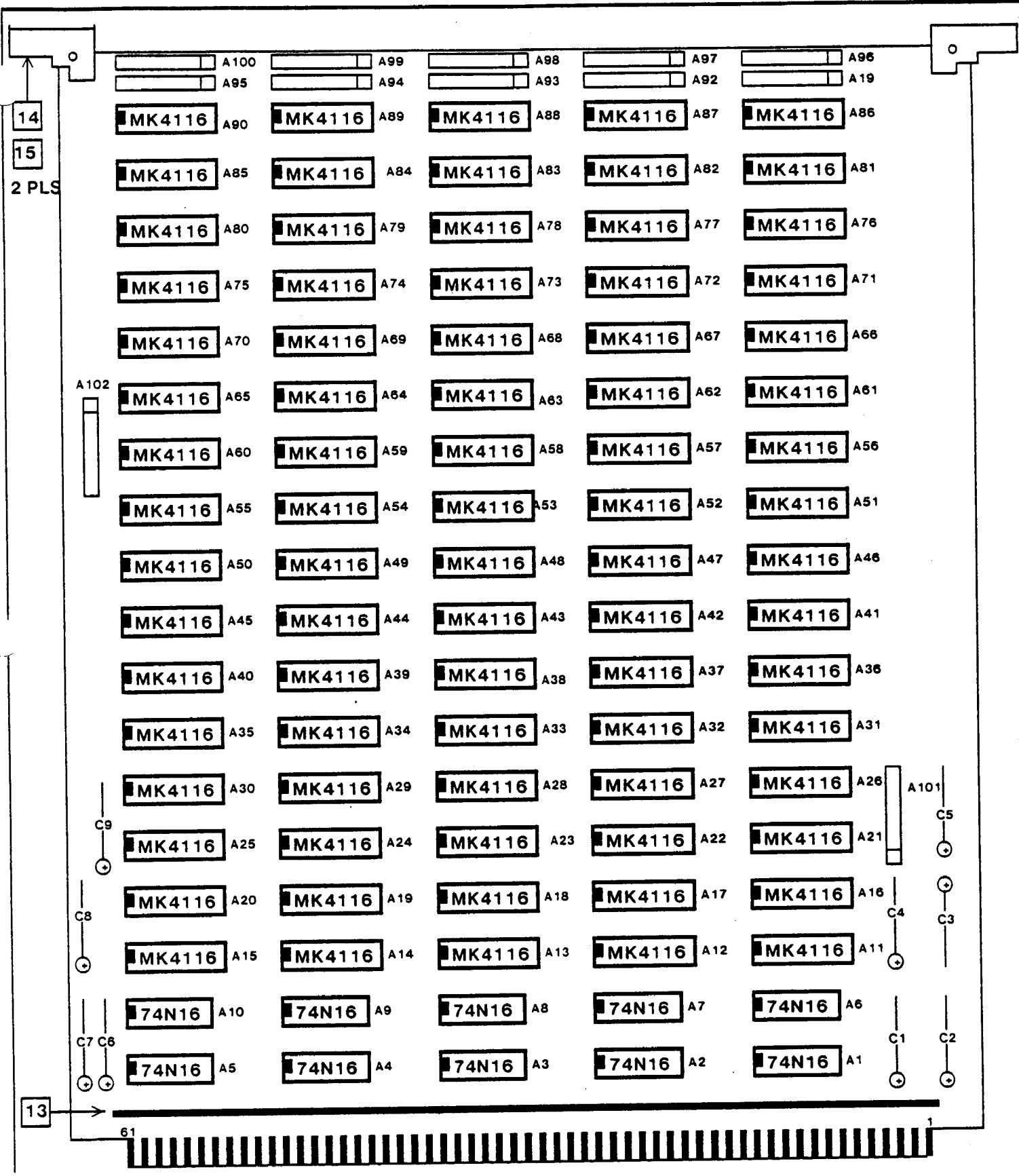
CARD 1	CARD 2	CARD 3	CARD 4
32 24 16 08 00	33 25 17 09 01	34 26 18 10 02	35 27 19 11 03
36 28 20 12 04	37 29 21 13 05	38 30 22 14 06	xx 31 23 15 07
↑	↑	↑	↑
chip position 11			

Chips 15, 25, 35, 45, 55, 65, 75, and 85 on board 4 aren't used. If you are out of replacement memory chips, you can use one of these, but then the board with the missing chips will only work in Slot 4.

MEMORY STORAGE MODULE

(ONE SUBGROUP, ALL EIGHT SUBGROUPS ARE IDENTICAL)





PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

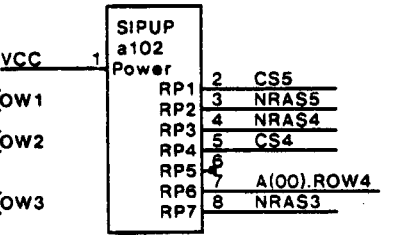
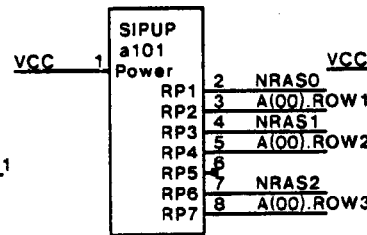
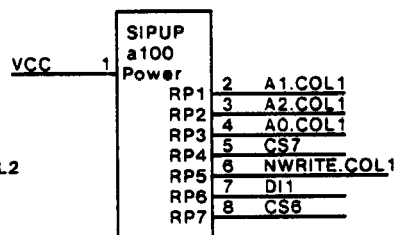
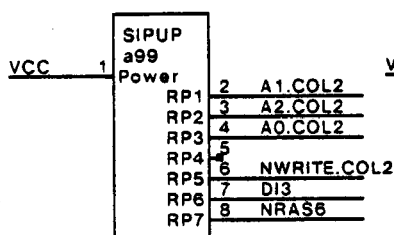
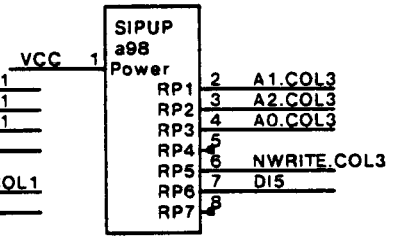
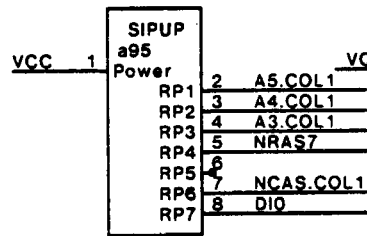
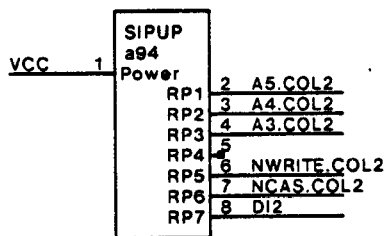
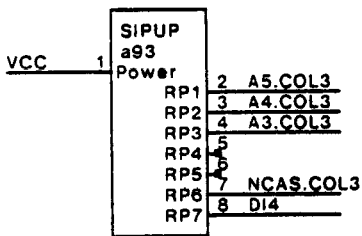
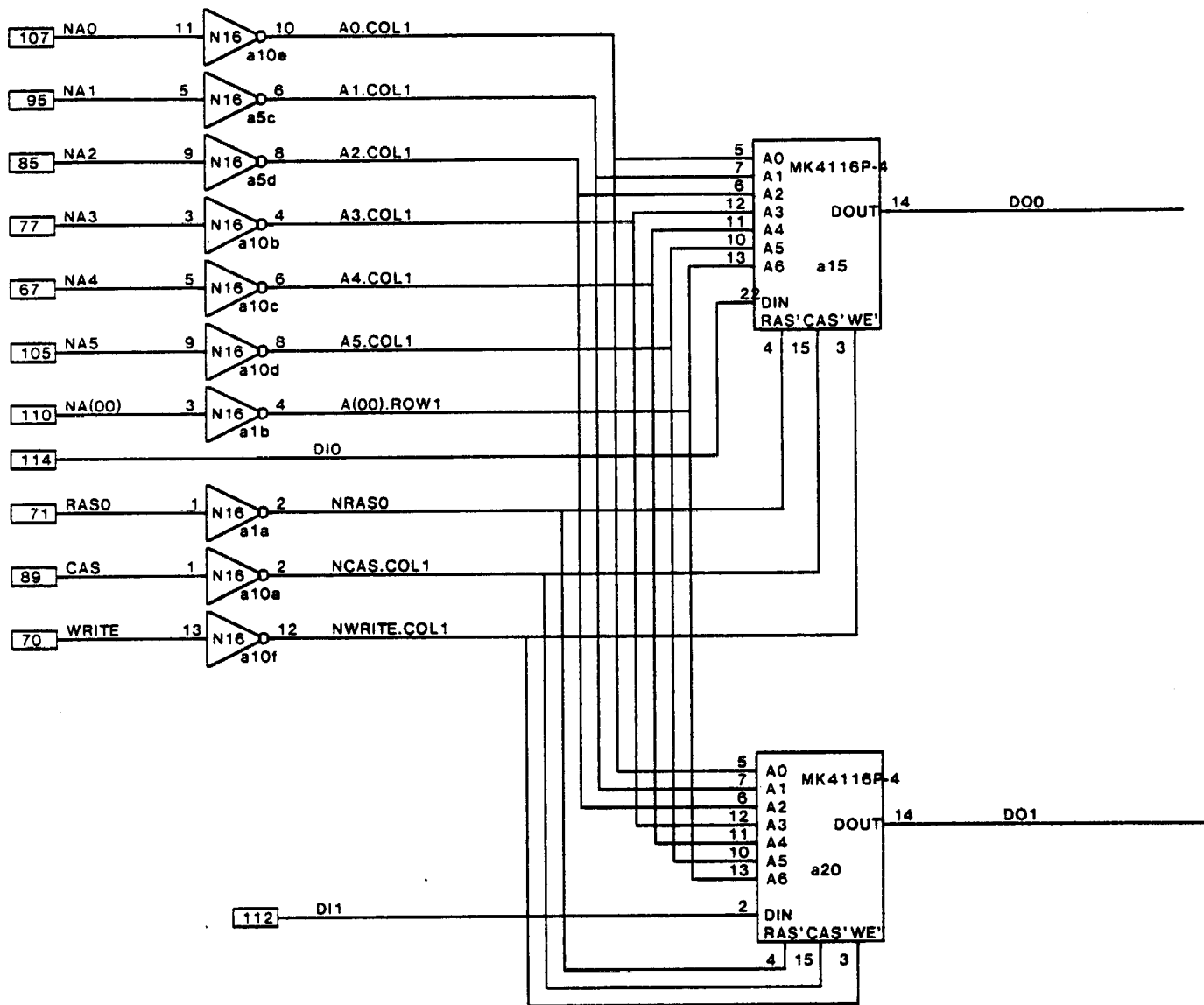
FILE: MEM256K03.SIL

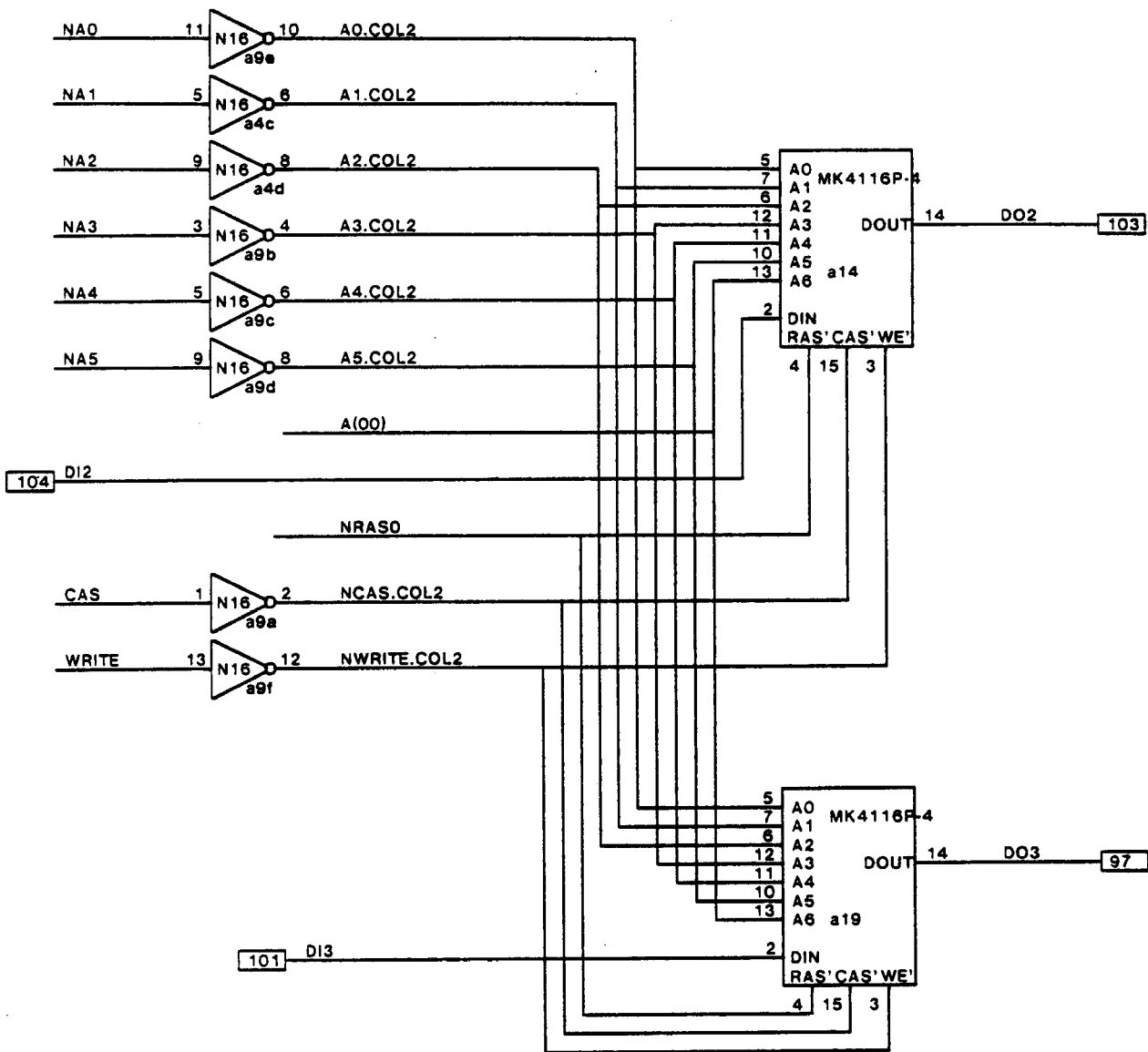
TITLE
Assembly, Printed Wiring
256K STORAGE
ALTO II XM

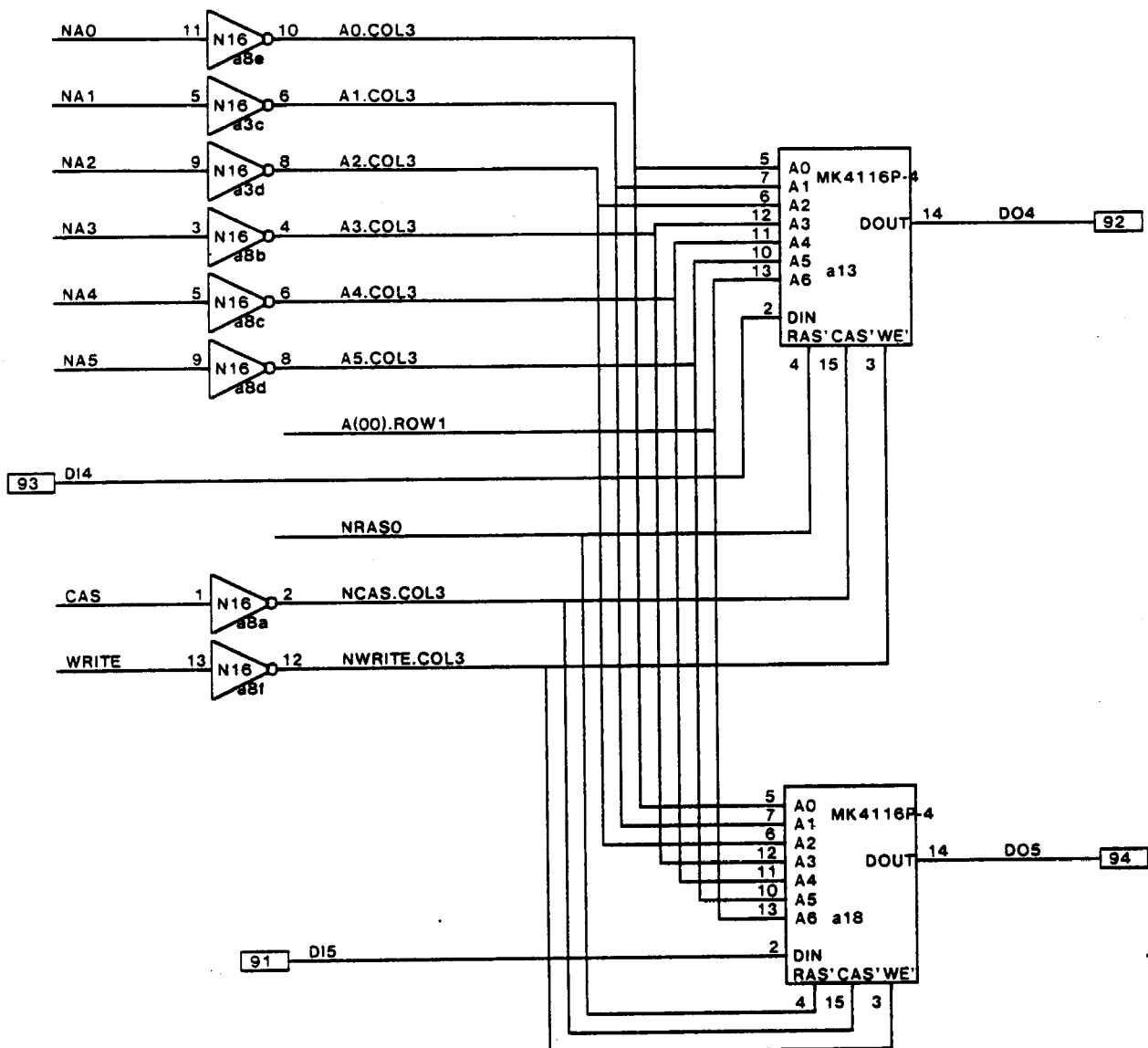
DWG.
 SIZE
 A41

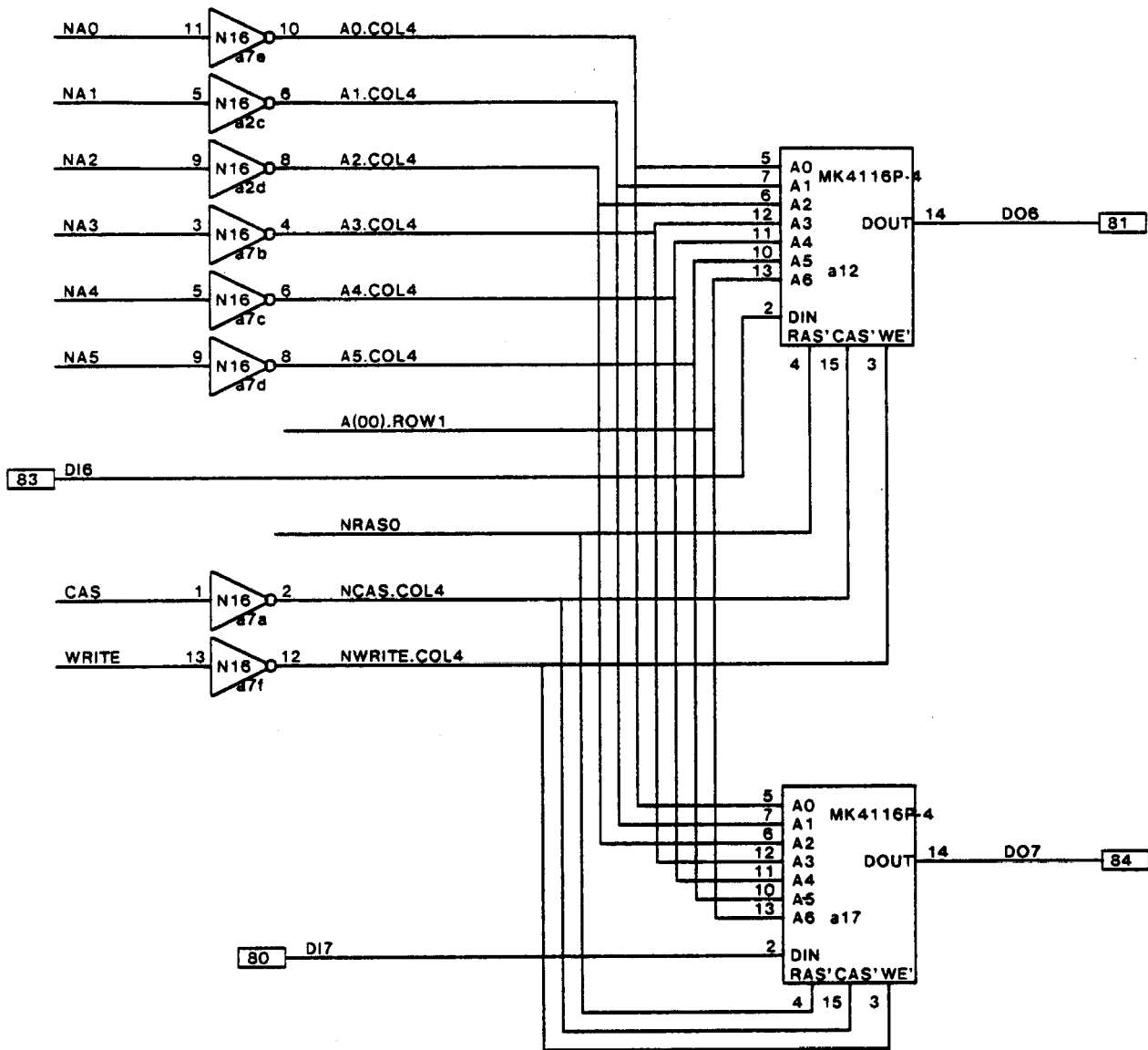
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 SHEET 3 OF 4

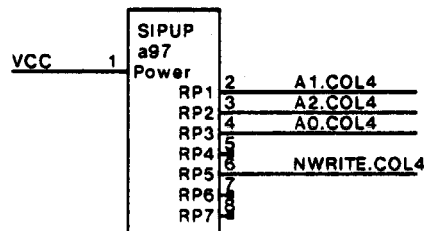
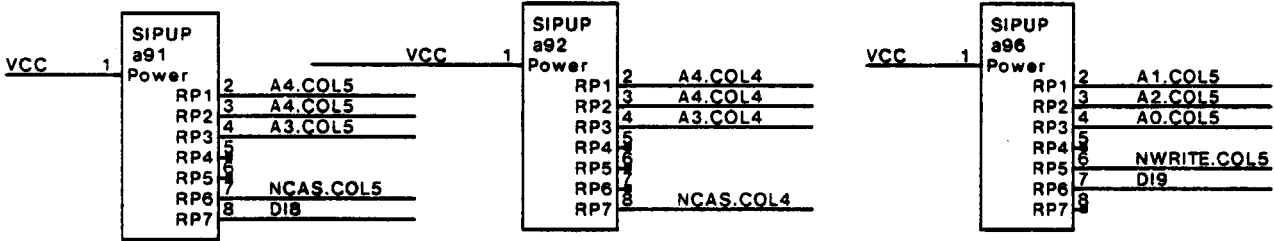
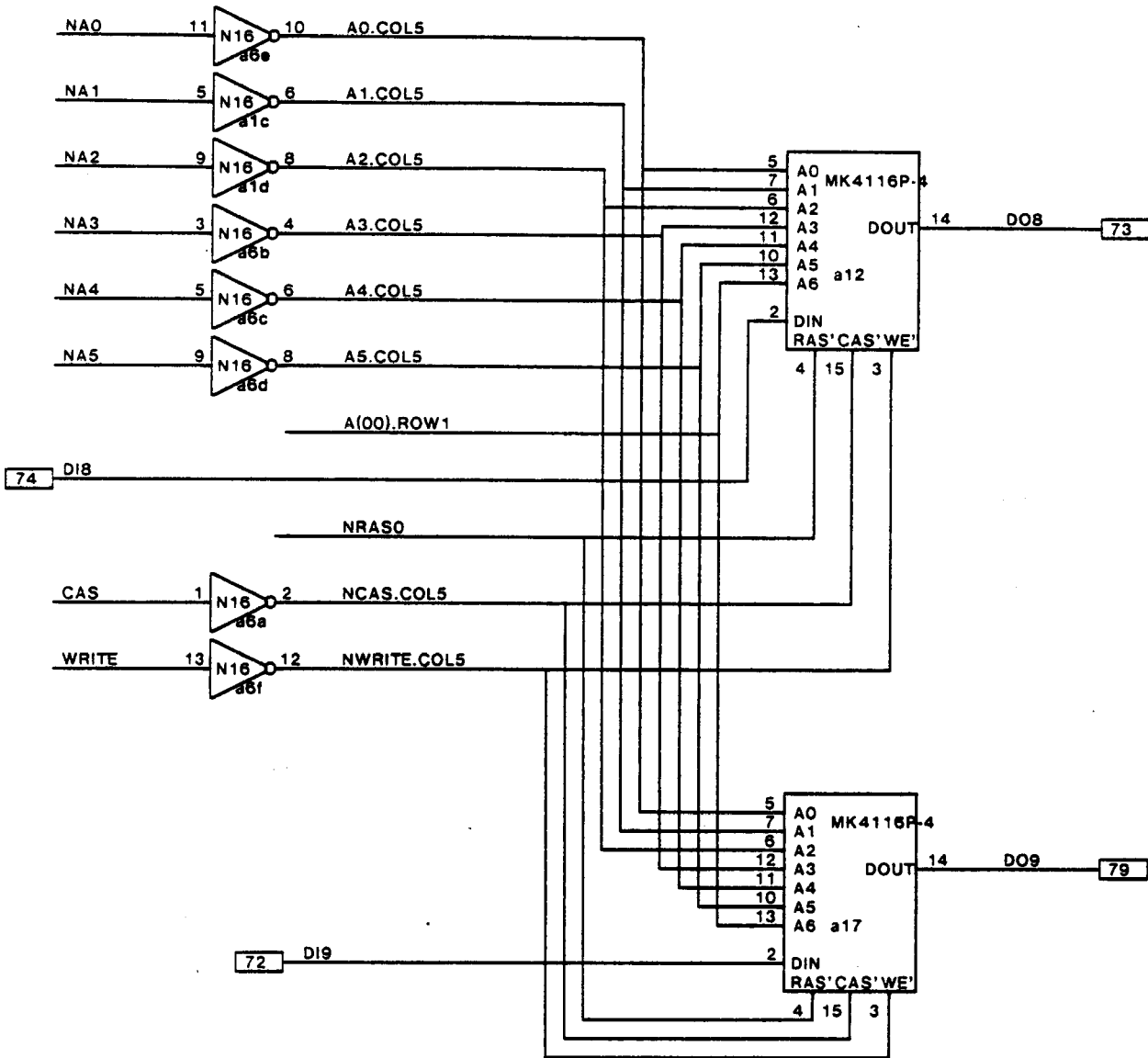
SHEET REV.
 B











220 OHMS

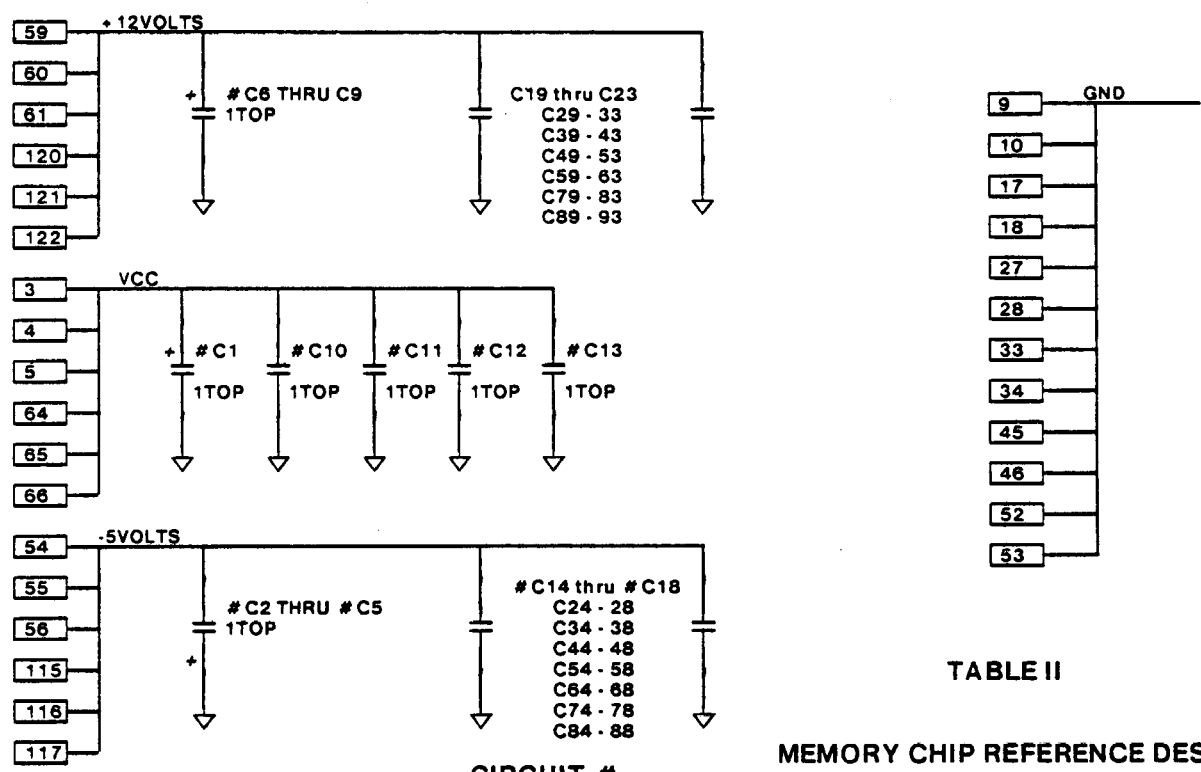


TABLE II
MEMORY CHIP REFERENCE DESIGNATOR

ROW #	CIRCUIT #																																
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8																	
1	A15	A20	A25	A30	A35	A40	A45	A50	A55	A60	A65	A70	A75	A80	A85	A90	1	A15	A20	A25	A30	A35	A40	A45	A50	A55	A60	A65	A70	A75	A80	A85	A90
2	A14	A19	A24	A29	A34	A39	A44	A49	A54	A59	A64	A69	A74	A79	A81	A89	2	A14	A19	A24	A29	A34	A39	A44	A49	A54	A59	A64	A69	A74	A79	A81	A89
3	A13	A18	A23	A28	A33	A38	A43	A48	A53	A58	A63	A68	A73	A78	A82	A88	3	A13	A18	A23	A28	A33	A38	A43	A48	A53	A58	A63	A68	A73	A78	A82	A88
4	A12	A17	A22	A27	A32	A37	A42	A47	A52	A57	A62	A67	A72	A77	A83	A87	4	A12	A17	A22	A27	A32	A37	A42	A47	A52	A57	A62	A67	A72	A77	A83	A87
5	A11	A16	A21	A26	A31	A36	A41	A46	A51	A56	A61	A66	A71	A76	A84	A86	5	A11	A16	A21	A26	A31	A36	A41	A46	A51	A56	A61	A66	A71	A76	A84	A86

CKT #	INP. PIN	SIGNAL NAME	INVERTER			PULLUP RESISTOR
			REF.	IN	OUT	
1	71	RAS0	A1	1	2	A101 R2
	110	NA(OO)	A1	3	4	A101 R3
2	79	RAS1	A2	1	2	A101 R4
	110	NA(OO)	A2	3	4	A101 R5
3	90	RAS2	A3	1	2	A101 R7
	110	NA(OO)	A3	3	4	A101 R8
4	86	RAS3	A3	11	10	A102 R8
	110	NA(OO)	A4	11	10	A102 R7
5	102	RAS4	A4	1	2	A102 R4
	110	CS4	A3	13	12	A102 R5
6	106	RAS5	A5	11	10	A102 R3
	110	CS4	A5	3	4	A102 R2
7	111	RAS6	A5	1	2	A99 R8
	110	CS4	A5	13	12	A100 R8
8	99	RAS7	A4	13	12	A95 R5
	110	CS4	A4	3	4	A100 R5

TABLE I

NOTE: FOR THE 32K X 10
THE RAMS ARE MK4096

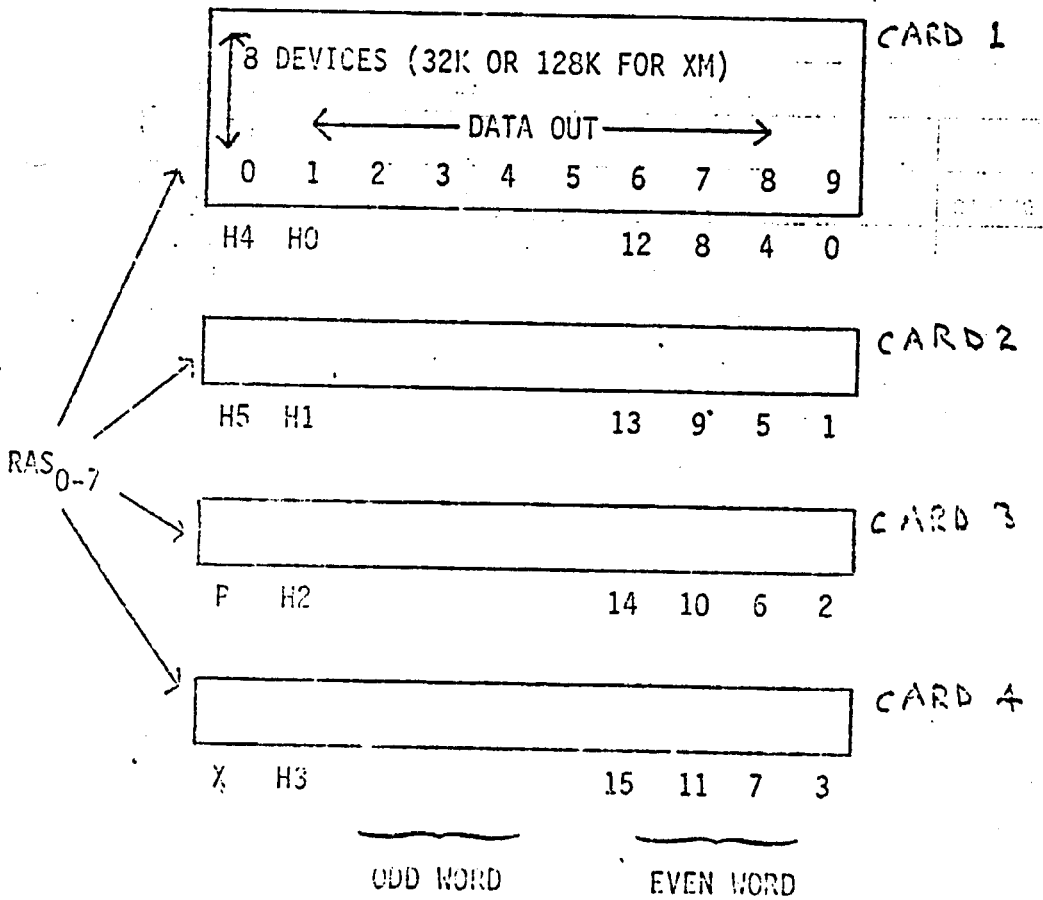
FOR THE 64K, 128K, 256K MODULES,
THEY ARE REPLACED WITH THE
MK4116P-4 CHIP.

ALTO MEMORY

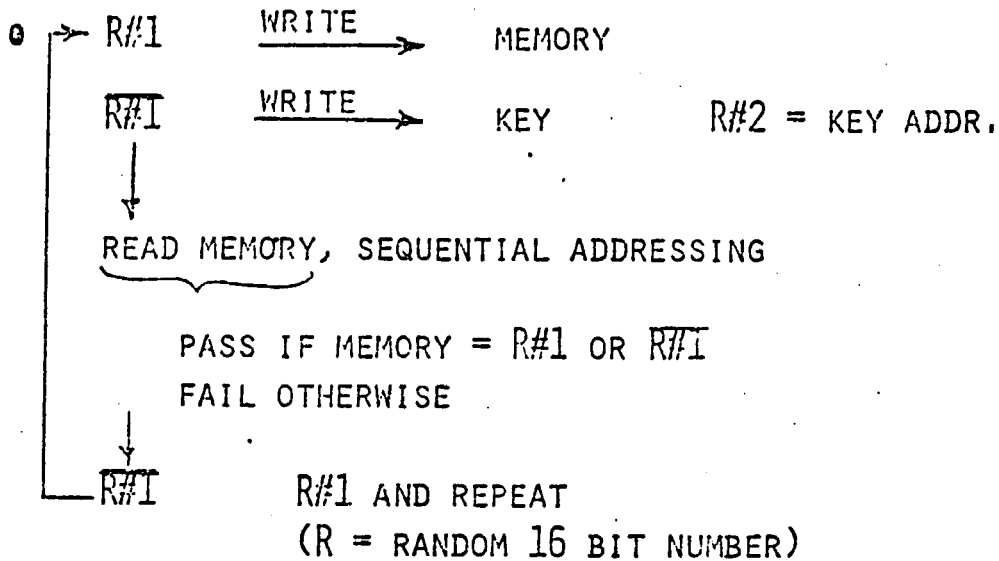
- o WORD = 16 BITS
- o ACCESS → 2 WORDS AT A TIME
 → 32 BITS + 6 BITS EC + PARITY + SPARE = 40 BITS
- c 10 BITS/MODULE 80 DRAMS/MODULE
- e 4 MODULES/ALTO 320 DRAMS/ALTO

ADDRESS A0-6, WE, $\overline{\text{CAS}}$

↓ TO ALL DEVICES



DMI - DIAGNOSTIC MEMORY TEST



- ⑥ EVERY OTHER COMPLETE TRIAL IS RUN WITHOUT ERROR CORRECTION AND RESULTS COMPARED.
- ⑦ NUMBER OF ERRORS IS STORED IN 320 WORDS OF MEMORY (65K ERRORS MAX.).
- ⑧ ON SCREEN CURSOR JUMPS ONCE EACH TIME THROUGH THE MAIN DMT LOOP.
- ⑨ S KEY CAUSES STATUS DISPLAY AND TRANSMIT ON NET. AUTO TRANSMIT EVERY 10K PASSES THROUGH DMT.
- ⑩ PEEK LOOKS AT NET AND STORES ALL DMT TRANSMISSION ON THAT NET.

ALTO II
EXTENDED MEMORY LAYOUT

BIT	BANK 0				BANK 1				BANK 2				BANK 3			
	00000-77777		100000-177777		00000-77777		100000-177777		00000-77777		100000-177777		00000-77777		100000-177777	
	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
0	1-16	1-18	1-26	1-28	1-36	1-38	1-46	1-48	1-56	1-58	1-66	1-68	1-76	1-78	1-86	1-88
1	2-16	2-18	2-26	2-28	2-36	2-38	2-46	2-48	2-56	2-58	2-66	2-68	2-76	2-78	2-86	2-88
2	3-16	3-18	3-26	3-28	3-36	3-38	3-46	3-48	3-56	3-58	3-66	3-68	3-76	3-78	3-86	3-88
3	4-16	4-18	4-26	4-28	4-36	4-38	4-46	4-48	4-56	4-58	4-66	4-68	4-76	4-78	4-86	4-88
4	1-11	1-13	1-21	1-23	1-31	1-33	1-41	1-43	1-51	1-53	1-61	1-63	1-71	1-73	1-81	1-83
5	2-11	2-13	2-21	2-23	2-31	2-33	2-41	2-43	2-51	2-53	2-61	2-63	2-71	2-73	2-81	2-83
6	3-11	3-13	3-21	3-23	3-31	3-33	3-41	3-43	3-51	3-53	3-61	3-63	3-71	3-73	3-81	3-83
7	4-11	4-13	4-21	4-23	4-31	4-33	4-41	4-43	4-51	4-53	4-61	4-63	4-71	4-73	4-81	4-83
8	1-17	1-19	1-27	1-29	1-37	1-39	1-47	1-49	1-57	1-59	1-67	1-69	1-77	1-79	1-87	1-89
9	2-17	2-19	2-27	2-29	2-37	2-39	2-47	2-49	2-57	2-59	2-67	2-69	2-77	2-79	2-87	2-89
10	3-17	3-19	3-27	3-29	3-37	3-39	3-47	3-49	3-57	3-59	3-67	3-69	3-77	3-79	3-87	3-89
11	4-17	4-19	4-27	4-29	4-37	4-39	4-47	4-49	4-57	4-59	4-67	4-69	4-77	4-79	4-87	4-89
12	1-12	1-14	1-22	1-24	1-32	1-34	1-42	1-44	1-52	1-54	1-62	1-64	1-72	1-74	1-82	1-84
13	2-12	2-14	2-22	2-24	2-32	2-34	2-42	2-44	2-52	2-54	2-62	2-64	2-72	2-74	2-82	2-84
14	3-12	3-14	3-22	3-24	3-32	3-34	3-42	3-44	3-52	3-54	3-62	3-64	3-72	3-74	3-82	3-84
15	4-12	4-14	4-22	4-24	4-32	4-34	4-42	4-44	4-52	4-54	4-62	4-64	4-72	4-74	4-82	4-84
	BANK 0				BANK 1				BANK 2				BANK 3			
H0	1-20		1-30		1-40		1-50		1-60		1-70		1-80		1-90	
H1	2-20		2-30		2-40		2-50		2-60		2-70		2-80		2-90	
H2	3-20		3-30		3-40		3-50		3-60		3-70		3-80		3-90	
H3	4-20		4-30		4-40		4-50		4-60		4-70		4-80		4-90	
H4	1-15		1-25		1-35		1-45		1-55		1-65		1-75		1-85	
H5	2-15		2-25		2-35		2-45		2-55		2-65		2-75		2-85	
P	3-15		3-25		3-35		3-45		3-55		3-65		3-75		3-85	

NOTE: 1. Card - Chip location.
2. The Memory Configuration Switch reverses high and low memory within a bank.