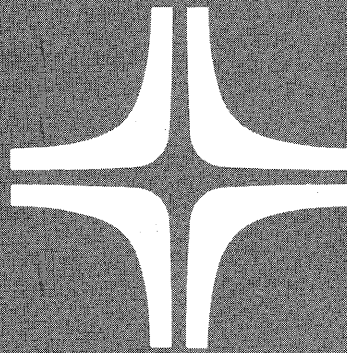


3766 Fixed Disk Storage Controller



Reference

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1. Introduction

This manual provides hardware information that permits a programmer to program the SPERRY 3766 Fixed Disk Storage Controller (FDC) more efficiently. The disk controller is housed in a freestanding cabinet (Figure 1-1). The controller (Figure 1-2) is located in the top portion of the cabinet and is capable of controlling up to four fixed disk drives, each with a net storage capacity of 101 megabytes (MB). The controller provides disk formatting, accessor positioning, searching, and data reading and writing. It also performs thorough parity checking on all disk data transfers and includes an extensive self-diagnostic capability. This diagnostic capability isolates faults in the controller and also performs seek, read, and write tests on the attached disk drives.

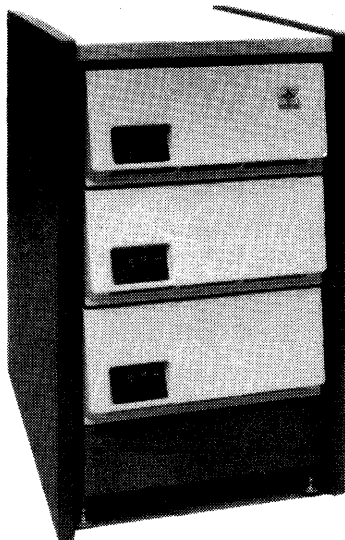


Figure 1-1. 3766 Fixed Disk Storage Controller

The controller has the same physical dimensions and electrical connector locations as a disk drive unit. A front control panel is provided for operator use. A thermal sensing unit in the cabinet provides high-temperature early warning.

The basic controller accommodates one disk drive but can be equipped with a multidrive feature to accommodate up to four disk drives. Also, a dual-host provision is available that permits two host systems to be connected to the controller.

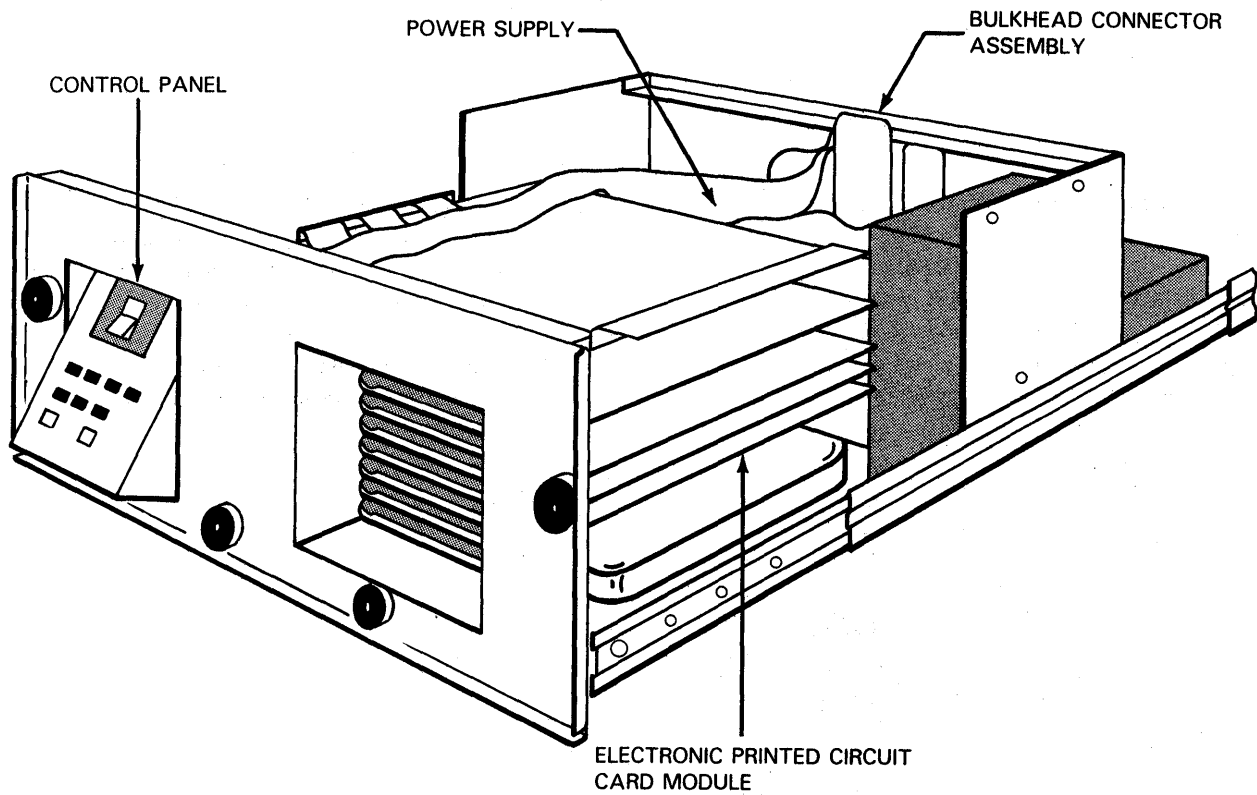


Figure 1-2. Controller

2. Subsystem Description

2.1. FIXED DISK CONTROLLER

The 3766 fixed disk storage controller (FDC) controls the drive interface, which provides head selection and positioner movement, generation of the proper bit patterns written by the drive unit, bit serialization and deserialization, and interpretation of the data read.

Head selection and cylinder positioning are accomplished by strobing the appropriate select bits and cylinder addresses on the interface lines.

During a write operation, the controller generates the proper track format, including gap characters, data fields, and error command codes (ECC). Data is then serialized and transmitted across the interface to the disk drive at an average rate of 1.2 megabytes per second (MB/s).

The controller performs the following functions:

- Analyzes data from the disk drive
- Separates various gaps
- Controls and identifies fields
- Verifies the check characters
- Transfers the appropriate data to the host system

The controller format uses address marks (AMs) to identify the beginning of a sector. Address marks are generated and detected by the disk drive under interface control. These marks have a unique pattern, contain no data or clock bits, and are recorded on the data tracks at the beginning of each sector field.

For error detection and correction, the controller generates and checks the cyclic redundancy check (CRC) code. This code is appended to the data fields. If an error is detected, the controller uses the ECC to correct the data read prior to transferring data to the host system.

2.2. FIXED DISK DRIVE

The disk drive is a direct access magnetic storage unit capable of storing and retrieving data from a fixed (nonremovable) rotating medium. The drive contains one head disk assembly (HDA) consisting of four magnetic sensitive platters, four movable data head/arm assemblies, and a single servo fixed head/arm assembly. (See Figure 2-1.) Each recording surface has two data heads. The HDA is a fully enclosed module, not removable by the user.

Each disk data surface is divided into two data bands, an outer band and an inner band. Each data band contains 561 tracks and a read/write head.

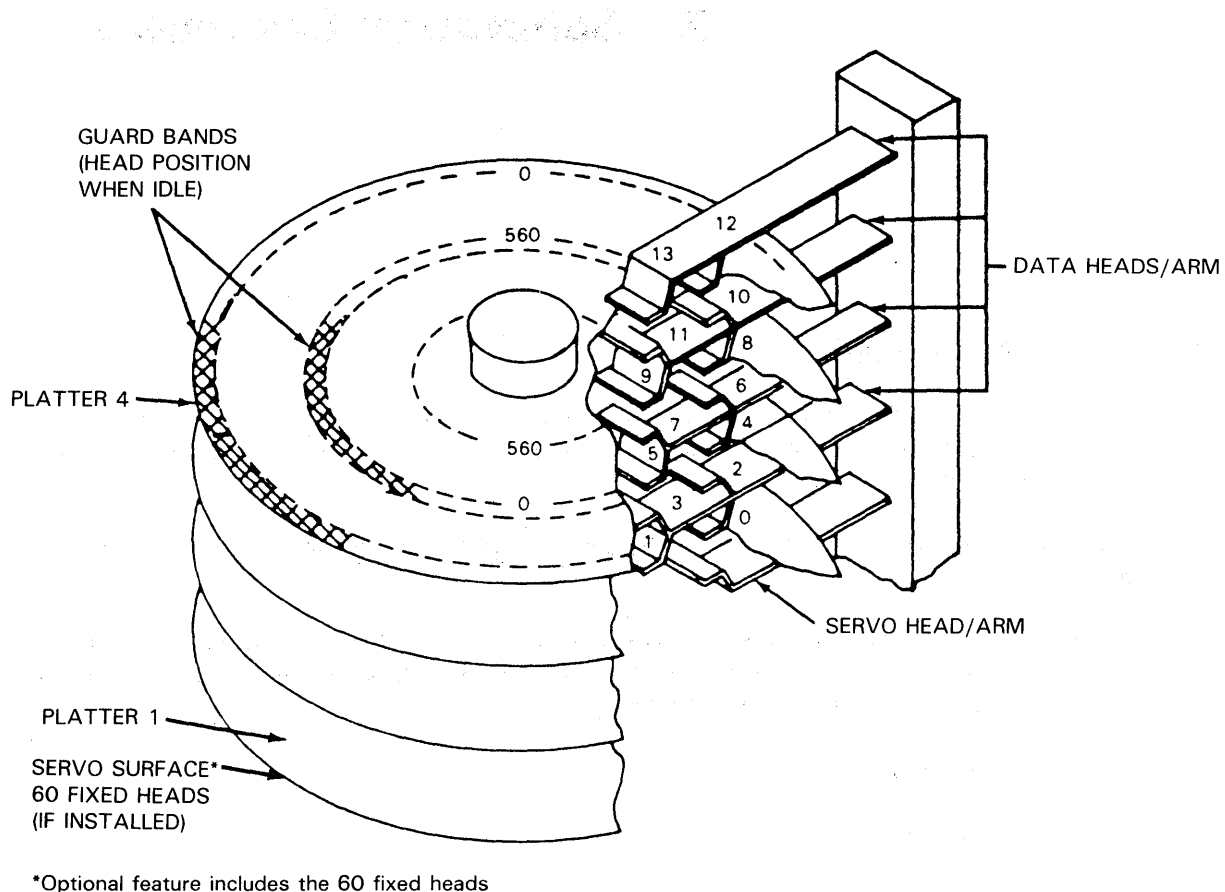


Figure 2-1. Head Disk Assembly

This provides 561 cylinders distributed over 7 data surfaces accessed by 14 magnetic heads. The bottommost surface (eighth surface) contains 561 servo tracks and 60 fixed heads. (See Figure 2-1.)

When directed by the controller, the disk drive performs a specified operation and signals its completion or any error conditions. The data on the disk is encoded by the disk drive electronics.

The disk drive provides the read circuitry required to recover data from the disk surface and converts it to a digital bit stream. A clock signal is provided to permit the controller to deserialize the bit stream and obtain byte timing synchronization. The drive contains its own power supply, coding control logic and electronics, and read/write circuitry. A data separator and address mark control are also part of the disk drive.

2.3. CONTROLLER CHARACTERISTICS

The fixed disk storage controller uses microprogrammed, bipolar, 4-bit slice microprocessors. The control storage configuration has 4096 (48-bit) words implemented with pluggable programmable read-only memory (PROM) devices.

Dual 512-byte random access memory (RAM) buffers are provided for local queueing, command parameter storage, and search key requirements.

A buffer expansion feature provides an additional 16K-byte buffer that is used as an elastic queue to accommodate host systems that cannot handle the disk transfer rate. A dual-host feature provides an interface to a second host system.

Data transfers from the host system to the FDC input buffer are controlled by FDC interface logic. A simultaneous transfer from the buffer to the disk occurs under control of the FDC microsequencer. When loaded or unloaded, the microsequencer interchanges the roles of the buffer to maintain a continuous data transfer between the disk drive and interface.

The 16 microprocessor working registers are supplemented with 64 bytes of RAM and may be used as additional storage.

Data integrity is assured by the overlapping of the host and FDC data path parity checking and by generation of the serial drive data error correction code. The serial drive data check characters consist of four bytes generated by a special error correction code (FIRE). Error correction of data fields recovered in error is performed by the controller. It then returns the corrected data to the host. Corrections are performed on all read and search operations. The FDC interface to the disk drive is an industry-standard, storage module device interface. The multidrive feature expands the basic control to provide drive interfaces for up to four disk drive units.

Single, dual-port, and fixed head drive capabilities are supported by the FDC.

PROM-based microdiagnostics are executed at cabinet power-up time, either under interface control or by the operator. Results of the diagnostics are passed back to the host system and also indicated on the operator control panel.

2.4. DISK DRIVE CHARACTERISTICS

Table 2-1 lists the general performance characteristics for the disk drive while operating with the 3766 fixed disk storage controller.

Table 2-1. Fixed Disk Characteristics (Part 1 of 2)

Item	Characteristic
Storage type	Fixed disks
Track density	476 tracks per inch 187 tracks per centimeter
Data surfaces	
Movable heads	7
Servo and fixed head	1
Heads per drive	
Movable (2 per surface)	14
Servo	1
Fixed heads (servo surface)	60 (56 + 4 spare)
Cylinders per drive	
Movable	561 (544 + 5 spare + 1 diagnostic + 9 alternate + 1 defect map + 1 for customer engineer use)
Fixed	5 (4 data cylinders and 1 partial cylinder for alternates)

Table 2-1. Fixed Disk Characteristics (Part 2 of 2)

Item	Characteristic
Tracks per drive Movable Fixed	7854 60
Recording technique	MFM
Bit density	6366 bits per inch 2506 bits per centimeter
Data transfer rate (nominal)	1.198 MB/s
Data capacity (unformatted) Track capacity (bytes) Drive data capacity (MB)	19,968 153.8 (movable) 1.09 (fixed)
Data capacity (formatted) Tracks per cylinder Bytes per sector Sectors per track Sectors per cylinder Bytes per track Bytes per cylinder Bytes per total cylinders (561) Bytes per data cylinders (544) Bytes per nondata cylinders (17) Bytes per data cylinders (4 fixed)	 14 256 52 728 13,312 186,368 104,552,448 101,384,192 3,168,256 745,472
Seek access time (movable) 1 cylinder Average Maximum	 7 milliseconds 35 milliseconds 70 milliseconds
Seek access time (fixed) Any track per cylinder	15 microseconds
Disk rotational speed	3600 ± 144 rpm
Disk latency time	16.67 ± 0.67 milliseconds
Start-up time (maximum)	25 seconds
Stop time (maximum)	60 seconds

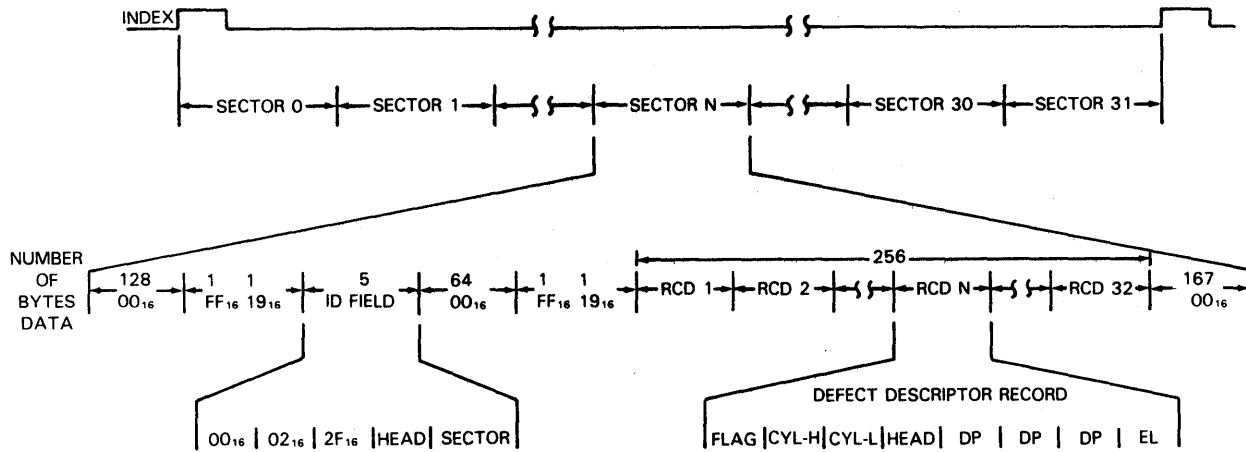
2.4.1. Head and Disk Assembly

The disk drive contains four fixed platters with two heads for each surface. Seven surfaces are used for data storage. The remaining surface is partially prerecorded with cylinder positioning information, and the remainder is reserved for fixed heads. There are two movable heads for each data surface, with each head covering its own separate band of 561 tracks. This results in an inner band and an outer band of 561 tracks each.

At any position among the 561 tracks (cylinders), 2 tracks for each surface are accessible. A total of 7 surfaces or 14 tracks are accessible at each head position. The eighth surface contains two servo tracks used to locate the accessor arm to a particular track position. Sixty fixed heads are mounted on two arm assemblies that span the servo surface. See Figure 2-1.

2.4.2. Prerecorded Defect Map

Cylinder address 559 contains a list of all surface defects that exist on the magnetic disk recording surfaces. These defects are identified and recorded during manufacturing and are required at the time the disk is initialized. The track and defect record format are shown in Figure 2-2.



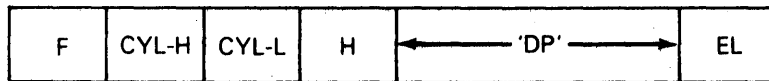
LEGEND:

- ID Identification
- RCD Record
- CYL Cylinder
- DP Defective position
- EL Error length

Figure 2-2. Track and Defect Record Format

2.4.3. Defect Record Format

The defect record format is:



■ Movable head defect descriptor:

F = Flag (1 byte)

The codes for the flag bytes are:

- 00₁₆ Valid defect information
- 20₁₆ Track contains a defect causing a potential false address mark (AM).
- 80₁₆ End of defect map and disregard

CYL-H, CYL-L = Cylinder number containing defect (two bytes)

H = Head and track number containing defect (one byte)

DP = Index to defect starting bit position (three bytes)

EL = Error bit length (one byte)

■ Fixed head defect descriptor:

F = 40₁₆ Specifies fixed head descriptor

CYL-H,CYL-L = 00₁₆ Address byte for each cylinder

H = XOOX XXXX, where X specifies the 6-bit address used for fixed head addressing

DP = Index to defect starting bit position (three bytes)

EL = Error bit length (one byte)

Tracks 0, 1, 2, 9, A, and B on cylinder 559 contain the defect map. All six tracks are identical and at least two out of the six tracks are free of defects.

Allowing 32 defect descriptors per sector and 32 sectors per tracks, a maximum of 1024 defects per head disk assembly can be handled. (The data track recording format has 52 sectors.)

Excluding the most significant byte of the defect records, the remaining bytes are prerecorded in ascending order. Defect descriptors following the last valid defect descriptor contain zeros. The same defect information is written on heads 3, 4, 5, 6, 7, and 8 in SUL format. Tracks 0 through B cannot be written on by the user. The FDC does not permit any operation other than the format-read function to access cylinder 559.

2.5. FIXED DISK CONTROLLER RECORDING FORMAT

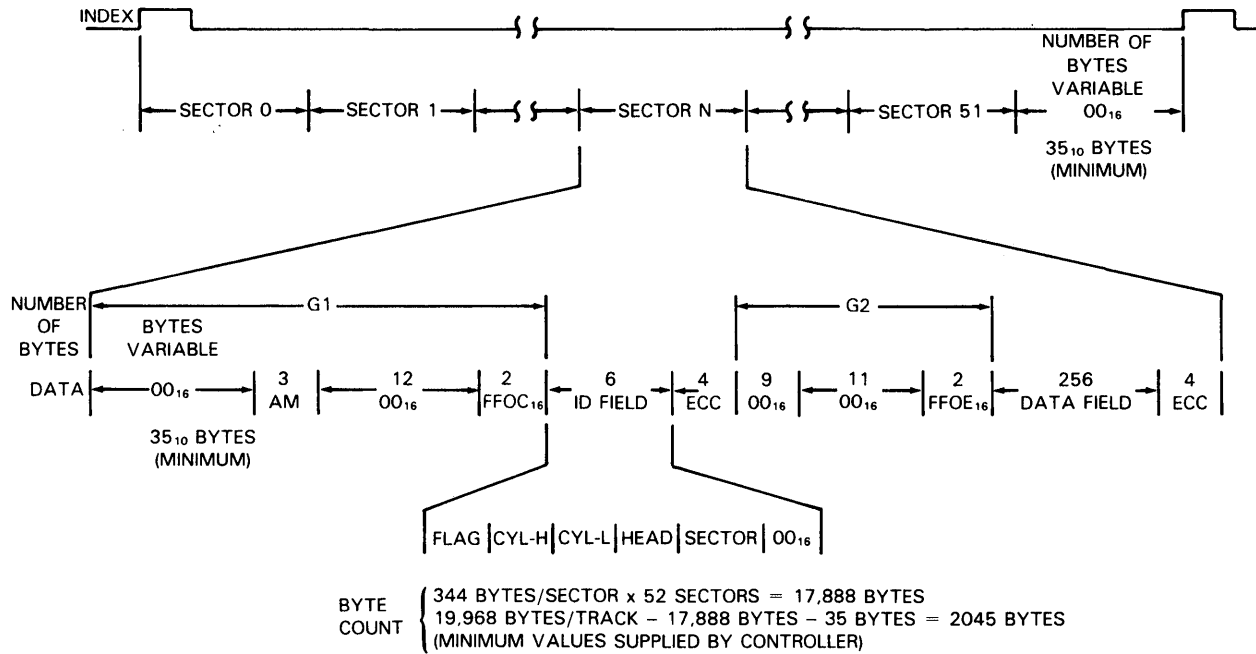
Each track is similarly formatted, containing 52 sectors of equal size. Gaps between sectors vary in size because of possible defects, since all media defects fall within the gaps. Nine alternate cylinders are available if all media defects cannot be handled in a track. Each sector consists of an ID field, gaps, and a data field. The data field contains 256 bytes of data and is identified by the address located in its associated ID field. Each data field is numbered sequentially starting at the index (data field 0) and continuing to the end of track (data field 51). Defect skipping is accomplished by varying the length of certain intersector gaps, thus avoiding the surface defect. Sufficient reserve space is provided to allow a minimum of three defects per track while still allowing 52 defect-free sectors. In the event that a track cannot be formatted to contain 52 defect-free sectors, the track is flagged and an alternate is assigned. The fixed disk controller format is shown in Figure 2-3.

2.5.1. Index

The index appears once for each revolution of the disk and indicates the beginning and end of a track. Track formatting starts with the first detection of the index and ends with the next detection of the index. The gap immediately following the index provides the necessary time to select and switch to the next head when directed. The index is prerecorded on the servo track located on the bottommost disk surface. See Figure 2-1.

2.5.1.1. Address Mark

The address mark (AM) appears at the beginning of each sector. It consists of a 3-byte position where no flux reversals are recorded on the disk data surface containing the data being read. The AM is required for soft sectoring and is used for sector orientation.



LEGEND:

CYL Cylinder
ECC Error command code

Figure 2-3. Fixed Disk Track Format

2.5.2. Sync Fields

The sync field appears before each identification (ID) and data field to distinguish the ID from the data field and to provide byte synchronization for the ECC. The sync fields are defined as follows:

Field	First Byte	Second Byte
ID	FF ₁₆	OC ₁₆
Data	FF ₁₆	OE ₁₆

2.5.3. Gaps

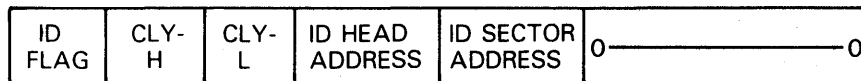
The various gaps shown in Figure 2-3 are provided to permit timing and speed variations caused by mechanical and electrical tolerances, and recovery or response times. The G1 gap varies in length to ensure that media defects fall within this gap. The minimum value of G1 ensures enough time to switch from writing a data field to reading the next ID field. For the special case where G1 comes immediately after the index, the minimum number of bytes ensures enough time to switch from one head to the next without missing a disk rotation.

Included as part of the G2 gap are bytes for discontinuities that occur when starting a write operation. During a read, the discontinuities are avoided by turning the read gate off before the discontinuity and back on after it.

A start-up region is provided as part of the gap before either the ID or data field. This start-up region permits the read recovery circuits to synchronize with the data rate of the disk.

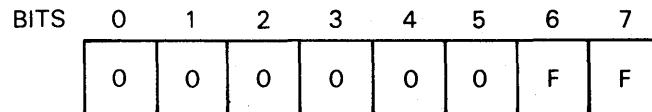
2.5.4. ID Field

The ID field contains the address for the sector. Prior to access of a data field for reading or writing, the associated ID field must be located during a scan operation. The format of the ID field is:



2.5.4.1. ID Flag Byte

The flag byte indicates the condition of the track. The format for the flag byte is:



The FF bits that specify track condition as good, alternate, or defective are as follows:

00 = Good track

01 = Alternate track

10 = Defective track

11 = Defective track

The disk initialization program assigns alternate and defective tracks. Once initialized, the controller firmware automatically switches to the alternate track when a defective track is encountered. The ID fields of the defective track are formatted to contain the flag byte setting (02₁₆) and the cylinder and track address of the alternate track. The ID fields of all sectors in the alternate track are formatted to contain the flag byte setting (01₁₆) and the cylinder and track address of the defective track. To ensure rapid access on fixed cylinders, alternate tracks are allocated on fixed cylinders.

2.5.5. ID Cylinder Address

The two ID cylinder address bytes, cylinder high (CLY-H) and cylinder low (CLY-L), are concatenated to form the cylinder address. The first cylinder (outermost) is designated 0 (00₁₆); the innermost cylinder is designated 560 (230₁₆).

Fixed heads are addressed by cylinders. (See Table 2-2.) All functions using fixed heads include a cylinder address and a head address.

Table 2-2. Cylinders Addressed by Fixed Heads

Fixed Head Defect Descriptor Byte (Hexadecimal)	Physical Location of Fixed Head	PCB Cylinder Address Track Number (Decimal)	PCB Head Address (Hexadecimal)
0 - 0D	Outer 0 - D	400	00 - 0D
10 - 1D	Outer 10 - 1D	401	00 - 0D
80 - 8D	Inner 0 - D	402	00 - 0D
90 - 9B	Inner 10 - 1B	403	00 - 0B
8E - 8F	Inner 0E - 0F	403	0C - 0D
0E - 0F	Outer 0E - 0F	404*	00 - 01
1E - 1F	Outer 1E - 1F	404*	02 - 03

* Partial cylinders reserved as alternates for defective fixed head tracks.

2.5.6. ID Head Address

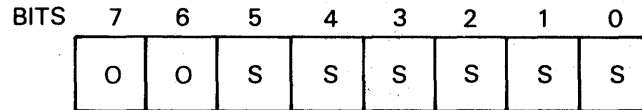
For movable heads, the ID head address byte contains the head select bits that address 1 of 14 data heads. The combination of cylinder and head addresses designates the track. The format of the movable head address bytes is shown in Table 2-3.

Table 2-3. Movable Head Address Bytes

Head Number (Decimal)	Head Number (Hexadecimal)	Disk Number	Surface	Band
0	00	1	Upper	Outer
1	01	1	Upper	Inner
2	02	2	Lower	Outer
3	03	2	Lower	Inner
4	04	2	Upper	Outer
5	05	2	Upper	Inner
6	06	3	Lower	Outer
7	07	3	Lower	Inner
8	08	3	Upper	Outer
9	09	3	Upper	Inner
10	0A	4	Lower	Outer
11	0B	4	Lower	Inner
12	0C	4	Upper	Outer
13	0D	4	Upper	Inner

2.5.7. ID Sector Address

The ID sector address byte contains the sector number. There are 52 sectors per track and they are numbered sequentially starting from the index. The first sector is 0 (00₁₆) and the last is 51 (33₁₆). The format of the sector address byte is:



where SSSSSS is the binary sector number.

Sector Number (Decimal)	Sector Number (Hexadecimal)
0	0 First sector from index
1	1 Second sector from index
.	.
.	.
51	33 Last sector from index, 52-sector format

2.5.8. ID Error Correction Code

Four bytes of a check character are appended to the ID field for error detection. No error correction is made on this field.

2.5.9. Data Field

The data field is 256 bytes in length for user data. This is the smallest addressable unit of data.

2.5.9.1. Data Field Error Correction Code

Four bytes are appended to the data field and are used to detect and correct data errors.

2.5.10. Error Correction Code

The error correction code (ECC) is generated by the hardware and appended to each ID and data field to ensure data integrity when writing on the disk. The ECC is used only for error detection in the ID fields and detection and correction of the data fields.

The FIRE code is in the form:

$$(X^{25} + 1) (X^7 + X^3 + 1)$$

This polynomial is capable of correcting a single burst error of up to seven bits, and detecting most single and multiple burst errors.

2.6. PERIPHERAL CONTROL BLOCK

The peripheral control block (PCB) is a fixed-length block of control information passed to the FDC and it specifies the function to be performed and its related parameters. The host transfers the PCB into the FDC buffer using interface protocol.

The PCB consists of 16 bytes, and its format is the same as all other subsystem operations. Validity checks are performed on the PCB. These are listed in Table 2-4. Parameter information that is not used in a particular function is not checked.

The PCB format is shown in Figure 2-4 and the bytes are described in Table 2-4. The bytes are always transmitted in the order shown in the defined byte location.

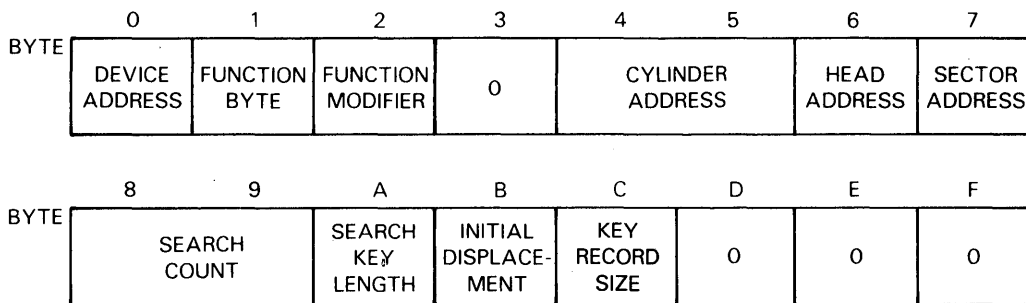


Figure 2-4. Peripheral Control Block

Table 2-4. Peripheral Control Block Byte (Part 1 of 2)

Byte	Description	Validity Check	Action if Validated
PCB 0	Device address	0 to 3	Function is terminated with status indicating a controller error.
PCB 1	Function byte	See Table 2-6 for valid function code.	Function is terminated and the ATTENTION line is raised. Status returned on next interface command (continue) indicates a controller error.
PCB 2	Function modifier	Individual bit interpretation as required per command execution	See Table 2-7, function modifier bits for a particular function.
PCB 3	Not used	Set to 0	A nonzero value indicates diagnostic testing.
PCB 4, PCB 5	Cylinder address	0 to 135 (87 ₁₆) – 25MB to 271(10F ₁₆) – 50MB to 407(197 ₁₆) – 75MB to 543 (21F ₁₆) – 100MB 544 (220 ₁₆) to 560 (230 ₁₆) 400 ₁₆ to 404 ₁₆ Fixed heads only	Function is terminated and the ATTENTION line is raised. Status returned on next interface command (continue) indicates a controller error.

Table 2-4. Peripheral Control Block Byte (Part 2 of 2)

Byte	Description	Validity Check	Action if Validated
PCB 6	Head address	0 to 13 ($0D_{16}$) Format read= 0,1,2,9,10,11.	Function is terminated and the ATTENTION line is raised. Status returned on next interface command (continue) indicates a controller error.
PCB 7	Sector address	0 to 59 ($3B_{16}$) Format read= 0 to 28 ($1C_{16}$)	Same as PCB 6
PCB 8, PCB 9	Sector count	Read, write search 1 to 65, 535 (or end of volume) Format read=4 Diagnostic read=1	Same as PCB 6
PCB A	Search key length	0 to 255 (OFF_{16}) where 0=256 bytes (See PCB C also.)	No invalid condition exists.
PCB B	Initial displacement	0 to 255 (OFF_{16}) where 0=0 bytes (See PCB C also.)	No invalid condition exists.
PCB C	Key record size	0 to 225 (OFF_{16}) PCB A+PCB B= < 256	Same as PCB 6
PCB D, PCB E, PCB F	Not used	Not checked	-

Table 2-5 gives the validity check and error status conditions for the PCB.

2.6.1. Device Address

The device address PCB 0 is always set as follows:

<u>Byte value</u>	<u>Disk drive number</u>
00_{16}	0
01_{16}	1
02_{16}	2
03_{16}	3

2.6.2. Function Byte

Function byte PCB 1 specifies the subsystem function to be executed. Table 2-6 lists the valid function codes. Hexadecimal values not listed are invalid and result in a validity check status condition. Table 2-7 describes each bit of this byte.

Table 2-5. PCB Validity Check and Error Status Conditions

Validity Check Byte	Peripheral Status Block		
	0	1	2
PCB 0 Illegal device address	C0 ₁₆ Function reject, device ready	00 ₁₆ Not defined	00 ₁₆ Not defined
PCB 1 Illegal function byte	44 ₁₆ /C4 ₁₆ Device ready, unit check, function reject	00 ₁₆ Not defined	20 ₁₆ Invalid format
PCB 2 No error condition (See Table 2-4.)			
PCB 3 Not used			
PCB 4 and PCB 5 Illegal cylinder address	44 ₁₆ /C4 ₁₆ 030 Function reject, device ready, unit check	00 ₁₆ Not defined	40 ₁₆ Invalid cylinder address
PCB 6 Illegal head address	44 ₁₆ /C4 ₁₆ Device ready, unit check, function reject	00 ₁₆ ^a -030 Not defined	20 ₁₆ Invalid format
PCB 7 Illegal sector address	44 ₁₆ /C4 ₁₆ Device ready, unit check, function reject	00 ₁₆ Not defined	20 ₁₆ Invalid format
PCB 8 and PCB 9 Illegal sector count	44 ₁₆ /C4 ₁₆ Device ready, unit check, function reject	00 ₁₆ Not defined	30 ₁₆ Invalid format or cylinder overflow
PCB A and PCB B No error condition (See Table 2-4.)			
PCB C Illegal search parameters	44 ₁₆ /C4 ₁₆ Device ready, unit check, function reject	00 ₁₆ Not defined	20 ₁₆ Invalid format

Table 2-6. Fixed Disk Valid Functions

Function Byte in Hexadecimal	Function
10	Recalibrate
11	Seek
20	Read-data
21	Read-ID
22	Search-equal
23	Search-high-or-equal
24	Format-read
25	Search-low
26	Diagnostic-read
28	Test-read
40	Write-data
44	Format-write

2.6.3. Function Modifier

Function modifier PCB 2 enables modification in the execution of the basic function. The following is the format of this byte. (Each bit is described in Table 2-7).

BITS	7	6	5	4	3	2	1	0
	ECC SUPPRESS	MULTIKEY SUPPRESS	IMPLIED SEEK SUPPRESS	ALTERNATE/ DEFECTIVE TRACK SUPPRESS	BYTE MODE	SEARCH IMMEDIATE SUPPRESS	OFFSET CONTROL	

Table 2-7. Function Modifier Byte, Bit Descriptions (Part 1 of 2)

PCB 2 Bit	Description
7	<p>ECC Suppress – When set to 0 and an ECC error is detected, an attempt is made to perform an error correction operation on the data read from the last sector.</p> <p>When set to 1, no error correction is performed by the controller and the ECC remainder is passed by way of the peripheral status block for host system correction or logging purposes.</p>
6	<p>Multikey Suppress – When set to 0, every record within the sector (after initial displacement) is searched for the key.</p> <p>If set to 1, the record starting at the initial displacement is searched for the key in that sector.</p>
5	<p>Implied Seek Suppress – When set to 1, a seek is suppressed when implied by the specified function. Cylinder switching and alternate/defective track management are also suppressed.</p> <p>When set to 0, function proceeds normally.</p>

Table 2-7. Function Modifier Byte, Bit Descriptions (Part 2 of 2)

PCB 2 Bit	Description															
4	<p>Alternate/Defective Track Suppress – When set to 0, the substitution of an alternate track for a defective track occurs automatically as part of the operation in progress. When indicated by track condition, a seek to an alternate track, verification, execution, and, finally, a position back to the defective track is performed, if necessary.</p> <p>When set to 1, the flag (not zero status condition) is set if an alternate or defective track is encountered. Also, if an alternate or defective track is being processed, head switching is suppressed. When implied seek is suppressed, head switching is implied.</p>															
3	<p>Byte Mode – When set to 1, data transfer (if required) between the FDC and the system takes place in byte-oriented, demand-acknowledge mode.</p> <p>When set to 0, burst mode is indicated.</p>															
2	<p>Search Immediate Suppress – When set to 1, a search operation must begin with the starting sector specified in the PCB.</p> <p>When set to 0, a search begins immediately. After searching the first sector, search immediate may wait for the starting sector to continue the search operation. This bit does not apply to the search-read-equal command, which always waits for the starting sector.</p>															
1,0	<p>Offset Control – These two bits determine the direction in which offset is applied. Offset displaces the read and write heads from the nominal track center by 250 microinches (approximately 98 microcentimeters). This function is used to recover marginal data resulting from small defects on the disk surface. The condition of these bits is ignored for any write operation. Offset is applied only to the track specified in the PCB. The bit definitions are encoded as follows:</p> <table border="1"> <thead> <tr> <th>Bit 1</th> <th>Bit 0</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No offset</td> </tr> <tr> <td>0</td> <td>1</td> <td>Negative offset</td> </tr> <tr> <td>1</td> <td>0</td> <td>Positive offset</td> </tr> <tr> <td>1</td> <td>1</td> <td>No offset</td> </tr> </tbody> </table>	Bit 1	Bit 0	Definition	0	0	No offset	0	1	Negative offset	1	0	Positive offset	1	1	No offset
Bit 1	Bit 0	Definition														
0	0	No offset														
0	1	Negative offset														
1	0	Positive offset														
1	1	No offset														

Table 2-8 lists the function modifier bits that apply to each basic function defined by the function byte. Only those modifier bits that are allowed (i.e., indicated by an X under the bit in question) are checked for validity prior to execution; all other bits are ignored.

Table 2-8. Applicable Function Modifier Combinations

Function Modifier	Bit							
	7	6	5	4	3	2	1	0
Recalibrate	-	-	-	-	-	-	-	-
Seek	-	-	-	-	-	-	-	-
Read-data	X	-	X	X	X	-	X	X
Read-ID	-	-	-	-	-	-	X	X
Search-equal	X	X	X	X	X	-	X	X
Search-equal-or-high	X	X	X	X	X	X	X	X
Search-low	X	X	X	X	X	X	X	X
Format-read	-	-	-	-	X	-	X	X
Test-read	X	-	X	X	-	-	X	X
Write-data	-	-	X	X	X	-	-	-
Format-write	-	-	X	-	-	-	-	-
Diagnostic-read	X	-	X	X	X	-	X	X

LEGEND:

X Modifier bits that are allowed

2.6.4. Cylinder, Head, and Sector Addresses

Cylinder bytes PCB 4 and PCB 5 form the starting cylinder address. Values range from 0 to 560 (00₁₆ to 230₁₆) for movable heads and 1024 to 1028 (400₁₆ to 404₁₆) for fixed heads. This represents 561 cylinders accessible by movable heads and four 14-track cylinders, plus one 4-track cylinder accessible by fixed heads.

The head address PCB 6 byte specifies the starting track for the operation. There are 14 heads within each cylinder numbering from 0 to 13 (00₁₆ to 0D₁₆). A validity check by the FDC ensures head address integrity.

The sector address PCB 7 specifies the starting sector number for the operation to be performed. Sector addresses range from 0 to 51 (00₁₆ to 33₁₆). The sector address is checked for validity.

2.6.5. Sector Count

The two sector count bytes PCB 8 and PCB 9 specify the number of sectors to be processed for a read, write, or search operation. Any value from 1 to 65,535 (01₁₆ to FFFF₁₆) is valid but limited by the following constraints:

- When the function starts on user cylinders (0-543), the sector count must not cause the controller to attempt a cylinder switch from the last sector to cylinder 543.
- When the function starts on nonuser cylinders (544-560), the sector count must not cause the controller to attempt a cylinder switch. Sector count plus starting count must be less than or equal to 728.
- When the function starts on the defect map cylinder (559), the sector count must be 4.
- When the function starts on a fixed head cylinder, the sector count must not cause the controller to attempt a cylinder switch from the last sector of cylinder 403₁₆.

- When the function starts on cylinder 404₁₆, sector count plus starting sector must be less than or equal to 208.

2.6.6. Search Parameters

The search parameter bytes PCB A, B, and C are used exclusively for search operations.

2.7. FUNCTION REPERTOIRE

Various functions are provided to control operations in the disk drive and controller. The PCB is retrieved by the controller from the host system prior to executing the specified function. These functions are:

- Positional functions
 - Seek
 - Recalibrate
- Read/write functions
 - Read-ID
 - Read-data
 - Test-read
 - Format-read
 - Write-data
 - Write-format
 - Diagnostic-read
- Search-read functions
 - Search-read-equal
 - Search-read-high-or-equal
 - Search-read-low

2.7.1. Positional Functions

The positional functions align the heads over the specified cylinder. Data transfers do not occur with these functions and the track position is not automatically verified.

2.7.1.1. Seek Function

The seek function positions the accessor to the cylinder address provided by the PCB. When positioned properly, an attention-interrupt request is generated and an interface status byte is presented.

The seek function requires the following PCB parameters:

<u>PCB byte</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	Device address	0 to 3
1	Function byte	11
4,5	Cylinder address	See 2.6.4
6	Head address (fixed head only)	See 2.6.4

No track verification is performed by this function.

If the disk drive completes the seek operation or an error is detected, an attention-interrupt request is generated and the appropriate status is transferred.

The seek function is not required for fixed head access.

2.7.1.2. Recalibrate Function

The recalibrate function clears a fault from the disk drive and then repositions the actuator to a known position, cylinder 0. This function is issued if a seek error occurs or successive track mismatches occur.

This function requires the following PCB parameters:

<u>PCB byte</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	Device address	0 to 3
1	Function byte	10 ₁₆

After the recalibrate operation is completed, an attention-interrupt request is generated and status is transferred. The positioning time for a recalibration function is a maximum of 250 milliseconds.

2.7.2. Read/Write Functions

The read/write functions transfer data between the host system and the disk drive. These functions, with three exceptions, result in the transfer of one or more 256-byte data fields. The exceptions are:

1. The read-ID function reads the ID field, then transfers the first five bytes of the field by way of the peripheral status block (PSB).
2. The format-write function writes the entire track, which results in a transfer of the ID field data.
3. The test-read function does not transfer any data to the system (host).

All read/write functions execute a seek function for the cylinder specified in the PCB. At this time, the implied seek suppress bit is set to 0 and the seek function verifies the cylinder (except for format-write and read-ID functions) and track address.

If the implied seek suppress (PCB 2, bit 5) is set to 1, no seek function is performed. Therefore, all executed read and write functions assume that the accessor is positioned to the desired cylinder specified in bytes PCB 4 and PCB 5.

All read and write functions (except diagnostic-read, read-ID, format-read, and format-write) can execute as multitrack and multicylinder operations. The function switches to the next sequential track when the last sector on a track has been processed and the sector count is not 0. When the last track (13) on a cylinder has been processed and the sector count is not 0, the function switches to the next cylinder if the next cylinder is within the user cylinder limits and the implied seek suppress bit (PCB 2, bit 5) is not set. A volume overflow error is presented by the controller if the sector count is not 0 and the last sector within the user cylinder limits has been processed.

Functions processed on cylinders 544 through 560 are limited to that cylinder (no cylinder switching is performed). A volume overflow error is presented by the controller if the sector count is not zero, and the last sector on the last track of the cylinder has been processed.

The read/write functions (excluding diagnostic-read, read-ID, format-read, and format-write) scan the ID fields for the starting sector address. If an ECC error occurs in an ID field during the sector scan, the scan continues. If an ECC error occurs in an ID field after finding the starting sector of a multisector operation, the function is immediately terminated and the ending status reports the error conditions. Error correction is not performed on the ID fields. Note that a data field can only be processed if its associated ID field is read. If an ID field is unrecoverable, a diagnostic-read function is available to recover the data field. This function allows one sector to be read, assuming that the previous ID field was read error free.

After successfully finding the appropriate ID field, the data field is processed. The smallest addressable block of data is one sector (256 bytes). If an ECC error is detected while reading the data and ECC correction is not suppressed (PCB 2, bit 7 set to 0), the controller performs an error correction operation and transfers the corrected data to the host system. This operation is performed using the interface buffer that contains the disk data retrieved from the last sector read. The ECC remainder is divided with the ECC polynomial by the firmware. If the error is determined correctable, the buffer is updated and the read function continues. Otherwise, the function is terminated. In either case, detailed status is presented for host system error recovery or error logging purposes. Only one error is described by the peripheral status block; thus, an operation is terminated upon the detection of a second error of any type.

2.7.2.1. Read-ID Function

The read-ID function selects the specified read/write head (track), scans for the first error-free ID field, and returns the contents of the field to the host system as part of the completion status.

The PCB parameters required for this function are:

<u>PCB byte</u>	<u>Bit</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	—	Device address	0 to 3
1	—	Function byte	21 ₁₆
2	1,0	Function modifier	See 2.6.3.
6	—	Head address	See 2.6.4.

The track offset control bits in the function modifier are valid. If a track offset is specified, the controller resets the offset register to zeros (no offset) following the execution of the function. After the error-free ID field is located, an attention-interrupt request is generated. The five most significant bits in the ID field are transferred to the host system in the peripheral status block. A read-status-block command sequence is required to retrieve the peripheral status block. If offset is specified, the interrupt is delayed for an additional 10 milliseconds before initiating the interrupt. This ensures that the heads are on track before another operation is initiated.

This function is normally used following a freestanding seek operation to verify the cylinder address.

2.7.2.2. Read-Data Function

The read-data function selects the specified track and scans for the starting sector ID field. When found, the associated data field is read and transferred to the host system. The sector count parameter is then decremented and the sector address parameter is incremented. Successive ID fields are read and each data field is transferred. This function is terminated if one of the following conditions occur:

1. Sector count register is decremented to 0.
2. An ID field ECC occurs after the starting sector was found.
3. An error is detected and a previous ECC was corrected while processing a data field.
4. The operation was not completed within a specified time period. This period begins upon receipt of the PCB and concludes after an integral number of index marks have been encountered.
5. Expected values for the sync and head address do not compare with information from the disk drive.
6. The function bytes and function modifier bytes specify an operation that cannot continue because of a discrepancy between the form of the data on the track and that assumed for the operation to continue.

The read-data function uses the following PCB parameters:

<u>PCB byte</u>	<u>Bit</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	—	Device address	0 to 3
1	—	Function byte	2016
2	7,5,4,3,1,0	Function modifier	See 2.6.3.
4,5	—	Cylinder address	See 2.6.4.
6	—	Head address	See 2.6.4.
7	—	Sector address	See 2.6.4.
8,9	—	Sector count	See 2.6.5.

If error correction is enabled (PCB 2, bit 7 set to 0) the disk data transfer is suspended upon detection of an ECC error. If it is correctable, the buffer is updated. The operation then continues using this corrected data. The ECC correction bit is set in the peripheral status block (PSB) and interface status byte to indicate that an error correction was performed. If the error is not correctable or a previous error was noted, the function is terminated and error status is presented.

If an implied seek operation is specified (PCB 2, bit 5 set to 0) the cylinder address value is used for a seek operation prior to the execution of the read-data function. If alternate/defective track management is specified (PCB 2, bit 4 set to 0), the FDC positions the heads to the alternate cylinder address obtained by

reading the ID field of the defective track. Using the ID information originally specified, data on the alternate track is processed. If no errors occur, a seek to the original cylinder to complete the function, if necessary, takes place. If byte mode is specified (PCB 2, bit 3) data is transferred in the byte mode. Otherwise, the transfer occurs in burst mode.

If head offset was specified (PCB 2, bits 1,0), the attention-interrupt request is delayed an additional 10 milliseconds after the offset operation. This ensures that the heads are on track before the next function is executed. Offset is cleared by the controller after the read operation has been completed on the track. Offset is implied only on the first track of a multitrack operation. The head and sector address bytes specify the starting sector address and the sector count bytes specify the numbers of sectors for this operation.

2.7.2.3. Test-Read Function

The test-read function is similar to the read-data function except that no data is transferred. The specified sectors are read and data errors are checked. If all data fields are read without error, a normal completion status is presented. Otherwise, the error is indicated in the peripheral status block and the operation is terminated.

If the ECC suppress bit (PCB 2, bit 7) is set to 0 and an ECC error is detected, the controller performs the correction but no data is transferred. The peripheral status block indicates the error status condition and sector address. If the ECC suppress bit is set to 1 and an ECC error is detected, no correction is made and the ECC remainder is passed to the system host by way of the peripheral status block.

More than 90 cylinders (65,535 sectors) can be verified in one operation by setting the appropriate parameters in the PCB.

Function parameters specified for the read operation apply to this function, but the function code must be set to 28₁₆. The function modifier bit 3 (byte/burst mode) is not applicable because no interface transfer takes place.

2.7.2.4. Format-Read Function

The format-read function is a special read operation used on cylinder 559 (022F₁₆). This cylinder contains surface defect information that is recorded during manufacturing using a unique track format. The defect map is written in sextuplicate on heads 0, 1, 2, 9, A, and B of cylinder 559. There are 32 sectors per track. The starting sector can be of any value from 00 to 28 (00₁₆ to 1C₁₆). The sector count is 4, which permits any 4 sector reads to be performed.

This special track format does not contain ECC bytes that are normally appended to the data fields. As a result, data errors are not detectable by the controller. The integrity of the data is assured by reading two of the six tracks and comparing the data. Because 0, 1, 2, 9, A and B are exact copies and two of the six tracks are guaranteed to be free of defects, at least two tracks compare when no errors exist. The PCB parameters for the format-read function are:

<u>PCB byte</u>	<u>Bit</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	—	Device address	0 to 3
1	—	Function byte	24
2	3, 1, 0	Function modifier	See 2.6.3.
4,5	—	Cylinder address	559 (022F)
6	—	Head address	0, 1, 2, 9, A, B
7	—	Sector address	Variable (maximum 1C)
8,9	—	Sector count	04

This function is for limited use and is restricted to cylinder 559. The controller provides the cylinder address when the function is decoded.

Data transferred to the system (host) is in 1024-byte increments or 4 sectors.

A miscompare of the flag, cylinder, head, or sector byte causes an error and the format-read function terminates.

2.7.2.5. Write-Data Function

The write-data function selects the specified track and scans for the starting sector ID field. When found, its associated data field is written using the data transferred from the host. The scan operation continues as described for the read-data function (2.7.2.2). All the function parameters are the same, except for the function code, which is 40_{16} . Also, the function modifier bits specified for the read-data function apply to write-data, except the offset and ECC suppress bits, which are ignored.

No data fields are written unless the ID field for that sector compares exactly, including verification of the check characters.

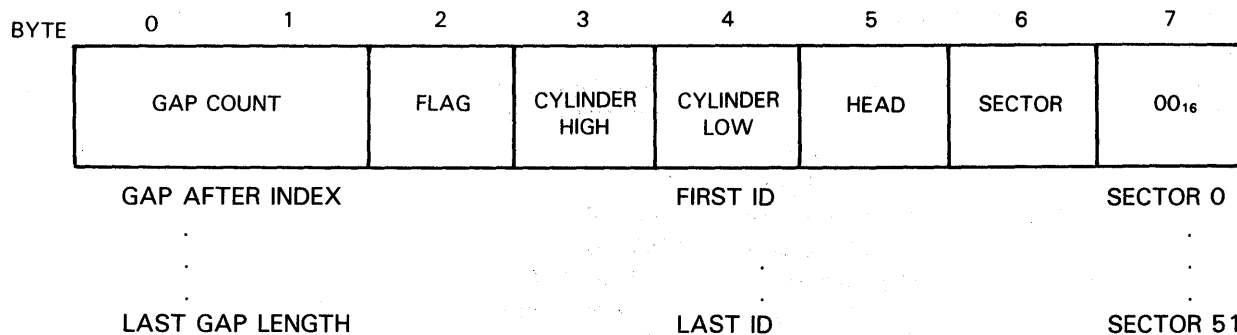
2.7.2.6. Format-Write Function

The format-write function records the basic track format. An entire track is written, including gaps, ID fields, data fields, and check characters. This function selects a head (track) and formats the track.

If an implied seek is enabled (PCB 2, bit 5 set to 0), a seek function to the cylinder specified in the PCB is performed prior to the format-write operation. Cylinder address verification is suppressed because the track may not be formatted.

The controller provides all gap characters, address mark characters, data field characters, check characters, timing, and sequence control for the entire write operation. Variable gaps exist between the ID field and the preceding data field. A minimum gap is provided by the controller. Additional gap spacing in excess of the minimum can be specified by the gap count bytes provided as part of this function. This variable gap provides a way to shift the sector location to avoid known surface defects. This is achieved by accessing the list of the defective areas on the recording surfaces (recovered by the format-read function) and using this list to vary the gaps so that all defects fall within gaps.

The ID fields, along with the variable gap values, are conveyed to the controller in the data transfer phase of the function. All gap counts and ID fields are transferred as a fixed-length block of data (416 bytes). This block transfer is accomplished in byte mode and must be successfully completed before track format recording can start. The transferred data block to the controller contains the intersector gap counts and ID field data within the following format:



The gap count field is the binary value of the number of bytes in the gap and must not exceed an accumulated value of 2044 (07FC₁₆) for all 52 sectors.

The controller accommodates the total number of variable gap bytes and rejects it when the maximum of 2044 bytes is exceeded. All gap counts must be even (LSB of byte 1 set to 0). Each gap count is checked for an even number; the function is rejected if it is not even. At the same time, the illegal format bit is set in the peripheral status block.

If it is determined that the 52 sectors cannot be recorded on the track due to the extent or the location of the defects, the track is flagged as defective. All ID field flag bytes must indicate a defective track condition and the track must be formatted with minimum gap spacing.

Software must flag and designate defective and alternate tracks. If the track being formatted is designated defective, the ID field must contain the cylinder address of its alternate track. Also, the ID field of the alternate track must contain the cylinder address of the defective track.

The controller starts the format-write operation at the index and proceeds using the gap count values provided to control the size of the intersector gaps. The contents of the ID fields are obtained from the contents of the data transferred. The controller appends the appropriate check characters. The controller generates the data field and fills this field with the worst-case repetitive data pattern, D9AC₁₆.

The PCB parameters required for this function are:

PCB Byte	Bit	Name	Value (hexadecimal)
0	—	Device Address	0 to 3
1	—	Function Byte	44
2	5	Function Modifier	See 2.6.3.
6	—	Head address	See 2.6.4.

Status is presented following the format-write operation or if an error is detected.

2.7.2.7. Diagnostic-Read Function

Diagnostic-read is a special function used only to recover marginal data that cannot be recovered using normal read functions. A data field cannot be read unless its address field (ID) is first retrieved. If this ID field is read in error, the data field is not recoverable. The diagnostic-read function recovers the data field by scanning for the previous ID field (which must be error free) and skipping ahead to the data field of the next sector specified by the PCB. Since variable intersector gaps can be specified, the operation of this function depends upon recovery of the address mark for the sector specified in the PCB. The PCB parameters required for this function are:

PCB byte	Bit	Name	Value (hexadecimal)
0	—	Device address	0 to 3
1	—	Function byte	26
2	7, 5, 4, 3, 1, 0	Function modifier	See 2.6.3.
4,5	—	Cylinder address	See 2.6.4.
6	—	Head address	See 2.6.4.
7	—	Sector address	See 2.6.4.
8,9	—	Sector count	01

2.7.3. Search-Read Functions

The search-read functions search the data field of a sector for a unique key. If the conditions of the search are satisfied, the data field is read and transferred to the host. Search operations process the sectors specified by the starting sector number and sector count. Once the search condition is satisfied, the data field containing the key field satisfying that search condition is transferred to the host and the operation is terminated.

A key argument is transferred to the controller as an extension of the PCB search parameters. This block is transferred in a separate data transfer sequence and its length is defined by the key length parameter (PCB A). This transfer is always in byte mode.

All search-read functions search in one of two modes. The multikey mode assumes that each sector is subdivided into smaller, equal-sized addressable data fields called records. Within each record, and at the same relative position, is a key field. The key field is compared with the search argument provided by the host system. In this mode, the search-read function compares the key bytes within all records of the sector.

The second mode assumes only one record per sector and searches only the one record specified by the initial displacement parameter.

Bit 6 of the function modifier (PCB 2) is used to specify the transfer mode of a sector returned to the host.

The search-read-high/equal function requires that the key data be written in ascending order. Data of the least magnitude must be in the first key of the first sector searched. Comparison is made between the disk and the key buffer, hence a 2 on the disk compared to a 1 from the key buffer satisfies the greater-than (high) requirement. The search-read-low function requires that the disk key fields be written in descending order.

If the search-immediate-suppress bit in the function modifier (PCB 2, bit 2) is not set to 1, a nonequal search operation begins immediately. This is true as long as the first sector encountered is within the range of the starting and ending sectors and the disk data is greater than (search-low) or less than (search-high/equal) the search key argument on the first sector encountered. Otherwise the operation is deferred until the starting sector is processed.

If search-immediate-suppress is active, the search operation unconditionally begins at the starting sector.

The search operation terminates when the search conditions are satisfied or a noncorrectable data error or multiple data errors are detected on the data within the range of sectors specified. A data error encountered on a data field outside the sector range is ignored. If an ECC error is detected, the search operation is suspended and the data in error is corrected. The buffer containing this data is then searched. Normally, for performance reasons, the disk data is compared byte by byte to the key argument as it is read from the disk drive unit. If the data in the buffer satisfies the search, the buffer is transferred to the host in a manner similar to a normal search operation without error correction. If the search condition is not satisfied, the search operation simply continues with the next sector.

If an error correction operation is performed, the ECC correction bit is set in the peripheral status block and the sector address is indicated for error logging purposes.

Search-read functions operate similarly to the read-data function regarding specification of the starting sector and sector count parameters. The sector count byte, unlike other functions, determines the number of sectors included in the search operation, not the number of sectors transferred. Only one sector is transferred to the host system in search operations. That sector is transferred under the following conditions:

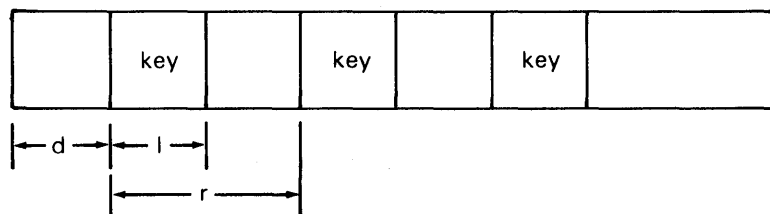
- When the search conditions are met
- When an ECC error occurs on a data field within the sector range specified and the ECC suppress bit is set to 1
- When an ECC error occurs on a data field within the sector range specified and a previous data field has already been ECC corrected

As part of the PCB, the following search parameters must also be specified:

- Initial displacement (PCB B)
- Key length (PCB A)
- Record size (PCB C)

Initial displacement indicates the absolute number of bytes that are skipped from the beginning of the data field to the start of a comparison. The key length indicates the length of the key and up to 256 bytes can be specified.

For multikey search operations, record length specifies the number of bytes in a record; therefore, subsequent keys can be located throughout the data field. Following the displacement, the controller compares (byte by byte) the data read from the disk to the argument that is stored in the key buffer. The comparison terminates when either the end of the data field is reached or when a field is read that satisfies the search condition. If a multikey operation is specified, the controller transfers the contents of the entire sector containing the key field satisfying the search to the host. The following format is required for proper execution of the search-data function:



where:

d

Is the initial displacement (PCB B); the number of bytes skipped prior to the first key field (0 to 255, where 0 indicates no displacement) in each sector.

l

Is the search key length (PCB A); a value equal to the number of bytes in the key field that are to be compared (0 to 255, where 0 is 256 bytes).

r

Is the key record size (PCB C); a value equal to the key length plus the number of bytes to the beginning of the next key (6 to 255) including 0, where 0 indicates 256 bytes. This is used only for multikey search; PCB 2 bit 6 set to 0.

These parameters must be specified in a valid manner or the controller rejects the function and presents a peripheral status block with the function reject bit set. The following checks are made:

$$\begin{aligned} r &\geq 6(0=256) \\ r-1 &\geq 5 \\ d+1 &\geq 256 \end{aligned}$$

The number of searched multikey fields is determined by the controller using the displacement and record size values that have only key fields fully contained within the data field searched. Unused space at the end of a sector is skipped.

Following the transfer of the PCB, the controller requests the transfer of the key argument. The key argument length, specified in PCB A, is used to determine the number of transferred bytes. The key argument is transferred in a separate data transfer sequence. Following this transfer, the system host must prepare to accept a 1-sector transfer (256 bytes), depending upon the result of the search operation.

2.7.3.1. Search-Read-Equal Function

This function requires that the search key information compares exactly before the data field can be recovered. It always begins the search operation at the starting sector location. Single or multikey searches can be specified. The search continues until:

- the sector count decrements to zero;
- a cylinder overflow condition is detected;
- an ID scan or format error is detected;
- a second data error is detected; or
- a key field match is found.

The following PCB parameters must be specified:

<u>PCB Byte</u>	<u>Bit</u>	<u>Name</u>	<u>Value (hexadecimal)</u>
0	—	Device address	0 to 3
1	—	Function byte	22
2	7, 6, 5, 4, 3, 1, 0	Function modifier	See 2.6.3.
4, 5	—	Cylinder address	See 2.6.4.
6	—	Head address	See 2.6.4.
7	—	Sector address	See 2.6.4.
8, 9	—	Sector count	See 2.6.5.
A	—	Search key length	See 2.6.
B	—	Initial displacement	See 2.6.
C	—	Key record size	See 2.6.

If the search condition is satisfied, the sector is transferred to the host, and normal completion status is presented. The unsuccessful search bit is set in the interrupt status byte and in the peripheral status block if the search condition is not satisfied and no error conditions are detected.

2.7.3.2. Search-Read-High/Equal Function

The search-read-high/equal function operates in much the same way as the search-equal function, except the search condition is satisfied with a high or equal condition. A low to high transition, except for the first field, is required to satisfy the high condition. If a search-high condition is satisfied, a detail status condition (PSB 2, bit 1) is set. A function byte value of 23₁₆ specifies this function.

2.7.3.3. Search-Read-Low Function

The search-read-low function operates in much the same way as the search-equal function, except the search condition is satisfied with a low condition. A high to low transition (except for the first field, which must be low) is required to satisfy the low condition. If a search-low condition is satisfied, a detail status condition (PSB 2, bit 1) is set. A function byte value of 25₁₆ specifies this function.

2.8. COMPLETION STATUS SEQUENCE

Completion status for an operation is passed back to the controlling system at two levels – interrupt status level and peripheral status block (PSB) level. Interrupt status level indicates normal or abnormal completion for an operation or a segment of an operation. This status is generally sufficient for normal completions. However, if an abnormal condition is indicated or a more detailed status is required pending a normal completion, the PSB should be requested.

The PSB contains a summary status byte and 15 additional bytes that detail additional drive and controller status and sense data required for error recovery or error logging purposes.

Unlike the read/write functions that generate a PSB to detail the exact cause of an abnormal termination, the positional functions (recalibrate and seek) do not generate a PSB because the interrupt status is sufficient to specify the logging and retry procedures.

2.8.1. Peripheral Status Block Format

The PSB of each host system consists of 16 bytes of data (defined in Table 2-9). The PSB of each host is valid until a new PCB is issued by that host.

Table 2-10. Valid PCB Parameters

Function	PCB 0	PCB 1	PCB 2										PCB 3	PCB 4 and PCB 5	PCB 6	PCB 7	PCB 8 and PCB 9	PCB A	PCB B	PCB C	PCB D, PCB E, and PCB F
	Device Address	Function byte	ECC suppress	Multikey suppress	Implied seek	Alternate/defective Track suppress	Byte mode	Search immediate suppress	Offset minus	Offset plus	Not used	Cylinder address	Head address	Sector address	Sector count	Search key length	Initial displacement	Key record size	Not used		
			7	6	5	4	3	2	1	0											
Seek	0-3	11 ₁₆										X									
Recalibrate	0-3	10 ₁₆																			
Read-ID	0-3	21 ₁₆							X	X			00D ₁₆								
Read-data	0-3	20 ₁₆	X		X	X	X		X	X		X	00D ₁₆	0-33 ₁₆	X						
Test-read	0-3	28 ₁₆	X		X	X			X	X		X	00D ₁₆	0-33 ₁₆	X						
Format-read	0-3	24 ₁₆					X		X	X		22F ₁₆	0-02 ₁₆ 9-B ₁₆	0-1C ₁₆	4						
Write-data	0-3	40 ₁₆			X	X	X					X	0-0D ₁₆	0-33 ₁₆	X						
Format-write	0-3	44 ₁₆			X							X	0-0D ₁₆								
Search-low	0-3	25 ₁₆	X	X	X	X	X	X	X	X		X	0-0D ₁₆	0-33 ₁₆	X	0-FF ₁₆	0-FF ₁₆	6-FF ₁₆			
Search-high/equal	0-3	23 ₁₆	X	X	X	X	X	X	X	X		X	0-0D ₁₆	0-33 ₁₆	X	0-FF ₁₆	0-FF ₁₆	6-FF ₁₆			
Search-equal	0-3	22 ₁₆	X	X	X	X	X		X	X		X	0-0D ₁₆	0-33 ₁₆	X	0-FF ₁₆	0-FF ₁₆	6-FF ₁₆			
Diagnostic read	0-3	26 ₁₆	X		X	X	X		X	X		X	0-0D ₁₆	0-33 ₁₆	X						

Cylinder	Sector Count
0-21F ₁₆	1-FFFF ₁₆
220-230 ₁₆ (EXC 22F ₁₆)	1-2D8 ₁₆

Cylinder Address	
0-87 ₁₆ 25MB	and 220 ₁₆ - 230 ₁₆ BUT NOT 22 ₁₆
0-10F ₁₆ 50MB	
0-197 ₁₆ 75MB	
0-21F ₁₆ 100MB	

Table 2-11. Peripheral Status Block Bit Descriptions (Part 1 of 4)

Name	PSB/Bit	Description
PSB 0 Summary Status		
Function reject	0, 7	Indicates the detection of an invalid parameter within the PCB prior to the execution of that function
Device ready	0, 6	Indicates that the drive is ready to execute a command. The following are drive conditions that cause this bit to be set to 1: <ul style="list-style-type: none"> ■ Drive selected ■ No unsafe conditions ■ Successful power-up sequence
Unsuccessful search	0, 5	Indicates that a record was not found in a search operation that ended normally
Sector not found	0, 4	Indicates that the desired sector was not found within a full disk revolution, or the FDC could not recover from a false address mark (AM)
Device end	0, 3	Indicates that the outstanding operation has completed without error (a successful ECC correction is not considered an error), and the FDC is ready to accept a new function
Unit check	0, 2	Indicates an abnormal condition was encountered while executing a function
Flag not zero	0, 1	Indicates the alternate/defective track suppress function modifier bit is set to 1 (PCB 2, bit 4) and either: <ul style="list-style-type: none"> ■ the function terminated normally on a defective or alternate track; or ■ the function was terminated in attempting to switch to or from an alternate or defective track. <p>This bit is not set and has no meaning if alternate/defective track management is invoked. PCB 2, bit 4 is not set.</p>
ECC correction	0, 0	Indicates an error correction operation was performed on the sector whose address is indicated in PCB C through PCB F. This bit is applicable only if error correction is enabled (PCB 2, bit 7 set to 0). If device-end bit is also set, the function completed successfully. If unit-check bit is also set, an additional error is indicated that prevents a successful completion.

Table 2-11. Peripheral Status Block Bit Descriptions (Part 2 of 4)

Name	PSB/Bit	Description
PSB 1 Detail Drive Status		
File protect	1, 7	The selected drive is file protected by the FILE PROTECT control on the operator panel.
Servo malfunction	1, 6	<p>Indicates attempt to select a fixed head was unsuccessful or a servo malfunctioned. The conditions causing a servo malfunction are:</p> <ul style="list-style-type: none"> ■ P LO unsafe ■ Write unsafe ■ Write servo offset unsafe ■ Index error <p style="text-align: right;">} Unsafe and not ready (FAULT CLEAR resets condition.)</p> <ul style="list-style-type: none"> ■ DC power unsafe ■ Disk speed unsafe <p style="text-align: right;">} Unsafe and not ready (POWER ON clears condition.)</p> <ul style="list-style-type: none"> ■ Guard band at wrong time ■ Illegal cylinder ■ Offtrack condition ■ Seek time expired (216 ms) <p style="text-align: right;">} Servo malfunction (RECAL resets condition.)</p>
Drive function terminated	1, 5	<p>During a write function, this bit indicates the function was terminated prior to normal completion. The sector being written at the time of termination is incompletely written and results in read errors for any subsequent read operations. Therefore, if set, an immediate rewrite should be issued. If a read operation is being executed, this bit indicates the function was terminated due to system host deselection prior to normal completion. Disk data is not altered; however, the positioner may have moved.</p> <p>A function can be terminated due to the detection of an abnormal condition in the disk drive, controller, or interface.</p>
Early warning	1, 4	Indicates the thermal sensing unit within the FDC cabinet has detected excessive heat. If uncorrectable and temperature continues to increase, AC power at the controller goes off and the disk drives are placed into standby mode.
AM not found	1, 3	Indicates an address mark cannot be located by the disk drive
Sync error	1, 2	Indicates error was found when reading the sync bytes in the data field or the sync bytes were not found in the required time frame
ID field error	1, 1	Indicates the detection of an ECC error in the ID field
Data field error	1, 0	Indicates the detection of an error in a data field. When set in conjunction with sync error, it indicates a data field sync error. When set alone, it indicates an ECC error in the data field. If error correction is specified (PCB 2, bit 7 is set to 0), this bit is set if the error is not correctable. If PSB 0 is also set, then a data field error in a previous sector has been corrected and no correction is attempted on this sector.

Table 2-11. Peripheral Status Block Bit Descriptions (Part 3 of 4)

Name	PSB/Bit	Description										
PSB 2 Detail FDC Status												
FDC parity error	2, 7	Indicates a parity error detected with the controller data path										
Illegal cylinder address	2, 6	Indicates that the cylinder address specified in the function packet is too large for the drive configured or falls within a reserved track area such as cylinder 559.										
Illegal format	2, 5	Indicates that an illegal PCB parameter was detected while the function was being executed: <ol style="list-style-type: none"> 1. Format write <ul style="list-style-type: none"> Odd gap length or cumulative gap length exceeded the maximum value 2. Invalid parameter <ul style="list-style-type: none"> Invalid starting sector, head, or sector count with the possibility that implied seek was performed 3. Zero sector count <ul style="list-style-type: none"> Zero sector count in PCB and PSB 2, bit 4 set 										
Cylinder, volume overflow	2, 4	Indicates an attempt was made to index past the uppermost valid cylinder because the sector count register was not equal to 0 following the operation on the last sector										
Cylinder miscompare	2, 3	Indicates a miscompare between the cylinder address value and the contents of the ID field during an implied seek operation or alternate track management										
Not used	2, 2	Set to 0										
Search satisfies high/low	2, 1	Indicates that the greater-than condition of the search-high-or-equal functions was satisfied or the search-low function was satisfied										
Alternate track	2, 0	Set while invoking alternate track management, the seek to the alternate track was unsuccessful, the alternate and defective track ID fields do not properly cross-reference each other, or function terminated in error on the alternate track										
PSB 3 Flag Byte												
Not used	3, 7-2	Set to 0										
FF bits	3, 1-0	FF bits defined as follows: <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: left;"><u>Bit 1, 0</u></th> <th style="text-align: left;"><u>Track Condition</u></th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Good track</td> </tr> <tr> <td>10</td> <td>Defective track</td> </tr> <tr> <td>01</td> <td>Alternate track</td> </tr> <tr> <td>11</td> <td>Defective track</td> </tr> </tbody> </table>	<u>Bit 1, 0</u>	<u>Track Condition</u>	00	Good track	10	Defective track	01	Alternate track	11	Defective track
<u>Bit 1, 0</u>	<u>Track Condition</u>											
00	Good track											
10	Defective track											
01	Alternate track											
11	Defective track											
PSB 4, PSB 5 Cylinder Address												
Cylinder address	4, 7-0 5, 7-0	Specifies (in two bytes) the cylinder being processed. If the alternate track bit is set (PSB 2, bit 0), the head may not physically be at this location										

Table 2-11. Peripheral Status Block Bit Descriptions (Part 4 of 4)

Name	PSB/Bit	Description
PSB 6, PSB 7 Head Address, Sector Address		
Head address	6, 7-0	Specifies (in two bytes) the head and sector address bytes of the ID field from the last sector processed. If an error prevents the data field from being processed, these bytes are the head and sector bytes of the sector expected to be processed. If alternate track processing is involved, the head address is that of the defective track.
Sector address	7, 7-0	
PSB 8 Sector Count High		
Sector count high	8, 7-0	Specifies the high residual sector count value
PSB 9, Sector Count Low		
Sector count low	9, 7-0	Specifies the low residual sector count value
PSB A		
Not used	A, 7-0	Not defined
PSB B Search Displacement Byte		
Search displacement	B, 7-0	Contains the binary value of the number of bytes preceding the key field within a sector satisfying a search condition (for search operation only).
PSB C through PSB F ECC Bytes		
ECC or cylinder address high	C, 7-0	<p>These four bytes are used for ECC management and are dependent on the ECC suppress bit setting in the function modifier PCB 2, bit 7.</p> <p>ECC suppress set to 0:</p> <p>If error correction is specified to be performed, these bytes are defined as follows:</p> <ul style="list-style-type: none"> ■ PSB C Cylinder high ■ PSB D Cylinder low ■ PSB E Head address ■ PSB F Sector address <p>These bytes contain the sector address of the sector on which an error correction was successfully performed as indicated when the ECC correction (PSB 0, bit 0 and interface status bit 3) status bits are set to 1. If these two bits are not set, the bytes are not defined.</p> <p>ECC suppress set to 1:</p> <p>If error correction is specified as "not to be performed", these bytes contain the 4-byte ECC remainder and are used for host error correction or error logging purposes.</p>
ECC or cylinder address low	D, 7-0	
ECC or head address	E, 7-0	
ECC or sector address	F, 7-0	

2.9. READ DATA ERROR CORRECTION

Read errors detected in the data field can generally be corrected by use of the ECC. Corrective action is attempted by the firmware routine in the controller; system software is not required to correct data errors. As a result, the ECC check bits are passed through a serial shift register in order to generate a read check bit group (four ECC bytes). Controller hardware signals a condition of all zeros in the group, indicating error-free data retrieval. If an error condition is signaled instead, a firmware routine is invoked and data correction is attempted. Successful correction is indicated to the controller by the correction routine, and control is returned to the firmware. The firmware then continues with the operation; completion status indicates the occurrence of the data correction operation. If the error is not correctable by the correction routine, rereading of the data is required.

2.10. ERROR RATES

The disk drive and controller error rate are determined from errors attributed to the disk drive only and do not include data errors attributed to flagged media imperfections. Media defects are managed by the use of defect skipping techniques and an error correction code for data fields.

2.11. SURFACE DEFECT MANAGEMENT

Because some uncertainty exists in mapping the defect into a particular sector or the possibility of the appearance of an undefined defect, it is necessary to perform a surface analysis following the initialization procedure. Additional uncorrectable errors are included and the appropriate tracks reinitialized.

2.11.1. Disk Initialization Procedure

Initialization can be invoked and executed on all cylinders (except 559, the defect information cylinder), a few specified cylinders, or one track alone.

Additional defects that occur after the drive is shipped or installed are determined empirically during surface analysis. To assist in avoiding defects, a defect map is written in sextuplicate on tracks 0, 1, 2, 9, A, B, or cylinder 559. Also, a printout accompanies the disk drive. It identifies all additional defects discovered in the manufacturing process after the defect map is written.

From these two sources, the initialization program receives the inputs required to start. To obtain the defect records from the disk drive, a format-read function must be executed.

The format-read function reads multiples of four sectors from the track specified in the PCB. Data from the tracks are recovered and compared to ensure that the data is free of errors. This comparison is required because no parity checking codes are appended to the data fields.

If the two blocks of data do not compare, the defect map from one of the remaining tracks must be read and compared with the map retrieved from either of the first tracks. Because two of the six tracks are guaranteed as being defect free, a match occurs before completely exhausting the head combinations. If a recoverable error occurs during a read operation, the head combination could be exhausted without a comparison. This necessitates a retry of the initialization procedure.

In order to format any track, the appropriate value of the gap count must be determined. These two bytes precede each ID field that is transferred to the FDC as part of the format-write operation. These bytes are used to determine the length of the variable gap between the ID field and the preceding data field.

2.11.1.1. Format Considerations

Disk storage capacity is based on the availability of 52 sectors per track resulting in 2044 uncommitted bytes. These bytes are available to assign as needed to avoid defects. There are 344 bytes in an entire sector, including gaps, ID field, ECC, etc. If an entire sector plus a 2-byte pad cannot be written between the last ECC byte and a defect, the initialization program assigns a gap count equal to the number of bytes between the last ECC byte and the defect. The next sector is then written starting immediately after this gap.

Variable gaps containing a defect must comply with the following when determining gap count:

1. All gap counts must be an even number of bytes, rounded down when required.
2. Variable gaps cannot occur between the ID field and its data field.
3. The total bytes used do not exceed 2044 bytes.

Alternate or defective track assignments are invoked where:

- the cumulative skip bytes exceeds 2044 bytes; and
- the defective map indicates that the track must be declared defective (flag = 20₁₆).

Alternate and defective management requires that all ID fields on the defective track have its alternate track number instead of the physical track number. The alternate ID contains the track address of the defective track.

2.11.1.2. Disk Surface Initialization

The following procedure is recommended to initialize the disk surface:

1. Read the surface defect map from track 559 from two different heads and compare the data. If there is no comparison, read and compare other head combinations until a data comparison occurs.
2. Collect all manual defect entries. Defective locations are specified as either a bit location from the index or a sector number.
3. Build a track ID format using the appropriate variable gaps. The gap sizes and ID field contents are presented to the FDC using the format-write function.
4. Write the disk, one track at a time, using the format-write function. Continue procedure until all tracks are formatted.
5. After formatting is complete, the entire disk must be verified using a test-read function. A multisector read can be used to determine if any errors exist.
6. A total of four read-verify passes must be made to ensure that all surface defects are skipped. If one ECC correctable error occurs during any verify pass, a transient error is presumed and the sector is not skipped. If more than one error is detected, a defect is presumed in the data field and the sector must be skipped by expanding the gap accordingly. If 52 good sectors cannot be written, the track must be flagged defective and an alternate assigned. Analysis of where the error occurred (ID field or which bytes in the data field) should be made to keep the gap count to a minimum.

A large defect in the intersector gap may appear as a false address mark (AM) to the controller. If the distance between the false AM and the real AM for a sector is less than 25 bytes, then the controller is not able to ignore the false AM and a sector-not-found error results. This defect may be successfully skipped by increasing the gap count, before the sector that is in error, to ensure at least 25 bytes between the false AM and the real AM.

2.12. CYLINDER ASSIGNMENTS

The disk has movable head cylinders and fixed-head cylinders. The movable head cylinders are divided into user cylinders and specially assigned innermost cylinders.

2.12.1. Movable Head Cylinders

Cylinders 0 through 543 are the user cylinders. These are divided equally to achieve four configurations. The total storage capacity is 25, 50, 75, or 100 megabytes, respectively. The last valid cylinder for each of the four capabilities is 135, 271, 407, and 543, respectively.

The FDC firmware checks the capacity configuration and rejects the specified function if the cylinder address is greater than the last cylinder of that configuration but less than cylinder 544. The remaining 17 innermost cylinders are assigned as follows:

- System use/miscellaneous (cylinder addresses 544–548)

These five cylinders are available for various system functions required by the host system. These cylinders are always addressable regardless of the capacity configuration. Automatic cylinder switching is not permitted on these cylinders.

- Alternate cylinders (cylinder addresses 549–551, 553–558)

These nine cylinders are used as alternate tracks for any defective tracks located within the user cylinders, system cylinders, or diagnostic cylinders. Alternate tracks should be assigned only if the requirement previously established for disk initialization procedures cannot be fulfilled. These cylinders are addressable by the FDC regardless of the capacity configured.

- Diagnostics (cylinder address 552)

This cylinder is reserved for firmware-based diagnostic purposes. As part of the diagnostic operation, the disk drive is tested by writing and reading data to this cylinder. The first seven sectors are used. The disk initialization procedure (prepping) accomplished at the factory uses part of this cylinder for software tables. The diagnostic cylinder is placed in the middle of the alternate cylinders for 8402 disk drive compatibility.

- Surface defect map (cylinder 559)

This cylinder contains a tabulation of surface defects located on the head disk assembly (HDA). This information is used by the disk initialization program. It is addressable only by the format-read function.

- Customer engineering (cylinder 560)

This cylinder is reserved for customer engineering use. It is addressable by the FDC regardless of the configured capacity.

2.12.2. Fixed Head Cylinders

When cylinders 1024 to 1028 (400_{16} to 404_{16}) are addressed, they access the fixed head tracks. The controller performs the address translation from the logical cylinder address (cylinder address, track address) to the physical drive address (fixed head track address). Four 14-track cylinders and one 4-track cylinder (404_{16}) are provided. Cylinder 404_{16} is provided for alternate track management for the other four cylinders.

2.13. DIAGNOSTIC OPERATION

The controller contains a firmware diagnostic routine that thoroughly checks the operation of the entire subsystem. It is automatically executed at the following times:

- At power on
- When a clear signal is received from the system host
- When the operator uses the DIAGNOSTIC MODE switch

During execution of the diagnostics, the controller is in an offline condition and does not respond to any interface request except the CLEAR signal. DIAGNOSTIC A, B, C, and D indicators are lit and the READY indicator is not lit during the execution of this routine.

The first part of diagnostics takes approximately 2 seconds:

- Clears controller and drive of any error conditions
- Executes controller diagnostics that test the operation of the sequencer and various sequencer controlled registers; checks the integrity of the data path, checks the RAM buffers using various test patterns; and performs internal controller loop-back operations
- Executes buffer expansion diagnostics that write, read, and check a test pattern

If a controller or buffer expansion fault is found, appropriate operator panel indicators are lit in binary and the appropriate configuration in byte 2 is set. (See Table 2-12.) A controller fault halts the controller while waiting for an operator or interface restart action.

The second part of diagnostics is disk drive diagnostics. Extensive drive tests are performed only at power-on time. Following the power-on sequence, each disk drive requires 25 seconds to become fully operational, displays the ready status indicator, and starts to power up the next disk drive. The controller waits for all configured drives to power up. A single drive subsystem waits until that drive becomes ready, while a 2-, 3-, or 4-disk drive subsystem waits approximately 30 seconds per drive for the number of disk drives configured.

Table 2-12. Diagnostic Indicator Display

	Diagnostic Mode Display Indicators				Diagnostic Description
	D	C	B	A	
0	0	0	0	0	Test completed successfully
1	0	0	0	1	Microprocessor 1 PCA failure
2	0	0	1	0	Microprocessor 2 PCA failure
3	0	0	1	1	Expansion I/O PCA required
4	0	1	0	0	Control storage parity error
5	0	1	0	1	DMA PCA failure
6	0	1	1	0	I/O PCA failure
7	0	1	1	1	Not used
8	1	0	0	0	Drive 0 R/W failure
9	1	0	0	1	Drive 1 R/W failure
A	1	0	1	0	Drive 2 R/W failure
B	1	0	1	1	Drive 3 R/W failure
C	1	1	0	0	Control storage parity error
D	1	1	0	1	Not used
E	1	1	1	0	Buffer expansion PCA failure
F	1	1	1	1	Test in progress

NOTE:

Diagnostic indicators extinguish at completion of diagnostics.

LEGEND:

0 Indicator off
1 Indicator lit

After this delay, each configured drive is then polled to see if it is available for further testing. Each disk drive that is powered down, busy, or write-protected is not tested further and the skip bit for that disk drive is set in configuration byte 3. Each disk drive not ready is not tested further and the fail bit for that drive is set in configuration byte 3.

Each of the remaining disk drives is tested with drive diagnostics that require approximately 5 seconds per drive. These tests position the accessor to diagnostic cylinder 552 and then perform read and write operations using firmware-generated test data. Seven sectors per track and all 14 tracks of the cylinder are tested. If the disk drive fails any part of the test, the fail bit for that disk drive is set.

If the dual-port option is supported, it may be necessary to change the PORT SELECT switch to a position that selects the controller performing the diagnostic routine to ensure that diagnostics are performed on that disk drive.

When the disk drive diagnostics are performed subsequent to the power-on time, the disk drives have already been powered up and tested. The test then consists of polling each configured disk drive. If the drive is powered down, busy, write protected, or ready, the skip bit is set for that drive. If the disk drive skip bit is not set, the drive is not ready, and the fail bit is then set for that disk drive.

Following the completion of the diagnostic routine, the ATTENTION line is asserted on the interface and a power-on-confidence status condition is presented to the system host. The not-ready bit is also set if a disk read/write error was detected. An unformatted diagnostic cylinder also causes this status condition.

3. Interface Command Control

3.1. SYSTEM INTERFACE

The system interface for the fixed disk controller is an 8-bit bidirectional byte interface. If the dual host feature is installed, the controller can be connected to two systems.

The fixed disk controller can sustain a data transfer rate of up to 1.2 megabytes per second (MB/s). A quad-sector buffer is provided in the interface section of the FDC to queue data being transferred between the host system and the disk drives. If the interface transfer rate is not sufficient and a buffer is not available, the FDC suspends the disk transfer until the buffer is available. Since the quad-sector buffer is organized into two 512-byte segments, at least two sectors (512 bytes) must be transferred on each revolution to ensure the buffer is available.

Data transfer sequences can be specified to operate in either burst mode (mode 3) or byte mode (mode 2).

This interface is activated when the system (host) invokes an operation by asserting a unique select line to a peripheral. The peripheral responds by asserting the output-request line to request an interface command byte from the host. In the process of executing the command, the input request (IR), output request (OR), acknowledge (ACK), data lines, clear, and last character lines may be utilized. The select line remains asserted during the entire sequence. Upon completion of the command or upon detection of an interface error, the peripheral asserts the interrupt and input request lines and transfers an interface status byte to the system host.

System deselection of the peripheral before normal interface command sequence completion is possible by deactivating the select line. The toggle bit in the status byte does not toggle in the status presented after an early deselection sequence.

3.1.1. Interface Command Sequences

To execute an operation in a peripheral, two or three interface sequences are required. In the FDC, disk operations are specified by means of a multibyte peripheral control block (PCB). The PCB is transferred to the controller as part of a PCB sequence. This sequence consists of an interface command specifying an extended command, a 16-byte control block, and an interface status byte.

If a data transfer operation is specified, one or two peripheral data transfer (PDX) sequences follow. Normally, one sequence is sufficient for disk data transfers, however, the search operation also requires the transfer of key data. The PDX sequence consists of an interface command (continue), data transfer, and an interface status byte.

Normal completion status for the operation is contained in the interface status byte. If an abnormal completion is indicated, the PSB should be retrieved for more detailed status, which is required for error logging or recovery purposes. This sequence consists of a read-status-block interface command, a 16-byte status block, and an interface status byte.

The status byte is presented at the conclusion of every select sequence and indicates the status for that sequence. This byte, presented at the conclusion of the continue command sequence (second continue sequence for search operations), indicates the completion status for the operation initiated by the PCB.

3.1.2. ATTENTION Lines

A unique ATTENTION line is provided for each peripheral attached to the interface. This line is used to notify the host system that a specified operation is complete and the peripheral device is ready for the next sequence.

Following the interpretation of the peripheral control block received in a PCB sequence, the FDC executes the function. The FDC notifies the host system by activating the ATTENTION line when it is ready to perform the next sequential operation. As specified by the control block, a PDX sequence follows.

An unsolicited ATTENTION signal is activated to each host:

- following the execution of the firmware-based diagnostic routine; and
- upon detection of a rising temperature in the peripheral cabinet.

A status byte of FDC error is presented and the PSB indicates unit check and early warning. The PSB indicates early warning as long as the temperature remains high; however, the unit check bit is presented only once.

A delay may be present between the activation of host selection and the output request by the FDC. If the FDC firmware is currently involved in a previous operation on the same or other host, this delay can be avoided by initiating the interface sequences to avoid selecting a busy controller.

3.1.3. Multidrive

The controller accepts a PCB for any valid address specified by the configuration switches. Once a PCB has been accepted, the controller is then dedicated to that PCB until the function terminates. The PSB is maintained for that function until the next PCB is sent.

3.1.4. Dual-Port Drives

The priority-select command and the release command provide control for port selection.

Initiating a function on a dual-port drive requires a normal PCB sequence. This may result in a busy interface status due to the alternate port (FDC) having previously reserved the disk drive. If the PCB is accepted, the disk drive is selected and thereby reserved for that port. Upon completion of the function, the disk drive is deselected but remains reserved for that port until it is released by the release command.

The priority-select command is available if a controller appears to be locked out from a disk drive that is reserved but not selected by the alternate port. Issuing this command selects and reserves a disk drive that is not selected, but may be reserved by the alternate port. Upon completion of this command, the disk drive is deselected but remains reserved for this port.

Note that the priority-select command should be used with caution because it may cause the alternate port to lose control of a disk drive by way of an automatic release during a seek or recalibrate function or a critical sequence of functions such as seek, read, or write.

3.1.5. Dual Hosts

When the controller contains a dual host capability, the controller polls both system hosts until a select probe is issued by either system host. If the controller is not reserved for the other host, the controller becomes temporarily reserved for the system issuing the select probe. The controller is reserved for the duration of the select sequence or a multiselect sequence function and will not honor a select probe from other systems during this time.

Once the function is completed, the controller becomes free (not reserved) to be selected by either host. A separate status byte and PSB are maintained for each host so that the PSB for a function is valid until the next PCB is sent by that host.

Dual host capability provides two new interface commands (reserve and release).

A reserve command reserves the controller for a host if it is not already reserved for the other host. A reserved controller is busy (interface/function (I/F) status bit 7) to any command from the other host except the release command. A reserved controller remains reserved to a host until either host issues a release command to the controller. A CLEAR I/F signal from either host unconditionally causes the controller to perform a power-on-confidence (POC) test, after which an unsolicited ATTENTION signal is raised to both hosts. The first status byte reported to each host has the POC bit set (status, bit 5). The release command should be used with caution since one host could release an existing reserve condition set by the other host.

3.1.6. Overlapped Seek Capability

The controller provides seek and read/write overlap as well as 4-way seek overlap. To fully utilize this capability, the host system must issue a seek or recalibrate function in addition to the normal read, write, or search function. The controller starts the seek function on the drive specified by the PCB and is then immediately available to accept another command or PCB from the host system.

The controller remains available to accept commands and PCBs from the host system until a data transfer PCB (read, write, search) is issued. Once the controller accepts this nonseek PCB, the controller is dedicated to this function until it completes.

After the controller presents completion status for this PCB function, the controller monitors any seek or recalibrate function in progress.

The completion of the first seek or recalibrate function generates an ATTENTION signal to the host, indicating that seek completion status is pending. The drive address and its completion status indicator are held pending until the send-seek-completion-status command is issued.

If other seek or recalibrate functions complete while there is seek/recalibrate completion status already pending, the completion status byte is updated with the drive address and its completion status indicator, but no ATTENTION signal is generated to the host. When the host responds to the initial ATTENTION signal with the send-seek-completion-status command, the completion status byte indicates all seek or recalibrate completion status that is pending at that time. Once this byte has been presented to the host and the pending status has been honored, those drives are free to accept another function. A PCB for a drive that has a seek/recalibrate function in progress or completion status pending is rejected with a busy interface status until the seek/recalibrate function finishes and the pending status has been presented to the host.

In a dual host environment, once one host starts an overlapped seek operation, the controller presents a busy status to any select probe from the other host until all overlapped seek/recalibrate functions have completed.

3.1.7. Interface CLEAR

An interface CLEAR signal causes the FDC to immediately and asynchronously terminate any ongoing operation and begin execution of FDC diagnostics. The PSB and other information regarding the state of the FDC is lost during this diagnostic testing. In the dual environment, a CLEAR signal from either host causes the FDC to clear.

3.2. INTERFACE COMMANDS

The interface commands with their codes are listed in Table 3-1.

Table 3-1. Interface Command Codes

Command	Binary Code								Hexadecimal Code
	D7	D6	D5	D4	D3	D2	D1	D0	
Read-status-block	0	0	1	0	1	0	1	1	2B
Extended	0	0	1	0	1	1	1	1	2F
Continue	0	0	1	0	1	0	0	1	29
Assume-mode 2, 3 operation	0	0	1	0	1	0	1	0	2A
Send-status	0	0	1	1	0	0	0	0	30
Send-past-status	0	0	1	1	1	0	0	0	38
Send-seek-completion-status	0	0	1	0	1	1	0	0	2C
Loop-back	0	0	1	0	1	1	1	0	2E
Reserve/priority-select	1	0	1	1	0	0	D	D	B0-B3, dual port B0 only, dual host
Release	1	0	1	1	1	0	D	D	B8-BB, dual port B8 only, dual host

3.2.1. Read-Status-Block Command

The read-status-block command ($2B_{16}$) reads the 16-byte peripheral status block (PSB).

3.2.2. Extended Command

The extended command ($2F_{16}$) is followed by 16 bytes of additional command parameters consisting of a PCB that is transferred in a PCB sequence. The contents of these bytes are defined in Table 2-4.

3.2.3. Continue Command

The continue command (29_{16}) informs the disk controller that the interface is ready to continue the operation as specified previously in the PCB. It is usually the data transfer segment (PDX) of the function.

3.2.4. Assume-Mode 2, 3 Operation Command

The assume-mode 2, 3 operation command ($2A_{16}$) causes the controller to return five bytes of configuration and diagnostic status. (See Table 3-2.)

3.2.5. Send-Status Command

The send-status command (30_{16}) transmits the current controller status since the last status byte was transmitted.

3.2.6. Send-Past-Status Command

The send-past-status command (38_{16}) transmits the last non- FF_{16} status byte to the system (host). The toggle bit does not change upon receipt of the command.

Table 3-2. Configuration and Diagnostic Status Byte/Bit Descriptions (Part 1 of 2)

Byte/Bit	Description																						
Byte 1																							
1, 7-0	52-sector FDC (09 ₁₆)																						
Byte 2, Configuration Byte 1																							
2, 7-6	Capacity of each disk drive <table border="1"> <thead> <tr> <th colspan="2"><u>Bit</u></th> <th rowspan="2">Capacity of each disk drive (megabytes)</th> <th rowspan="2">Cylinder range</th> </tr> <tr> <th>7</th> <th>6</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>25</td> <td>0-135 (87₁₆)</td> </tr> <tr> <td>0</td> <td>1</td> <td>56</td> <td>0-271 (10F₁₆)</td> </tr> <tr> <td>1</td> <td>0</td> <td>75</td> <td>0-407 (197₁₆)</td> </tr> <tr> <td>1</td> <td>1</td> <td>100</td> <td>0-543 (21F₁₆)</td> </tr> </tbody> </table>	<u>Bit</u>		Capacity of each disk drive (megabytes)	Cylinder range	7	6	0	0	25	0-135 (87 ₁₆)	0	1	56	0-271 (10F ₁₆)	1	0	75	0-407 (197 ₁₆)	1	1	100	0-543 (21F ₁₆)
<u>Bit</u>		Capacity of each disk drive (megabytes)	Cylinder range																				
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2, 5-4	Number of drives installed <table border="1"> <thead> <tr> <th><u>Bit</u></th> <th>5</th> <th>4</th> <th>Number of disk drives</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>2</td> <td>2</td> </tr> <tr> <td>1</td> <td>0</td> <td>3</td> <td>3</td> </tr> <tr> <td>1</td> <td>1</td> <td>4</td> <td>4</td> </tr> </tbody> </table>	<u>Bit</u>	5	4	Number of disk drives	0	0	1	1	0	1	2	2	1	0	3	3	1	1	4	4		
<u>Bit</u>	5	4	Number of disk drives																				
0	0	1	1																				
0	1	2	2																				
1	0	3	3																				
1	1	4	4																				
2, 3	Fixed heads installed (set to 1 if installed), drive 3																						
2, 2	Fixed heads installed (set 1 if installed), drive 2																						
2, 1	Fixed heads installed (set 1 if installed), drive 1																						
2, 0	Fixed heads installed (set to 1 if installed), drive 0																						
Byte 3, Configuration Byte 2																							
3 7-0	Feature installed and operational if set to 1: <table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Feature</u></th> </tr> </thead> <tbody> <tr> <td>7-3</td> <td>Not used</td> </tr> <tr> <td>2</td> <td>Buffer expansion</td> </tr> <tr> <td>1</td> <td>Dual port</td> </tr> <tr> <td>0</td> <td>Dual host</td> </tr> </tbody> </table> <p>If both dual port and dual host are configured, only bit 1 is set.</p>	<u>Bit</u>	<u>Feature</u>	7-3	Not used	2	Buffer expansion	1	Dual port	0	Dual host												
<u>Bit</u>	<u>Feature</u>																						
7-3	Not used																						
2	Buffer expansion																						
1	Dual port																						
0	Dual host																						

Table 3-2. Configuration and Diagnostic Status Byte/Bit Descriptions (Part 2 of 2)

Byte/Bit	Description
Byte 4	
4, 7-4	<p>Drive test skipped indicates disk drives configured that were not tested due to being either powered down, busy (dual port only), or write-protected</p> <p>xxx1 xxxx Drive 0 skipped during POC test xx1x xxxx Drive 1 skipped during POC test x1xx xxxx Drive 2 skipped during POC test 1xxx xxxx Drive 3 skipped during POC test</p>
4, 3-0	<p>Drive test failed indicates which, if any, configured drives failed the drive portion of the POC test:</p> <p>xxxx xxx1 Drive 0 failed POC test xxxx xx1x Drive 1 failed POC test xxxx x1xx Drive 2 failed POC test xxxx 1xxx Drive 3 failed POC test</p>
Byte 5, PROM Revision Level	
5, 7-0	Contains a double hexadecimal digit representation of the PROM revision level of the firmware installed in the disk controller

3.2.7. Send-Seek-Completion-Status Command

The send-seek-completion-status command (2C₁₆) sends one byte indicating the completion status of seek and recalibrate functions. This format of this byte is as follows:

<u>Bit</u>	<u>Description</u>	<u>Drive</u>
7	Abnormal termination	3
6	Abnormal termination	2
5	Abnormal termination	1
4	Abnormal termination	0
3	Seek/recalibrate status pending	3
2	Seek/recalibrate status pending	2
1	Seek/recalibrate status pending	1
0	Seek/recalibrate status pending	0

The appropriate bits are set as each seek or recalibrate function completes. The byte is cleared after it is sent to the host.

3.2.8. Loop-Back Command

The loop-back command (2E₁₆) allows the system host to verify the integrity of the 8-bit interface data and control lines by transferring data and parity in both directions.

Upon receipt of this command byte, the FDC accepts one byte of data. This is returned along with three additional bytes (55₁₆, AA₁₆, 01₁₆) and the status byte.

The status byte is returned with good parity if the data byte was received with good parity, or bad parity if the data byte was received with bad parity.

The status byte has bit 4 (FDC error) set if the data byte was sent with the last-character I/F signal active.

3.2.9. Reserve/Priority-Select Command

The reserve/priority-select command reserves the controller to the system host issuing the command (dual host feature installed).

If a dual-port feature is present, this command selects the specified drive.

3.2.10. Release Command

The release command releases the controller from either host. (Dual host feature is present.)

If dual-host feature is present, this command releases the specified drive.

3.3. INTERFACE STATUS

The interface status byte is presented at the end of every completed select sequence. This byte indicates the completion status for the sequence just completed. This byte is presented at the end of a sequence and is indicated when the interrupt signal is asserted. Descriptions of the interface status bits are given in Table 3-3.

Table 3-3. Interface Status Bit Description (Part 1 of 2)

Name	Bit	Description
Busy	7	<p>When set, indicates one of the following:</p> <ul style="list-style-type: none"> ■ The PCB was not accepted because the device specified in PCB 0 has either a seek in progress or a seek completion status pending. ■ The command byte was not accepted because the other host has a seek in progress or a seek completion status pending (dual host). ■ The other host has the controller reserved (dual host). ■ The drive cannot be selected because the other controller has the drive reserved (dual port).

Table 3-3. Interface Status Bit Description (Part 2 of 2)

Name	Bit	Description								
Not ready	6	Indicates that the disk drive was not ready or a diagnostic error in the disk read/write test was detected								
Power on confidence (POC)	5	This bit is set to indicate that the controller has just completed the firmware-based diagnostic routine. This bit is set with the first status byte presented to each host following POC of the controller.								
FDC error	4	This bit is set if the FDC function has not completed successfully. One of the following bits in PSB 0 has also been set: <table style="margin-left: 40px;"> <tr> <td>Bit 7</td> <td>Function reject</td> </tr> <tr> <td>Bit 4</td> <td>Sector not found</td> </tr> <tr> <td>Bit 2</td> <td>Unit check</td> </tr> <tr> <td>Bit 1</td> <td>Flag not zero</td> </tr> </table> A read-status-block command should be issued to determine the cause of the error. If this status byte is responding to a loop-back command, this bit indicates that the last character I/F line was activated.	Bit 7	Function reject	Bit 4	Sector not found	Bit 2	Unit check	Bit 1	Flag not zero
Bit 7	Function reject									
Bit 4	Sector not found									
Bit 2	Unit check									
Bit 1	Flag not zero									
ECC correction	3	Set when PSB 0, bit 0 is set (ECC corrected). A read-status-block command may be issued to determine the sector corrected.								
Unsuccessful search	2	Set when PSB 0, bit 5 is set (unsuccessful search). A read-status-block command may be issued to determine the last sector searched.								
Toggle	1	Set to 1 by reset or power-on-clear. This bit is then reset to 0 on the first valid status reported. On each successive function completion, this toggle bit changes state. It will not change state on receipt of a send-past-status command, an unrecognizable command due to a parity error on the command byte resulting from an invalid command byte configuration, or due to the select line dropping prior to the command interrupt and status sequence.								
Data error	0	Set if a parity error is detected during an FDC/host PCB or PDX sequence, or if the data transfer sequence is terminated prematurely during a write operation. If the data transfer is terminated prematurely, the last sector written may be in error.								
Invalid command		An FF ₁₆ status byte is presented to indicate that the controller detected an invalid command, an illegal command sequence, or a parity error in the command byte.								

NOTE:

If bit 6, 4, or 0 is set, or if a FF₁₆ value is presented by the FDC, any operation in progress is terminated.

Glossary

A

AM

Address mark

C

CLY-H or CH

Cylinder high

CLY-L or CL

Cylinder low

D

DP

Defect position

E

ECC

Error correction code

EL

Error length

ESIOR

Equipment specification I/O recovery

F**FDC**

Fixed disk (storage) controller

FIRE

A special type of error correction code

H**HDA**

Head disk assembly

I**ID**

Identification

I/F

Interface/function

IR

Input request

L**LSB**

Least significant byte

M**MB**

Megabyte

MFM

Modified frequency modulation

MSB

Most significant byte

N**NA**

Not applicable

ND

Not defined

O**OR**

Output request

P**PCB**

Peripheral control block

PDX

Peripheral data transfer

POC

Power on confidence

PROM

Programmed read only memory

PSB

Peripheral status block

R**RAM**

Random access memory

RCD

Record

T**TPI**

Tracks per inch

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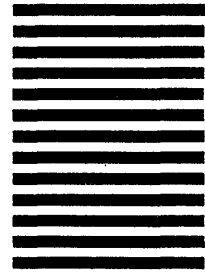
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