SA800/801
Diskette Storage Drive

Theory of Operations

Shugart Associates

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1.0 General Operations

The SA800/801 Diskette Drive consists of read/write and control electronics, drive mechanism, read/write head, track positioning mechanism, and the removable Diskette. These components perform the following functions:

- Interpret and generate control signals.
- Move read/write head to the desired track.
- Read and write data.

The relationship and interface signals for the internal functions of the SA800/801 are shown in Figure 1.

The Head Positioning Actuator positions the read/write head to the desired track on the Diskette. The Head Load Actuator loads the Diskette against the read/write head and data may then be recorded or read from the Diskette.

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits (Sector/Index) for 801.

2. Head Position Actuator Driver

3. Head Load Actuator Driver

4. Read/Write Amplifier and Transition Detector

5. Data/Clock Separation Circuits

6. Safety Sensing Circuits

7. Write Protect (SA801 only)

1.1 Head Positioning

An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw clockwise or counter-clockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

1.2 Diskette Drive Spindle

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the latch handle fixes the Diskette to the registration hub.

1.3 Read/Write Head

The read/write head is a ceramic head and is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

The SA800/801 ceramic head is a single element read/write head with straddle erase elements to provide erased areas between data tracks. Thus

normal tolerance between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Acutator lead screw. The Diskette is held in a place perpendicular to the read/write head by one platen located on the base casting. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.
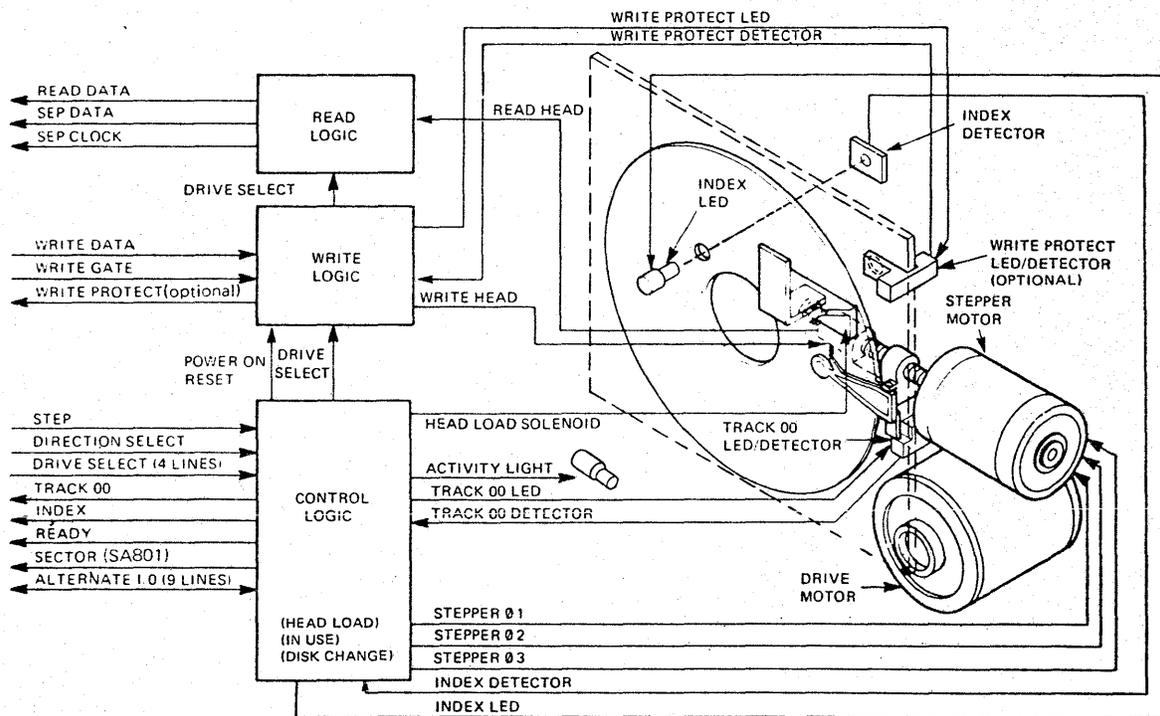

Figure 1   SA800/801 Functional Diagram

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2.0 Recording Format (Single Density)

2.1 The format of the data recorded on the Diskette is totally a function of the host system. Data is recorded on the diskette using frequency modulation as the recording mode, i.e., each data bit recorded on the diskette has an associated clock bit recorded with it, this is referred to as FM. Data written on and read back from the diskette takes the form as shown in Figure 2. The binary data pattern shown represents a 101.
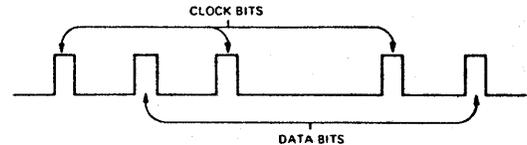

Figure 2 Data Pattern

2.2 Bit Cell

As shown in Figure 3, the clock bits and data bits (if present) are interleaved. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.
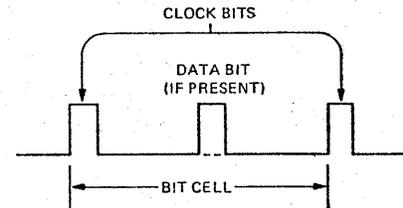

Figure 3 Bit Cell

2.3 Byte

A Byte, when referring to serial data (being written onto or read from the disc drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disc drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disc first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 4 illustrates the relationship of the bits within a byte and Figure 5 illustrates the relationship of the bytes for read and write data.

2.4 Recording Format (Double Density)

Double capacity can be obtained by use of M^2FM (modified, modified frequency modulation) rather than FM (frequency modulation) which is the standard method of encoding data on the diskette.

The differences between FM and M^2FM encoding are shown in Figure 6. Note that M^2FM results in a 1 to 1 relationship between the "flux changes per inch" and the bits per inch recorded on the diskette. This also results in a doubling of the data transfer rate, from 250 to 500 KBS, when compared to FM.

Data error rate performance equal to standard capacity diskettes using FM encoding can be achieved by using:

● The SA800/801 diskette drive with its proprietary ceramic/ferrite read/write head.

● Phase locked loop (VFO) data separator with asymmetrical (60/40) data and clock windows.

● Write precompensation.

Provision of the phase locked loop data separator and write precompensation circuitry is the responsibility of the user of the SA800/801 diskette drive.

Shugart Associates will provide design information, as required, to SA800/801 users who desire to incorporate double capacity diskette drives in their end products.

The bit cell for M^2FM encoded data is one half the duration of the bit cell for FM encoded data. Also, unlike FM, the M^2FM bit cell does not always contain a clock bit at its leading edge. This lack of a clock bit makes data separation more complex. Also, the window size is half the FM window size, which results in less tolerance to bit shift. The only reliable method to separate M^2FM encoded data is

Figure 4   Byte

BIT CELL 0 OF BYTE 0 IS FIRST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING

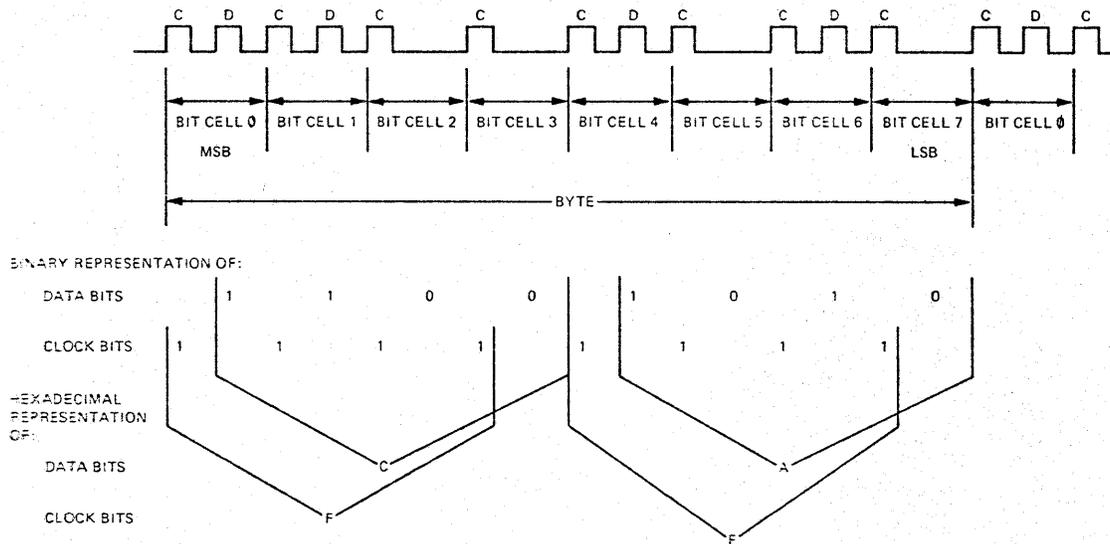BIT CELL 7 OF BYTE 17 IS LAST DATA TO BE SENT TO THE DRIVE WHEN WRITING AND FROM THE DRIVE WHEN READING
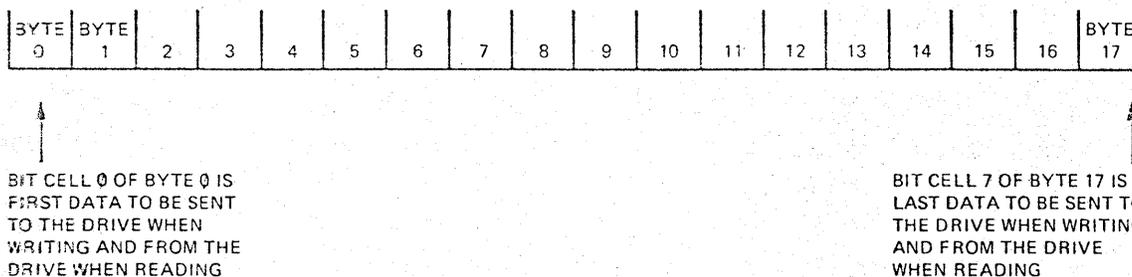
Figure 5   Data Bytes

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through use of a phase locked loop (VFO) type of data separator. The VFO, once synchronized, tracks the data and generates clock and data windows, improving the bit shift tolerance over the conventional "hard" data separators commonly used in FM recording, which use windows of fixed timing.

2.5 Tracks

The SA800/801 drive is capable of recording up to 77 tracks of data. The tracks are numbered 0-76. Each track is made available to the read/write head by accessing the head with a stepper motor and carriage assembly. Track accessing will be covered in Section 3.

Basic Track Characteristics:

No. bits/track Single Density	41,300 bits
No. bits/track Double Density	82,600 bits
Index Pulse Width	1.7 ± .5 ms
Index/Sector Pulse Width (SA 801 only)	.4 ± .2 ms

2.6 Track Format

Tracks may be formatted in numerous ways and is dependent on the using system. The SA800/801 use index and sector recording formats respectively.

2.6.1 Sector Recording Format

In this Format, the using system may record up to 32 sectors (records) per track. Each track is started
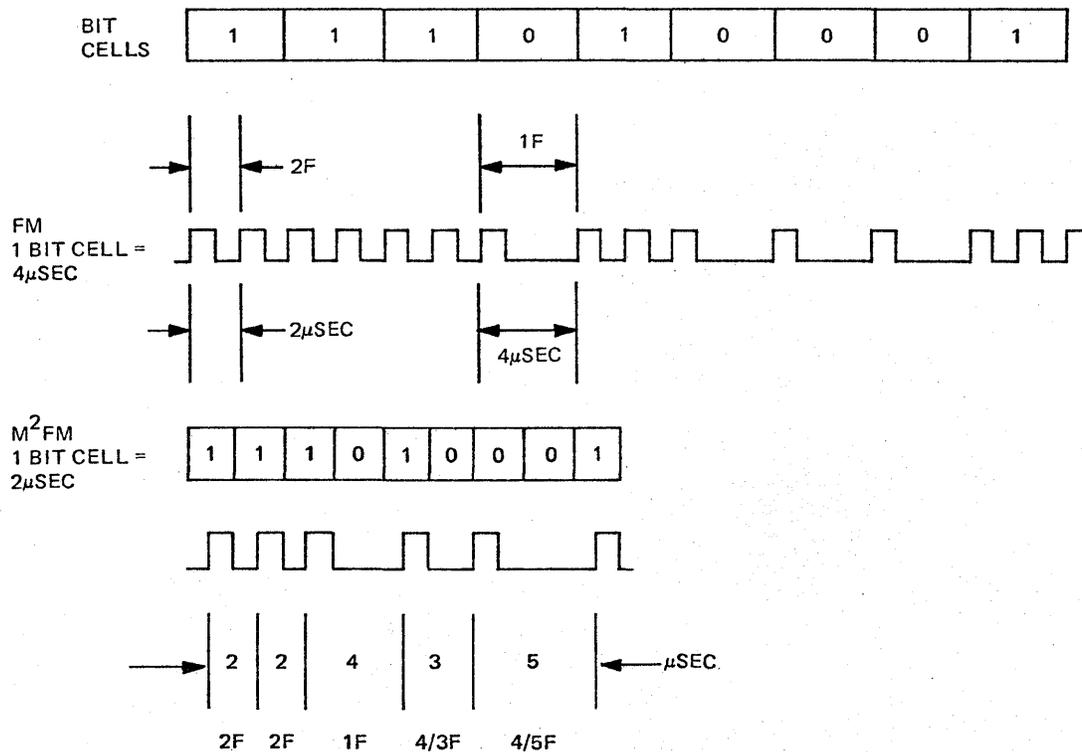
FM Encoding:
   • Write data bits at the center of the bit cell
   • Write clock bits at the leading edge of the bit cell

M^2FM Encoding:
   ➤ Write data bits at the center of the bit cell
   ➤ Write clock bits at the leading edge of the bit cell if:
      1) There is no data bit or clock bit written in the previous bit cell, and
      2) There will be no data bit written in the present bit cell.

NOTE: In M^2FM, the write oscillator frequency is doubled, while maintaining the same flux changes per inch as FM. Thus, the bit cell in M^2FM is ½ that in FM. Data transfer rate is also doubled, since a 1 to 1 relationship exists between flux changes per inch and bits per inch (2 to 1 in FM).

Figure 6   FM and M^2FM Encoding

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by a physical index pulse and each sector is started by a physical sector pulse. This type of recording is called hard sectoring Figure 7 shows a typical Sector Recording Format.

2.6.2 Soft Sector Recording Format

In this Format, the using system may record one long record or several smaller records. Each track is started by a physical index pulse and then each record is preceded by a unique recorded identifier. This type of recording is called soft sectoring. Figure 8 shows a soft sector format. (IBM compatible)

2.7 Typical Track Index Format

Figure 8 shows a track Format, which is IBM compatible, using Index Recording Format with soft sectoring.

2.7.1 Gaps (Ref. Fig. 8)

Each field on a track is separated from adjacent fields by a number of bytes containing no data bits. These areas are referred to as gaps and are provided to allow the updating of one field without affecting adjacent fields. As can be seen from Figure 8, there are four different types of gaps on each track.

Gap 1 Post-Index Gap

This gap is defined as the 32 bytes between Index Address Mark and the ID Address Mark for Sector one (excluding the address mark bytes). This gap is always 32 bytes in length and is not affected by any updating process.
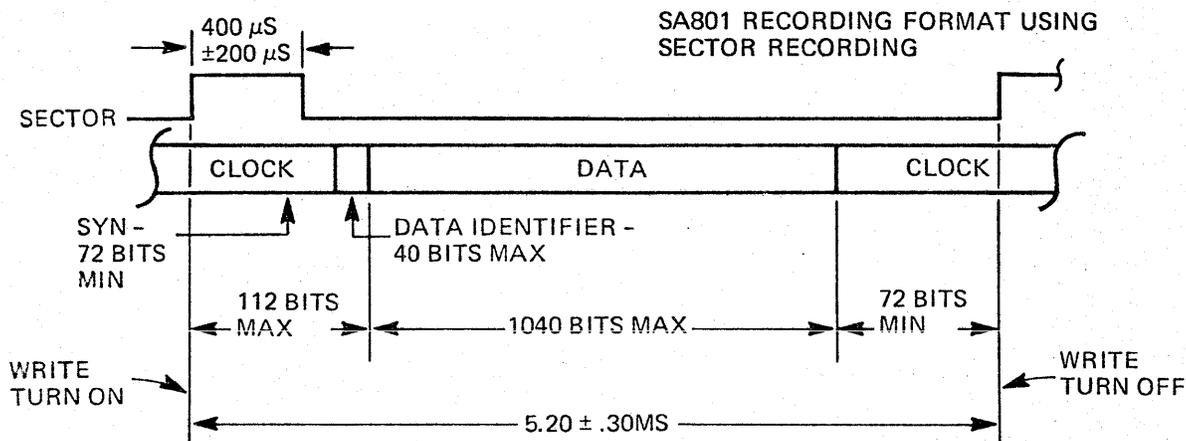

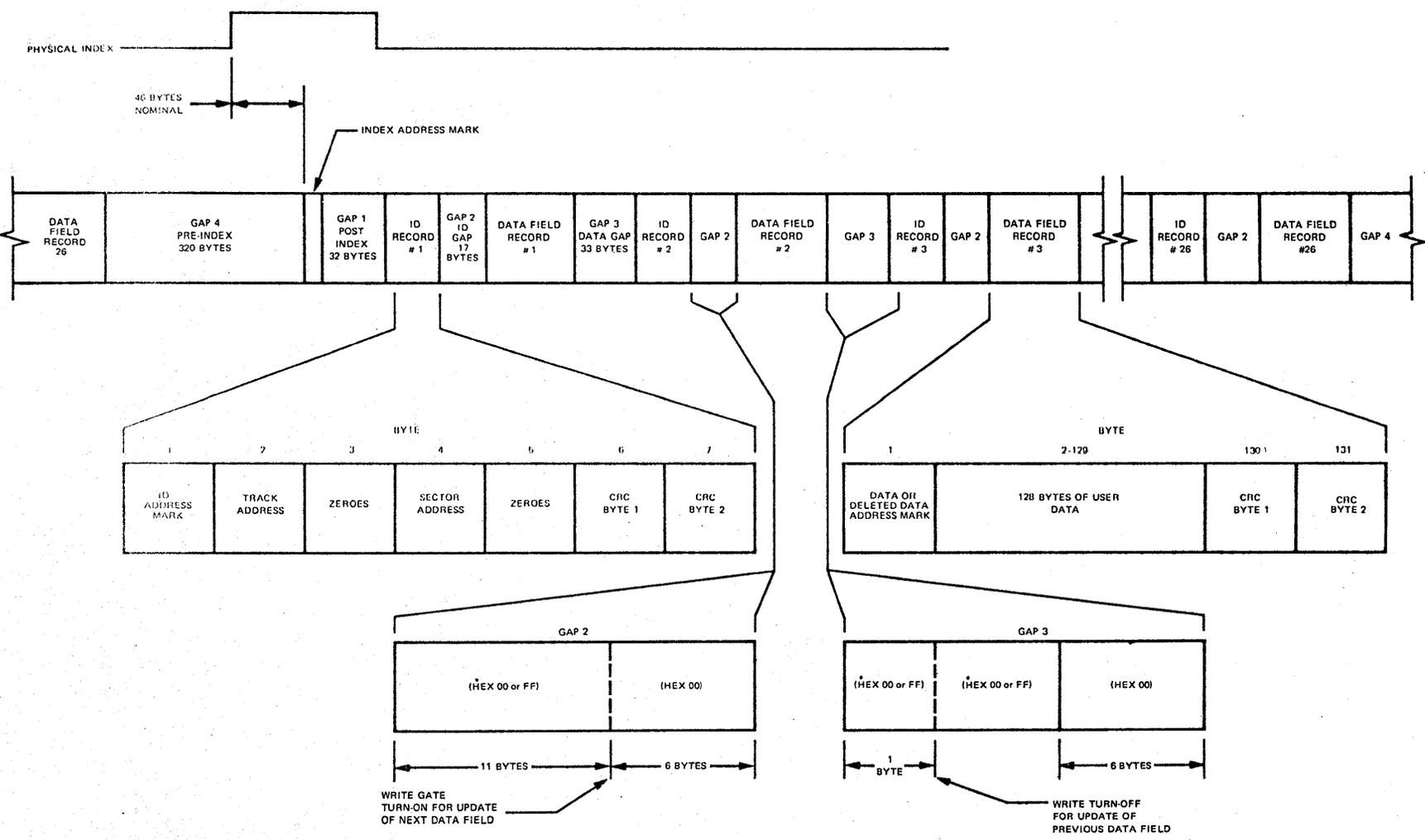**Figure 7   Sector Recording Format**

Figure 8 Track Format

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PHYSICAL INDEX

46 BYTES NOMINAL

INDEX ADDRESS MARK

| DATA FIELD RECORD 26 | GAP 4 PRE-INDEX 320 BYTES | GAP 1 POST INDEX 32 BYTES | ID RECORD #1 | GAP 2 ID GAP 17 BYTES | DATA FIELD RECORD #1 | GAP 3 DATA GAP 33 BYTES | ID RECORD #2 | GAP 2 | DATA FIELD RECORD #2 | GAP 3 | ID RECORD #3 | GAP 2 | DATA FIELD RECORD #3 | ID RECORD #26 | GAP 2 | DATA FIELD RECORD #26 | GAP 4 |

BYTE

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |

| ID ADDRESS MARK | TRACK ADDRESS | ZEROES | SECTOR ADDRESS | ZEROES | CRC BYTE 1 | CRC BYTE 2 |

BYTE

| 1 | 2-129 | 130 | 131 |

| DATA OR DELETED DATA ADDRESS MARK | 128 BYTES OF USER DATA | CRC BYTE 1 | CRC BYTE 2 |

GAP 2

| (HEX 00 or FF) | (HEX 00) |

◄─── 11 BYTES ───►◄─── 6 BYTES ───►

WRITE GATE TURN-ON FOR UPDATE OF NEXT DATA FIELD

GAP 3

| (HEX 00 or FF) | (HEX 00 or FF) | (HEX 00) |

◄─ 1 BYTE ─►◄─── 6 BYTES ───►

WRITE TURN-OFF FOR UPDATE OF PREVIOUS DATA FIELD

*Where Hex 00 or FF is optional, FF is recommended.

Gap 2 ID Gap

The seventeen bytes between the ID Field and the Data Field is defined as Gap 2 (ID Gap). This gap may vary in size slightly after the Data Field has been updated.

Gap 3 Data Gap

The thirty-three bytes between the Data Field and the next ID Field is defined as Gap 3 (Data Gap). As with the ID Gap, the Data Gap may vary slightly in length after the adjacent Data Field has been updated.

Gap 4 Pre-Index Gap

The three hundred and twenty bytes between the last Data Field on a track and the Index Address Mark is defined as Gap 4 (Pre-Index Gap). Initially, this gap is nominally 320 bytes in length; however, due to write frequency tolerances and disc speed tolerances this gap may vary slightly in length. Also, after the data field of record 26 has been updated, this gap may again change slightly in length.

2.7.2 Address Marks

Address Marks are unique bit patterns one byte in length which are used in this typical recording format to identify the beginning of ID and Data Fields and to synchronize the deserializing circuitry with the first byte of each field. Address Mark bytes are unique from all other data bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell). There are four different types of Address Marks used. Each of these are used to identify different types of fields.
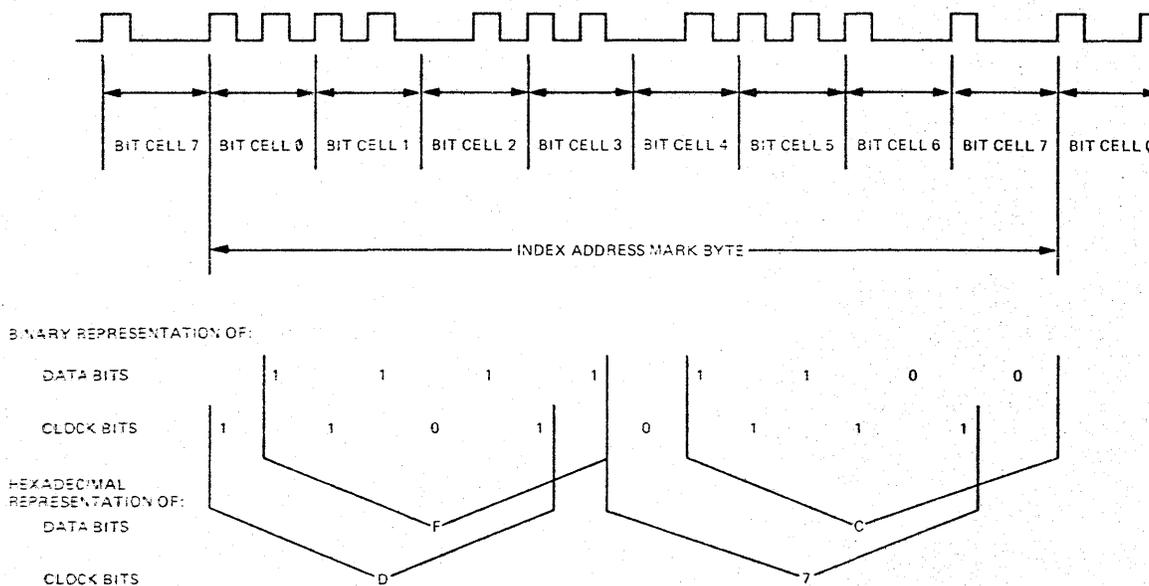

Figure 9 Index Address Mark

Index Address Mark

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record. The bit configuration for the Index Address Mark is shown in Figure 9.

ID Address Mark

The ID Address Mark byte is located at the beginning of each ID Field on the diskette. The bit configuration for this Address Mark is shown in Figure 10.

Data Address Mark

The Data Address Mark byte is located at the beginning of each nondeleted Data Field on the diskette. The bit configuration for this Address Mark is shown in Figure 11.

Deleted Data Address Mark

The Deleted Data Address Mark byte is located at the beginning of each deleted Data Field on the diskette. The bit configuration for this Address Mark is shown in Figure 12.

2.7.3 CRC

Each field written on the diskette is appended with two Cyclic Redundancy Check (CRC) bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the address mark and ending with bit seven of the last byte within a field (excluding the CRC bytes). When a field is read back from a diskette, the data bits (from bit zero of the address mark to bit seven of the second CRC byte) are divided by the same generator polynomial. A non-zero remainder indicates an error within the data read back from the drive while a remainder of zero indicates the data has been read back correctly from the disk.
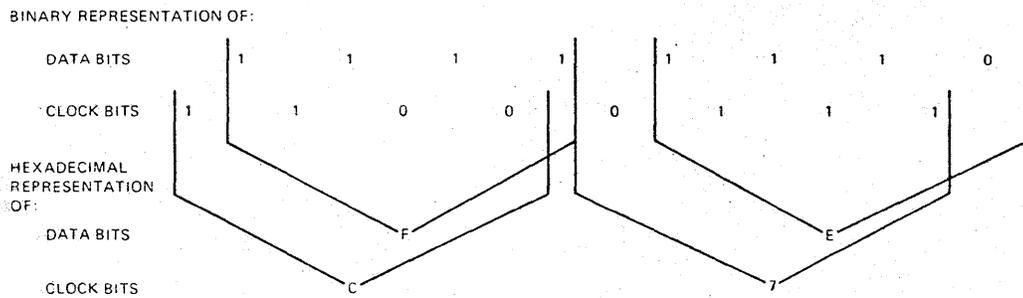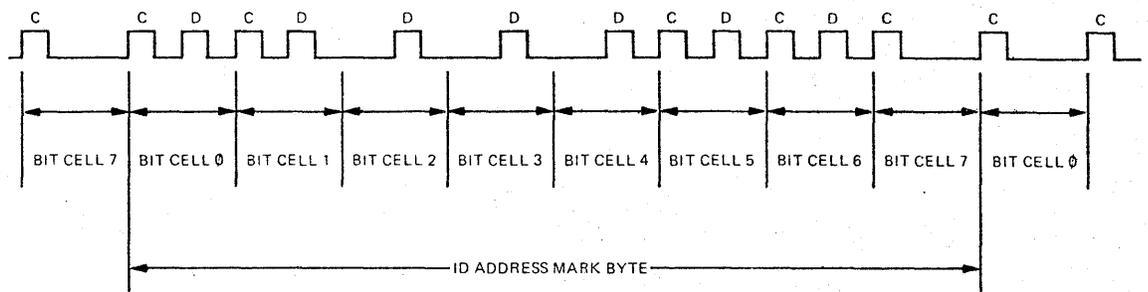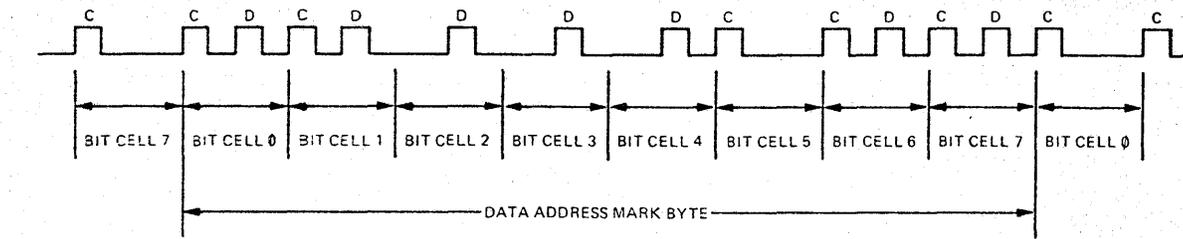

Figure 10   ID Address Mark

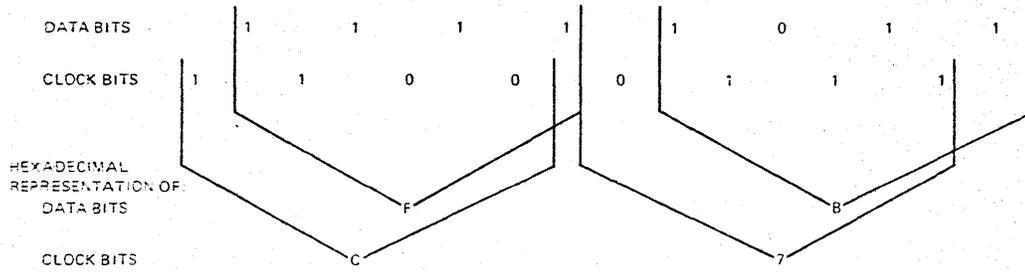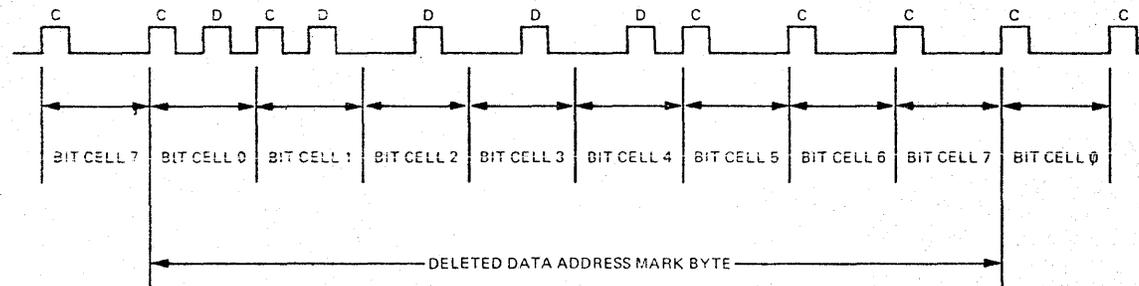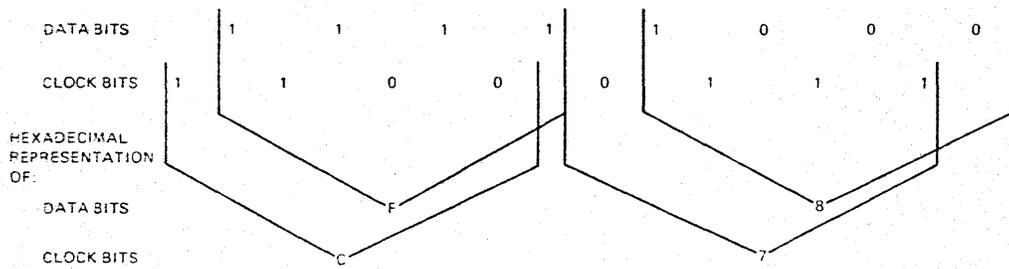**Figure 11 Data Address Mark**

Figure 12 Deleted Data Address Mark

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3.0 Track Accessing

- Stepper Motor
- Stepper Control Logic
- Reverse Seek
- Forward Seek
- Track 00 Flag

3.1 Seeking the read/write head from one track to another is accomplished by selecting the desired direction utilizing the Direction Select interface line, loading the read/write head, and then pulsing the Step line. Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the read/write head to move one track either in or out depending on the Direction Select line.

3.2 The stepper motor used on the SA800/801 drive is a three-phase, fifteen degree, variable reluctance stepper motor. Figure 13 shows the logic diagram of the motor.
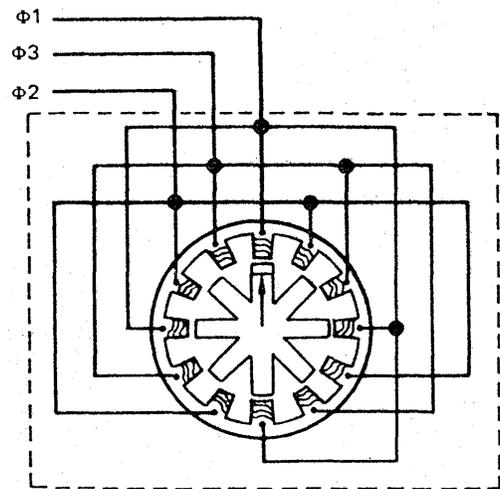

Figure 13 Stepper Motor

3.2.1 The stepper motor has 12 stator windings and a rotor with 8 teeth. The 12 stator windings are wired together in groups of four, 90 degrees apart. Each group of stator windings is wired to one phase of the stepper control logic. The rotor has its eight teeth spaced 45 degrees apart.

3.2.2 Figure 14 shows the stepper motor (rear view) with phase 1 of the stepper control logic active. Phase 1 is applied to the four stator windings at $0°, 90°, 180°$ and $270°$. This causes the four rotor teeth closest to those windings to move and line up with the stator windings.
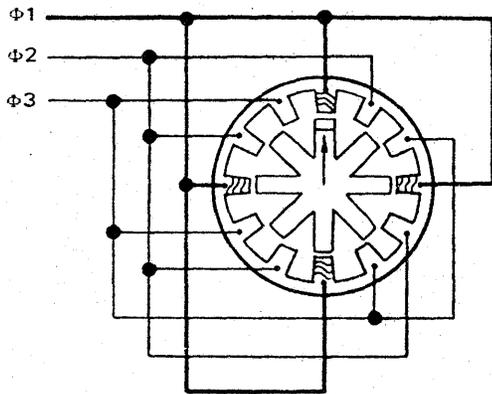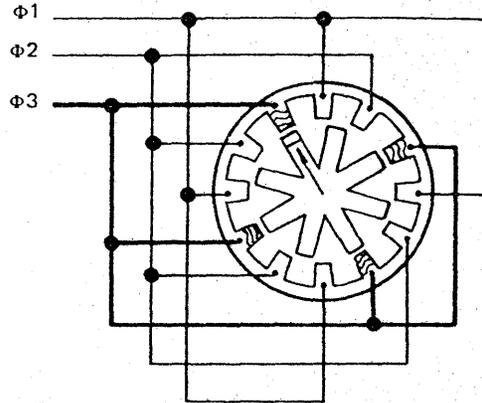
11

Figure 14 Position 1 (Trk 00)

Figure 16 Position 3 (Trk 02)

3.2.3 Figure 15 shows the stepper motor with phase 2 of the stepper control logic active. Phase 2 is applied to the stator windings at $30°, 120°, 210°,$ and $300°$. This causes the four rotor teeth closest to those windings to move and line up with the stator windings. The result is a $15°$ turn of the stepper motor lead screw.
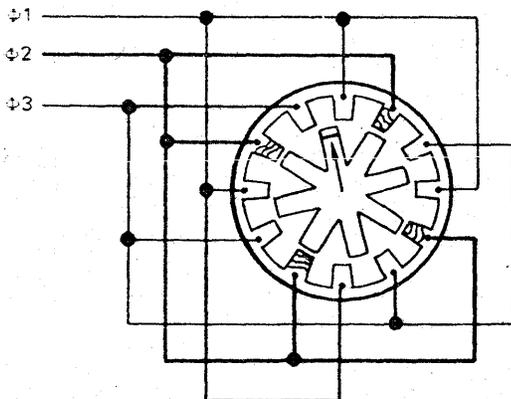

Figure 15 Position 2 (Trk 01)

3.2.4 Figure 16 shows the stepper motor with phase 3 of the stepper control logic active. Result is another $15°$ turn of the stepper motor lead screw.

3.3 Stepper Control Logic (Figure 17)

3.3.1 Power on Reset

At power on, FF1 and FF2 are reset and the not outputs activate Φ1 driver. With the Φ1 driver active, the position 1 windings in the stepper motor are excited and cause the rotor in the stepper motor to align as in Figure 14.

3.3.2 Forward Seek

● Seek a forward direction five tracks

● Assume:
  Present position of read/write head to be Track 00.
  Direction select at a minus level (from using system).
  Write gate is inactive.
  Head is loaded and door is closed.
  Five step pulses to be received (from using system).
  FF1 and FF2 are reset, phase 1 driver active.

Figures 17 and 18 show stepper control logic and timing diagram respectively. Minus Direction Select is inverted and becomes +Forward, this enables A2 and A3 of FF1 and FF2. Since both FF1 and FF2 are reset at this point, the FF1 line further enables A3.

When the first step pulse is sent to the control logic, it is anded with not write gate and then the step pulse clocks FF2 on. With FF2 on and FF1 off, phase 2 driver is activated and the Stepper Motor moves $15°$ in a counter-clockwise direction moving the carriage assembly one track towards the center of the diskette (track 01).

With FF2 on and FF1 off, AND blocks A2 and A3 are enabled. Upon receipt of the next step pulse, FF1 is clocked on and FF2 is clocked off. With FF1 on and FF2 on, phase 3 driver is activated and the stepper motor moves $15°$ in a counter-clockwise direction moving the carriage assembly one more track towards the center (track 02).

With FF1 on and FF2 off, AND blocks A2 and A3 are disabled. Upon receipt of the next step pulse,
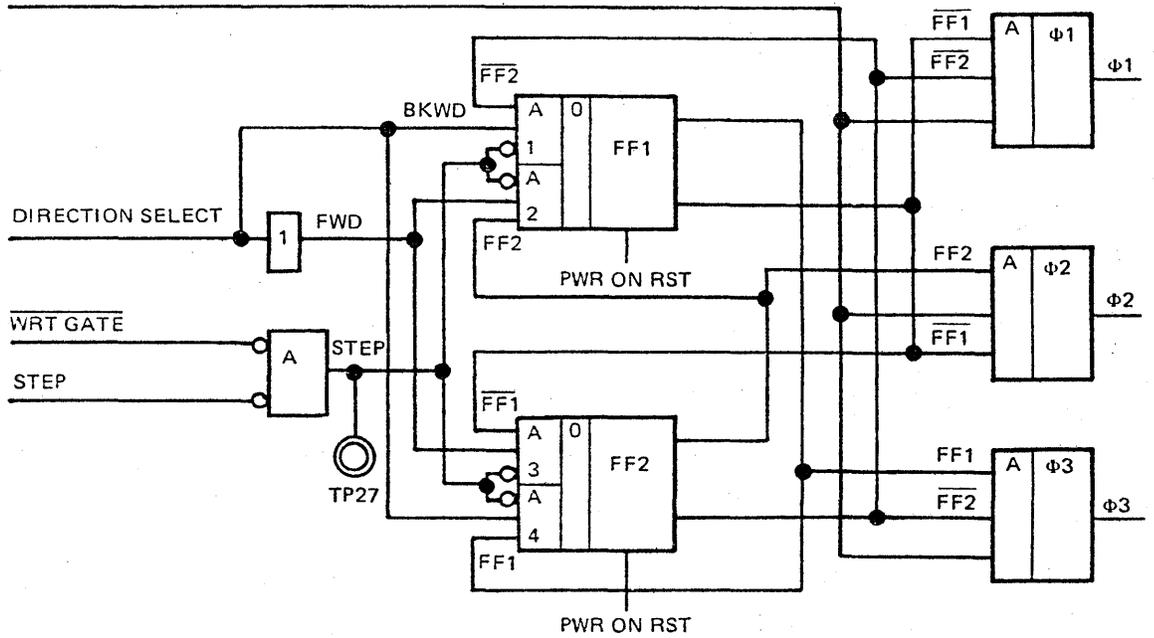
12

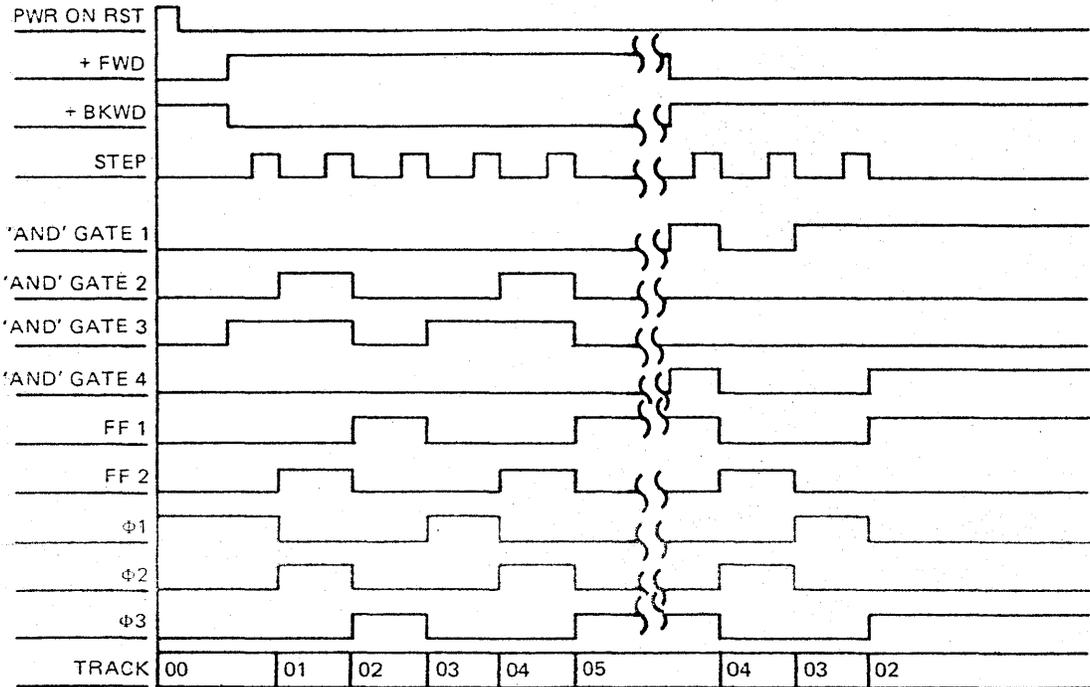Figure 17 Track Accessing (Stepper Control Logic)

Figure 18 Track Accessing

FF1 is clocked off and FF2 remains off. This causes phase 1 driver to be activated, turning the stepper motor an additional 15° in the counter-clockwise direction moving the carriage assembly one more track closer to the center (track 03).

The above process is continued until the host system stops sending step pulses, i.e., Track 05. At that time, FF1 is on and FF2 is off leaving phase 3 driver active. Figure 19 shows the stepper motor at this position.
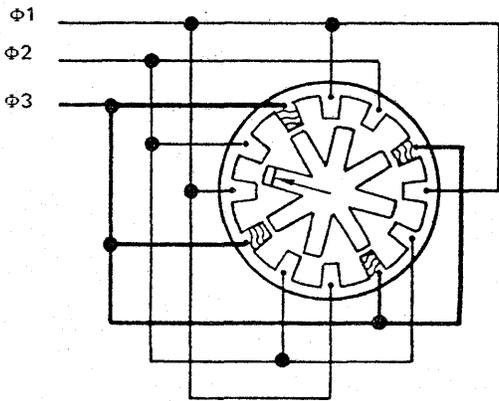

Figure 19 Stepper Motor at TRK 05

3.3.3 Reverse Seek (Ref. Figures 17 and 18)

● Seek in a Reverse Direction three tracks.

● Assume:
  Present position of read/write head to be Track 05.
  Direction Select at a positive level.
  Write gate is inactive.
  Head is loaded and door closed.
  3 step pulses to be received.
  FF1 is on, FF2 is off, phase 3 driver active.

Direction Select line, being positive, enables AND gates A1 and A4. With FF1 on and FF2 off, the first step pulse received is going to clock FF1 off and clock FF2 on. Phase 2 driver is activated by FF1 off and FF2 on, moving the stepper motor in a clockwise direction 15° or moving the carriage in a reverse direction one track.

The next step pulse received is going to clock FF2 off and leave FF1 off. This will cause phase 1 driver to become active and move the stepper motor an additional 15° in the clockwise direction

moving the read/write head one more track in the reverse direction.

With FF1 off and FF2 off AND gate A1 is enabled. The next step pulse received is going to clock FF1 on which in turn will activate phase 3 driver. This will again move the stepper motor in a clockwise direction 15° and the read/write head back to Track 02. The stepper motor will end up in the position as shown in Figure 20.
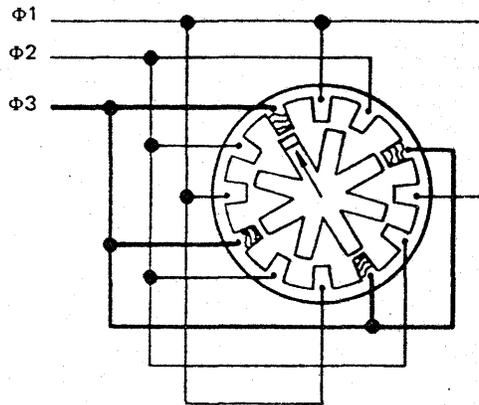

Figure 20 Stepper Motor at TRK 02

3.4 Track Zero Indicator

Track 00 Pin 42 is provided to the using system to indicate when the read/write head is at track zero.

Figures 21 and 22 show the logic and timing for Track Zero indication. The Track zero flag on the carriage assembly is adjusted so that the flag covers the photo transistor at track one. When the FF1 and FF2 are set off and the stepper moves to track zero, phase 1 is anded with Drv Sel Int and then is anded with Track Zero detect and Track Zero indication is sent to the using system.

Figure 21 Track 00 Flag

DRV SEL INT

TRACK | 4 | 3 | 2 | 1 | 0

|← →| 10MS

STEP

DIRECTION

FF1

FF2

TRACK 00
FLAG (TP 26)

ADJUST TO
TURN ON @ TK 01

TRACK 00
@INTERFACE
PIN 42

(TK 0 FLAG • Φ1)

Φ1
Φ2   ($\overline{FF1}$ • $\overline{FF2}$)

Φ3
($\overline{FF1}$ • FF2)

(FF1 • $\overline{FF2}$)

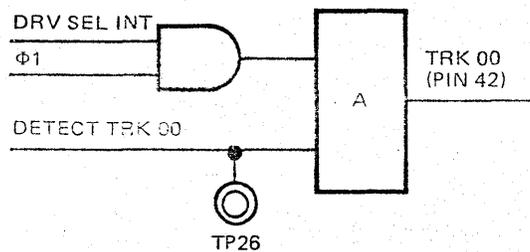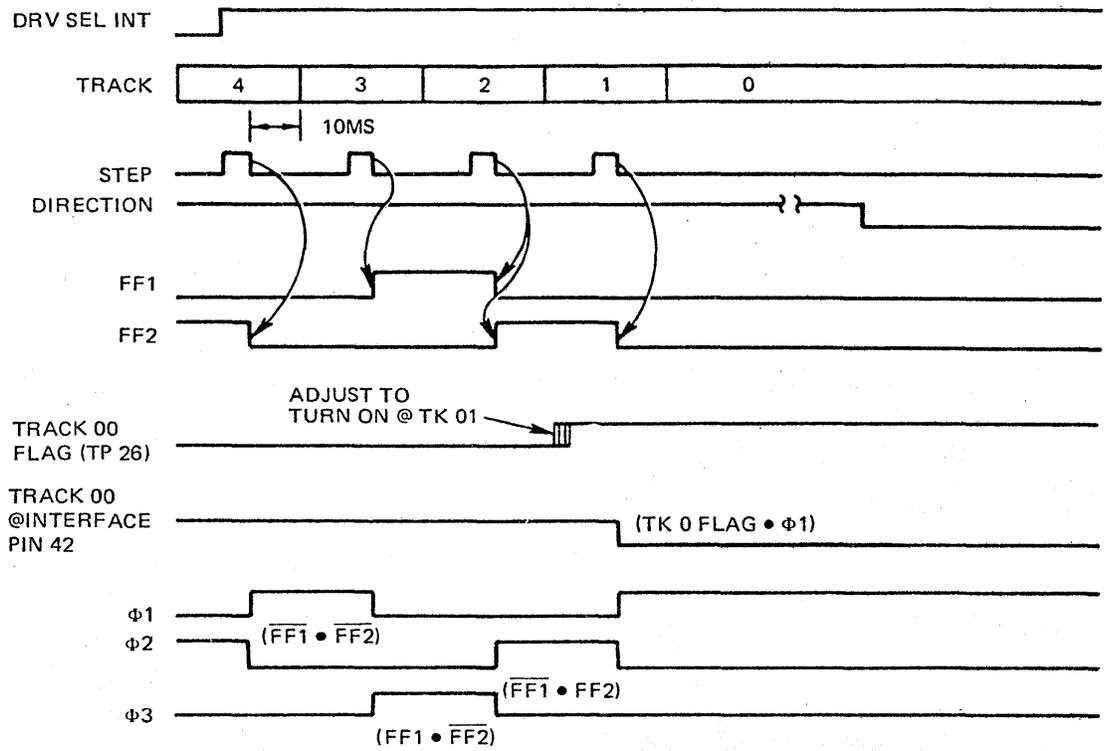**Figure 22   Track 00 Timing**

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4.0 READ-WRITE OPERATIONS

- SA800/801 uses double frequency NRZI recording method.

- The read/write head, in general, is a ring with a gap and a coil wound at some point on the ring.

- During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil.

- During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface.

4.1 The SA800/801 drive uses the double-frequency (2F) horizontal non return to zero (NRZI) method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell time thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, are provided by the using system. See Figure 23.

4.2 The read/write head is a ring with a gap and a coil wound some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a horizontal direction. See Figure 24.

4.3 During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized in one direction while the portion under the gap is magnetized in the opposite direction. This flux reversal represents a bit. See Figure 25.

4.4 During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface. The gap first passes over an area that is magnetized in one direction, and a constant flux flows through the ring and coil. The coil registers no output voltage at this point. When a recorded bit passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See Figure 26.
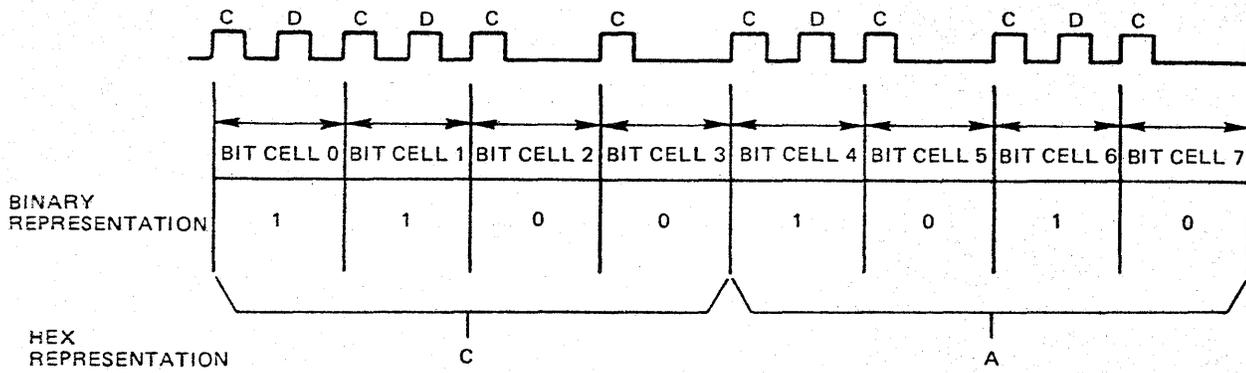
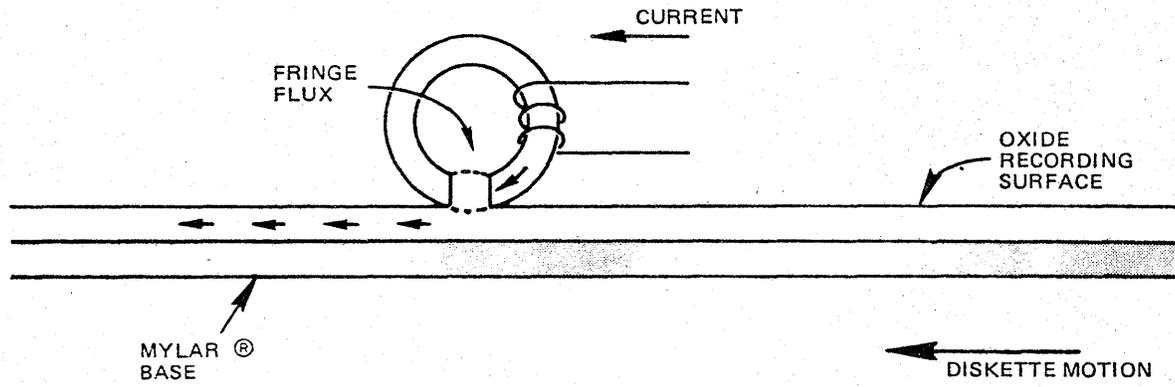|	BIT CELL 0	BIT CELL 1	BIT CELL 2	BIT CELL 3	BIT CELL 4	BIT CELL 5	BIT CELL 6	BIT CELL 7
BINARY REPRESENTATION	1	1	0	0	1	0	1	0

HEX REPRESENTATION   C   A

Figure 23   Bit Cell

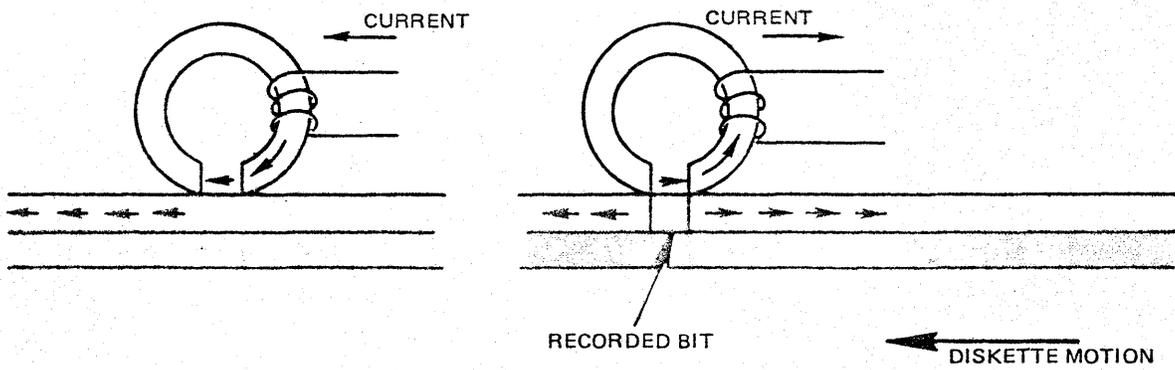
Figure 24   Basic R/W Head

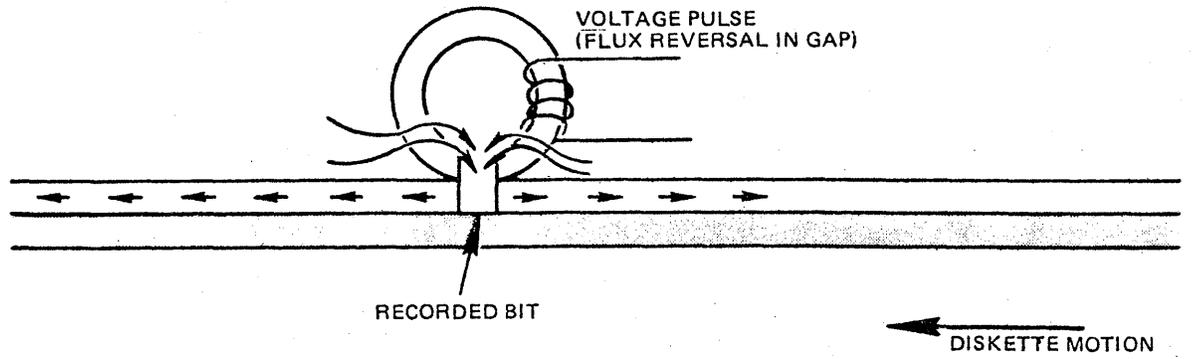**Figure 25   Recorded Bit**

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Figure 26 Reading a Bit

4.5 Figure 27 shows the 1F and 2F recording flux transitions with pulse relationship.
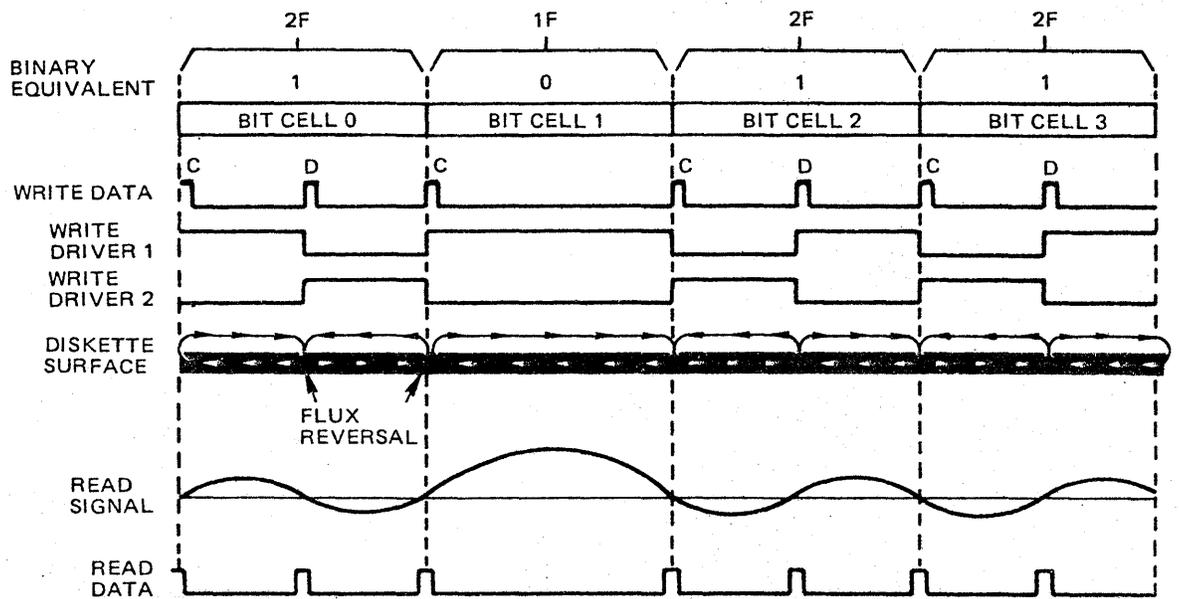

Figure 27 1F and 2F Recording Flux and Pulse Relationship

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5.0 READ/WRITE HEAD

● The read/write head contains three coils.

● When writing, the head erases the outer edges of the track to insure data recorded will not exceed the .012 track width.

● The head is ceramic.

5.1 The read/write head contains three coils. Two read-write coils are wound on a single core, center tapped and one erase coil is wound on a yoke that spans the track being written. The read-write and erase coils are connected as shown on Figure 28.

5.2 On a write operation, the erase coil is energized. This causes the outer edges of the track to be trim erased so as the track being recorded will not exceed the .012" track width. The straddle erasing allows for minor deviations in read/write head current so as one track is recorded, it will not "splash over" to adjacent tracks.

5.3 Each bit written will be directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. This will cause a change in the flux pattern for each bit. The current through either of the read/write coils will cause the old data to be erased as new data is recorded.

5.4 On a read operation, as the direction of flux changes on the diskette surface as it passes under the gap, current will be induced into one of the windings of the read/write head. This will result in a voltage output pulse. When the next data bit passes under the gap, another flux change in the recording surface takes place. This will cause current to be induced in the other coil causing another voltage output pulse.
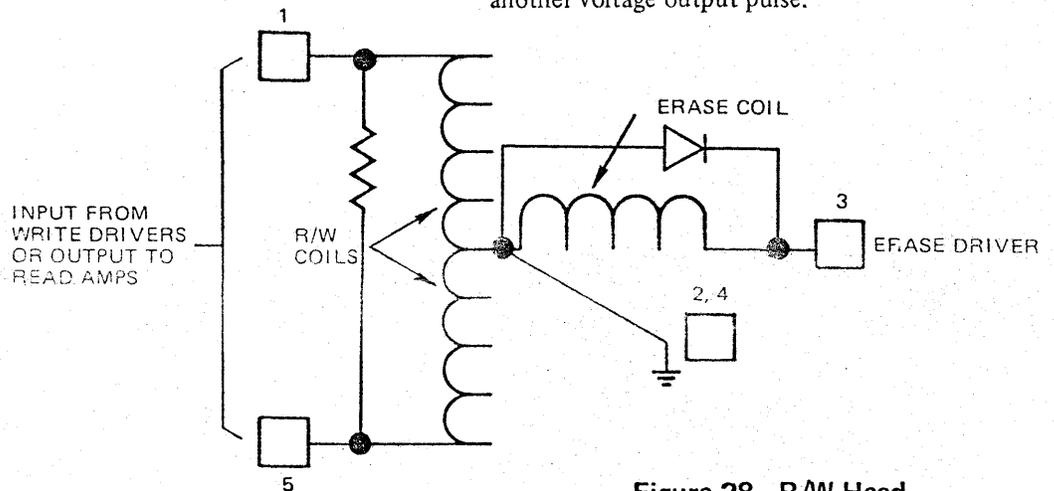

Figure 28 R/W Head

6.0 WRITE CIRCUIT OPERATION (FIGURE 29)

- The binary connected Write Data Trigger flips with each pulse on the Write Data line.

- The Write Data Trigger alternately drives one or the other of the Write Drivers.

- Write Gate allows write current to flow to the Write Driver circuits.

- Write Current sensed allows Erase Coil current.

6.1 Write data pulses (clock & data bits) are supplied by the using system. The Write Trigger "flips" with each pulse. The Q and Q outputs are fed to alternate Write Drivers.

6.2 Write Gate, from using system, and not Write Protect, are anded together to provide write current.

6.3 The output of one of the Write Drivers allows write current to flow through one half of the read/write coil. When the Write Trigger "flips", the other Write Driver provides write current to the other half of the read/write coil.

6.4 When write current is sensed flowing to the Write Drivers, a signal is generated to provide erase coil current.
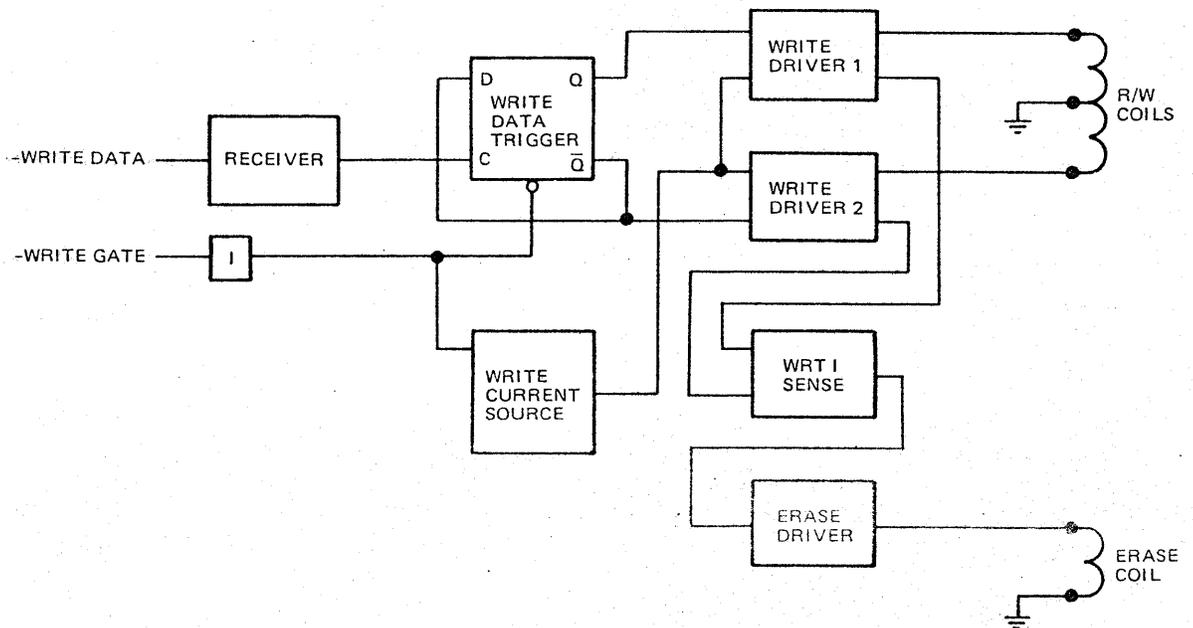

Figure 29   Write Circuit Functional Diagram

7.0 READ CIRCUIT OPERATION (FIGURE 30)

- Duration of all read operations is under control of the using system.

- When the head is loaded, the read signal amplitude becomes active and is fed to the amplifier.

- As long as the head is loaded and write gate is not active, the read signal is amplified and shaped, the square wave signals are sent to the data separator.

- The data separator separates the read data into clock pulses and data pulses.

7.1 When the using system requires data from the diskette drive, the using system must first load the head. With loading of the head and write gate being inactive, the read signal is fed to the amplifier section of the read circuit. After the amplification, the read signal is fed to a filter where the noise spikes are removed. The read signal is then fed to the differential amplifier.

7.2 Since a pulse occurs at least once every 4 μs and when data bits are present once every 2 μs, the frequency of the read data varies. The read signal amplitude decreases as the frequency increases. Note the signals on Figure 30. The differential amplifier will amplify the read signals to even levels and make square waves out of the read signals (sine waves).

7.3 The data separator is a two time constant separator, that is, the clock and data pulses must fall within pre-specified time frames or windows.
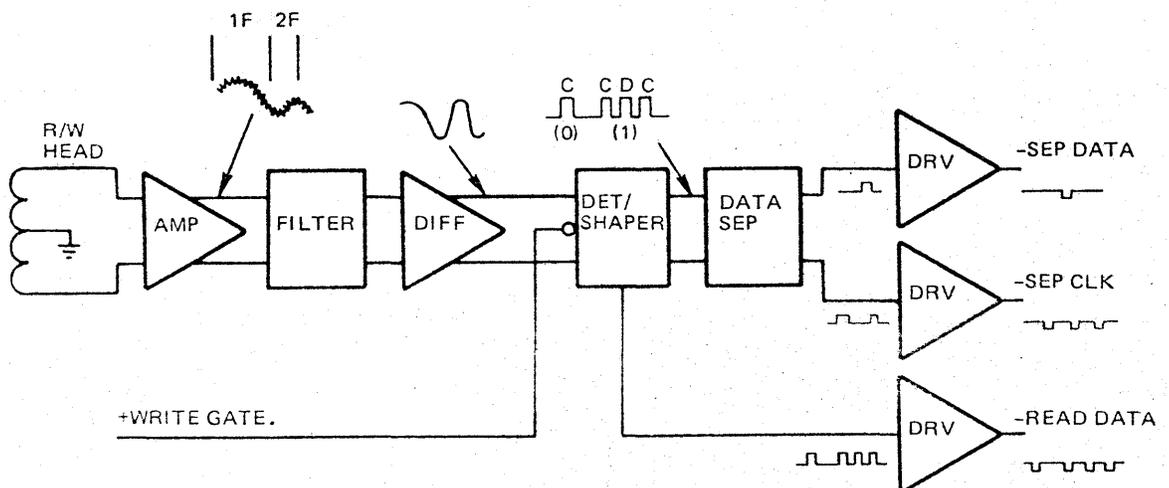
Figure 30 Read Circuit Functional Diagram

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The clock and data windows are developed in the data separation circuit. Figure 31 shows the functional diagram and Figure 32 shows the timing diagram of the circuit.

7.3.1 Two data windows are supplied. The short window, 2.9 μs, is used when the previous bit cell had a data pulse in it. The long window, 3.1 μs, is used when the previous bit cell had no data pulse.

7.3.2 If the data pulse initially falls in the data window, -separated data is sent back to the OR block that generates the data window to assure that the full data pulse is allowed through before the window falls.

7.3.3 The clock window will take up the remainder of the bit cell time, either 1.1 μs or 0.9 μs.

7.4 In discussing the data separator circuit, Figure 30, initially assume all circuits are reset (inactive)

and that the +READ DATA line contains what is shown in Figure 32.

7.4.1 With both SS1 and SS2 off, +Clk Window is active. The first Read Data pulse will be allowed through AND A2 and out as -Sep. Clk. -Sep. Clk. is sent out onto the interface line and to L1, SS1 and SS2. Since FF1 is off, SS1 will be held reset. The -Sep. Clk. pulse will trigger SS2. The output of SS2 is sent to the OR block which in turn becomes + Data Window enabling AND A1. The next pulse on + Read Data will be allowed through A1 becoming -Separated Data. -Separated Data sets L1 which in turn enables FF1. FF1 is clocked on by SS2 timing out (3.1 μs) and + Clk Window becoming active. The Q output of FF1 will hold SS2 reset and allow SS1 to trigger with receipt of the next clock pulse.

7.4.2 The next clock pulse, bit cell 1, is anded with +Clk Window and becomes the next -Sep. Clk.
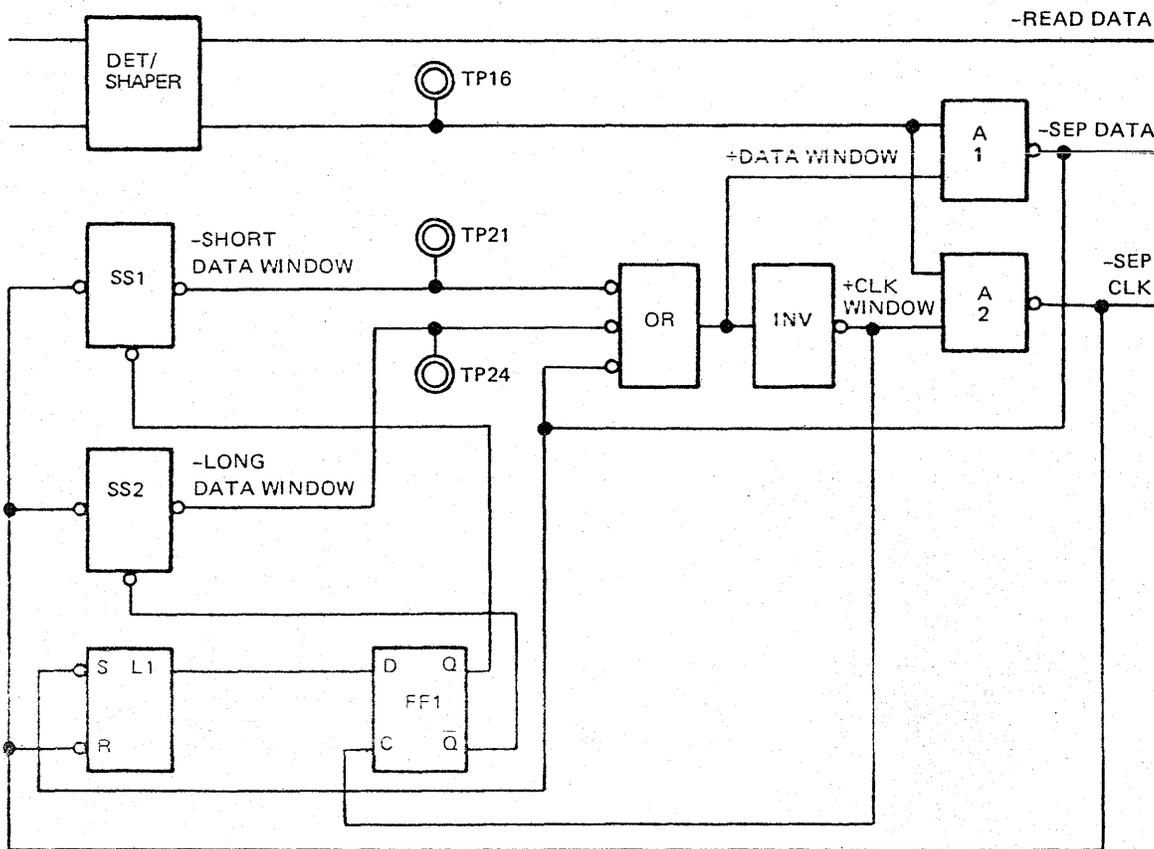

Figure 31   Data Separator Functional Diagram

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-Sep Clk will reset L1 and Trigger SS1 on. When SS1 becomes active, + Data Window becomes active enabling AND A1. Since bit cell 1 has no data bit in it, L1 will remain reset which will enable FF1 to be clocked off when +Data Window falls (2.9 μs). When FF1 is clocked off the Q output will hold SS1 reset and allow SS2 to be triggered.

7.4.3 The next clock pulse, bit cell 2, is anded with +Clk Window and becomes -Sep Clk. -Sep Clk will further reset L1, which was off, and trigger

SS2 on. When SS2 becomes active, -Long Data Window, and enables AND A1 allowing the data pulse in bit cell 2 to become -Sep Data. -Sep Data will set L1 which enables FF1 to be clocked on when +Data Window falls. When +Data Window falls, the $\overline{Q}$ output will hold SS2 reset and allow SS1 to trigger.

7.4.4 This procedure continues until the using system terminates the Read Operation by unloading the head.
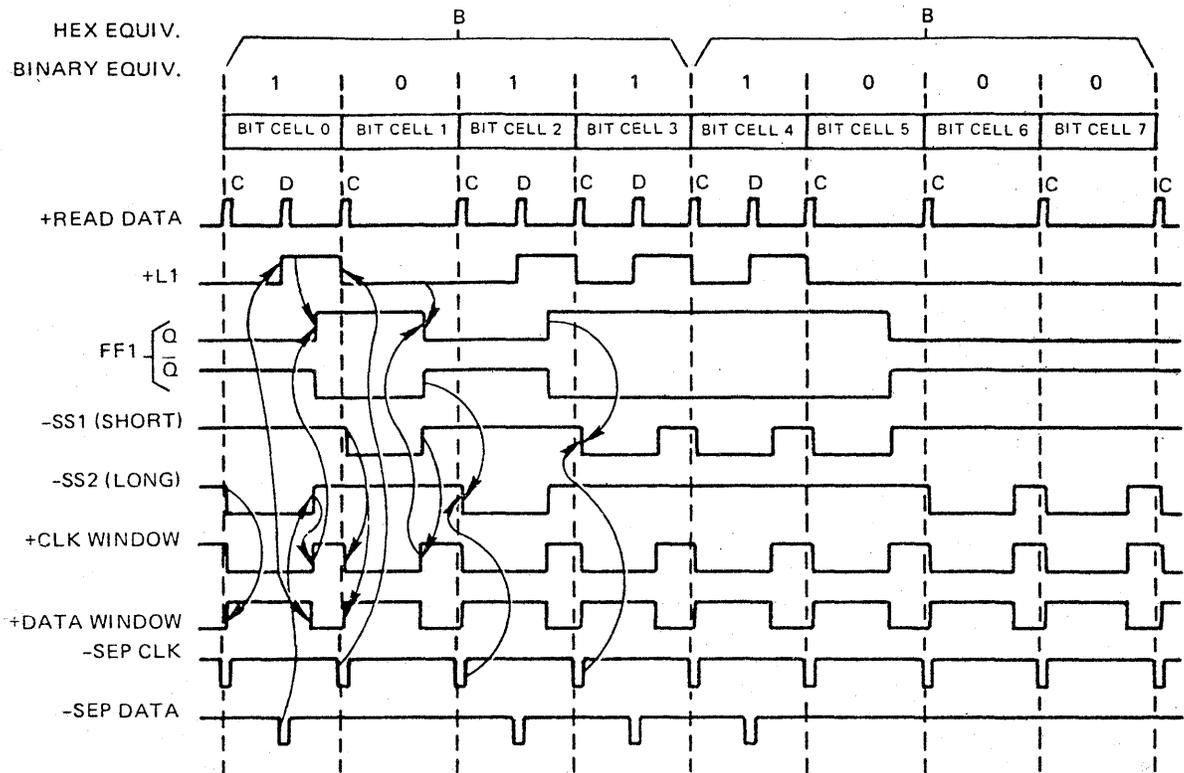

Figure 32 Data Separation Timing Diagram

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8.0 INTERFACE

The electrical interface between the SA800/801 drive and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third connector, J4, provides the AC power and frame ground.

8.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge card connector. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying. Refer to Figure 33.

8.2 AC Power

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined below for standard as well as optional AC power.

8.3 DC Power

DC power to the drive is via connector P5/J5 located on non-component side of PCB near the P4 connector. The three DC voltages and their specifications along with their P5/J5 pin designators, are outlined below.

P4 PIN	60 Hz		50 Hz	
	110 V (Standard)	208/230 V	110 V	220 V
1	90-127 VAC	180-253 VAC	90-127 VAC	180-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	90-127 V Rtn	180-253 V Rtn	90-127 V Rtn	180-253 V Rtn
MAX CURRENT	0.5 Amps	0.4 Amps	0.6 Amps	0.4 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	
P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max** 1.3 A Typ	100 mv
2	+24 V Return*			
3	− 5 V Return			
4	− 5 VDC	±0.25 VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional −7 to −16 VDC (Cut Trace 'L'	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

*The +24 VDC power requires a separate ground return line. Also, the +24 V Return, other Ground Return lines, and Frame Ground must be connected together at the main power supply.

Figure 33 Interface Connections
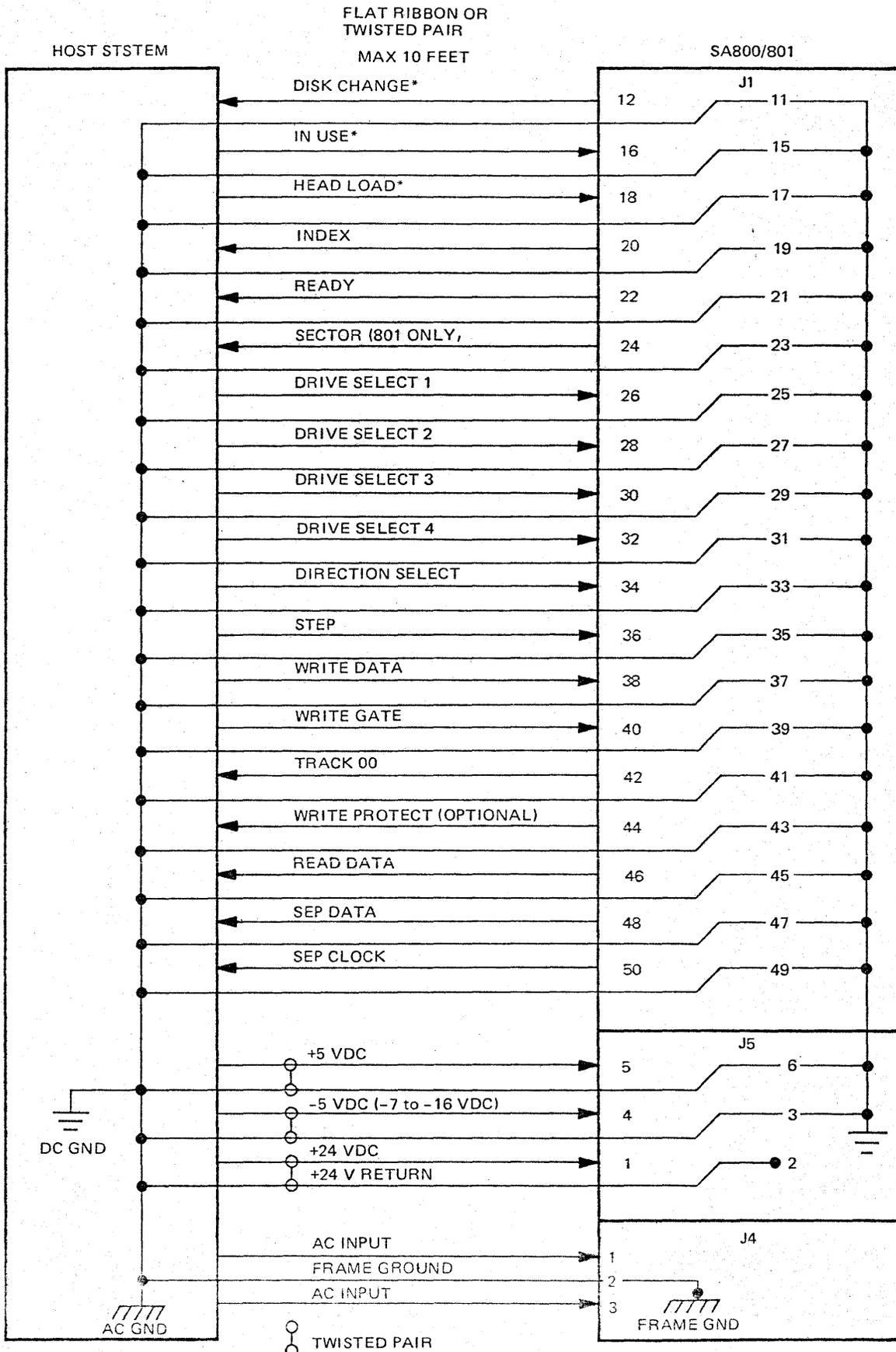
NOTE: Not shown are the nine Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10 and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9, 13 and 19 respectively. Reference section 7 of the 800/801 DEM Manual for uses of these lines.

*These interface lines are activated through a normally open trace which has pins installed. These lines can be used by either using, 1. a shoring plug, 2. wire wrapping, 3. soldering across.

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8.4 Output Lines

There are seven (7) output lines from the SA800 and eight (8) from the SA801. There also is one (1) optional output line from the SA800/801.

The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state the driver is off and the collector current is a maximum of 250 microamperes. The receiver should be a Schmidt trigger type device. Refer to Figure 34 for circuit.
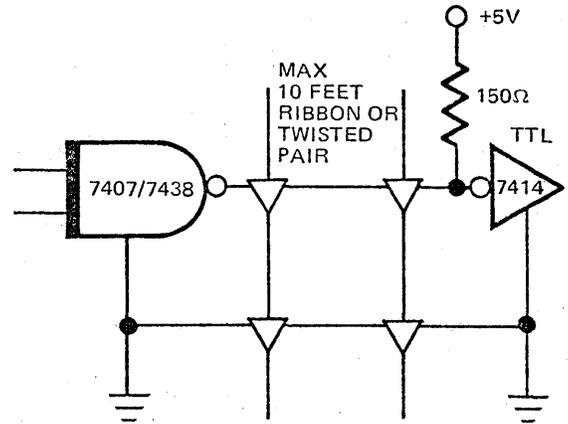

Figure 34

Shugart Associates