PM-REV11 Console Bootstrap ROM Module Manual

Plessey
Peripheral
Systems

PM-REV11 Console Bootstrap ROM Module Manual

September 1978 Revision A

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET 0-0

Preface

This manual provides the information needed to install and operate the PM-REV11 Console Bootstrap ROM Module manufactured by Plessey Peripheral Systems, Irvine, California.

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET 0-1

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Section 1

General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the PM-REV11 Console Bootstrap ROM Module manufactured by Plessey Peripheral Systems, Irvine, CA 92714.

The material is arranged into the following sections:

- Section 1 - General Information

  This section contains a brief general description of the PM-REV11 and the specifications of the bootstrap module.

- Section 2 - Installation

  This section explains the procedures for equipment installation.

- Section 3 - Functional Description

  This section contains a detailed functional description of the PM-REV11 including bank addressing, DMA refresh operation, switch register and bus termination.

- Appendices - Drawings

  The appendices contain the parts list, logic diagrams, and assembly drawings required for the maintenance of this unit.

1.2 GENERAL DESCRIPTION

The PM-REV11 is a Bootstrap ROM Loader Q-bus device designed to operate with the DEC LSI-11. There are four configurations of the PM-REV11 which contain various combinations of a bootstrap ROM, Switch Register, DMA Refresh, and Bus Termination. The model configurations are shown on the following page.

Model Number	Plessey Reference	Function Devices
PM-REV11A	701665-100	Bootstrap ROM, Switch Register, DMA Refresh, and Bus Terminator
PM-REV11B	701665-101	Bootstrap ROM, DMA Refresh, and Bus Terminator
PM-REV11C	701665-102	Bootstrap ROM, DMA Refresh, and Switch Register
PM-REV11D	701665-103	Bootstrap ROM, DMA Refresh

These different configurations are accomplished by depopulating functions which are not required on the basic PM-REV11 printed circuit board.

1.2.1 Bootstrap ROM

The bootstrap ROM consists of two blocks of 256 x 16 bit words which can be addressed in the upper 4K bank of memory (peripheral). The PM-REV11 bootstrap ROM can be switch selected to respond starting at memory location 173000_8, which is the location accessed by the processor on power-up sequence.

1.2.2 Switch Register

For Switch Register operation, the PM-REV11 is connected to a user supplied bank of 16 switches via the 20-pin connector. The Switches can be accessed at location 177570_8 which corresponds to the console Switch Register.

1.2.3 DMA Refresh

The PM-REV11 has the ability to refresh all semiconductor memories in the system. The PM-REV11 obtains bus control (DMA) and refreshes one row of memory every 30μsec.

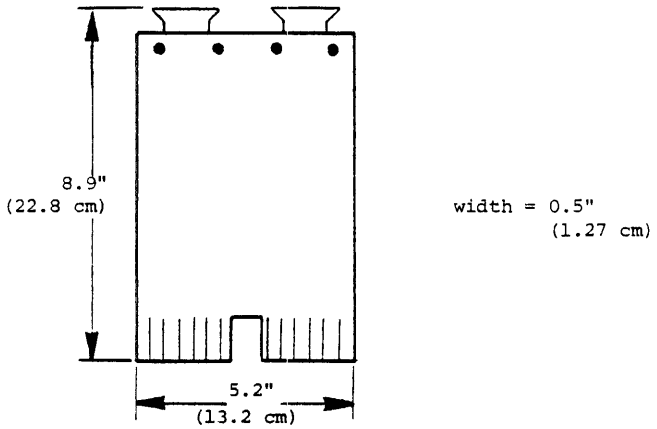
1.2.4 Bus Terminator

A 120Ω Bus Terminator is provided in the PM-REV11 versions A and B.

1.3 SPECIFICATIONS

1.3.1 Physical Specifications

The PM-REV11 is contained on a single dual-wide printed circuit board with dimensions as shown below. It is a multi-layer etch board with internal power and ground planes, and logic traces on solder and component sides.



1.3.2 Environmental Specifications

Temperature:

Operating	0°C to 50°C
Nonoperating	-40°C to 85°C

Relative Humidity: 10% to 95% without condensation

1.3.3 Power Requirements

+5VDC 0.8A

Section 2

Installation

This section provides information for the installation and operation of the PM-REV11 bootstrap ROM module.

2.1 UNPACKING AND INSPECTION

The PM-REV11 is shipped in a special packing carton designed to keep the board from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

To unpack the PM-REV11, remove any packing materials and visually inspect for physical damage.

2.2 INSTALLATION AND SWITCH SETTINGS

Refer to Figure 2-1 for switch locations.

2.2.1 ROM Bank Addressing

Bank addressing is determined by switch settings. Refer to Section 3.1.1 for Bank Ø addressing and to Section 3.1.2 for Bank 1 addressing. Each bank can be switch disabled as shown in Table 2-1 below.

SW1 POSITION	FUNCTION	OPTIONS
8	Bank Ø enable	ON = Bank Ø responds when addressed (See Tables 2 and 3)
		OFF = Bank Ø disabled
6	Bank 1 enable	ON = Bank 1 responds when addressed (See Table 4)
		OFF = Bank 1 disabled

Table 2-1: Bank Ø and Bank 1 Disabled

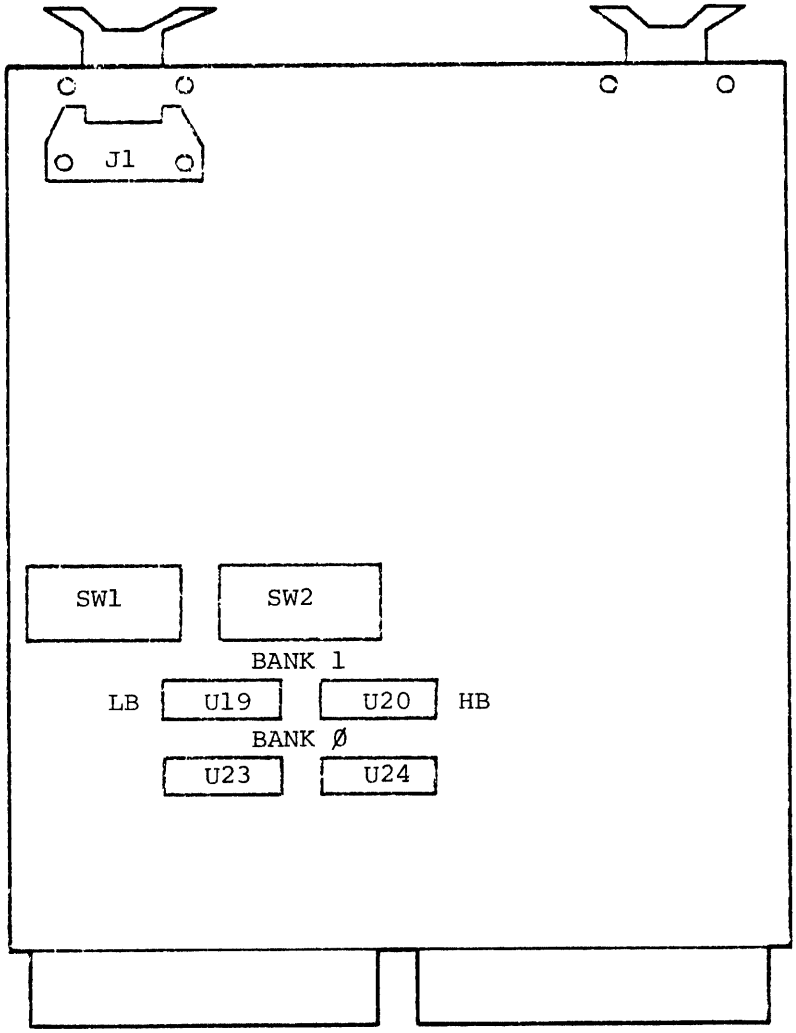


Figure 2-1: Switch Locations

2.2.2 Backplane Installation

The PM-REV11 can be mounted in the following Q-bus backplanes:

- PM-F11/LS4 Plessey 4-slot backplane
- PM-F11/LS9 Plessey 9-slot backplane
- PM-F11/QU Plessey 9-slot backplane
- H9270 DEC 4-slot backplane
- DDV11-B DEC 9-slot backplane
- H9281 DEC backplane

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2.2.3 DMA Refresh

The DMA refresh option is switch selectable to enable refresh or allow refresh by another source. Refer to Table 2-2 for DMA refresh switch (SW1) selection.

SW1 POSITION	FUNCTION	OPTION
1	Refresh Disable	ON = no refresh OFF = PM-REV11 refreshes

Table 2-2: DMA Refresh Option

If models PM-REV11A or B are to be used to refresh, no other DMA device may be used, and the module should be placed in the last location on the bus. If another DMA device is to be used, models PM-REV11C or D (no bus termination) may be used providing the PM-REV11 has the highest DMA priority.

2.2.4 Switch Register Option

Switch register operation is available with versions PM-REV11A or C. This option can be switch disabled as shown in Table 2-3. Only the switch register interface is supplied with the PM-REV11. The user is responsible for supplying switches, mounting panel and interface cables for the switches.

SW1 POSITION	FUNCTION	OPTION
3	Switch Register Disable	ON = no switch register OFF = switch register read at $1,7570_8$

Table 2-3: Switch Register Disable

NOTE: On versions REV11B and REV11D, SW1 position 3 must be on.

2.2.5 Module Installation

When addressing and option switches have been set, plug the PM-REV11 module into the appropriate priority backplane slot.

Section 3

Functional Description

3.1 BOOTSTRAP ROM OPERATION

The bootstrap ROM function consists of two banks of 256 words of storage. The two banks (Bank Ø and Bank 1) have different addressing capabilities so each will be described separately. Both banks must reside in the upper 4K of memory (peripheral). Each bank can be individually switch disabled as shown in Table 2-1.

The PM-REV11 is designed to use type SN74S471 PROMS which are organized as 256 x 8. Each bank requires two PROMS. The pin addressing is shown in Figure 3-1. Addresses are high true at PROM's (non-inverted). Data is high true (non-inverted).

3.1.1 Bank Ø Addressing

The starting address of Bank Ø may be placed at any 256 word boundary in upper 4K of memory (160000_8 through 177777_8). Switch 2 (SW2, positions 2, 3, 6, and 7, determine the starting address of Bank Ø and represent address bits AØ9, A1Ø, A11, and A12 respectively. The size of Bank Ø can be controlled by selecting the final address. SW2 positions 1, 4, 5, and 8, which represent address bits AØ8, AØ7, AØ6, and AØ5 respectively, control the final address to which Bank Ø will respond. These switch positions allow size increments of 16 words up to 256. Refer to Table 3-1 for address switch settings. See Figure 2-1 for switch locations.

STARTING ADDRESS

ADDRESS	S2-7	S2-6	S2-3	S2-2	NOTE
160000	ON	ON	ON	ON	
161000	ON	ON	ON	X	
162000	ON	ON	X	ON	
163000	ON	ON	X	X	
164000	ON	X	ON	ON	
165000	ON	X	ON	X	
166000	ON	X	X	ON	
167000	ON	X	X	X	
170000	X	ON	ON	ON	
171000	X	ON	ON	X	
172000	X	ON	X	ON	
173000	X	ON	X	X	POWER-UP ADDRESS
174000	X	X	ON	ON	
175000	X	X	ON	X	
176000	X	X	X	ON	
177000	X	X	X	X	

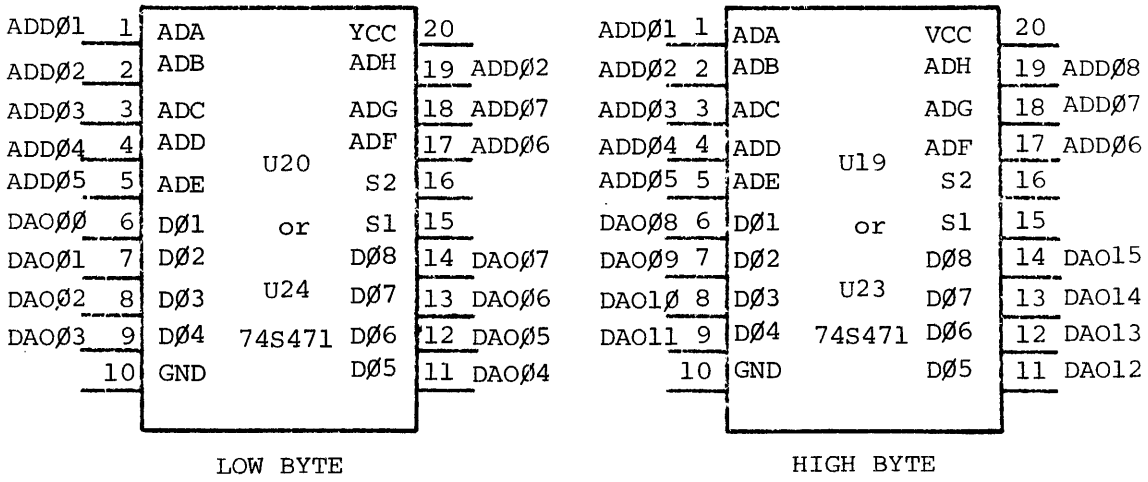
(X = OFF)

BANK Ø SIZE

ADDRESS	S2-1	S2-4	S2-5	S2-8	BANK SIZE (WORDS)
XXX036	ON	ON	ON	ON	16
XXX076	ON	ON	ON	X	32
XXX136	ON	ON	X	ON	48
XXX176	ON	ON	X	X	64
XXX236	ON	X	ON	ON	80
XXX276	ON	X	ON	X	96
XXX336	ON	X	X	ON	112
XXX376	ON	X	X	X	128
XXX436	X	ON	ON	ON	144
XXX476	X	ON	ON	X	160
XXX536	X	ON	X	ON	176
XXX576	X	ON	X	X	192
XXX636	X	X	ON	ON	208
XXX676	X	X	ON	X	224
XXX736	X	X	X	ON	240
XXX776	X	X	X	X	256

(X = OFF)

Table 3-1: Bank Ø Addressing



EXAMPLE 1: If the data shown below is to be read from PROM after programming at address = 164002_8 and data = 031705_8, the voltage (logic) levels at each pin would be:

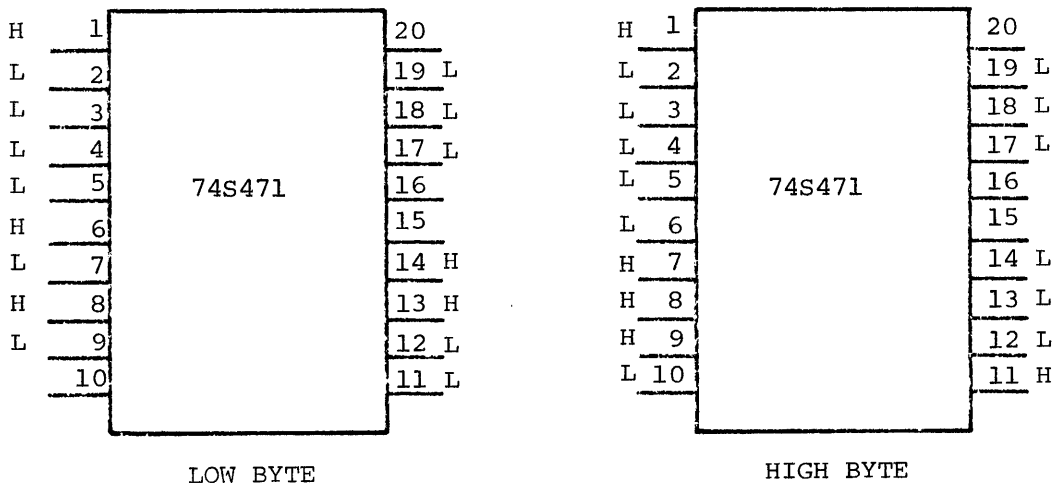


Figure 3-1: PROM Addressing

SIZE	CODE IDENT NO.	DWG NO.
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EXAMPLE 2: If you choose to have 96 words starting at the 256 word boundary, 173000_8, the first memory location which Bank Ø will respond is 173000_8 which is determined by SW2 positions 2,3,6, and 7. Final location in Bank Ø is 173336_8 (one less than 173340_8) which is determined by SW1 positions 1,4,5, and 8. Bank Ø is 96 (6 x 16) words long. Switch positions and address bits for this example are shown in Table 3-2.

SW2 POSITION	ADDRESS BIT	EXAMPLE STATE
1	AØ8	ON
2	AØ9	OFF
3	A1Ø	OFF
4	AØ7	OFF
5	AØ6	ON
6	A11	ON
7	A12	OFF
8	AØ5	OFF

Table 3-2: SW2 Positions for Bank Ø Addressing and ON/OFF State for Example 2.

3.1.2 Bank 1 Addressing

The starting address of Bank 1 is selected similarily to Bank Ø except that there is not provision for size control. When Bank 1 is used it responds to all 256 locations. The starting address can be at any 256 word boundary in the upper 4K (160000_8 through 177776_8) of memory (Refer to Table 3-3 for address switch settings). Switch 2 (SW2) positions 2, 4,5, and 7 represent address bits AØ9, A1Ø, A11, and A12 respectively.

EXAMPLE 3: If you choose to have 256 words starting at the 256 word boundary, 164000_8, the first memory location to which Bank 1 will respond is 164000_8. Final location in Bank 1 is 164776 (one less than 165000_8). SW2 positions and corresponding address bits are shown in Table 3-2.

STARTING ADDRESS

ADDRESS	S1-7	S1-5	S1-4	S1-2	NOTE
160000	ON	ON	ON	ON	
161000	ON	ON	ON	X	
162000	ON	ON	X	ON	
163000	ON	ON	X	X	
164000	ON	X	ON	ON	
165000	ON	X	ON	X	
166000	ON	X	X	ON	
167000	ON	X	X	X	
170000	X	ON	ON	ON	
171000	X	ON	ON	X	
172000	X	ON	X	ON	
173000	X	ON	X	X	POWER-UP ADDRESS
174000	X	X	ON	ON	
175000	X	X	ON	X	
176000	X	X	X	ON	
177000	X	X	X	X	

(X = OFF)

Table 3-3: Bank 1 Addressing

SW2 POSITION	ADDRESS BIT	EXAMPLE STATE
7	A12	ON
5	A11	OFF
4	A1Ø	ON
2	AØ9	ON

Table 3-4: SW2 Positions for Bank 1 Addressing and ON/OFF State for Example 3.

3.2 DMA REFRESH OPERATION

The PM-REV11 is capable of refreshing up to 32K words of dynamic semiconductor memory. Every 30µsec the PM-REV11 requests control of the I/O bus and becomes bus master. After becoming bus master the PM-REV11 logic executes one DMA cycle which refreshes one of 64 rows of memory. The maximum time interval allowed between identical row refreshes is 2 msec. (For 64 rows of memory, 64 rows x 30µsec = 1.92 msec, which meets the interval requirement).

If models PM-REV11A or B are to be used to refresh, no other DMA device may be used, and the module should be placed in the last location on the bus. If another DMA device is to be used, models PM-REV11C or D (no bus termination) may be used providing the PM-REV11 has the highest DMA priority. The DMA refresh option is also switch selectable to enable refresh or allow refresh by another source.

3.3 SWITCH REGISTER

The provision for switch register operation is available with versions PM-REV11A or C. Via connector J1, a bank of 16 external switches can be read at location 177570_8. The option can be switch disabled as shown in Table 2-3. The connector pin designations are shown in Figure 3-2. External switches must be high true (high = 5V, low = ØV) and the respective signals are defined in Table 3-5.

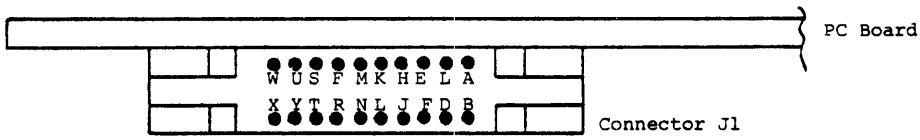


Figure 3-2: Pin Designations

REV11

CONNECTOR PIN	SIGNAL
J1-A	SWRØØ
B	SWRØ1
C	SWRØ2
D	SWRØ3
E	SWRØ4
F	SWRØ5
H	SWRØ6
J	SWRØ7
K	SWRØ8
L	SWRØ9
M	SWR1Ø
N	SWR11
P	SWR12
R	SWR13
S	SWR14
T	SWR15
U	+5VDC
V	N/C
W	N/C
J1-X	GND

Table 3-5: Switch Register Connector Pin Designations

3.4 BUS TERMINATION

The PM-REV11A or B contains Bus Termination as shown in Figure 3-3. This configuration terminates bus lines to 3.42 volts and 123Ω.

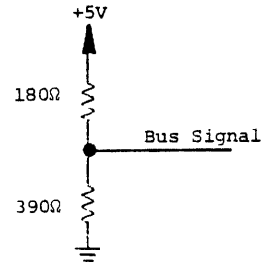


Figure 3-3: Bus Termination

Termination is provided for all bussed signals on the Q-bus.

Appendix A

Parts List

PL701665-100 REV. C

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET A-1

PARTS LIST	Plessey Microsystems	PREPARED BY: IAQUINTA 11-17-77	PARTS LIST NO: PL701665-100	REV LTR: C
ASSY TITLE: BOARD ASSEMBLY CONSOLE & BOOT ROM BOARD PM-REVII-A		CHECKED BY: [illegible] 12-1-77	CODE IDENT NO: 52648	DWG NO: 1234570 REV: B
		REP ENGR: [illegible] 12-5-77		SH 1 OF 7
		OTHER: [illegible] 12-6-77	CONTRACT NO:	

LTR	DESCRIPTION	DATE	APPROVED
A	REL TO PROD EO2348	7-18-78	[illegible]
B	INCORP EO 2496	8-28-78	[illegible]
C	INCORP EO 2619	10-11-78	[illegible]

LTR	DESCRIPTION	DATE	APPROVED

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR	C	C	A	B	A	A	C			
	SHEET	1	2	3	4	5	6	7	8	9	10

INTERPRET SYMBOLS USED AS FOLLOWS:

A = PURCHASED ITEM; B = FABRICATED ITEM; C = SPECIFICATION OR SOURCE CONTROL ITEM; D = ALTERED ITEM; E = SELECTED ITEM; F = CUSTOMER FURNISHED ITEM; G = BULK ITEM

PARTS LIST	Plessey Microsystems	CODE IDENT NO: 52648	PARTS LIST NO: PL701665-100	SH 2	REV LTR: C

CROSS INDEX OF REFERENCE DESIGNATIONS TO FIND NO.

REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.
U4	6	R2	27		48		
U3	7	R7,9	28	C8	49		
U6,14	8	R5,16	29	C7	50		
U10	9	R6,17	30	C4	51		
U9	10	R8,14,15	31	C9	52		
U22	11		32	C15,16	53		
U12	12		33	CR1	54		
U13,16,18	13	R10	34	SW1,2	55		
U27,28	14	R4	35				
U34	15	R12,19,20	36				
U17	16	R11	37				
U1,2,21	17	R3	38				
U15	18		39				
U7	19	RU3 THRU 7	40				
U25	20	RU8 THRU 12	41				
U26,30,31,32	21	RU13,14	42				
U5,11	22	RU1,2	43				
U29,33	23		44				
U8	24	R1	45				
U23	25	C1,2,5,6,10 THRU 14	46				
U24	26	C3	47				

SIZE	CODE IDENT NO.	DWG NO.	
A	52648	MA 701665	
SCALE	REV A	SHEET A-2	

REVISION	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE			
										C/I CODE	INV ON HAND	PAR	UNIT COST
		1	701664-001	P.W.B/ CONSOLE & BOOT ROM BD. PM-REVII				1					
								2					
								3					
		1	701339-001	HANDLE				4					
								5					
		1	SN7404	I.C./ HEX INVERTER	T.I.			6					
		1	SN7408	I.C./ QUAD 2-INPUT AND				7					
		2	SN7474	I.C./ DUAL D FLIP FLOP				8					
		1	SN74S00	I.C./ QUAD 2-INPUT NAND				9					
		1	SN74S04	I.C./ HEX INVERTERS				10					
		1	SN74S09	I.C./ QUAD 2-INPUT AND, O.C.				11					
		1	SN74S10	I.C./ TRIPLE 3-INPUT NAND				12					
		3	SN74S85	I.C./ 4 BIT MAGNITUDE COMPARATORS	T.I.			13					
		2	SN74S373	I.C./ OCTAL D LATCHES	T.I.			14					
B		1	SN74S08	I.C / HEX INVERTER				15					
		1	SN74LS393	I.C./ DUAL 4 BIT BINARY COUNTER				16					
		3	SN74LS244	I.C./ OCTAL 3 STATE BUFFERS				17					
		1	SN74123	I.C./ DUAL MONO. MULTIVIBRATOR				18					
		1	SN74175	I.C./ QUAD D FLIP-FLOP	T.I.			19					
		1	DS8136	I.C./ 6 BIT COMPARATOR	NATIONAL			20					
		4	DS8641	I.C./ QUAD BUS TRANSCEIVER	NATIONAL			21					
		2	136000-038	I.C./ QUAD 2-INPUT NAND, O.C.				22					
		2	136021-381	I.C./ QUAD NOR RECEIVER				23					
		1	NE555	I.C./ TIMER	SIGNETICS			24					
		1	100120-002	I.C./ 256 X 8 BIT PROM				25					
		1	100120-001	I.C./ 256 X 8 BIT PROM				26					

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET A-3

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
	1	RC07GF 101J	RESISTOR/100Ω, ±5%, 1/4 W	MIL-R-11			27					
	2	RC07GF 151J	150Ω				28					
	2	RC07GF 181J	180Ω				29					
	2	RC07GF 391J	390Ω				30					
	3	RC07GF 471J	470Ω				31					
							32					
							33					
	1	RC07GF 102J	1K				34					
	1	RC07GF 332J	3.3K				35					
	3	RC07GF 472J	4.7K				36					
	1	RC07GF 103J	10K				37					
	1	RC07GF 223J	RESISTOR/22K, ±5%, 1/4 W	MIL-R-11			38					
							39					
	5	100013-012	RESISTOR MODULE, 180Ω				40					
	5	100013-011	RESISTOR MODULE, 390Ω				41					
	2	750-81-R4.7K	RESISTOR MODULE, 4.7KΩ	CTS			42					
	2	100013 -003	RESISTOR MODULE, 1K				43					
							44					
	1	3005P-1-103	TRIMPOT, 10K, ±10%, 1/2 W	BOURNS			45					
	9	CGA103Z0Z	CAPACITOR, .01μf	UNITRODE			46					
	1	CK05BX 102K	.001μf, ±10%, 200V	MIL-C-11015			47					
							48					
	1	CM05ED 560J03	56pf, ±5%, 500V	CDE			49					
	1	CM05FD 331J03	330pf, ±5%, 500V	CDE			50					
	1	CD15FD 471J0S	470pf, ±5%, 500V	CDE			51					
	1	CM05CD 050D03	CAPACITOR, 5pf, 500V	CDE			52					

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET A-4

ASSY CODE	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE			
										C/I CODE	INV ON HAND	PAR	UNIT COST
		2	150D156 X0020B2	CAPACITOR, 15μf, ±20%, 20V	SPRAGUE			53					
C		1	138000-001	DIODE				54					
		2	435668-7	SWITCH, DIP, 8 POS	AMP			55					
		1	3428 -1002	CONNECTOR	3M			56					
		2	MS16535-154	RIVET/ TUBULAR OVAL HD .123 DIA X.188 LG ALALY				57					
								58					
		REF	SD701665	SCHEMATIC DIAGRAM				59					
								60					
								61					
								62					
								63					
								64					
								65					

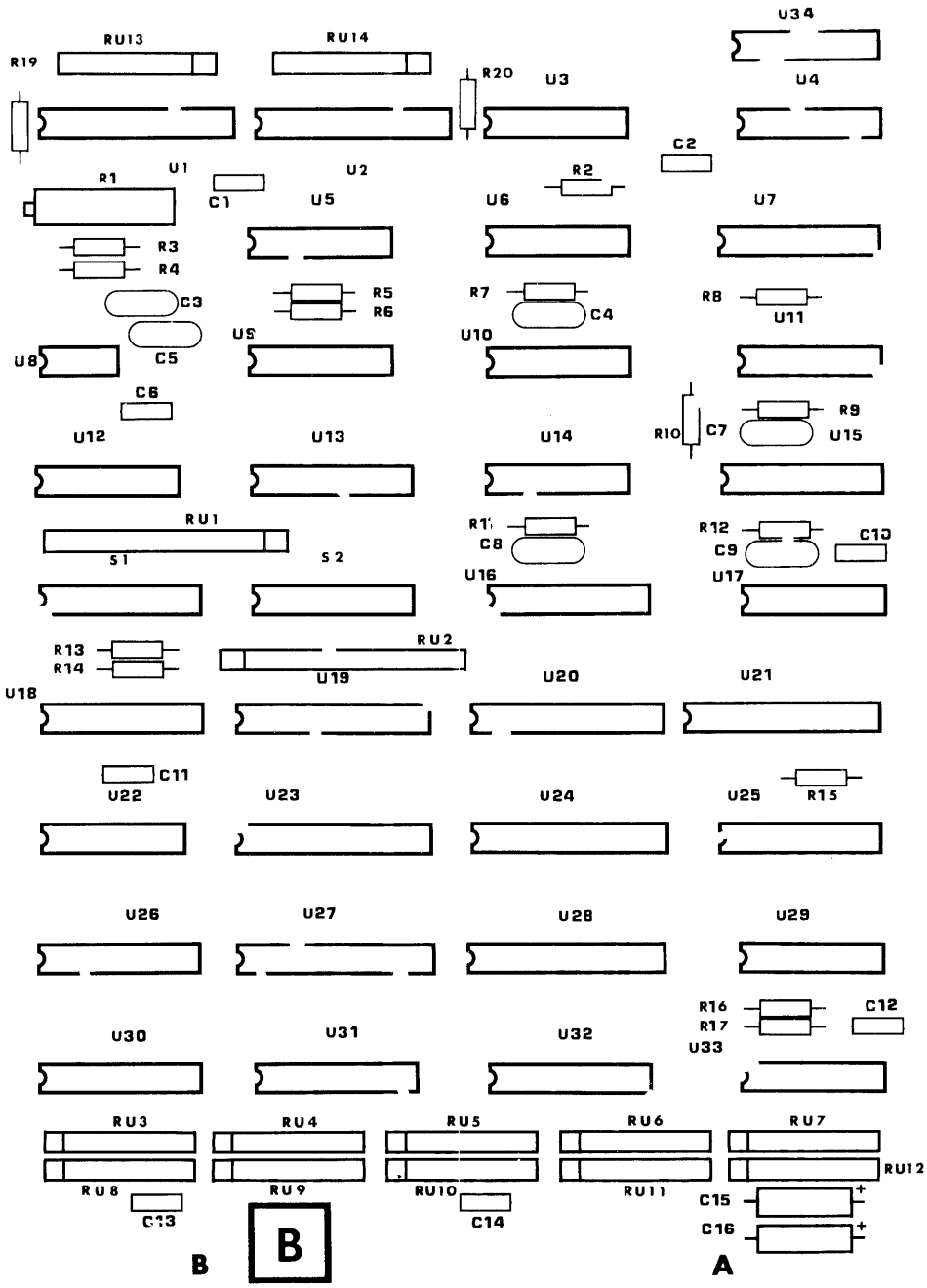
SIZE	CODE IDENT NO.	DWG NO.	
A	52648	MA 701665	
SCALE	REV A	SHEET A-5	

Appendix B

Assembly Drawing

701665 REV. C

SIZE	CODE IDENT NO.	DWG NO.	
A	52648	MA 701665	
SCALE	REV A	SHEET B-1	



JUMPER LIST	
FROM	TO
U34-3	U12-4(PIN)
U34-2	U6-6
U34-1	U4-1
U34-7	U4-7
U34-14	U4-14

SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 701665
SCALE	REV A	SHEET B-2

FORM 000021

Appendix C

Schematic Diagrams

SD701665 REV. C

SIZE	CODE IDENT NO.	DWG NO.	
A	52648	MA 701665	
SCALE	REV A	SHEET C-1	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL TO PROD EO2348	7-18-78	
	B	INCORP EO2496	8-28-78	
	C	INCORP EO 2619	10-11-78	

LAST REFERENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U34
RESISTOR	R20
CAPACITOR	C16
RESISTOR MODULE	RU14
SWITCH	S2
DIODE	CR1

REFERENCE DESIGNATION NOT USED	
RESISTOR	R13, 18

REF DESIG.	GATES USED PER TOTAL	PART NUMBER
U9	4/6	74S04
U14	1/2	7474
U34	1/4	74S08

SOLDER SIDE CONNECTOR			COMPONENT SIDE CONNECTOR
SIDE 2		SIDE 1	
+5V	A	B SPARE 1	A
	B	B SPARE 2	
GND	C	BAD16	
	D	BAD17	
BDOUTL	E		
BRPLYL	F		
BDINL	H		
BSYNCL	J	GND	
BWTBTL	K		
BIRQL	L		
BIAKIL	M	GND	
BIAKOL	N	BDMRL	
BBSYL	P	BHALTL	
BDMGIL	R	BREFL	
BDMGOL	S		
BINITL	T	GND	
BDAL0L	U		
BDAL1L	V		
+5V	A	BDCOKH	B
	B	BPOKH	
	C	GND	
	D		
BDAL2L	E		
BDAL3L	F		
BDAL4L	H		
BDAL5L	J	GND	
BDAL6L	K		
BDAL7L	L		
BDAL8L	M	GND	
BDAL9L	N	BSACKL	
BDAL10L	P	B SPARE 6	
BDAL11L	R	BEVNTL	
BDAL12L	S		
BDAL13L	T	GND	
BDAL14L	U		
BDAL15L	V	+5V	

J1	
A	SWR00
B	SWR01
C	SWR02
D	SWR03
E	SWR04
F	SWR05
H	SWR06
J	SWR07
K	SWR08
L	SWR09
M	SWR10
N	SWR11
P	SWR12
R	SWR13
S	SWR14
T	SWR15
U	
V	
W	
X	GND

5. CAPACITOR VALUES ARE MICROFARADS.
4. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W.
3. DESIGNATIONS SHOWN IN PARENTHESIS INDICATES WHERE SIGNAL ORIGINATES OR TERMINATES.
   (2/B3)
   - 2 — ZONE DESIGNATION
   - B3 — SHEET NUMBER
2. SIGNALS SHOWN IN RECTANGLES ARE I/O CONNECTIONS.
   - A A I
     - A — BOARD SIDE
     - A — PIN DESIGNATION
     - I — CONNECTOR DESIGNATION
1. FOR ASSEMBLY DRAWING SEE 701665

NOTES: UNLESS OTHERWISE SPECIFIED:

PRODUCTION RELEASE

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST			

PART/ASSY NO. & QTY PER ASSY

PART/ASSY REV LTR

701665 PM-REV11

PART NO. | NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .005 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1

STANDARD HOLE TOLERANCE PER ANSI B4.2

TOLERANCES ON .XX = ± .03 .XXX = ± .010 ANGLES = ± 0° 30'

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

DRAWN	M IAQUINTA	11-8-77
CHECK	R Trunkis	12-1-77
ENGR	C Baldwin	12-2-77
PROJ. ENGR.		12-5-77
PROD. DESIGN		12-5-77
		2-6-78
OTHER APPROVALS		

Plessey Microsystems

DWG TITLE SCHEMATIC DIAGRAM CONSOLE & BOOT ROM PM-REV 11

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701665

SCALE: ~ SHEET 1 OF 3

DISTR NO. 1990

C-2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

DAIØØ (N/C)
DAIØ1 (5/A8)
DAIØ2 (5/B8)
DAIØ3 (5/B8)
DAIØ4 (5/B8)
DAIØ5 (5/A8)
DAIØ6 (5/A8)
DAIØ7 (5/B8)
DAIØ8 (5/A8)
DAIØ9 (5/A8)
DAI10 (5/A8)
DAI11 (5/A8)
DAI12 (5/A8)

(6/B9) BDALØL — BDALØL — AV2 — DAOØØ (3/C1, 4/B1, 5/C6)
(6/B6) BDAL1L — BDAL1L — AV2 — DAOØ1 (3/C1, 4/C1, 5/C6)
(6/B6) BDAL2L — BDAL2L — BE2 — DAOØ2 (3/C1, 4/C1, 5/C6)
(6/B6) BDAL3L — BDAL3L — BF2 — DAOØ3 (3/C1, 4/C1, 5/C6)
(3/A1) LODOENL
8641 U32

(6/B6) BDAL4L — BDAL4L — BH2 — DAOØ4 (3/C1, 4/C1, 5/C6)
(6/B6) BDAL5L — BDAL5L — BJ2 — DAOØ5 (3/C1, 4/B1, 5/C6)
(6/D4) BDAL6L — BDAL6L — BK2 — DAOØ6 (3/C1, 4/B1, 5/C6)
(6/D4) BDAL7L — BDAL7L — BL2 — DAOØ7 (3/C1, 4/B1, 5/C6)
(6/C4) BDAL12L — BDAL12L — BS2
(6/C9) BDAL13L — BDAL13L — BT2
(6/C9) BDAL14L — BDAL14L — BU2
(6/C9) BDAL15L — BDAL15L — BV2
8641 U31

(6/D4) BDAL8L — BDAL8L — BM2 — DAOØ8 (3/C1, 5/C6)
(6/D4) BDAL9L — BDAL9L — BN2 — DAOØ9 (3/C1, 5/C6)
(6/D4) BDAL10L — BDAL10L — BP2 — DAO10 (3/C1, 5/D6)
(6/C4) BDAL11L — BDAL11L — BR2 — DAO11 (3/C1, 5/D6)
8641 U26

(4/A1) REFH

74S373 U28
1D 2D 3D 4D 5D 6D 7D 8D — 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q — OUT — G
AØ1 (3/D5)
AØ2 (3/D5)
AØ3 (3/D5)
AØ4 (3/D5)
AØ5 (3/C8, D5)
AØ6 (3/C8, D5)
AØ7 (3/C8, D5)

SYNCH (5/A8) — U9 — 74S04

74S373 U27
AØ8 (3/C8, D5)
AØ9 (3/B8, D8)
A10 (3/B8, D8)
A11 (3/B8, D8)
A12 (3/B8, D8)
BS7H (3/A8, 5/A8)

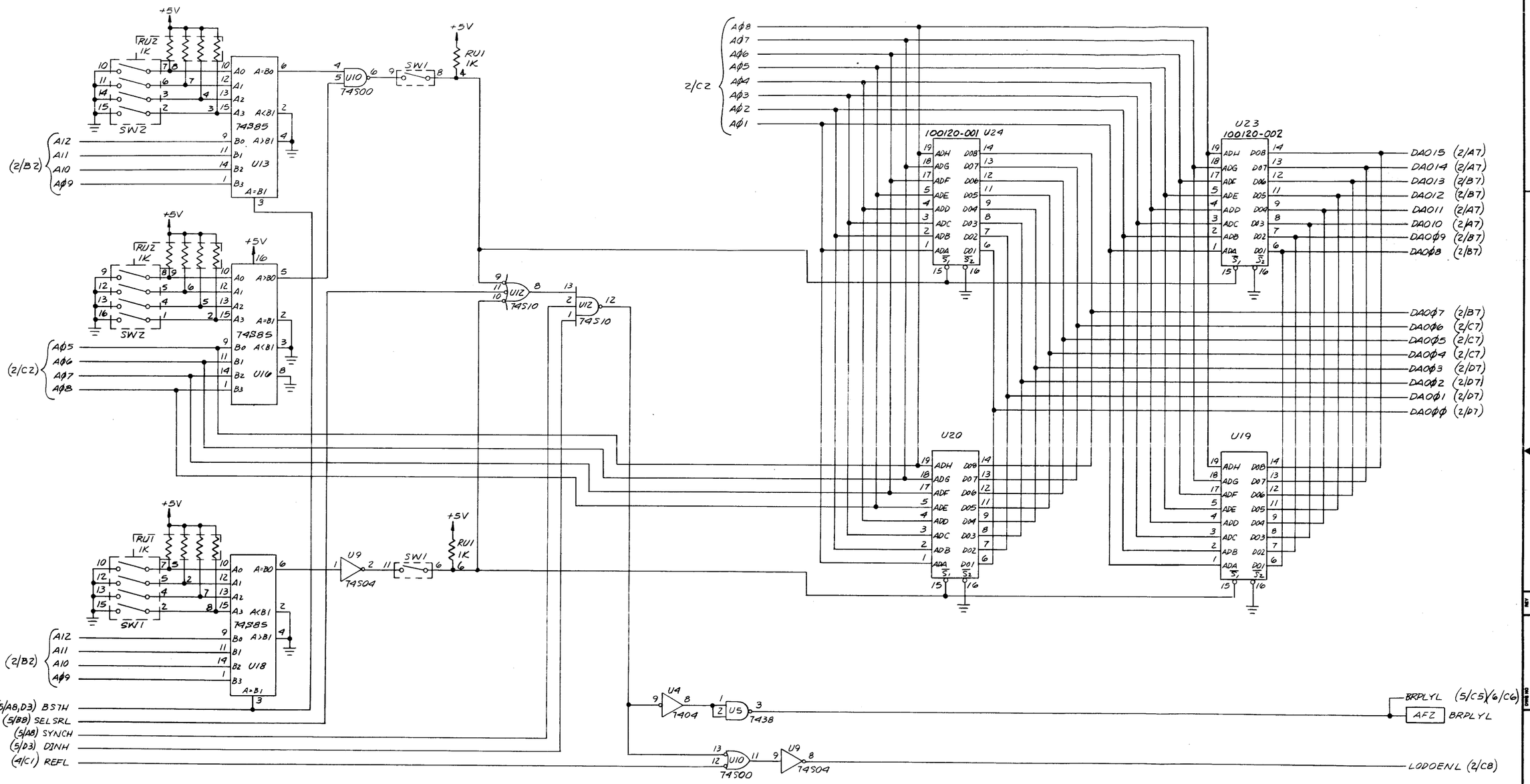
PU.
(5/D3) BSEL7H

8641 U30
DAO12 (3/C1, 5/D6)
DAO13 (3/D1, 5/D6)
DAO14 (3/D1, 5/D6)
DAO15 (3/D1, 5/D6)

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD7016665
SCALE: —	REV C	SHEET 2 OF
		DISTR NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

BOOT ROM



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701665
SCALE: —	REV C	SHEET 3 OF
		DISTR NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

DMA REFRESH LOGIC

BDMRL (6/D6) — AN1 BDMRL

ASZ BDMGOL

SACKH (4/C8) — BN1 BSACKL

SACKL (4/C8)

BREFL (6/D6) — AR1 BREFL

REFL (3/AB)

DAOϕ1, DAOϕ2, DAOϕ3 (2/D8)

DAOϕ4, DAOϕ5, DAOϕ6 (2/C8)

DAOϕϕ (2/D7)

DAOϕ7 (2/B8)

CLKI (4/C8)

REFH (2/A7)

BSYNCL (5/C5)(6/C6) — AJ2 BSYNCL

AH2 BDINL — BDINL (5/D5)(6/C6)

REFCLRL (4/C3)

(4/C1) SACKL

(5/D3) DCOKL

(5/C3) SACKINHL

DMG1H (5/C3)

REFCLRL (4/A1)

(4/C1) SACKH

(4/A1) CLKI

(5/C3) REPLYH

(5/D3) INITH

R1 10K, R2 100, R3 22K, R4 3.3K, R5 180, R6 390, R7 150, R8 470, R9 150, R11 10K, R12 4.7K

C3 .001, C4 470pf, C5 .01, C7 330pf, C8 56pf, C9 5pf

CR1 138000-001

SW1

U8 NE555

U6 7474

U7 74175

U11 7438

U3 7408

U4 7404

U10 74S00

U34 74S08

U12 74S10

U14 7474

U17 74LS393

U21 74LS244

U15 74123

+5V

PU.

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701665
SCALE: —	REV C	SHEET 1 OF
		DISTR NO.

C5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SWITCH REGISTER LOGIC

GND J1-X

+5V

RP19 4.7K

RU13 4.7K U1 74LS244

SWR15	J1-T	1A1	1Y1	DA015 (2/A4)
SWR14	J1-S	1A2	1Y2	DA014 (2/A4)
SWR13	J1-R	1A3	1Y3	DA013 (2/B4)
SWR12	J1-P	1A4	1Y4	DA012 (2/B4)
SWR11	J1-N	2A1	2Y1	DA011 (2/A7)
SWR10	J1-M	2A2	2Y2	DA010 (2/A7)
SWRØ9	J1-L	2A3	2Y3	DAØ9 (2/B7)
SWRØ8	J1-K	2A4	2Y4	DAØ8 (2/B7)

1G, 2G

RU14 4.7K R20 4.7K U2 74LS244

SWRØ7	J1-U	1A1	1Y1	DAØ7 (2/B7)
SWRØ6	J1-H	1A2	1Y2	DAØ6 (2/C7)
SWRØ5	J1-F	1A3	1Y3	DAØ5 (2/C7)
SWRØ4	J1-E	1A4	1Y4	DAØ4 (2/C7)
SWRØ3	J1-D	2A1	2Y1	DAØ3 (2/D7)
SWRØ2	J1-C	2A2	2Y2	DAØ2 (2/D7)
SWRØ1	J1-B	2A3	2Y3	DAØ1 (2/D7)
SWRØØ	J1-A	2A4	2Y4	DAØØ (2/D7)

1G, 2G

(3/A8) SELSRL

P.U. — R15 470 — U9 74S04

U25 8130 (B1–B6, Y; T1–T6, T2)

SW1

(2/D3)	DAIØ7	T1
	DAIØ4	T3
	DAIØ3	T4
	DAIØ2	T5
	DAIØ1	T6

(2/C5, 3/A8, 5/C3) SYNCH — R14 470

U22 74S09

(2/D3)	DAII2	
	DAII1	
	DAII0	
	DAIØ9	
	DAIØ8	
	DAIØ6	
(3/A8)	BS7H	
(2/D3)	DAIØ5	

(6/D6) BDCOKH — BDCOKH BA1 — DCOKL (4/C8)

(6/C6) BBS7L — BBS7L AP2 — U33 8640 — BSEL7H (2/B4)

(6/B6) BINITL — BINITL AT2 — INITH (4/A8) (5/A8)

(4/A1) BDINL — DINH (3/A8)

(4/A1) BSYNCL — SYNCH (5/A8)

(3/A1) BRPLYL — U29 8640 — REPLYH (4/B8)

BDMGIL AR2 — R16 180, R17 390 — DMGIH (4/D5)

SACKINHL (4/C3)

+5V — AA2, BA2, BV1

GND — AC2, AU1, AM1, AT1, BC2, BU1, BM1, BT1

BIAKIL AM2

BIAKOL AN2

+5V — C1 .01, C2 .01, C6 .01, C10 .01, C14 .01, C15 15, C16 15

+5V — R10 1K — P.U.

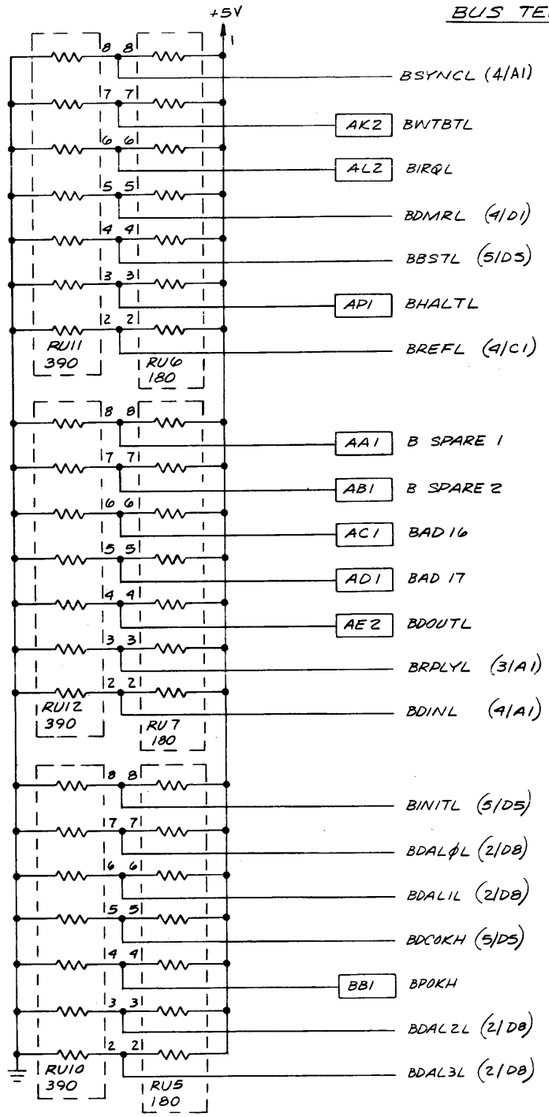
SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701665

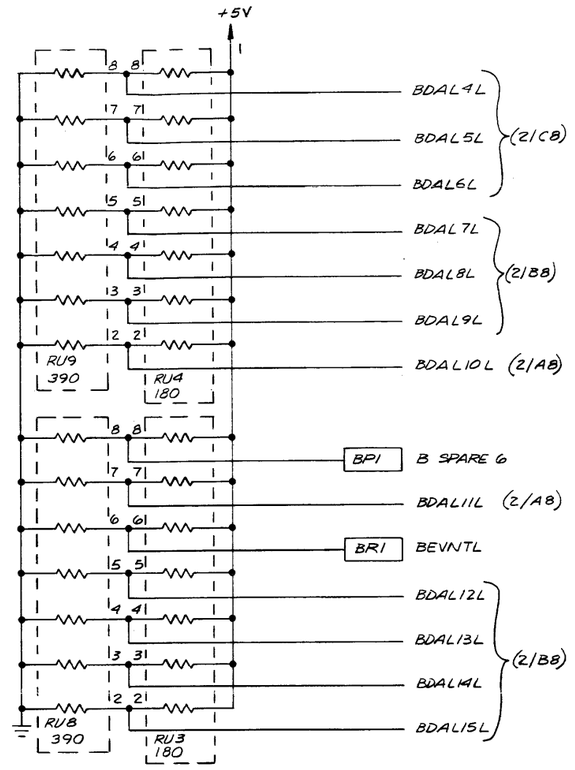
SCALE: — | REV C | SHEET 5 OF 6 | DISTR NO.

REV C — SD701665

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

BUS TERMINATION





SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701665
SCALE: —	REV C	SHEET 6 OF
		DISTR NO.

NORTH AMERICAN SALES OFFICES

CALIFORNIA:	Irvine	(714) 540-9945
	Mountain View	(415) 968-3681
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MARYLAND:	Gaithersburg	(301) 840-9455
MASSACHUSETTS:	Waltham	(617) 890-2654
MICHIGAN:	Troy	(313) 643-0420
MINNESOTA:	Minneapolis	(612) 881-0190
NEW JERSEY:	South Plainfield	(201) 757-2211
NEW MEXICO:	Albuquerque	(505) 294-5790
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WASHINGTON:	Olympia	(206) 866-2001
CANADA:	Mississauga	(416) 677-5410

EUROPEAN SALES OFFICES

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FINLAND:	Helsinki	(090) 58 51 33
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WEST GERMANY:	Munich	(089) 2362 1
	Cologne	(0221) 58 50 07
	Hamburg	(04531) 12 73 4
	Eschborn	(06196) 48777
	W. Berlin	(030) 24 72 12
ITALY:	Milan	(02) 688 2334
	Turin	(011) 61 63 33
HOLLAND:	Zeist	(03404) 21 344
NORWAY:	Oslo	(02) 15 00 90
SPAIN:	Madrid	(01) 433 24 12
SWEDEN:	Stockholm	(08) 23 55 40
SWITZERLAND:	Geneva	(022) 82 55 30
ENGLAND:	Northampton	(0604) 62175
	Tolworth (Surrey)	(01) 330-4100
	Manchester	(061) 440-8485
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SOUTH AFRICA:	Johannesburg	724-7241
INDIA:	Madras	81 07 41
PAKISTAN:	Karachi	43 73 15

(SERVICE CENTERS ARE UNDERLINED)

FORM 000081