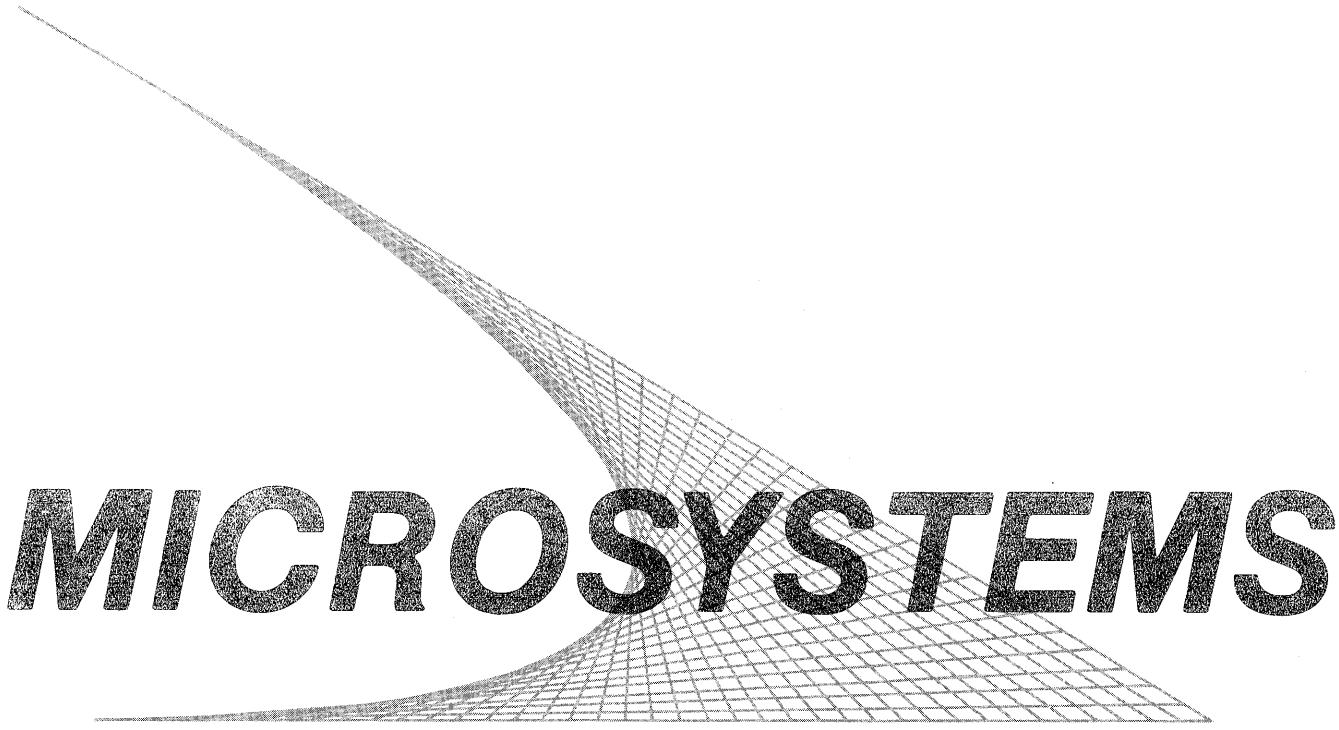
MOTOROLA

M68KVSDM/D1

VME/10
Microcomputer System
Diagnostics Manual



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M68KVSDM/D1

OCTOBER 1983

VME/10 MICROCOMPUTER SYSTEM

DIAGNOSTICS MANUAL

First Edition

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

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CHAPTER 1

DIAGNOSTICS TEST PHILOSOPHY

1.1 INTRODUCTION

This manual describes the test philosophy, system requirements and configuration, and operator procedures for the diagnostic test package to verify the overall functionality of the VME/10 Microcomputer System (VME/10).

The diagnostic test package provides a friendly, simple to use, comprehensive test programs that isolate a malfunction down to a functional block, and at least down to a faulty module.

Application of the tests described in this manual are as follows:

- Incoming inspection
- System operation verification
- Periodic confidence checks
- Fault isolation down to module or functional block (group of circuits) within a module
- Troubleshooting

In troubleshooting the system, procedural steps as described must be performed in the sequence given. Any deviation from this sequence voids the verification of the system function being tested.

1.2 FAULT CATEGORIES

a. MORTAL FAULT - Any fault that affects the basic functions of the system. This type of fault typically prevents any type of communication with the user.

b. FATAL FAULT - Any fault that prevents entering the TENbug monitor. This type of fault affects the most basic functionality of the system, and must be repaired.

c. CRITICAL FAULT - Any fault that prevents booting the operating system. This type of fault affects major functional blocks of the system, and must be repaired.

d. WARNING FAULTS - Any other fault. These faults affect the functionality of system components not critical to the operating system. However, these faults should be repaired to attain full functionality of the system. Furthermore, because the module diagnostic tests isolate only single faults, the results could be erroneous if prior faults are not repaired.

1.3 SYSTEM DIAGNOSTICS DESCRIPTION

The system diagnostic test package is comprised of two major sections.

a. Power-up/reset self-test
b. Disk Resident Module Diagnostics tests

1.3.1 Power-Up/Reset (PWRT) Self-Test

The PWRT is the first test executed in the system diagnostic test package. It is comprised of two major parts. In the first part, all the basic functions of the system are tested to be operational. All faults encountered are considered to be fatal faults. The second part of the PWRT verifies that the VME/10 can create the interrupt driven, multitasked environment that the real-time operating system requires. Faults encountered can be mortal, fatal, critical, or a warning, depending on the faulty function. This is essentially a pass/fail test with enhanced fault information. The user has no control over this test once it is started.

Refer to Chapter 2 for further information on the PWRT self-test.

1.3.2 Disk Resident Module Diagnostics (DRMD) Tests

The DRMD is a complete test package. The system must be in the TENbug monitor. Each module is tested by a single program, which is independently loaded and executed. All tests display fault information to the user via the display console. This fault information isolates a faulty block or establishes the functionality of the module under test. Faults encountered during this phase of the system diagnostic program may be either critical or warning faults, depending on the effect they have on the total system.

The System Controller Module test must be executed before attempting any other DRMD (see Chapter 3). This test verifies that the basic system under test is operational.

The remaining DRMD tests described can then be executed in any sequence. These tests are:

a. Keyboard (KBD) DRMD test (see Chapter 4)
b. Winchester Disk Controller (WDC) DRMD test (see Chapter 5)
c. MVME400 Dual Serial Port DRMD test (see Chapter 6)
d. MVME410 Dual Parallel Port DRMD test (see Chapter 7)

All the disk resident module diagnostics tests:

- are completely self-contained and independent of each other.
- are designed to extensively test one module or one functional block.
- are designed to isolate faults down to the module, or functional block level.
- provide a friendly interface by using standard input/output procedures.
- display fault information via the display console.
- make use of split screens to preserve diagnostic information.

1.3.2.1 User Commands. Throughout the DRMD tests, the following pushbuttons/keyboard keys initiate their described functions:

RESET - Reset the system and enter TENbug monitor.

ABORT - S/W abort, stop current task, display the registers of the MC68010 and enter control phase.

BREAK - Function varies with the diagnostic mode.

CTRL W - Pause on current task, resume when any key on the keyboard is depressed.

The following one character commands (either uppercase or lowercase) must be terminated by a carriage return:

H (Help) - Display a message that will expand on the use, or function of the presented option. Additional help pages may be called by entering an X when applicable.

Y (Yes) - Turn the option on.

N (No) - Turn the option off.

B (Bug) - Enter the TENbug monitor.

O (O/S) - Boot the operating system.

P (Print) - The information printed varies with the diagnostic mode. This option requires that a dual parallel port I/O module (MVME410) addressed at $F1C1E1 be installed in the system's I/O Channel card cage, and that a printer be connected to port 1 of the module.

R (Restart) - This function varies with the diagnostic mode.

Additional options that may be presented are explained when applicable.

1.3.2.2 Starting DRMD Tests. Each DRMD is loaded and executed by entering the BO command, followed by the device number, controller number, and the name of the selected test. The name of the test must include the VERSAdos user number and catalog name, unless the file resides in user number 0 with a null catalog name. Throughout this manual, the DRMD's are assumed to reside in user number 0 and under a null catalog.

1.3.2.3 Aborting DRMD Tests. During execution of a DRMD, the test can be aborted by depressing the BREAK key or by pressing the ABORT pushbutton. The action taken depends on the phase of the DRMD, which is described in paragraphs 1.4 through 1.6.

Refer to Chapters 3 through 7 for further information on DRMD tests.

1.4 DISK RESIDENT TEST PHASES

After booting in the requested diagnostic program, all DRMD's will present a consistent interface.

The top line of the CRT states the full name of the module that is being tested, and the revision date of the DRMD.

Line 25 of the screen displays a status line as described in paragraph 1.7.

To simplify the following discussion, the DRMD's are divided into three distinct operation phases:

- mode selection phase - paragraph 1.4.1
- test execution phase - paragraph 1.4.2
- control phase - paragraph 1.4.3

1.4.1 Mode Selection Phase

The mode selection phase is entered immediately after a DRMD has been downloaded into memory. The user is presented with a list of possible inputs, and then is requested to select the operation mode for the DRMD. The screen displays:

Mode Selection Phase

Input options:

H - Help
Y - Turn the option on
N - Turn the option off
R - Restart mode selection phase
B - Enter TENbug
O - Boot operating system

The user is requested to select the required option for the following three modes:

- Continuous execution of the test, or a single pass of the DRMD.

  Continuous testing ?

  Y = continuous
  N = single pass

- Stop execution upon encountering a failure, or continue execution.

  Stop on first fault ?

  Y = stop on fault and enter control phase
  N = continue on fault

- Execute an interactive or a non-interactive test. An interactive test is defined as one that requires any type of operator inputs, such as visually verifying the state of a LED, pressing a pushbutton, selecting tests, installing user-prepared test fixtures such as the loop back cable, etc.

```
Interactive testing ?

Y = interactive test requested
N = non-interactive test requested
```

The user may be requested to select additional modes for specific DRMD's. The additional modes are described when applicable, both in this manual and through a help message that is provided at mode selection phase.

If a BREAK is detected at any time during mode selection phase, the TENbug monitor is re-entered (same as the BO command).

After the user selects the operation modes, the screen is cleared, the selected modes are displayed on the status line, and the test execution phase is entered.

NOTE

When diagnosing the system for an unknown fault, it is recommended that the user first run each of the DRMD's under the following modes: single pass, stop on fault, and interactive (when applicable). Depending on the nature of the fault, the user may then choose to execute the continuous mode, or enter the DRMD diagnostic loop as described in paragraph 1.5.

1.4.2 Test Execution Phase

Test execution phase is entered when mode selection phase is completed.

All subtests of a DRMD display a subtest title and, on the same line, the status of the subtest as follows:

- In progress - when the test is being executed.
- Passed - if the test was completed successfully.
- FAILED - if a fault was encountered. All failing subtests display the code Ln (refer to paragraph 1.5) to be used when invoking the DRMD Diagnostic Loop, and the loop the subtest failed on if the user has opted for a continuous test. Additional fault information for specific tests may be displayed and is described in Chapters 3 through 7. It should be noted that once a fault is encountered, the subtest displays the fault information, aborts execution, and proceeds to the next subtest.
- Bypassed - if a test was bypassed by entering a carriage return.

The previously described information is presented to the user if the single pass mode was selected. However, in the continuous mode of operation, all passing tests titles are over-written, leaving only a record of failing tests.

The control inputs available to the user during test execution phase are the BREAK, carriage return, and CTRL W.

When a BREAK is detected, test execution immediately halts and control is transferred to the control phase. Some subtests, however, cannot be stopped; therefore, all control inputs, including BREAK, are ignored.

Entering a carriage return causes a test to be bypassed.

Depressing the CRTL and the W keys simultaneously halts the currently executed test. Execution resumes after any key is depressed.

During test time, the user may be requested to enter additional inputs if the interactive testing mode was selected. These inputs are described in Chapters 3 through 7.

In any case, test execution phase is halted and control phase entered after 50 faults have been encountered.

1.4.3 Control Phase

The control phase is entered when the user has:

- Selected a single pass of the DRMD, and test execution phase is completed.
- Selected the stop on fault option, and a fault is encountered during test execution phase.
- Selected the continue on fault mode, and 50 faults are recorded during test execution phase.
- Entered a BREAK during test execution phase of the DRMD, and also while executing a subtest that allows control inputs.
- Pressed the ABORT pushbutton.

When the control phase is entered, the DRMD's display:

. A message giving the status of the DRMD in field 1 of the status line.

. A menu of available control inputs and a prompt:

Control Phase active
H/R/M/B/O/P/Ln >

where:

H - Displays a help message.

R - Restarts test execution phase, under the same modes selected at the previous mode selection phase. The DRMD starts execution at the first functional test of the DRMD.

M - Re-enters mode selection phase and re-initiates the DRMD.

B - Enters TENbug monitor.

O - Boots the operating system.

P - Prints the contents of the screen to the line printer.

Ln - Invokes the DRMD diagnostic loop as described in paragraph 1.5.

While in the control phase, BREAK has no effect, and program control remains at the control phase.

1.5 DRMD DIAGNOSTIC LOOP

The diagnostic loop permits the user to loop continually on a specific failing test, thus allowing a more detailed analysis of the fault. It should be noted that when in the diagnostic loop, the selected sub-test executes continually. To clarify this point, consider a memory test. If a fault is detected during the test execution phase, the executive displays the fault information and then proceeds to the next test. However, while in the diagnostic loop and after displaying the fault information for the failing address, the test proceeds to examine the next memory address. This provides a more comprehensive diagnosis of memory. Because memory is continually accessed, other means, such as scoping, may be used to troubleshoot the malfunction.

When a sub-test fails, it is assigned an L code which is displayed with the "FAILED" message. The format for the L code is the letter L followed by a digit (e.g., L2).

The diagnostic loop is invoked from the control phase by entering the L code for the required sub-test. After the diagnostic loop is activated, the screen splits to provide space for loop results, while preserving the results of the just-completed test execution phase for later use or reference.

The window assigned for the diagnostic loop is at the right of the screen, and displays a title line stating the test that is being executed, the status of the loop (either "active" or "stopped"), and a diagnostic loop counter. While in the loop, the only information displayed will be fault messages, stating the fault number, the loop the fault was detected in, and any additional fault messages specific to the test.

The control characters available to the user while in the loop are BREAK and CTRL W. CTRL W has the same function as in test execution phase, and causes the loop to pause, allowing, for example, examination of the fault information. The loop resumes execution after any key is depressed. Entering a BREAK is the only way to terminate the diagnostic loop. At this time, the loop status is changed to STOPPED, and a loop command monitor is entered.

In addition to the standard commands, the loop command monitor provides the following three commands:

C - Return to control phase. The same function is performed when the BREAK key is depressed.

F - Display the last 50 faults detected by the loop. At least 50 faults are saved by the loop executive, and are scrolled in the loop's screen window. The scrolling function is slowed down to allow easier examination of the information. However, the CTRL W input is still accepted, and the user can pause the process.

F;P - Same as F, with the information being echoed to the line printer. This input requires the same hardware as the P command described in paragraph 1.3.2.1.

1.6 DRMD STATUS LINE

Line 25 of the CRT displays the status of the diagnostic program. During the execution of the DRMD's, the status line is divided into four fields.

Field 1 displays the following status:

. passed - when entering the control phase, and if no faults are encountered during test execution phase.

. failed - when entering the control phase, and if a fault is detected during test execution phase.

. stopped - when entering the control phase by depressing the BREAK key during test execution phase.

. aborted - when entering the control phase by pressing the software ABORT pushbutton.

. restart - when entering test execution phase by selecting the R command in the control phase.

Field 2 displays ' Single pass ', if so selected, or the loop counter if the continuous mode was selected -- 'Loops completed 0000'. The loop counter is updated to reflect the number of test execution loops that were completed. The loop counter rolls over back to 0 after 9999 loops were completed.

Field 3 displays the message ' Stop on fault ', or a fault counter if the continue on fault option was selected -- 'Faults detected 00'. The fault counter is incremented during test execution phase with each detected fault.

Field 4 is used by some of the subtests to display additional information. For example, this may be a countdown clock for time limited tests, or a disk track counter for media tests. The use of this field is described when applicable.

Figure 1-1 is a block diagram of the DRMD phases.

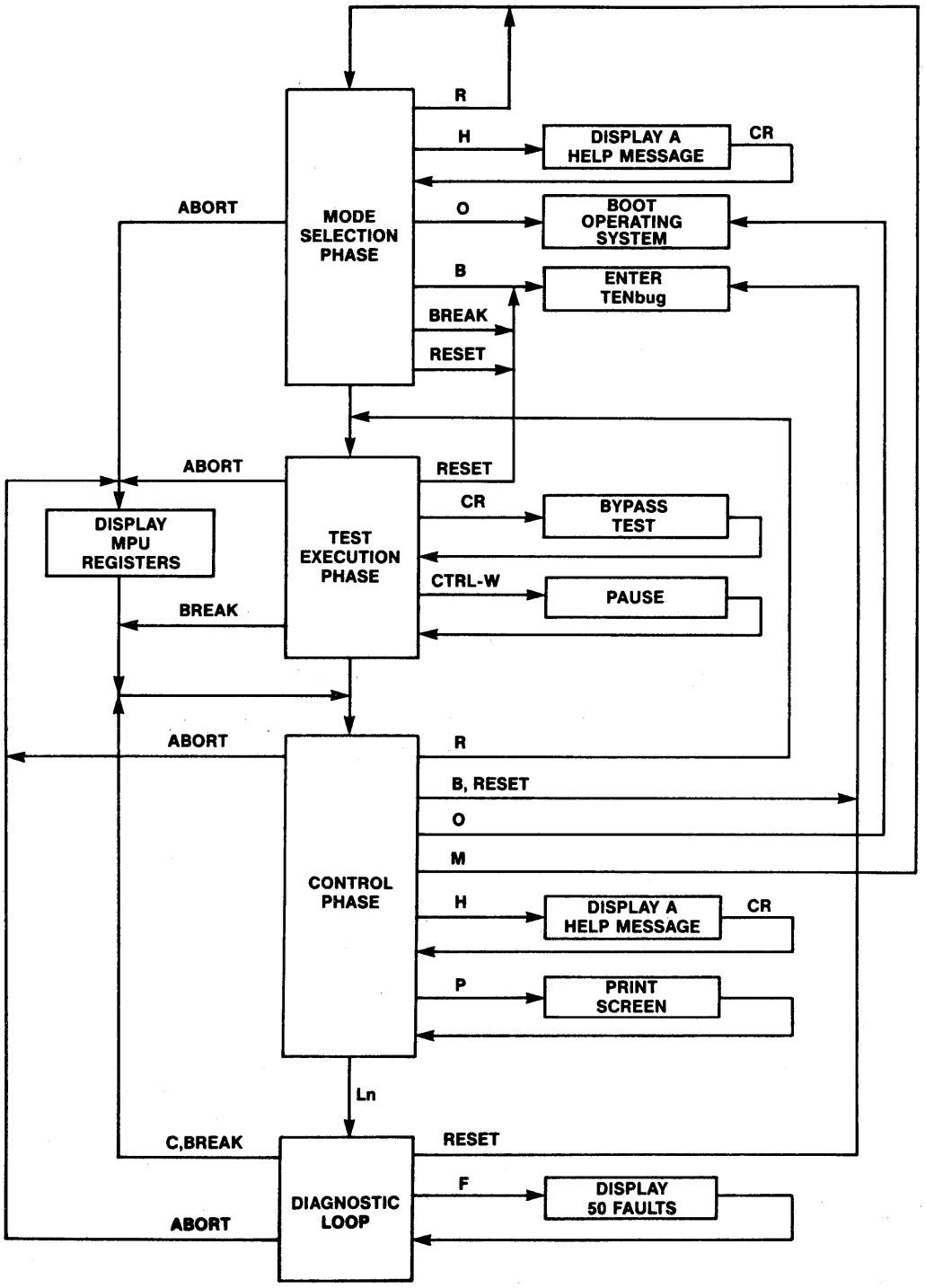


FIGURE 1-1. DRMD Phases Block Diagram

CHAPTER 2

POWER-UP/RESET SELF-TEST

2.1 INTRODUCTION

The power-up/reset (PWRT) self-test verifies the functionality of the system resources necessary to initiate the factory-supplied operating system. The PWRT execution time varies from five seconds to one minute, and depends on the disk spin-up time. In any case, the PWRT is completed in less than five seconds from the time the system is ready to be used.

The PWRT self-test provides two levels of testing. In the first level, a batch type test is performed on the basic functions of the system. In this type of test, each function is tested in a controlled fashion, after the previous test has completed its execution. The tests executed are described in paragraph 2.5.

The second level simulates the multitasking, asynchronous processing environment that the VME/10 creates for its operating system. A functional description of this part is provided in paragraph 2.6.

2.2 SYSTEM CONFIGURATION

Refer to paragraph 8.1 for the required initial factory configuration of the system.

2.3 START/RESTART/ABORT INFORMATION

The PWRT self-test is executed when the system is powered up or when a reset is initiated by pressing the RESET and the ABORT pushbuttons simultaneously, then first releasing the ABORT pushbutton, and then the RESET. The PWRT self-test cannot be aborted.

2.4 TEST RESULTS

At the start of the PWRT self-test, the screen displays a message stating that the PWRT self-test is in progress, followed by a message stating that the disk is spinning up to its required operational speed. Because it may take up to one minute for the disk to attain this speed, the brightness of the delay message changes periodically to assure the user that the test is still running. When the system is configured with a color monitor, the color of the message changes.

If the PWRT self-test passes, a message to that effect is displayed, and control is transferred to the TENbug monitor.

If a failure is encountered during this phase, fault information is presented to the CRT, and then the system enters an infinite loop. Fault information is as explicit and informative as possible. As a minimum, it states the failing test and the message 'FAILED'.

The user can enter the TENbug monitor by pressing the RESET pushbutton. However, it should be noted that it may not be possible to display any information on the CRT if the fault is a mortal one, or that the TENbug monitor may not be entered if a fatal fault is encountered.

2.5 BATCH LEVEL TESTS

There are seven batch level tests.

- Temporary stack
- CRT controller (CRTC)
- Low RAM
- Display RAM
- Character and attribute generator RAM
- MPU
- Firmware

The following paragraphs describe these batch level tests.

2.5.1 Temporary Stack

The first test attempts to establish a temporary stack area in the static display RAM. The test is an in-line test, using only one of the MPU's registers so as to minimize the system base required to execute the test. Any fault is mortal.

2.5.2 CRT Controller (CRTC)

The CRT controller is initialized to control an 80-character, 25-line screen. The cursor is positioned at the top left corner of the screen. The CRTC's cursor registers are then read to verify the accessibility and accuracy of the write and the read path to the CRTC. Any fault detected in the CRTC logic is mortal.

2.5.3 Low RAM

Memory from $0-$1000 is tested next, so as to be able to establish basic system vectors because they are used in normal screen access routines. The memory is tested for address bus validity and for random data acceptance using multi-register transfers.

2.5.4 Display RAM

The display RAM is sized and then tested, using the same memory tests used in the low memory test. At the end of the test it is initialized to display null spaces on the CRT. Faults detected are either mortal or fatal.

The following is an example of fault information:

```
RAM FAILED
Failing address  :  00F17010
Required data    :  00412345
Received data    :  00C12345
```

2.5.5 Character and Attribute Generator RAM

The character and the attribute generator RAM are tested for random data acceptance, and then initialized with the ASCII character set and with the attribute table. Faults detected are either mortal or fatal.

The following is an example of fault information:

```
Character RAM FAILED  or  Attribute RAM FAILED
Failing address  :  00F14023
Required data    :  41099876
Received data    :  C1099876
```

Note that the fault message states the failing data as if it were four contiguous bytes. In reality, the generator memory is located in the VME/10 I/O memory map, in which only odd bytes are valid.

2.5.6 MPU

The following MC68010 functions are tested:

- All data and address registers
- Bit manipulation instructions
- Condition code register
- Arithmetic instructions
- Addressing modes

An MPU fault is either mortal or fatal.

Fault information:

```
MPU FAILED
```

2.5.7 Firmware

The firmware-based TENbug routines are verified to be valid by calculating the PROM's checksum bytes and comparing them to the one stored in the PROM's. Faults detected are of the fatal type.

Fault information:

```
TENbug checksum test FAILED
```

2.6 MULTITASKED TESTS

The PWRT self-test simulates the multitasked, asynchronous environment that the VME/10 provides for the operating system. This is achieved by taking advantage of the priority interrupt structure as defined in Chapter 4 of the VMEbus Specification Manual, MVMEBS. The functional blocks which are tested in this mode are the system RAM, the Enhanced Peripheral Controller Interface (EPCI), the Time-of-Day Clock (TDC), and the disk. An indirect test of the systems interrupt handler is also performed. Refer to the Power-Up/Reset Self-Test Flow Chart, Figure 2-1, for detailed information on the multitasked test environment.

2.6.1 Time-of-Day Clock (TDC)

The TDC's battery backed-RAM and its registers are tested, and then the TDC counters are enabled, and control is transferred to the EPCI test. Increment of the TDC's count is verified from within the EPCI's service routine. If the TDC's counters are functional, the periodic interrupts are enabled. All periods are checked with an interrupt-driven test, which is active concurrently with the EPCI interrupts.

All TDC faults are considered to be warning faults because, even though affecting the full functionality of the operating system, they will not prevent it from executing in some modes.

Fault information states the function that failed and any additional fault messages, if applicable.

2.6.2 Enhanced Peripheral Controller Interface (EPCI)

The data property of the EPCI which interfaces the keyboard to the main chassis is tested using the internal data loop-back feature of the EPCI. At the beginning, the test verifies that the EPCI is accessible and that it is capable of transmitting and receiving data. When this is verified, the EPCI's interrupts are enabled, and control is transferred to the system RAM test.

All 256 possible bytes are tested in an interrupt-driven test which executes concurrently with the TDC's and the disk's interrupt-driven tests.

At the end of the test, the EPCI is initialized to interface with the system's keyboard. EPCI faults are of the fatal type.

Fault information states the failing function and any additional fault message, if applicable.

2.6.3 System RAM

The system memory from $1000 through $5FFFE is tested for address validity, random data acceptance, and fast accesses, using multiple register operations. Faults at this stage of the PWRT are considered to be critical.

Fault information states the failing address, the required data, and the received data (see paragraph 2.5.4).

The RAM test is interrupted by all the three interrupt-driven tests. However, when the three interrupt-driven tests are completed, the RAM test aborts and the PWRT self-test is terminated.

2.6.4 Winchester Disk Controller (WDC)

The TDC periodic interrupt checks the state of the WDC every half-second for completion of its internal self-test. The TDC serves as the main disk test watchdog, and allows about a minute and a half for the WDC's self-test to complete. The TDC is activated as the disk watchdog only after the TDC has successfully completed its interrupt-driven test; if it did not, the PWRT executive waits for the EPCI to complete its interrupt driven test, and then activates it as the alternate disk watchdog. After the WDC's self-test is verified, the host port of the FIFO is tested.

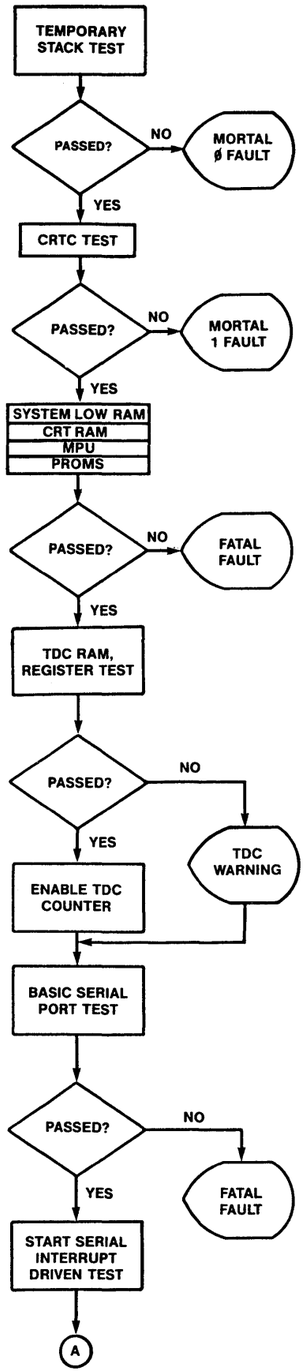
The PWRT tests the first disk it finds to be present and ready, as reflected in the disk status bytes in the sense block of the WDC. The order in which the disks are searched for is: Winchester drives #0, #1; then floppy drives #2, #3.

After a drive has been identified, the WDC's command interrupts are enabled, a command to scan track 0 is sent to the drive, and control is restored to whichever task had it at that time. The service routine for a command interrupt verifies a successful completion of the scan command, enables data interrupts, sends a read sector 0 command, and returns from exception. The service routine for the data interrupt reads sector 0, and verifies that the diagnostic pattern stored in sector 0 is correct. A requirement for this test is that the media has been initialized using the VERSAdos standard INIT utility.

NOTE

The Winchester disk has been factory-initialized.

WDC faults are considered to be critical faults. Fault information states the function that failed and any additional fault message, if applicable.



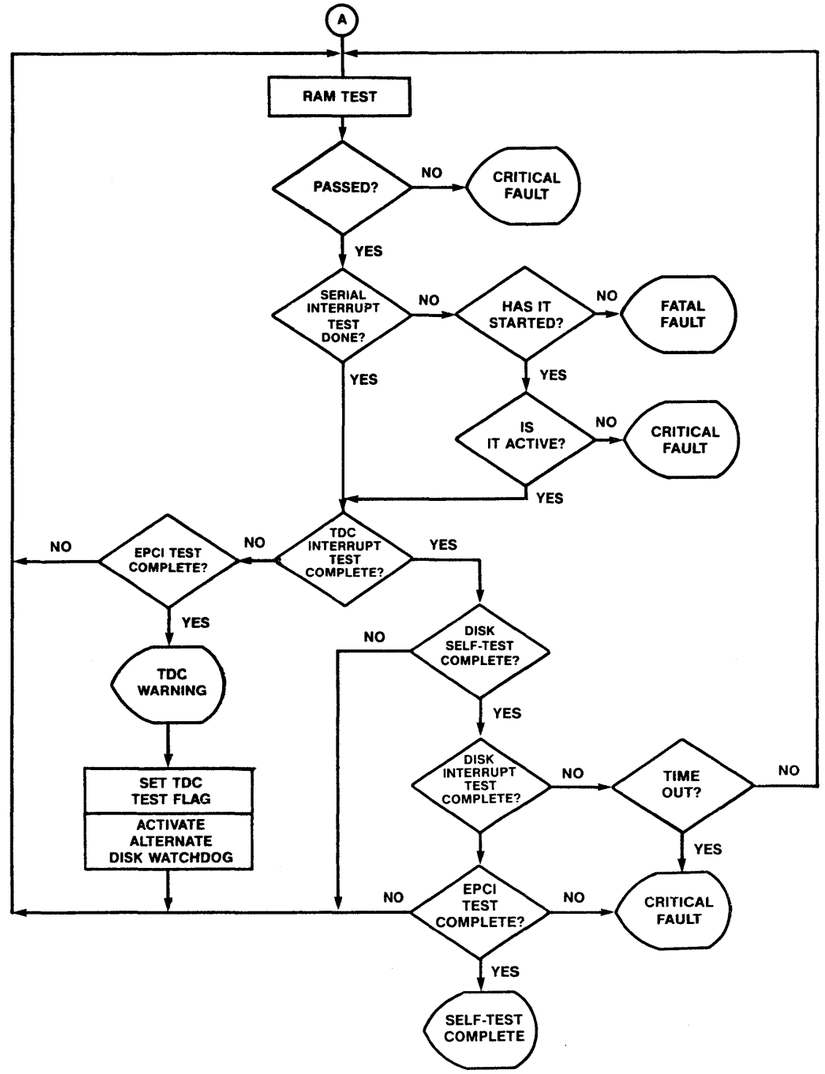
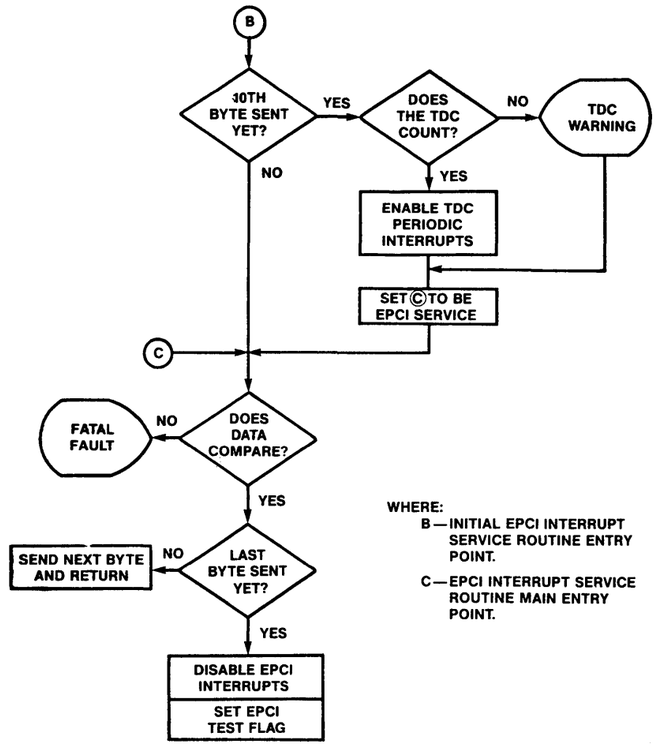


FIGURE 2-1. Power-Up/Reset Self-Test Flow Chart (Sheet 1 of 2)

EPCI SERVICE ROUTINE

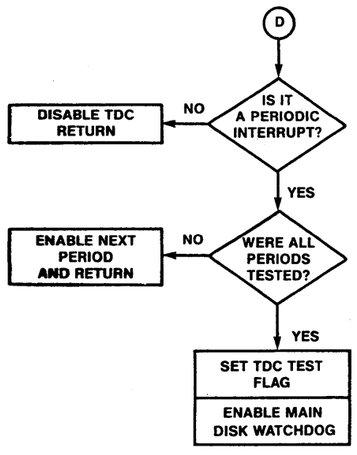


WHERE:

B—INITIAL EPCI INTERRUPT SERVICE ROUTINE ENTRY POINT.

C—EPCI INTERRUPT SERVICE ROUTINE MAIN ENTRY POINT.

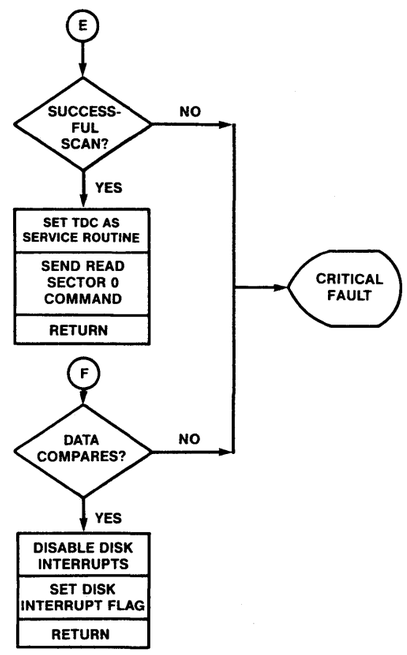
TDC PERIODIC INTERRUPT SERVICE ROUTINE



WHERE:

D—TCD INTERRUPT SERVICE ROUTINE ENTRY POINT.

DISK INTERRUPT SERVICE ROUTINE

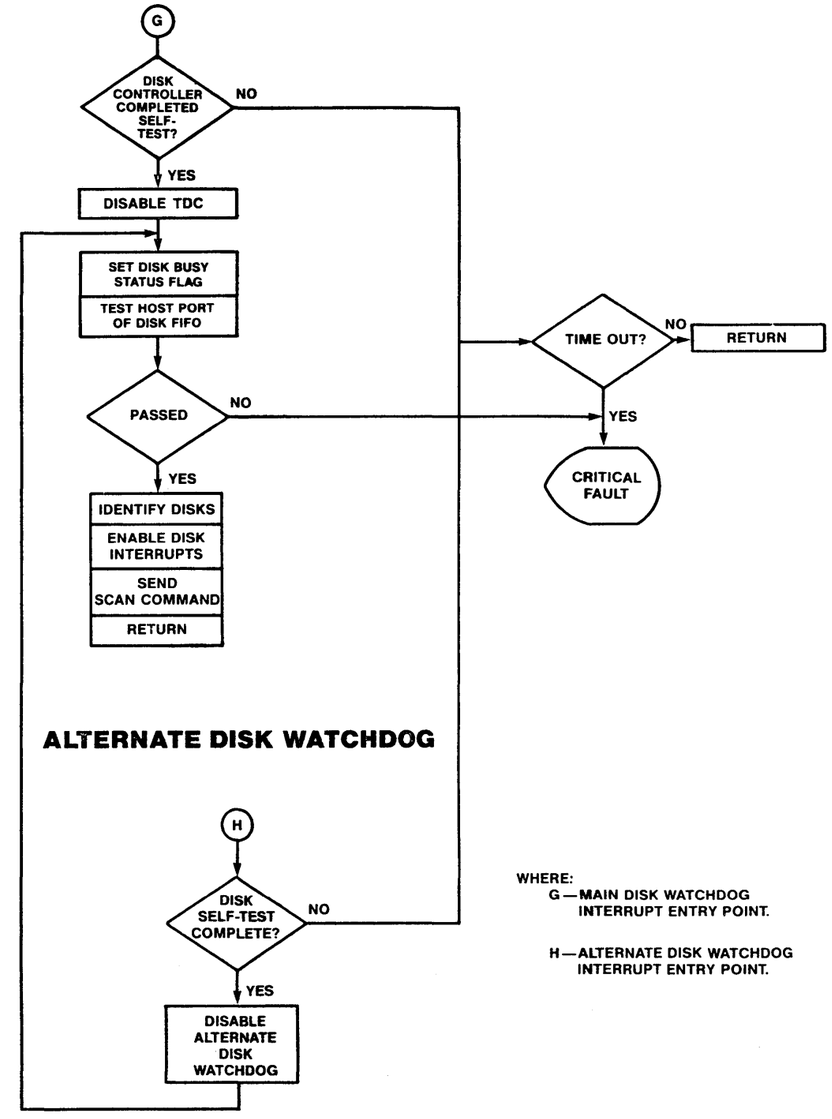


WHERE:

E—DISK COMMAND INTERRUPT SERVICE ROUTINE ENTRY POINT.

F—DISK DATA INTERRUPT SERVICE ROUTINE ENTRY POINT.

MAIN DISK WATCHDOG



ALTERNATE DISK WATCHDOG

WHERE:

G—MAIN DISK WATCHDOG INTERRUPT ENTRY POINT.

H—ALTERNATE DISK WATCHDOG INTERRUPT ENTRY POINT.

FIGURE 2-1. Power-Up/Reset Self-Test Flow Chart (Sheet 2 of 2)

CHAPTER 3

SYSTEM CONTROLLER MODULE DISK RESIDENT MODULE DIAGNOSTIC TEST

3.1 INTRODUCTION

This chapter describes the System Controller Module (SCM) DRMD test, which either establishes that the SCM is fully functional or isolates the faulty function. Any fault encountered during this test is considered to be critical.

3.2 SYSTEM CONFIGURATION

Verify system configuration per paragraph 8.1. The system must be in the TENbug monitor.

3.3 START/RESTART/ABORT INFORMATION

The SCM DRMD test is initiated by entering the following command:

TENbug x.y > BO 0,0,SCM (CR)

3.4 TEST RESULTS

A successful completion of the SCM DRMD test is indicated on the display terminal by displaying the "passed" status in field 1 of the status line, and then entering the control phase. At that time, the user is presented with all the command options described in paragraph 1.4.3.

The results of all executed tests as described in paragraph 3.5 are displayed on the screen.

3.5 FUNCTIONAL DESCRIPTION

The SCM DRMD test verifies that the SCM is functional.

If the continuous mode of operation is selected, execution defaults to the non-interactive tests. Following is a detailed description of the subtests performed.

3.5.1 MPU

The following MC68010 functions are tested:

- All data and address registers
- Bit manipulation instructions
- Condition code register
- Arithmetic instructions
- Addressing modes
- Except processing

User inputs : none

Execution modes: all

3.5.2 TENbug Checksum Test

The TENbug checksum test verifies that the PROM resident code has not been altered.

Fault information is minimal and states only the fact that the test has failed.

User inputs : none

Execution modes: all

3.5.3 Memory Test

The memory test verifies that the on-board memory is functional by executing three different test routines as follows:

- Address bus test - checks the address bus path to memory.
- Memory pattern test - writes to memory and then verifies the patterns FF00, 00FF, 55AA, AA55, 33CC, and CC33.
- Fast random test - uses multiple register transfers to write, and then verifies to memory 32 random bytes at a time.

The above-described tests are performed on memory starting at the end of the SCM DRMD program area, and ending at the top of the on-board memory. The on-board memory is sized to determine if it is 384K or 1.5M bytes deep.

During test time, the status message for the memory test is changed to assure the user that the test is still active.

Fault information states the failing address, the required data, and the received data.

User inputs : none

Execution modes: all

3.5.4 Pixel Access Test

This test verifies that the graphics RAM is accessible both in the pixel access mode and in the byte access mode.

In the interactive mode, the graphics are enabled to be displayed on the screen. Only a block will be written to, so as not to obscure the test execution phase display.

In the non-interactive mode, the graphic banks in control register 1 of the SCM are turned off, and all of the graphic RAM is tested.

Fault information is similar to the one in the memory test.

User inputs : none

Execution modes : as described above

3.5.5 VMEbus Interface

The following VMEbus interface functions are tested:

- All 7 levels of VMEbus interrupts, their associated control bits and vector register in the SCM control registers.
- VMEbus interrupt acknowledge (VBIA*) interrupt function and its associated bits in the SCM control and status registers.
- BFAIL* interrupt and SYSF status.
- Bus arbitration as controlled through SCM control registers.

Fault information states the failing function and, if applicable, additional fault information.

User inputs : none

Execution modes : all

3.5.6 Enhanced Peripheral Controller Interface (EPCI)

The EPCI is set to its internal data loop back mode and tested for data transmission and receiving, and interrupt generation for all 256 possible bytes.

All control characters as described in paragraph 1.4.3 are ignored because the keyboard is disabled during this test. The EPCI and the keyboard are initialized at the end of the test.

Fault information states the failing function, the required byte, and the received byte.

User inputs : none

Execution modes : all

3.5.7 Time-of-Day Clock (TDC)

The following TDC functions are tested:

- Data acceptance of the battery backed-up RAM and write registers.
- All time slices of the periodic interrupt.
- Time update and its interrupt.
- Alarm interrupt.
- Validity of the battery back-up/power since last read of the VRT bit.

Fault information will state any information relevant to the faulty function.

User inputs : none

Execution modes : all

3.5.8 Graphic Cursor

The graphic cursor is moved around a block on the screen, and the user is prompted for a test result.

Field 4 of the status line is utilized as an elapsed time counter, displaying a countdown test timer starting at one minute. Failure to respond to the test prompt within this time is considered a test fault.

Fault information is minimal.

User inputs : Y (yes), if the cursor is moving.
N (no), to indicate that it is not.

Execution modes : Single pass, interactive test mode only.

3.5.9 ABORT Pushbutton

The user is prompted to press the ABORT pushbutton to verify the software abort circuitry.

Field 4 of the status line is used as a countdown clock, allowing the user 15 seconds to activate the abort. Failure to process an abort sequence, either because of a malfunction or because of an operator error, is processed as a test failure.

Fault information is minimal.

User inputs : press software ABORT pushbutton.

Execution modes : single pass, interactive test mode only.

3.5.10 RESET Pushbutton

The reset circuitry is tested by prompting the user to press the RESET pushbutton.

Field 4 of the status line is utilized in the same manner as in the ABORT pushbutton test.

Fault information is minimal.

User inputs : press the RESET pushbutton.

Execution modes : single pass, interactive test mode only.

CHAPTER 4

KEYBOARD DISK RESIDENT MODULE DIAGNOSTICS TEST

4.1 INTRODUCTION

This chapter describes the keyboard (KBD) DRMD test, which allows the user to interactively check out the keyboard. This test has only one mode of operation; therefore, mode selection phase is not entered.

4.2 SYSTEM CONFIGURATION

Verify system configuration per paragraph 8.1. The system must be in the TENbug monitor.

4.3 START/RESTART/ABORT INFORMATION

The KBD DRMD test is initiated by entering the following command:

TENbug x.y > BO 0,0,KBD (CR)

4.4 TEST RESULTS

A successful completion of the KBD DRMD test is indicated on the display terminal by displaying the "passed" status in field 1 of the status line, and then entering the control phase. At that time, the user is presented with all the command options described in paragraph 1.4.3.

4.5 FUNCTIONAL DESCRIPTION

The KBD DRMD test enables the user to perform a manual check of all keyboard keys. The screen displays a graphic representation of the keyboard and a message explaining the test procedure. The user then depresses any of the keyboard keys and verifies that the corresponding graphic key was illuminated in the graphic display. The keyboard is reset, and then its initialized procedure verified prior to starting the test. The fault messages are related only to initialization errors. The user should verify proper operation of the keys. The test can be stopped by depressing the CTRL and the ALT keys simultaneously.

User inputs : N/A

Execution modes: N/A

CHAPTER 5

WINCHESTER DISK CONTROLLER
DISK RESIDENT MODULE DIAGNOSTICS TEST

5.1 INTRODUCTION

This chapter describes the Winchester Disk Controller (WDC) DRMD test, which either establishes that the WDC is fully functional or isolates the faulty function. Any fault encountered is considered to be critical.

5.2 SYSTEM CONFIGURATION

Verify system configuration per paragraph 8.1. The system must be in the TENbug monitor.

5.3 START/RESTART/ABORT INFORMATION

The WDC DRMD test is initiated by entering the following command:

TENbug x.y > BO 0,0,WDC (CR)

5.4 TEST RESULTS

A successful completion of the WDC DRMD test is indicated on the display terminal by displaying the "passed" status in field 1 of the status line and then entering the control phase. At that time, the user is presented with all the command options as described in paragraph 1.4.3.

The results of all executed tests, as described in paragraph 5.5, are displayed on the screen.

Field 4 of the status line is used as a sector counter, and displays the currently accessed sector. This field is cleared when entering the control phase, unless a sector-oriented test has either failed or was bypassed. In this case, field 4 reflects the last accessed sector of the disk.

Whenever a command error is detected, fault information includes a list of the sense bytes as read from the WDC sense block and the command packet that was sent to the disk. Refer to the Winchester Disk Controller User's Manual (M68KWIN1) if further interpretation of this data is required. Throughout this chapter, this type of fault information is referred to as control fault data.

5.5 FUNCTIONAL DESRIPTION

The WDC DRMD test verifies that the WDC is fully functional. The non-interactive test performs only control and read tests of the disk, while the interactive test also writes to the media.

Some safety measures were taken to prevent accidental writes to the media:

- The media must have been initialized by the VERSAdos standard INIT utility as described in the M68000 Family VERSAdos System Facilities Reference Manual, M68KVSF; otherwise, the test will abort.

NOTE

As supplied, the Winchester disk has been factory-initialized and contains the operating system software; it should not be re-initialized as all software will be lost.

- The media must have been initialized with diagnostic tracks. In case they are not found, the test will abort if the media under test is a Winchester. If the media is a floppy disk, the user is provided with the option to initialize it with diagnostic tracks. If the user answers "no" to this option, the test will abort.

WARNING

INITIALIZING THE DIAGNOSTIC TRACKS ON A FLOPPY DISK
WILL SCRATCH THE DISK, INVALIDATING ALL DATA ON IT.

The WDC DRMD test includes a retry algorithm that is applied whenever error codes 12 or 13 are detected. Refer to the Winchester Disk Controller User's Manual (M68KWIN1). Each soft error increments the soft error counter for the accessed device. After five retries, the error is considered to be a hard failure. The current soft error counters for the tested drives are displayed at the conclusion of each loop if any soft errors were detected. The VERSAdos lockout table is monitored prior to accessing the drives so that known bad sectors do not affect the results of the test.

5.5.1 Drive Selection

An additional selection option is presented to the user at mode selection phase. This option allows the user to test the various disk drives that are connected to the WDC.

After the user has selected the options for the three standard modes, the screen displays:

```
Test drive 0-3/A   ?
```

To test a single drive, enter its device number. The disk drives are numbered such that the Winchester drives are devices number 0 and 1, and the floppy disk drives are devices number 2 and 3. As shipped from the factory, the system includes Winchester driver device number 0, and floppy drive device number 2. To test all the drives that are connected to the WDC, enter an "A" when presented with the above mode option. Note that only the drive status is displayed if the drive is either not present or not ready.

The H command presents a help message that explains the presented options.

5.5.2 Reset Self-Test

A reset self-test is initiated via the control registers of the WDC, and once completed, its results are polled. This test is performed only once during each loop of the DRMD test execution phase. If the "A" option was selected, the WDC is exposed to only one self-test per loop, rather than four.

Fault information states the function that failed the WDC self-test.

User inputs : none - all control inputs are ignored while this test is executed.

Execution modes: all

5.5.3 FIFO Host Port

The WDC FIFO host port is tested using a walking bit test. This test is performed only once per loop.

Fault information states the required and the received data.

User inputs : none - all control inputs are ignored during the FIFO test.

Execution modes: all

5.5.4 Drive Status

All subsequent tests display a message that states, in addition to the tested function, the drive device number under test.

In this test, a drive status command is sent, and the drive status is verified to be correct.

Fault information includes required drive status and the received drive status.

User inputs : none

Execution modes: all

5.5.5 Drive Recalibrate

The drive under test is recalibrated, and command completion is verified through the drive sense block.

Control fault data is displayed if a fault is encountered in this test.

User inputs : none

Execution modes : all

5.5.6 Track 0 Scan

Each sector in track 0 is scanned, and its CRC checked.

Fault information includes the control fault data.

User inputs : none

Execution modes: all

5.5.7 Sector 0 Read

The first 256 bytes of track 0 are read, and VERSAdos initialization data is verified. If the initialization information is absent, the test is aborted. If a data error is detected, the data fault is presented, and execution proceeds according to the selected modes.

Fault information varies with the type of fault. All data oriented faults state the required data byte and the received data byte, while all control oriented faults list the control fault data.

User inputs : none

Execution modes: all

5.5.8 Drive Configuration

The disk configuration information, as defined by the VERSAdos configuration sector, is read, and then the WDC is configured accordingly.

Fault information is control-oriented, stating the drive sense block and the command packet.

User inputs : none - all control inputs are ignored while the WDC is being configured.

Execution modes: all

5.5.9 Drive Forward Sequential Scan

The disk is scanned, a track at a time, and command completion is verified. All control inputs are available for this test.

User inputs : none

Execution modes: all

5.5.10 Random Sector Seek and Recalibrate

A random sector number is calculated, and that specific sector is seeked. Then the head is repositioned on track 0 via the recalibrate command. This is repeated 150 times for a floppy drive, 300 times for a Winchester.

Fault information is the standard control fault data.

User inputs : none

Execution modes: all

5.5.11 WDC Interrupts

Both command and data interrupts are generated and serviced.

Fault information includes the failing function and the control fault data, if applicable.

User inputs : none. All control inputs are ignored during this test.

Execution modes: all

5.5.12 Diagnostics Track Set-up

This part of the DRMD is entered only if a diagnostic track directory was not found to be present on the media under test.

If the diagnostic tracks are not present, the user is provided with the option to initiate them if the media tested is a floppy drive. However, if the media is a Winchester drive, the test is aborted, and a write to the disk is not performed.

This part of the test is bypassed if the media has been initialized to set up the diagnostic tracks.

User inputs : Y (yes), if the user chooses to proceed with the test. N (no), if the media is not to be written to and the test is to be aborted. Any other character is treated as if the user entered an N.

Execution modes: interactive test, and only if no diagnostic tracks are found.

5.5.13 Diagnostics Data Verification

The validity of the diagnostic data is verified. This data is written to the diagnostic tracks by either the VERSAdos INIT utility, or by the diagnostic track set-up test. If the data is valid, the test proceeds. If it is not, the user is presented with an option to either abort the test or proceed with it and perform writes to the disk.

User inputs : same as in Paragraph 5.5.12

Execution modes: interative test only

5.5.14 Data Write/Read

A walking bit pattern is written to the diagnostic tracks of the disk, and then read and verified to be intact.

Fault information states the required data byte and the read data byte.

User inputs : none

Execution modes: interactive test only

5.5.15 Random Data

A random data block is calculated, written to the diagnostic tracks, and then read and verified to be correct.

Fault information is the same as in the write/read test.

User inputs : none

Execution modes: interactive test only

5.5.16 Diagnostics Data Initialization

The pre-defined diagnostic data is rewritten to the diagnostic tracks, and then verified so that future disk tests are valid.

To prevent invalidation of future tests, the diagnostics data initialization test cannot be stopped or bypassed. Furthermore, if any of the interactive tests are stopped by use of the BREAK key, control is transferred to this test. The control phase is entered only after the diagnostic data has been reinitialized on the disk.

Fault information is data-oriented, and is the same as in all data tests.

User inputs : none. All control inputs are ignored.

Execution modes: interactive test only

CHAPTER 6

DUAL SERIAL PORT I/O MODULE DISK RESIDENT MODULE DIAGNOSTICS TEST

6.1 INTRODUCTION

This chapter describes the Dual Serial Port (MVME400) DRMD test, which either establishes the module is fully functional or isolates the faulty function. Any fault encountered is considered to be a warning.

6.2 SYSTEM CONFIGURATION

Verify system configuration per paragraph 8.2. The system must be in the TENbug monitor.

6.3 START/RESTART/ABORT INFORMATION

The MVME400 DRMD test is initiated by entering the following command:

TENbug x.y > B0 0,0,MVME400 (CR)

6.4 TEST RESULTS

A successful completion of the MVME400 DRMD test is indicated on the display screen by displaying the "passed" status in field 1 of the status line, and then entering the control phase. At that time, the user is presented with the command options described in paragraph 1.4.3. The results of all executed tests as described in paragraph 6.5 are displayed on the screen.

6.5 FUNCTIONAL DESCRIPTION

The MVME400 DRMD test verifies that the board is fully functional. To execute interactive test, connect the user-prepared loop back test cable between ports 1 and 2 of the module.

6.5.1 Port 1 and Port 2 Existence Test

This test verifies that the MVME400 is located in its designated address in the I/O Channel memory map.

User inputs : none

Execution modes: all

6.5.2 Module Initialization

The MVME400 is verified to initialize as follows:

CA1 and CA2 for both ports are set to be inputs.
POS and IRQ for both ports are masked.
PA0-PA2 are set to be inputs, PA3-PA4 are set to be outputs, PA5-PA7 are set to be inputs.
PB0-PB7 are set to be outputs.
The baud rate is set to 9600.
The 7201 is set for 8 bit data, 2 stop bits, and X16 clock rates.
The FAIL LED is reset to off.

Fault information states the failing function:

User inputs : none

Execution modes: interactive test only

6.5.3 Port 1 and 2 Control Lines

The 7201 control lines DCD, CTS, and RTS for both ports are tested for proper functionality.

User inputs : none

Execution modes: interactive test only

6.5.4 Port 1 and 2 Data Test

In these tests, data is sent to port A of the 7201, and then read from port B. The same test is repeated, with port B transmitting to port A of the 7201.

Fault information states the required data byte and the received data byte in addition to any relevant information.

User inputs : none

Execution modes: interactive test only

6.5.5 7201 Interrupts Tests

The 7201 is tested to verify that it can generate data, as well as DSR and IR interrupts.

User inputs : none

Execution modes: interactive test only

6.5.6 FAIL LED Test

In this test, the user is prompted to verify the state of the MVME400 FAIL LED.

User inputs : Y (yes), the FAIL LED is in the required state;
N (no), it is not

Execution modes: single pass, interactive mode only

CHAPTER 7

DUAL PARALLEL PORT I/O MODULE DISK RESIDENT MODULE DIAGNOSTICS TEST

7.1 INTRODUCTION

This chapter describes the Dual Parallel Port (MVME410) DRMD test, which establishes that the module is fully functional or isolates the faulty function. Any fault encountered is considered to be a warning.

7.2 SYSTEM CONFIGURATION

Verify system configuration per paragraph 8.3. The system must be in the TENbug monitor.

7.3 START/RESTART/ABORT INFORMATION

The MVME410 DRMD test is initiated by entering the following command:

TENbug x.y > BO 0,0,MVME410 (CR)

7.4 TEST RESULTS

A successful completion of the MVME410 DRMD test is indicated on the display screen by displaying the "passed" status in field 1 of the status line, and then entering the control phase. At that time, the user is presented with the command options described in paragraph 1.4.3. The results of all executed tests, as described in paragraph 7.5, are displayed on the screen.

7.5 FUNCTIONAL DESCRIPTION

The MVME410 DRMD test verifies that the module is fully functional. To execute the interactive test, insert the two user-prepared loop back test connectors on the module output ports.

7.5.1 Port 1 and 2 Existence Test

This test verifies that both ports are located in their designated address in the I/O Channel memory map.

User inputs : none

Execution modes: all

7.5.2 Port 1 and 2 Data Tests

In these tests, data is sent to port 1, and then read from port 2 and verified to be correct. The test requires that the loop back test connectors be mounted on ports 1 and 2 of the MVME410.

User inputs : none

Execution modes: interactive test only

7.5.3 Port 1 and 2 Interrupt Tests

These tests verify the functionality of control lines CA1, CA2, CB1, CB2, IRQA, and IRQB of both ports, as well as the ability of the SCM to service I/O interrupts. The tests require that the loop back test connectors be mounted on ports 1 and 2 of the MVME410.

User inputs : none

Execution modes: interactive test only

7.5.4 FAIL LED Test

In this test, the user is prompted to verify the state of the MVME410 FAIL LED.

User inputs : Y (yes), the LED is in the required state
N (no), it is not

Execution modes: single pass, interactive mode only

CHAPTER 8

VME/10 MICROCOMPUTER SYSTEM CONFIGURATION

8.1 BASIC SYSTEM CONFIGURATION

Table 8-1 defines the initial factory configuration.

TABLE 8-1. Basic System Configuration

BOARD	JUMPER BLOCK	CONFIGURATION PINS	JUMPER	JUMPER FUNCTION	NOTE
SYSTEM	J2	1 to 2	IN	User option	2
		3 to 4	IN	System has a monochrome CRT	3
		5 to 6	IN	Execute power up test	1
	J3	1 to 2	OUT	64K RAM chips installed	3
CONTROLLER	J9	as required		PROM type selection jumper	3,4
	J10	1 to 2	IN	Processor clock is 10 MHz	2
		3 to 4	OUT	Processor clock is 8 MHz	2
MODULE	J11	1 to 2	IN	I/O channel enable	1
		2 to 3	OUT	I/O channel disabled	
	J15	1 to 3	IN	Backup power source for TDC	3
		2 to 4	IN	connected to a battery	
	J7	1 to 2	OUT	5-1/4 inch Winchester in drive 0	1
WINCHESTER	J8	1 to 2	OUT	5-1/4 inch Winchester in drive 1	1
	J9	1 to 2	OUT	Negative voltage source	4
		2 to 3	IN		
	J10	1 to 2	OUT	INT4 assigned to data interrupt	1
		3 to 4	OUT	INT4 assigned to command interrupt	
CONTROLLER		5 to 6	IN	INT3 assigned to data interrupt	
		7 to 8	IN	INT3 assigned to command interrupt	
		9 to 10	OUT	INT2 assigned to data interrupt	
		11 to 12	OUT	INT2 assigned to command interrupt	
		13 to 14	OUT	INT1 assigned to data interrupt	
		15 to 16	OUT	INT1 assigned to command interrupt	
MODULE	J11	1 to 2	OUT	I/O address of the WDC is $F1C0D1	1
		3 to 4	OUT		
		5 to 6	IN		
		7 to 8	OUT		

TABLE 8-1. Basic System Configuration (cont'd)

BOARD	JUMPER BLOCK	CONFIGURATION PINS	JUMPER	JUMPER FUNCTION	NOTE
	J12	1 to 2	IN		1,4
	J13	1 to 2	OUT		
	J14	1 to 2	OUT		
	J15	1 to 2	IN		
	J16	1 to 2	OUT	96 TPI track density for floppy	3,4
		3 to 4	IN	5-1/4 floppy drive	1,4
		5 to 6	OUT	Floppy head stepping timing = 10Msec	
		7 to 8	IN	Floppy head stepping timing = 10Msec	
		9 to 10	IN	Fixed Winchester for DRV1	1,4
		11 to 12	IN	Buffered step for DRV1	
		13 to 14	IN	Fixed Winchester for DRV0	1,4
		15 to 16	IN	Buffered step for DRV0	
	J17	1 to 2	IN		1,4
	J18	1 to 2	IN		1,4
	J19	1 to 2	OUT		1,4
KEYBOARD	E8	N/A	OUT	Select 512 baud	1
	E9	N/A	OUT	Keyboard address is $0	1
	E10	N/A	OUT	Keyboard address is $0	1
	E11	N/A	OUT	User option	2
	E12	N/A	OUT	User option	2
	E13	N/A	OUT	User option	2

NOTES:

1. Essential for proper operation of the diagnostic program. Jumpers that are not mentioned must be out.
2. Configuration has no effect on the diagnostic program.
3. The diagnostic program self-modifies to match the configuration.
4. For more information, refer to the user manual of the respective module.

8.2 MVME400 CONFIGURATION

8.2.1 Module Configuration

Table 8-2 defines the initial factory configuration. This allows an interactive mode of test to be performed. The non-interactive mode of test requires that only header J6 be configured as defined in Table 8-2. Refer to the MVME400 Dual RS-232C Serial Port Module User's Manual (MVME400) for detailed information.

TABLE 8-2. MVME400 Configuration

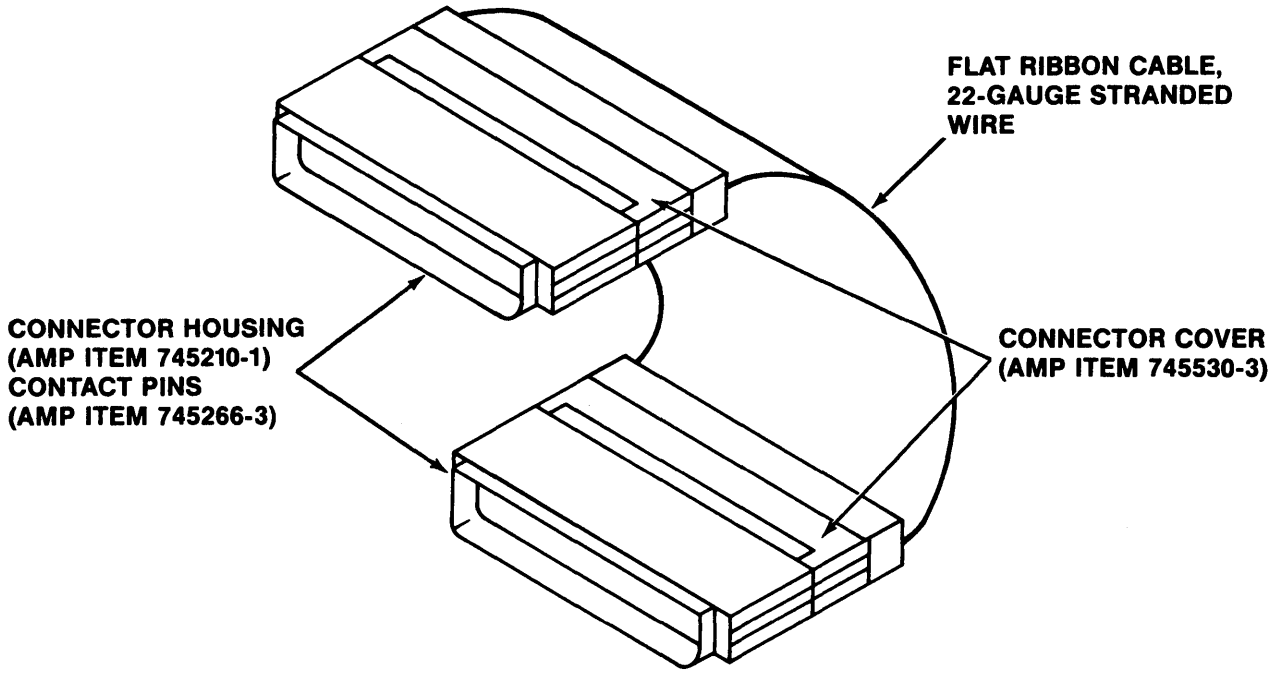
JUMPER BLOCK	CONFIGURATION PINS	JUMPER	JUMPER FUNCTION
J2	1 to 2	IN	Port 2 TxC select
	2 to 3	OUT	
J3	All jumpers OUT		Port 2 external clock select
J4	1 to 2	IN	Transmit and receive clocks for port 2
	3 to 4	IN	are generated internally on-board
	5 to 6	OUT	
	7 to 8	OUT	
	9 to 10	IN	
	11 to 12	IN	
J5	4 to 6		PIA IRQA connected to INT4
	10 to 12		PIA IRQB connected to INT4
	16 to 18		7201 interrupt connected to INT4
J6	1 to 2	OUT	Base address is set at $F1C1C1
	3 to 4	OUT	
	5 to 6	OUT	
	7 to 8	IN	
J7	5 to 7	IN	CTS control for port 2
	6 to 8	IN	
J8	All jumpers OUT		Select terminal for port 2
J9	All jumpers IN		Select terminal for port 2
J10	1 to 2	OUT	Select baud rate of 9600 for
	3 to 4	IN	both ports
	5 to 6	IN	
	7 to 8	OUT	
	9 to 10	IN	
	11 to 12	IN	

TABLE 8-2. MVME400 Configuration (cont'd)

JUMPER BLOCK	CONFIGURATION PINS	JUMPER	JUMPER FUNCTION
J11	1 to 2 2 to 3	IN OUT	Port 1 TxC select
J12	Same as J3		Port 1 external clock select
J13	Same as J4		Port 1 internal clock select
J14	All jumpers OUT		Select terminal for port 1
J15	All jumpers IN		Select terminal for port 1
J16	5 to 7 6 to 8	IN IN	CTS control for port 1

8.2.2 Loop Back Test Cable

If an interactive test is to be performed, connect the user-prepared loop back test cable between ports 1 and 2 of the MVME400. The loop back cable contains two RS-232C connectors, and provides the pin connections defined in Figure 8-1.



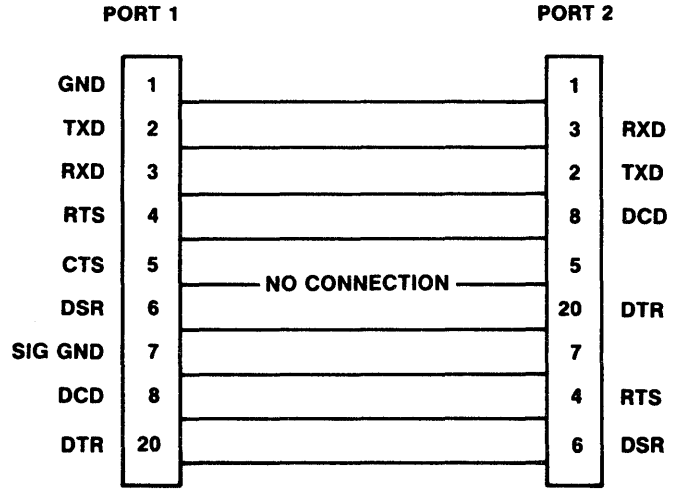


FIGURE 8-1. MVME400 Loop Back Cable and Pin Connections

8.3 MVME410 CONFIGURATION

8.3.1 Module Configuration

Table 8-3 defines the initial factory configuration. This allows an interactive mode of test to be performed. The non-interactive mode of test requires that only J14 be configured as defined in Table 8-3. Refer to the MVME410 Dual Parallel Port Module User's Manual (MVME410) for detailed information.

TABLE 8-3. MVME410 Configuration

JUMPER BLOCK	CONFIGURATION PINS	JUMPER	JUMPER FUNCTION
J2	1 to 2 2 to 3	OUT IN	LED monitor
J3	1 to 2	IN	P1CA2 is an output
J4	1 to 2 3 to 4	IN OUT	P1PA0-P1PA7 are outputs
J5	1 to 2		P1CB2 is an output
J6	1 to 2 3 to 4	OUT OUT	P1PB0-P1PB7 are inputs
J8	1 to 2	IN	P2CA2 is an output
J9	1 to 2 3 to 4	IN OUT	P2PA0-P2PA7 are outputs
J10	1 to 2	IN	P2CB2 is an output
J11	1 to 2 3 to 4	OUT OUT	P2PB0-P2PB7 are inputs
J12	2 to 4 8 to 10	IN IN	IRQ1A is connected to INT1 IRQ1B is connected to INT1
J13	2 to 4 8 to 10	IN IN	IRQ2A is connected to INT1 IRQ2B is connected to INT1
J14	All jumpers OUT		Base address is set at $F1C1E1
J15	2 to 3	IN	P1PB7 dedicated to FAIL LED

8.3.2 Loop Back Test Connectors

If an interactive test is to be performed, connect the two user-prepared loop back cable test connectors on both ports of the MVME410. The loop back cable test connector is wired with 28-gauge stranded wire as shown in Figure 8-2.

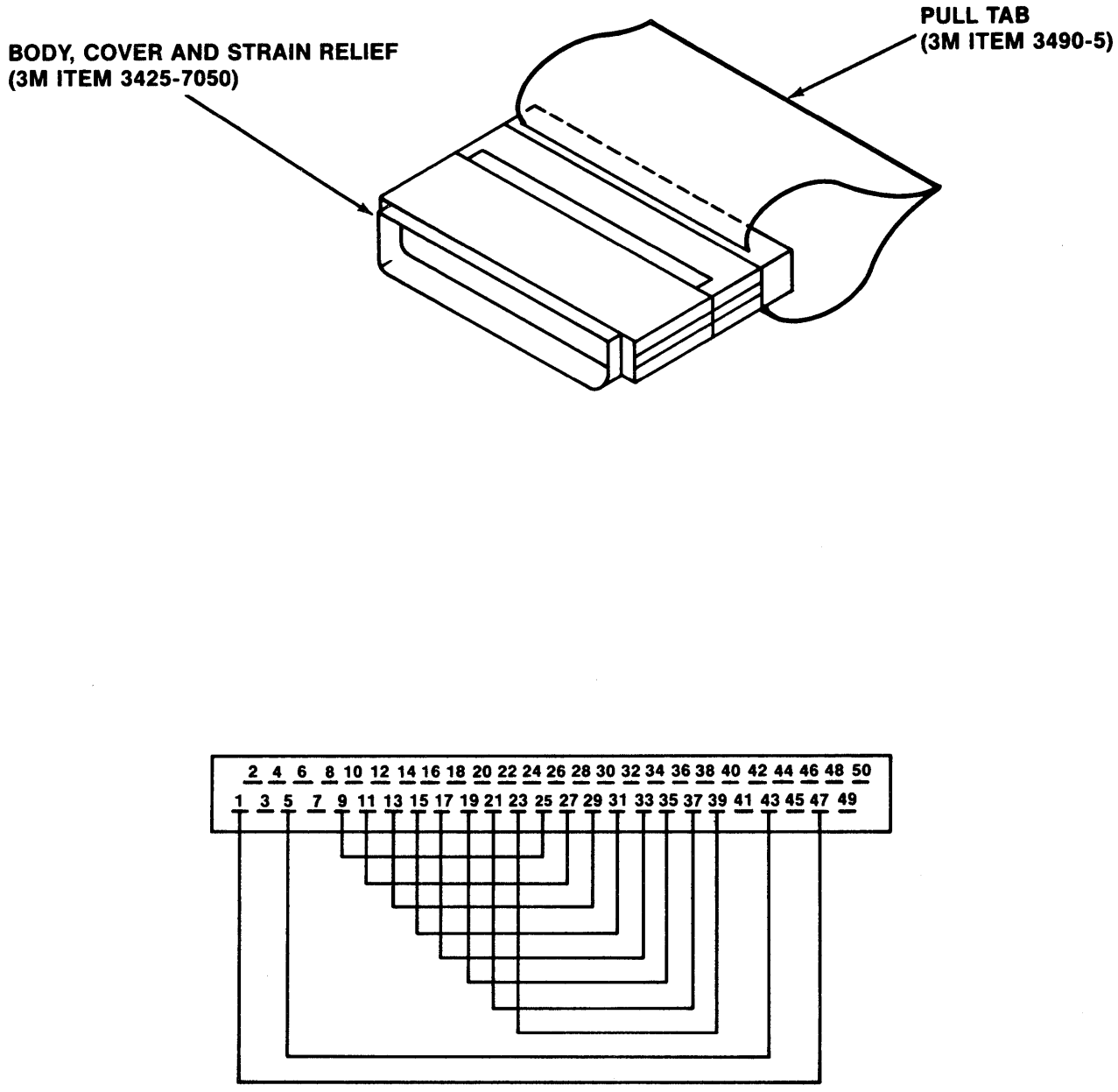


FIGURE 8-2. MVME410 Loop Back Cable and Pin Connections

ADDENDUM
TO
VME/10 MICROCOMPUTER SYSTEM
DIAGNOSTICS MANUAL
(M68KVSDM/D1)

This addendum supersedes addendum A1 issued on November 1983.

This addendum corrects procedural steps described in the M68KVSDM/D1 diagnostics manual. These corrections resulted from the VERSAdos 4.3 program changes now incorporated into the VME/10 Microcomputer System diagnostics (maintenance) program.

Correction information pertains to the execution of the Disk Resident Module Diagnostic (DRMD) tests performed in Chapters 3 through 7. To initiate a DRMD test for a specific component, the following command structure was used:

TENbug x.y > BO 0,0,filename(CR)

or

TENbug x.y > BO 0,0,:0.VME10.filename(CR)

NOTE

Underscored nomenclature is user-entered on keyboard.

This command structure is now altered as follows:

TENbug x.y > BO,0,0,:0.VMES10.filename(CR)

Throughout Chapters 3 through 7, correct the command structure as shown above.

In addition to the above corrections, this addendum adds a new Chapter 9 to the diagnostic manual. Insert these new text pages (attached to this addendum page) into your M68KVSDM/D1 manual.

This page of the addendum should be placed after the diagnostic manual title page and used as a record page of the changes made to your manual.

CAUTION

The following diagnostic is not to be used with SYSTEM V/68 installed. Do not attempt to perform this diagnostic:

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CHAPTER 9

SYSTEM MEMORY DISK RESIDENT MODULE DIAGNOSTIC TEST

9.1 INTRODUCTION

This chapter describes the system memory (RAM) DRMD test, which either establishes that a user defined block of memory is functional or isolates the faulty address. Note that the SCM DRMD test described in Chapter 3 tests the SCM RAM. The RAM DRMD test provides a more versatile method of testing the SCM RAM as well as additional RAM boards installed on the VMEbus.

9.2 SYSTEM CONFIGURATION

The memory block to be tested must be configured by the user per the user manual to be valid in the VME/10 system memory map. The system must be in the TENbug monitor.

9.3 START/RESTART/ABORT INFORMATION

The RAM DRMD test is initialized by entering the following command:

TENbug x.y > BO 0,0,:0.VMES10.RAM

9.4 TEST RESULTS

A successful completion of the RAM test is indicated on the display terminal by displaying the "passed" status in field 1 of the status line, and then entering the control phase. At that time, the user is presented with all the command options described in paragraph 1.4.3.

The results of all executed tests as described in paragraph 9.5 are displayed on the screen.

9.5 FUNCTIONAL DESCRIPTION

The RAM DRMD test verifies that a user defined, contiguous memory block is fully functional.

9.5.1 Block Selection

An additional selection option is presented to the user at mode selection phase. This option allows the user to select the memory block that is to be tested. The memory block is selected by entering its start and end address, expressed in hex, and preceded by a dollar sign ($). The address range must be at least 4 bytes, but for a full functionality of the test it should be at least 32 bytes. The routine incorporates an algorithm that will verify that:

a. The start address of the memory block is greater than the end address of the RAM DRMD program.

b. The end address of the memory block is greater than its start address.

c. The memory block is at least 4 bytes long.

d. The requested address is preceded by a dollar sign.

The user will be prompted to re-enter the requested parameter if any are found to be at fault.

The start address of the memory block to be tested is defaulted to the top of the RAM resident test program, and the end to the top of the SCM resident memory ($60000).

In addition, all other mode selection entry options are available to the user.

9.5.2 Address Bus Test

The address bus test verifies that the address bus to memory is free from faults. The test is performed by writing the address of a memory location into the 4 bytes that can be accessed using this address. After the whole memory block has been written, the data stored is read and verified to be correct by comparing it to the required address. This process is then repeated using the complement of the RAM address.

Fault information states the failing address, the required data, and the data actually read from memory. The user can then interpret this data and relate it to a faulty address line.

User inputs : none

Execution modes: all

9.5.3 Patterned Data Test

The patterned data test stores complementary patterns to memory, and then verifies them to be correct. The patterns are designed to toggle the state of the data bus with each data transfer.

Fault information states the failing address, the required data, and the data acutally read from memory.

User inputs : none

Execution modes: all

9.5.4 Fast Random Data Test

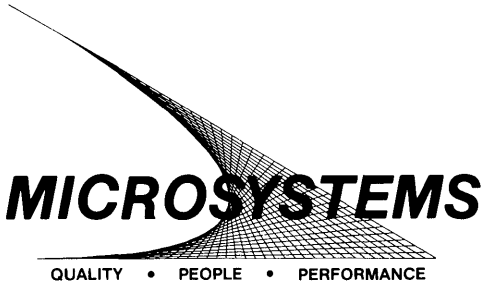
The fast random data test calculates and stores a random pattern in a block of memory, and then verifies it to be correct. The test incorporates multi-register transfers, so that the data bus, as well as memory, is exposed to higher rates of data transfers.

Fault information states the failing address, the required data, and the data actually read from memory.

User inputs : none

Execution modes: all - provided that the memory block is at least 32 (hex 20) bytes long.

SUGGESTION/PROBLEM REPORT



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