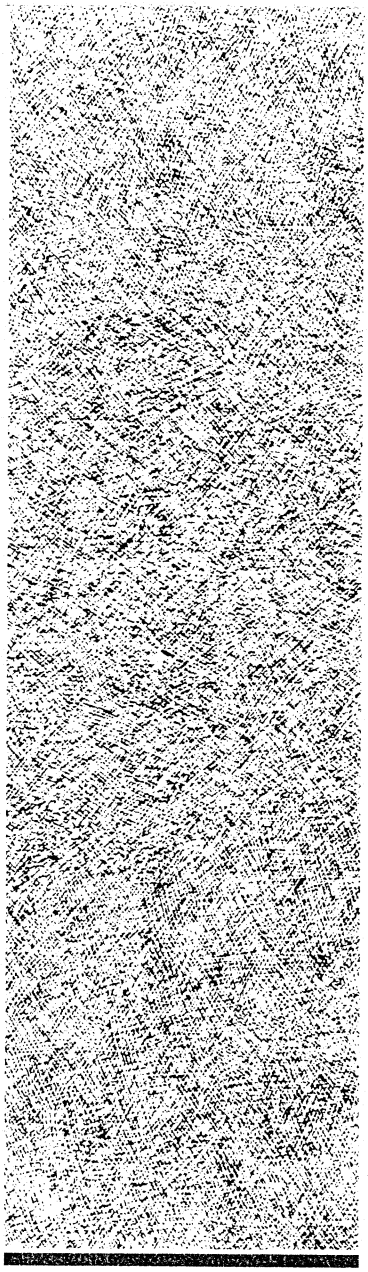
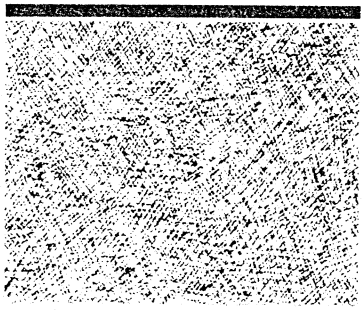


MOTOROLA



MVME374/D1

MVME374
Multi-Protocol Ethernet Interface Module User's Manual

MVME374

MULTI-PROTOCOL ETHERNET INTERFACE MODULE

USER'S MANUAL

(MVME374/D1)

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Motorola reserves the right to make changes to any products herein to improve reliability, function, or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of others.

PREFACE

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME374 Multi-Protocol Ethernet Interface Module.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *related documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

First Edition July 1988

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME374 Multi-Protocol Ethernet Interface Module. This module is referred to as MVME374 throughout the remainder of this manual.

1.2 FEATURES

The features of the MVME374 include:

- AM7990 Local Area Network Controller (LANCE) and AM7992B Serial Interface Adapter (SIA), for IEEE 802.3 Media Access Control (MAC) layer
- MC68020 16.0 MHz microprocessor
- 1Mb of one-wait-cycle shared dynamic RAM (DRAM) with parity, organized as a longword (32-bit wide) port accessed by the processor, LANCE, or the VMEbus
- One MC68901 Multi-Function Peripheral (MFP)

  Programmable interrupt handler

  Two 8-bit programmable timers, chainable into one 16-bit timer

  One asynchronous serial debug port

  Programmable baud rate counter

  Watchdog timer
- Local bus arbitration between the MPU, LANCE, VMEbus, and RAM refresh
- VMEbus interrupter, with programmable level and vector
- Four 32-pin JEDEC standard sockets for EPROM - 8K x 8, 16K x 8, 32K x 8, 64K x 8, 128K x 8; or EEPROM - 8K x 8 or 32K x 8
- Power-on/reset EPROM-resident diagnostics, part of the four EPROMs containing the 374Bug debugging package
- One asynchronous serial debug port (part of MC68901 MFP)
- Cable interface (from P2) for debug terminal connection
- Bus requester with Release-on-Local-Cycle mode (a subset of RWD)

- Status LEDs for FAIL and for +12V Ethernet transceiver power
- Memory-mapped slave interrupt
- 256 x 4 of EEPROM-based NVRAM for module-specific variables
- A32:D16 or A24:D16 VMEbus master interface
- A32:D16 or A24:D16 VMEbus slave interface
- Partial VMEbus system controller for stand-alone operation
  - Single level arbiter
  - Global bus time-out
  - Reset driver
  - SYSFAIL monitoring and indication
  - System clock available
- Minimum VMEbus interrupt handler on level 3 only for stand-alone operation
- Jumper-selectable VMEbus base address
- Front panel RESET and ABORT switches
- Front panel DB-15 connector for interfacing Ethernet transceiver

1.3 SPECIFICATIONS

General specifications for the MVME374 module are provided in Table 1-1. Paragraphs 1.3.1 and 1.3.2 detail cooling requirements and FCC compliance, respectively.

TABLE 1-1. MVME374 Specifications

CHARACTERISTICS	SPECIFICATIONS
Microprocessor	MC68020
Clock signal	16.0 MHz derived from 32 MHz oscillator
Memory size	
RAM	1Mb
EPROM	Four sockets support 8K x 8, 16K x 8, 32K x 8, 64K x 8, or 128K x 8

TABLE 1-1. MVME374 Specifications (cont'd)

CHARACTERISTICS	SPECIFICATIONS
Memory size (cont'd)	
EEPROM	EPROM sockets also support 8K x 8 or 32K x 8 EEPROMs
NVRAM	256 bits x 4 for module-specific variables
Temperature	
Operating (refer to paragraph 1.3.1)	0 degrees to 55 degrees C at point of entry of forced air (approximately 320 LFM)
Storage temperature	-40 degrees to 85 degrees C
Relative humidity	5% to 90% (non-condensing)
Physical characteristics (not including front panel)	
Width	6.299 inches (160.00 mm)
Height	9.187 inches (233.35 mm)
Thickness	0.83 inches (21 mm)
Power requirements	+5 Vdc @ 4.5 A (typical), 4.9 A (maximum) +12 Vdc @ 360 mA (typical), 400 mA (maximum) -12 Vdc @ 40 mA (typical), 50 mA (maximum)
Connectors	
To VMEbus	DIN No. 41612C96 male (P1, P2)
To Ethernet	DB-15 female (J1)

1.3.1 Cooling Requirements

The Motorola MVME374 VMEmodule is specified, designed, and tested to operate reliably with an incoming air temperature range from 0 degrees C to 55 degrees C (32 degrees to 131 degrees F) with forced air cooling at a velocity typically achievable by using a 71 CFM axial fan. Temperature qualification is performed in a standard Motorola VMEsystem 1000 chassis. Twenty-five watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of two axial fans, rated at 71 CFM per fan, is placed directly under

the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 12 CFM and 320 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55 degrees C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

1.3.2 FCC Compliance

The MVME374 was tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

a. Shielded cables on all external I/O ports.

b. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.

c. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.

d. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the module.

1.4 GENERAL DESCRIPTION

The MVME374 is a double-high VMEmodule. It is a high performance, VMEbus compatible, Multi-Protocol Ethernet Interface Module that utilizes the AM7990 LANCE chip to provide the MAC layer for an IEEE 802.3 Local Area Network (LAN) node. The MVME374 utilizes an MC68020 MPU to provide the processing power required to efficiently implement ISO-OSI (International Standards Organization - Open Systems Interface) protocol layers 2 through 7 on a single VMEbus board. The MVME374 also contains a large dual port RAM, a debug serial port, programmable timers, and a programmable VMEbus interrupter. A partial VMEbus system controller, interrupt handler, and A32:D16 VMEbus master capability are provided for stand-alone operation.

The MVME374 Multi-Protocol Ethernet Interface is a complete front end protocol processor which provides connection between an Ethernet network and the VMEbus. To relieve a VMEbus host of protocol burden, the MVME374 can serve as a front end for processing TCP/IP (Transmission Control Protocol/Internet Protocol), XNS, DECnet, TOP and other protocols downloaded into its 1Mb of shared RAM. When executing Motorola's optional MicroTOP software, for example, it frees the VMEbus host from nearly all protocol processing.

All functionality of the seven layers of the TOP protocol is supported by the MicroTOP software. Rapid data throughput and fast real-time response are achieved using the MC68020 to execute the TOP protocol suite from shared RAM and the LANCE chip set to interface the Ethernet transceiver.

An advanced MVME374 design that takes full advantage of its high performance VLSI devices including the MC68020 32-Bit Microprocessor and the AM7990 LANCE/AM7992B SIA set provides the power for concurrently executing application and Ethernet protocol software.

For stand-alone operation such as might be needed in a bridge or gateway, the MVME374 has a system controller. Using application software developed by the user, an Ethernet-to-Token Bus bridge, for example, could be built around just three modules (MVME374, the MVME372 MAP Interface Module, and the MVME371 Broadband Modem) avoiding the need for a separate MPU or system controller board. Other implementations, for example, Ethernet-to-X.25, or Token Bus-to-asynchronous serial could use combinations of the MVME374, the MVME332xt Intelligent Communications Controller and the MVME333 Intelligent Communication Controller.

The MVME374 provides a DB-15 connector on its front panel for connection to the offboard, TCL Inc. Ethernet transceiver.

The MVME374 achieves the performance required of a front end capable of processing a protocol such as TOP and of concurrently interfacing Ethernet at 10Mbits/s by using fast 100ns devices for its fully-shared 1Mb of parity DRAM. This offers the 16 MHz MC68020 one-wait-state accesses for its 32-bit instructions and offers the LANCE chip one-wait-state accesses for its 16-bit operations. Execution time is further minimized by the instruction cache of the MC68020. High performance can also be obtained by executing a program residing in the EPROM, configured from 150ns devices.

Functions interfacing the VMEbus Data Transfer Bus (DTB) interface include DRAM, a requester, an interrupter, a slave control/status register and a system controller which includes a single level arbiter, global bus time-out circuitry, a RESET line driver, SYSFAIL line monitoring and a level three VMEbus interrupt handler.

Functions/resources interfacing the local bus include: DRAM, ROM, non-volatile RAM organized as 256 x 4, two control registers, a local bus arbiter/refresh control, reset circuitry, the LANCE, and an MC68901 Multi-Function Peripheral device used for the VMEbus interrupt handling and for the serial debug port available on the module's P2 connector pins.

1.5 RELATED DOCUMENTATION

The following publications are applicable to the MVME374. If these manuals are not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, AZ 85282; telephone (602) 994-6561. Non-Motorola documents may be obtained from the sources listed.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
VMEbus Specification Manual	HB212
MC68020 32-Bit Microprocessor User's Manual	MC68020UM
MC68901 Multi-Function Peripheral User's Manual	MC68901
374Bug Debugging Package User's Manual	MVME374BUG

Local Area Network Controller Am7990 (LANCE), Technical Manual, order #06363A, Advanced Micro Devices, Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

Am7992B Serial Interface Adapter (SIA), data sheet, order #03378E, Advanced Micro Devices, Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088.

1.6 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides hardware preparation and installation instructions for the MVME374.

2.2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

2.3 HARDWARE PREPARATION

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

The MVME374 options allow users to configure the module for the requirements of a particular application. Header locations and factory jumper placements for the MVME374 are shown in Figure 2-1. The selectable functions include:

- VMEbus grant level (J2)
- VMEbus request level (J3)
- System controller operation (J4)
- EPROM/EEPROM device size (J5)
- Local address line select (J6)
- Module base address select (J7)
- VMEbus address line select (J8)
- Auxiliary Ethernet connection (J9)

2

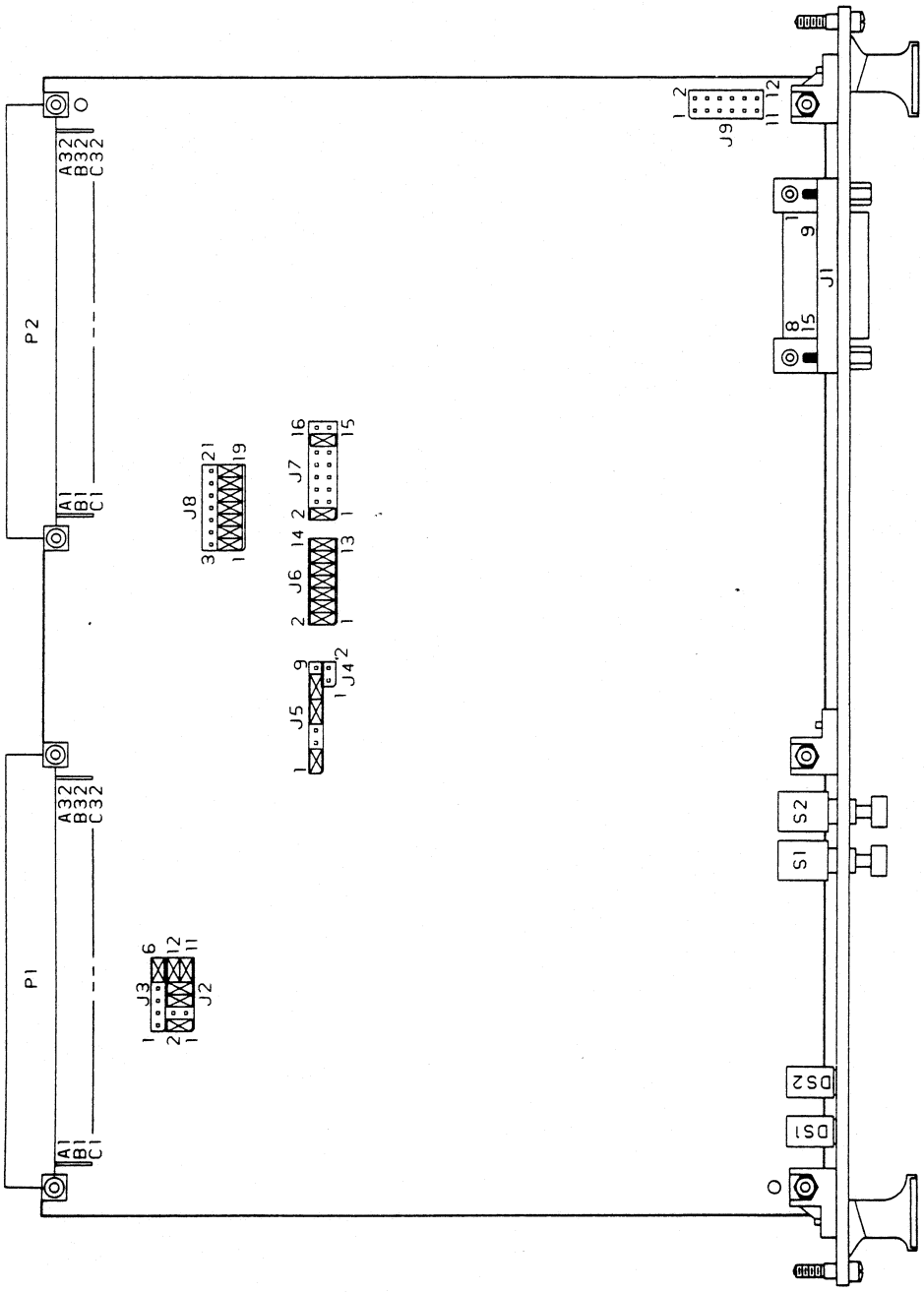
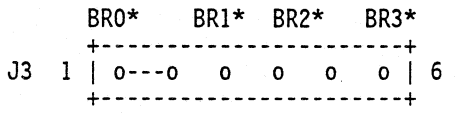


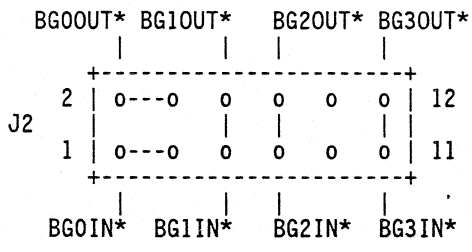
FIGURE 2-1. MVME374 Header Locations and Factory Jumper Placements

2.3.1 VMEbus Grant and Request Level Select Headers (J2, J3)

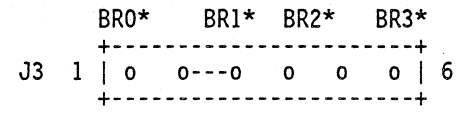
Headers J2 and J3 are used to select the level at which the MVME374 grants and requests the VMEbus when executing global memory cycles. This request level is also used whenever a Read-Modify-Write cycle is being executed by the local MPU.

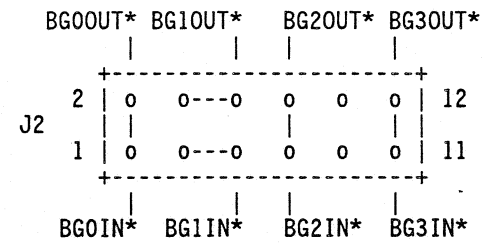
The as-shipped configuration is for bus grant and bus request at level 3. The level for bus grant and bus request must be the same. The desired level is selected by jumper configuration as shown below:



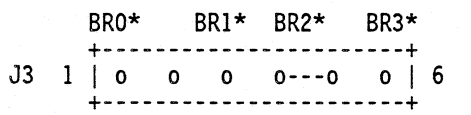


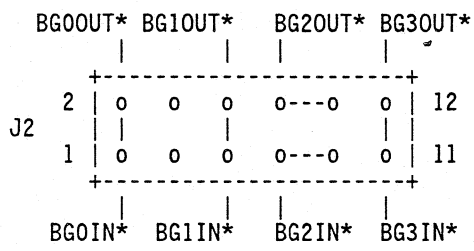
LEVEL 0



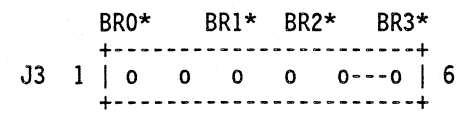


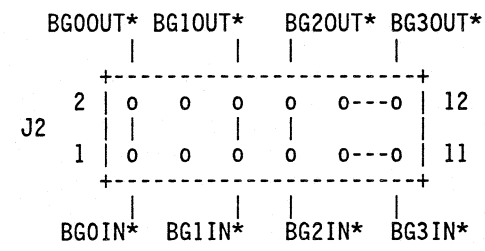
LEVEL 1





LEVEL 2

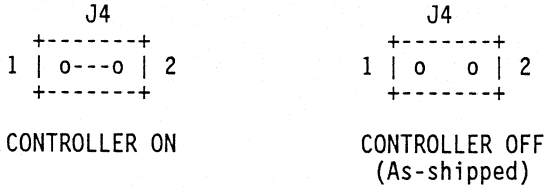




LEVEL 3
(As-shipped)

2.3.2 System Controller Select Header (J4)

Header J4 is used to select the MVME374 as the system controller for small system or stand-alone operation. Only one module per system should be selected as the system controller and that module should be in slot 1 of the VME chassis. The module is shipped with the system controller off.

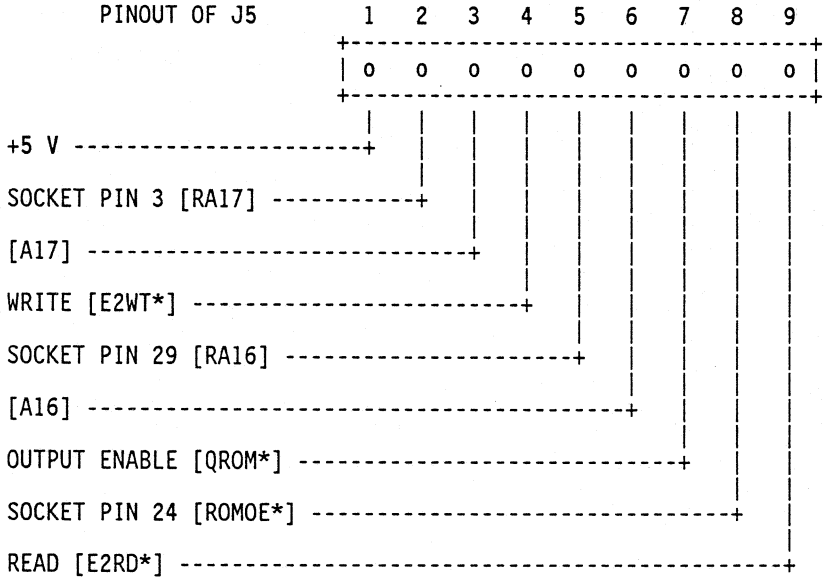


2.3.3 EPROM/EEPROM Device Size Header (J5)

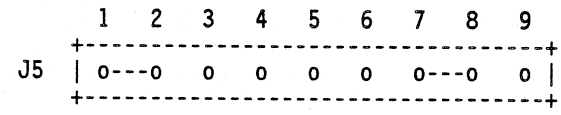
Header J5 is used to configure the four 32-pin, JEDEC standard sockets to hold one of several device types. All four devices must be of the same type and should have an access time that is less than 170ns for a read data cycle. If EEPROMs are used, refer to EEPROM programming considerations in Chapter 4.

CAUTION

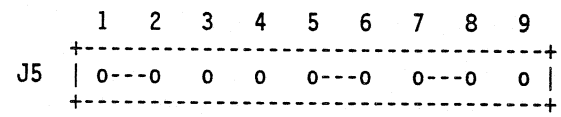
IF 28-PIN DEVICES ARE USED IN THE 32-PIN SOCKETS, THEY MUST BE INSERTED AT THE "BOTTOM" OF THE SOCKET, SUCH THAT DEVICE PIN 1 IS IN SOCKET PIN 3 AND DEVICE PIN 28 IS IN SOCKET PIN 30. OTHERWISE, THE DEVICES WILL BE ELECTRICALLY DAMAGED OR DESTROYED.



Header configuration for 8K x 8 and 16K x 8 EPROM devices is shown below:

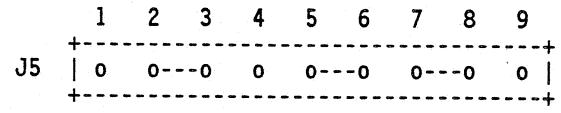


Header configuration for 32K x 8 EPROM devices is shown below:

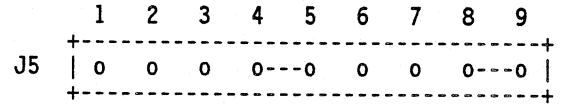


(As-shipped)

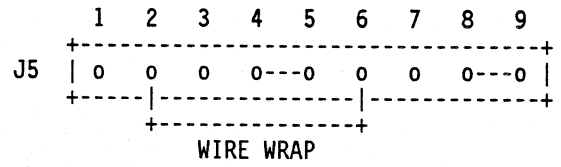
Header configuration for 64K x 8 and 128K x 8 EPROM devices is shown below:



Header configuration for 8K x 8 EEPROM devices is shown below:



Header configuration for 32K x 8 EEPROM devices is shown below:

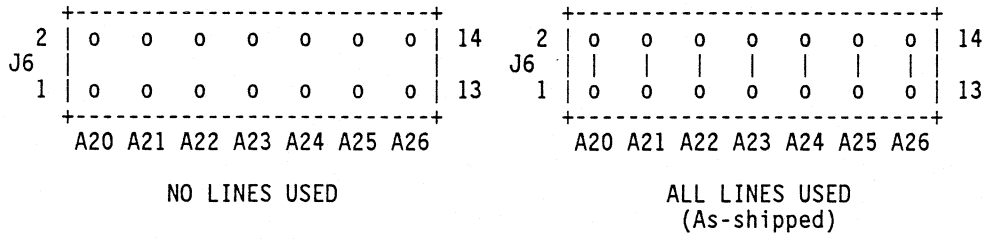


2.3.4 Module Base Address Selection

The MVME374 memory appears as a 1Mb address space on the VMEbus, and in two 1Mb spaces in the local memory map. In addition to the fixed local address of $FFF00000 through $FFFFFFFF, the memory also appears in the local memory map at the same address as the module VMEbus memory. Thus, the memory base address selection includes a module address select header (J7), a VMEbus address line select header (J8) (for use by the VMEbus slave interface), and a local address line select header (J6) (for use by the module VMEbus master interface). The MVME374 responds to address modifiers $09, $0D, $39, and $3D when the jumper on J7 pins 1 and 2 is removed, and to address modifiers $09 and $0D when the jumper is installed.

2.3.5 Local Address Line Select Header (J6)

J6 selects which of the local address lines are used by the local address comparator logic to determine if the address on the local bus is the same as the module VMEbus address. When the A24 address space (standard) is selected, remove jumpers from J6 pins 9 and 10, 11 and 12, and 13 and 14.



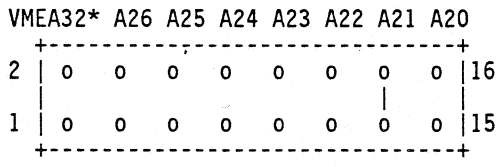
NO LINES USED

ALL LINES USED
(As-shipped)

2.3.6 Module Base Address Select Header (J7)

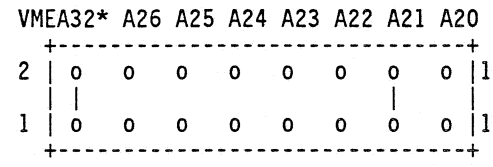
J7 selects the module VMEbus base address and the address space (extended or standard). J7 pins 1 and 2 select extended (A32) address space (jumper installed) or standard (A24) address space (removed). The remaining pins select address lines A20 through A26 as one (jumper removed) or zero (installed). J7 pins 1 and 2 also specify the state of address lines A27 through A31 for each of the two address spaces. When A32 address space is selected, lines A31 through A27 = $F8. This adds $F8000000 to the base address selected by the rest of the jumpers on J7. Thus, if J7 was connected for A32 and the base address was selected as $07D00000, the final address is $FFD00000. If A24 address space is selected, lines A24 through A26 must be terminated because they are undefined in the standard address space. This termination is done by removing jumpers from J7 pins 3 and 4, 5 and 6, 7 and 8, and the related jumpers from J6 and J8. The remaining high order address lines are ignored by the comparator logic. If an extended address is received from the VMEbus, and lines A31 through A24 = $00, this is decoded as an equivalent A24 address and compared against address lines A23 through A20. The MVME374 responds to address modifiers $09, $0D, $39, and $3D when the jumper on J7 pins 1 and 2 is removed; and to address modifiers $09 and $0D when the jumper is installed.

J7



VMEbus BASE ADDRESS = $D00000 (A24)
AND $00D00000 (A32)

J7

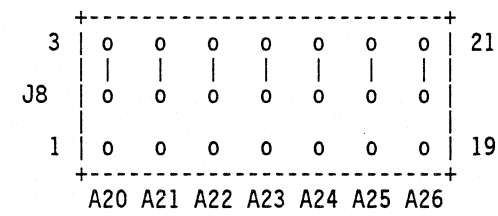


VMEbus BASE ADDRESS = $FFD00000 (A32)
(As-shipped)

2.3.7 VMEbus Address Line Select Header (J8)

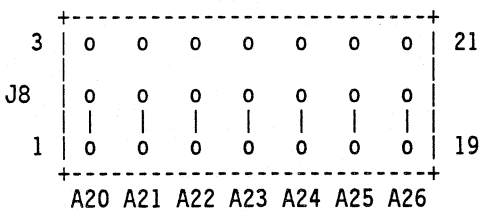
J8 selects which of the VMEbus address lines are used by the VMEbus address comparator logic to determine if the address on the VMEbus is the same as the module selected VMEbus address. When the A24 address space (standard) is selected, remove jumpers from J8 pins 13 and 14, 16 and 17, 19 and 20; and add jumpers between J8 pins 14 and 15, 17 and 18, 20 and 21.

TO PART OF RESISTOR PACK R17



NO LINES USED

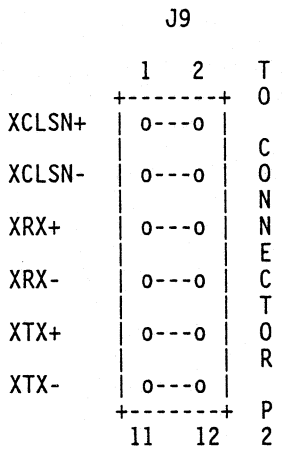
TO PART OF RESISTOR PACK R17



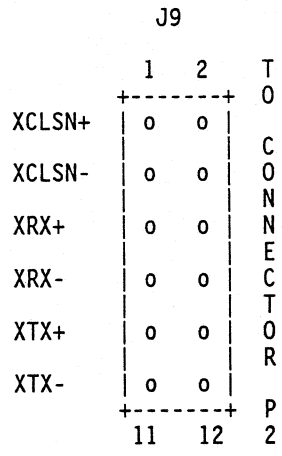
ALL LINES USED
(As-shipped)

2.3.8 Auxiliary Ethernet Connection Header (J9)

The MVME374 connects to an IEEE 802.3 transceiver through connector J1 on the front panel. Header J9 permits connecting these Ethernet signals to connector P2. The as-shipped configuration is with the signals not connected.



ETHERNET SIGNALS
CONNECTED TO P2



ETHERNET SIGNALS
NOT CONNECTED TO P2
(As-shipped)

2.3.9 Debug Port (Optional Remote RESET and ABORT Switches) Connector

Signals are provided to rows A and C of the P2 connector to enable the connection of a serial debug port. The pinout of this connector is configured to allow a customer-supplied 25-pin ribbon cable to be press-fitted to a DB-25 connector on one end and at the pin 1 end of a 64-pin DIN connector. This cable allows a terminal to interface to the serial debug port on the MVME374.

Refer to Appendix A for a parts list and an assembly drawing for the debug cable assembly.

Although RESET and ABORT switches are mounted on the front panel of the MVME374, optional remote switches may also be attached to the same pins through P2 and a special customer-made cable.

CAUTION

DO NOT USE THE OPTIONAL ABORT SWITCH WITHOUT FIRST REMOVING THE FRONT PANEL ABORT SWITCH (S1). IF S1 IS NOT REMOVED, MODULE OPERATION MAY BE INCORRECT.

2.4 INSTALLATION INSTRUCTIONS

Now that the MVME374 module is ready for installation, proceed as follows:

a. Turn all equipment power off.

CAUTION

INSERTING OR REMOVING MODULES WHILE POWER IS APPLIED COULD DAMAGE MODULE COMPONENTS.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

b. Set the jumpers that determine if the MVME374 is to be system controller. Refer to paragraph 2.3.2. If the MVME374 is system controller, pressing its front panel RESET switch resets the entire system.

c. Check the setting of the MVME374 base address. Refer to paragraph 2.3.6.

d. If the debug package 374Bug is to be used, check that the EPROM device size header J5 is set for 32K x 8 EPROMs. Refer to paragraph 2.3.3. Next check that the four debug EPROMs are installed in the correct sockets as U10 , U12, U34, and U35.

e. Check all other header jumpers for factory configuration.

f. Check backplane jumpers on the system chassis. Make sure that they are compatible with the jumpering of the MVME374 for bus grant and request.

g. The MVME374 module requires power from both P1 and P2. It may be installed in any double-height unused card slot, if it is not configured as system controller. If the MVME374 was jumpered as system controller in step b., it must be installed in the left-most card slot (slot 1) to correctly initiate the bus-grant daisy-chain and to have proper operation of the IACK daisy-chain driver.

h. Carefully slide the MVME374 module into the desired card slot in the system chassis. Be sure the module is seated properly into the connectors on the backplane. Fasten module in chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.

i. If the debug package 374Bug is to be used, connect the debug cable (customer-manufactured per Appendix A) to connector P2. This cable is not provided with the MVME374 module. Connect a debug terminal to the other end of the cable. Set up the terminal as follows:

   . eight bits per character
   . one stop bit per character
   . parity disabled (no parity)
   . 9600 baud to agree with default baud rate of MVME374 debug port at power-up.

j. Attach a transceiver (Ethernet) cable to the MVME374 front panel connector J1. This cable is not provided with the MVME374 module. Connect the rest of the cable to the rest of the Ethernet system.

k. Turn equipment power ON.

l. Check that the FAIL LED (red) is off and that the +12V LED (green) is on.

CHAPTER 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the information required to use the MVME374 in a system configuration.

3.2 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

3.3 INDICATORS AND CONTROLS

The MVME374 has FAIL and +12V indicators, front-panel RESET and ABORT switches, an asynchronous serial debug port through connector P2, and connections for an 802.3 (Ethernet) interface.

3.3.1 FAIL Indicator (DS1)

The red LED FAIL indicator is lit when any of the following conditions exist:

a. The MVME374 has just been reset and is conducting self tests.

b. The MVME374 has detected a failure of some portion of the self test.

c. The MVME374 is system controller and another VMEbus module is driving the VMEbus SYSFAIL*.

d. The user's application turns it on.

e. The MPU on the MVME374 has halted.

It should be noted that if the MVME374 is accessing the VMEbus while the host is accessing the MVME374's shared RAM, the FAIL indicator illuminates dimly. This is a normal occurrence; it does not mean that the board has failed.

3.3.2 +12V Indicator (DS2)

The green LED +12V indicator is lit whenever +12 Vdc fused power is supplied to the Ethernet front panel connector J1.

3.3.3 RESET and ABORT Switch Connections

The MVME374 provides front-panel RESET and ABORT switches (S2 and S1, respectively), but also provides for the connection of optional remote RESET and remote software ABORT switches through the P2 connector, if desired. The pinout of both optional remote switches is defined in Table 5-2. The connections at P2 can be made from a customer-supplied 64-pin flat ribbon cable connector to user-supplied momentary switches. Pressing either the onboard or the optional remote RESET switch causes a reset pulse to be applied to the onboard devices (and offboard devices if the MVME374 is system controller). Pressing either the onboard or the optional remote software ABORT switch causes a level 7, auto-vectored interrupt at the local MPU, if the interrupts are enabled. IF THE REMOTE ABORT CONNECTION IS USED, FRONT PANEL ABORT SWITCH S1 MUST BE REMOVED.

3.3.4 Asynchronous Serial Debug Port Connection

A debug terminal can be connected to a customer-supplied 64-pin flat ribbon cable at connector P2. The serial port is configured for terminal use only, and the baud clock is programmed to 9600 baud by the firmware shipped with the MVME374. For the pinout of the end of the debug port cable that connects to P2, refer to Table 5-2. The other end of the cable must have the standard DB-25 connections normally used for a reduced set of signals from RS-232C. Appendix A provides a parts location diagram and a parts list for the debug cable.

3.3.5 Ethernet Interface Connection

The MVME374 connects to an IEEE 802.3 transceiver through connector J1 on the front panel. It is a 15-pin (DB-15) connector on the MVME374 module in order to be pin-compatible with 802.3 specifications. The Ethernet signals on the pins of J1 are defined in Table 5-3.

Header J9 permits connecting the Ethernet signals to connector P2. Refer to Chapter 2 for details.

3.4 MEMORY MAP

The use of dual ported RAM and a VMEbus slave interface on the MVME374 requires an understanding of the local MC68020 memory map and the MVME374 memory map when viewed from the VMEbus.

3.4.1 Local MPU Memory Map

The memory mapped resources of the local MPU and their respective addresses are shown in Table 3-1. All registers, except VLSI (MC68901 and AM7990), are read/write.

TABLE 3-1. MVME374 Local MPU Memory Map

ADDRESS	EVEN BYTE	ODD BYTE
00000000	VMEbus ACCESS	
FFE00000	BUS ERROR	
FFE0FFFE		
FFE10000	AM7990 LANCE REGISTERS (NOTE 1)	
FFE1FFFE		
FFE20000	NOT USED	MC68901 MFP (NOTE 2) GPIP D7=ACFAIL* D6=RTS* (DEBUG PORT) D5=CMMND* (VME COMMAND) D4=SYSFAIL D3=CPU PARITY ERROR* D2=VMEbus ERROR* D1=ABORT* D0=SYSCON ENABLED
FFE20002	NOT USED	MFP AER
FFE20004	NOT USED	MFP DDR
FFE20006	NOT USED	MFP IERA
FFE20008	NOT USED	MFP IERB
FFE2000A	NOT USED	MFP IPRA
FFE2000C	NOT USED	MFP IPRB
FFE2000E	NOT USED	MFP ISRA

TABLE 3-1. MVME374 Local MPU Memory Map (cont'd)

ADDRESS	EVEN BYTE	ODD BYTE
FFE20010	NOT USED	MFP ISRB
FFE20012	NOT USED	MFP IMRA
FFE20014	NOT USED	MFP IMRB
FFE20016	NOT USED	MFP VR
FFE20018	NOT USED	MFP TACR
FFE2001A	NOT USED	MFP TBCR
FFE2001C	NOT USED	MFP TCDCR
FFE2001E	NOT USED	MFP TADR
FFE20020	NOT USED	MFP TBDR
FFE20022	NOT USED	MFP TCDR
FFE20024	NOT USED	MFP TDDR
FFE20026	NOT USED	MFP SCR
FFE20028	NOT USED	MFP UCR
FFE2002A	NOT USED	MFP RSR
FFE2002C	NOT USED	MFP TSR
FFE2002E	NOT USED	MFP UDR
FFE20030 – FFE3FFFE	NOT USED	MC68901 MFP REDUNDANT REGISTER SPACE
FFE40000 – FFE4FFFE	NOT USED / NVRAM, 256x4 D3-D0 ONLY	NOT USED
FFE50000 – FFE57FFE	CONTROL REGISTER 1 D7=FAIL D6=CTS* D5=STORE* (NVM) D4=NOVRUN D3=VMEINTEN* D2=WIP* D1=PARDIS* D0=INTEN*	NOT USED

TABLE 3-1. MVME374 Local MPU Memory Map (cont'd)

ADDRESS	EVEN BYTE	ODD BYTE
FFE58000	CONTROL REGISTER 2 D7-D6 NOT USED D5-D0=AM5-AM0 DURING VMEbus MASTERSHIP	NOT USED
FFE5FFFE		
FFE60000	VME IRQ LEVEL REGISTER D7=INTERRUPT ENABLE D6-D4=IRQ LEVEL (1-7) D3-D0 NOT USED	NOT USED
FFE67FFE		
FFE68000	NOT USED	IRQ VECTOR REGISTER D7-D0=VME IRQ VECTOR
FFE6FFFE		
FFE70000	NOT USED	NOT USED
FFE7FFFE		
FFE80000	EPROM/EEPROM SOCKETS (LWORD)	
FFEFFFFE		
FFF00000	RAM (MPU AND LANCE ONLY; NO VME ACCESS ALLOWED)	
FFF0007E		
FFF00080	RAM (SHARED BY MPU, LANCE, AND VME)	
FFFFFF7E		
FFFFFF80	RAM (SHARED BY ALL; WRITES FROM VME INTERRUPT THROUGH MC68901 I/O5 PIN (CMMND*))	
FFFFFFFE		

NOTES: (1) Refer to the AM7990 LANCE manual.
(2) Refer to the MC68901 MFP manual.

3.4.2 Register Definitions

This section provides bit definition details for various MVME374 registers.

AM7990 LOCAL AREA NETWORK CONTROLLER (LANCE) $FFE10000

Refer to the AM7990 manual for functional details.

MC68901 MULTI-FUNCTION PERIPHERAL (MFP) $FFE20000

The General Purpose I/O Register (GPIP) on the MC68901 is configured as all inputs. The following are the pin definitions, with comments on whether the bits are used in the edge sensitive or level sensitive mode. Refer to the MC68901 manual for additional functional details.

D7 - VME ACFAIL*.	This input is used as a low-level sensitive interrupt initiating source. It is cleared by the VMEbus ACFAIL* signal.
D6 - RTS*.	Low-level or edge sensitive indication (to serial communications facilities in the firmware) that the RTS* signal from the debug port has been received.
D5 - CMMND*.	This line pulses low when the uppermost 128 bytes of VME shared memory (interrupting RAM) is written to. It is used as a falling edge sensitive interrupt initiator which indicates to module firmware that data is available in the shared RAM.
D4 - VME SYSFAIL.	High-true level or edge sensitive. The VMEbus SYSFAIL signal clears this bit thereby initiating an interrupt.
D3 - CPU Parity Error* (PERR*).	Falling edge sensitive. This bit is cleared when a parity error occurs and this level is used by firmware to notify the MPU of this condition.
D2 - VMEbus ERROR*.	Pulses low when the MVME374 receives a VMEbus ERROR* signal. Falling edge sensitive interrupt initiator.
D1 - ABORT*.	Falling edge sensitive interrupt initiator. With D3 and D2, it determines the source of a level 7 auto-vectored interrupt (refer to paragraph 3.4.5). It pulses low as a result of the ABORT* signal.
D0 - SYSCON enabled.	Level sensitive. This bit is set high if the MVME374 is configured as system controller.

CONTROL REGISTER 1 (CR1) **$FFE50000**

This register controls individual signals on the MVME374. On reset, the contents of this register are set to $FF.

D7 controls the FAIL signal; when high, the FAIL light is illuminated and (if bit 1 in the SYSFAIL Control/Status Register is set) the SYSFAIL* signal is activated on the VMEbus.

D6 controls the CTS signal on the serial debug port. When low, CTS is activated.

D5 controls the STORE* line to the NVRAM. This bit should be cleared, then set, whenever the static RAM portion of the NVRAM is to be stored in the EEPROM portion. The NVRAM should not be accessed for 10 ms after the store line is activated and then deactivated.

D4, when high, causes a VME cycle to be gracefully aborted whenever the LANCE needs the local bus (refer to Chapter 4). This bit should be kept high, except when reading or writing to slow I/O devices over the VMEbus (e.g., serial chips and IPC control registers).

D3, when low, allows handling of VMEbus interrupts on IRQ3*. When high, the state of IRQ3* is ignored.

D2, when high, causes RAM parity to be written and read as odd parity. When low, parity is even.

D1 disables parity when low.

D0 enables all interrupts when low.

CONTROL REGISTER 2 (CR2) **$FFE58000**

Control Register 2 allows the selection of address modifier used when the MVME374 is VMEbus master. Bits D7 and D6 are not used; D5-D0 correspond to AM5-AM0. This register is undefined after reset. Generally, the address modifier is set to either $3D (A24 standard supervisor data) or $0D (A32 extended supervisor data).

VME IRQ LEVEL REGISTER (IRQLEV) **$FFE60000**

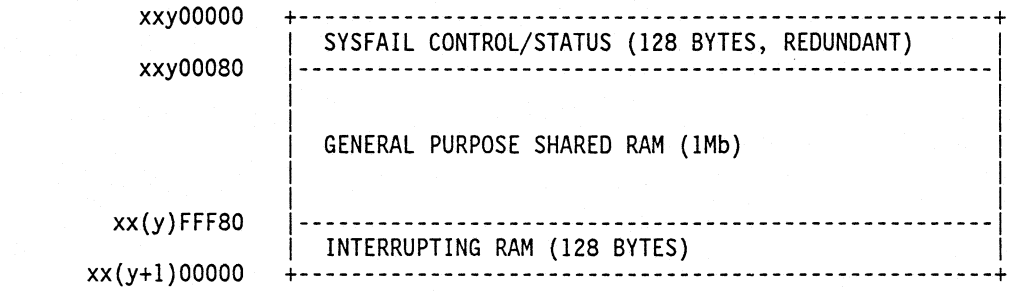
A value written by a local resource into the even byte (only) of this register (redundant through $FFE67FFE) is used to initiate a VMEbus interrupt request and to select the level of the request. On system reset, this register is cleared. D7 enables interrupt when high. D6-D4 select the interrupt level (1-7 correspond to IRQ1*-IRQ7*). When the interrupt has been acknowledged, D7-D4 are cleared automatically. D3-D0 are not used.

IRQ VECTOR REGISTER (IRQVECT) **$FFE68001**

Prior to causing an MVME374 interrupt of the VMEbus by writing a value into the IRQ Level Register, the MPU writes an 8-bit acknowledge vector into the odd byte at $FFE68001 - the IRQ Vector Register. The contents of this register (all 8 bits) are used as the Interrupt Acknowledge vector for a VMEbus interrupt (given by writing to the IRQ Level Register). After an Interrupt Acknowledge, the contents of the IRQ Vector Register have not changed. Following a reset of the module, register contents are undefined.

3.4.3 VMEbus Memory Map

The base address of the MVME374 is hardware programmable by jumper selection on J7 as defined in paragraph 2.3.6. The MVME374 appears as 1Mb, with a 128 byte redundantly mapped register (for application programs and general diagnostic use), and with a 128 byte space that causes an interrupt of the local MPU when written to from the VMEbus. The VMEbus memory map of the MVME374 is shown below.



NOTE: xxy is the value of the jumpers on the Slave Base Address Header J7.

3.4.4 SYSFAIL Control/Status Register Definition (Odd Bytes Only)

This register is read and written from the VMEbus. Even bytes are undefined; odd bytes are all identical.

D7-D4 are not defined.

D3 (write only) is set to one from the VMEbus to reset the MVME374. The bit is automatically cleared after the MVME374 resets.

D2 (read only) is set high by the MVME374 when the VMEbus HALT* line is driven low.

D1 (read/write) is cleared (set to zero) to disable the MVME374 from driving SYSFAIL. At power on and system reset, this bit is set to one.

D0 (read only) reflects the status of the FAIL LED (low = FAIL on).

3.4.5 Local Processor Interrupt Sources

The following is a description of all the interrupt sources the MPU can receive. Interrupts are disabled after reset until the interrupt enable bit in Control Register 1 is cleared.

Level 7 - Auto-vectored

CPU parity error. If parity is enabled and the CPU reads an onboard memory location that is detected to have bad parity, a level 7 interrupt is generated. A parity error causes bit D3 in the MFP GPIO port to toggle, which can be seen in the Interrupt Pending Register (if the MFP is initialized properly).

Abort. Pressing an ABORT switch causes a level 7 interrupt. An abort interrupt causes bit D1 in the MFP GPIO port to toggle, which can be seen in the Interrupt Pending Register (if the MFP is initialized properly).

VMEbus error. Any bus error the MPU receives also causes a level 7 interrupt. This ensures no task switching occurs before the bus error is completely handled. A VMEbus error causes bit D2 in the MFP GPIO port to toggle, which can be seen in the Interrupt Pending Register (if the MFP is initialized properly).

Local bus time-out. A bus error is generated whenever accessing non-existent memory on the local map. This also causes a level 7 interrupt. A local bus time-out can be deduced as a source of bus error (and level 7 interrupt) because the other three sources or level 7 interrupts are not detected.

Level 6 - No interrupt.

Level 5 - MC68901 Multi-Function Peripheral (MFP)

The MC68901 is the only source of level 5 interrupt. The vector can be programmed directly in the MC68901. Consult the MC68901 manual for more details.

Level 4 - AM7990 Local Area Network Controller (LANCE)

The AM7990 is the only source of level 4 interrupt. The level 4 interrupt is handled through the level 4 auto vector. The AM7990 does not provide a vector.

Level 3 - VME Interrupt IRQ3*

This interrupt is provided for stand-alone operation, and operates in accordance with the VMEbus specification. This interrupt is disabled when the VMEINTEN* bit in Control Register 1 is set to 1.

Level 2 - No interrupt.

Level 1 - No interrupt.

CHAPTER 4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides an overall block diagram level description of the MVME374 module. The general description provides an overview of the MVME374 module, followed by a detailed description of each block diagram section. A block diagram of the MVME374 Multi-Protocol Ethernet Interface Module is shown in Figure 4-1.

4.2 GENERAL DESCRIPTION

The MVME374 is a peripheral controller module that utilizes the MC68020 MPU and 32-bit RAM and EPROM to enhance the capability of the module to quickly execute the software required to implement the Technical Office Protocol (TOP) or other communication protocols. In general, the MPU fetches and executes user programs from RAM or EPROM in support of the message packets that are passed to and from the AM7990 Local Area Network Controller (LANCE) chip. The MVME374 VMEbus interface provides a shared RAM area, a VMEbus requester, the ability to generate and receive interrupts to/from the VMEbus, and a limited VMEbus system controller option. The MVME374 also includes Status and Control registers and a Non-Volatile RAM (NVRAM) that is used to hold information which is specific to each module such as the network station address. Front panel switches provide for a local RESET function and a software ABORT function. A serial debug terminal port is also provided through the P2 connector of the MVME374 module. This port is configured for use with a terminal only (DCE). The baud rate clock is set to 9600 baud by the onboard firmware. The optional serial port is normally used for debugging.

4.3 BLOCK DIAGRAM DESCRIPTION

The MVME374 operates through the following functional blocks:

- MPU
- LANCE and SIA
- EPROM/EEPROM
- RAM
- Local bus arbiter
- VMEbus DTB interface
- VMEbus requester
- System controller
- VMEbus interrupter
- Interrupt handler
- Multi-function peripheral
- Non-volatile RAM
- Reset circuitry

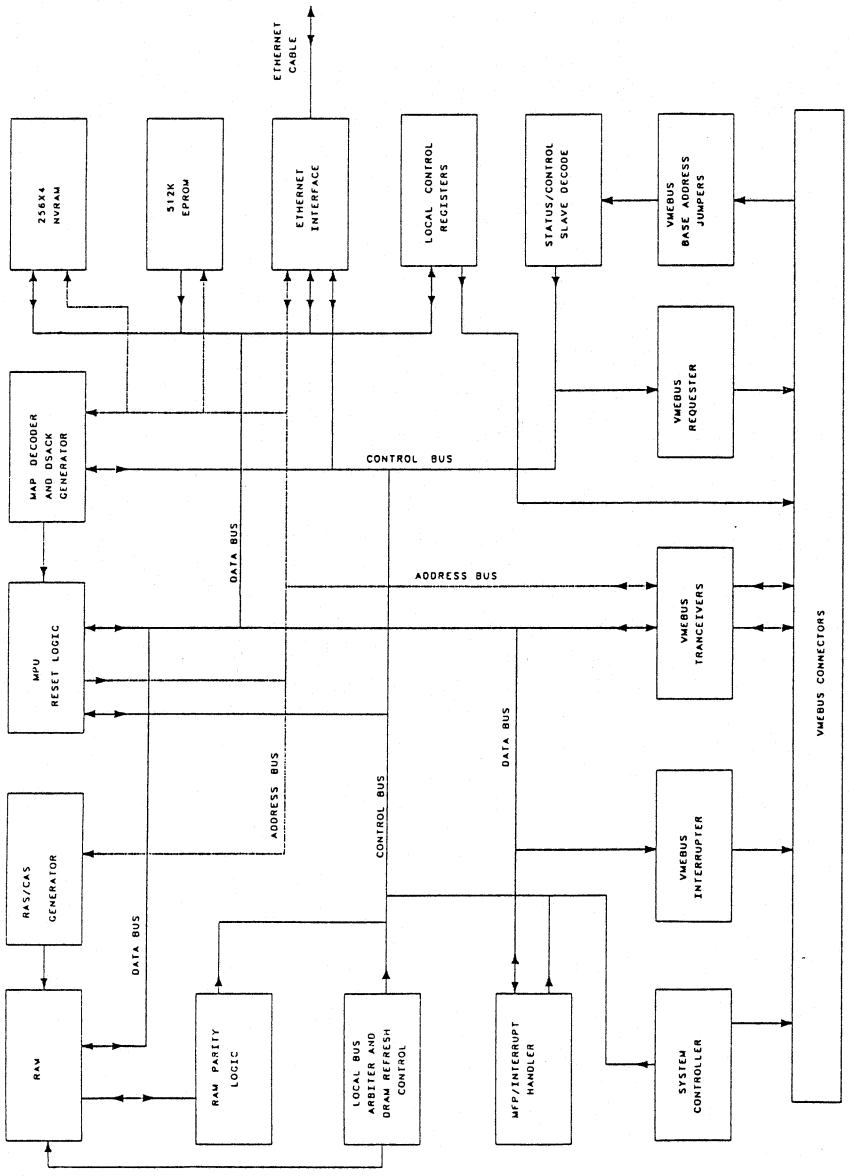


FIGURE 4-1. MVME374 Block Diagram

4.3.1 MPU

The 32-bit MC68020 MPU is used on the MVME374 to take advantage of its improved instruction execution cycle, internal cache memory, and low power consumption. The MC68020 is the first device within the MC68000 family providing external 32-bit address and data paths, and has higher clock rates, advanced architecture, enhanced addressing modes, and an onchip instruction cache. Its 32-bit data and address architecture equip the MC68020 for application in the asynchronous, non-multiplexed VMEbus environment, and it has the power required for a protocol processor/Ethernet interface design.

The MPU and its associated circuitry are optimized to operate at a fixed frequency of 16.0 MHz. A 32 MHz clock is used to generate 16.0 MHz and other clocks for board level timing. Most instructions that the MPU executes appear as read or write cycles to the MVME374 hardware.

A few instructions are exceptions to this general rule. The first exception is the Read-Modify-Write (RMW) type instructions (e.g., TAS, CAS, CAS2). To support the various addressing modes and to provide the uninterruptable bus cycles for these instructions, the VMEbus is requested at the beginning of the RMW instruction, and bus mastership must be received before the instruction can proceed. RMW-type instructions should not be confused with divisible instructions such as CLR, BCLR, and BSET, which also read, modify, and rewrite a memory value.

NOTE

A TAS instruction to MVME374 shared memory must be cleared by using a CAS.B instruction.

All types of MC68020 TAS or CAS multibyte indivisible instructions are allowed as long as all addresses are onboard. Normal VMEbus restrictions apply for offboard accesses. These restrictions are that only single byte indivisible instructions (where AS* can be held low on the VMEbus) are truly indivisible across the bus. The same restrictions apply for VMEbus accesses to MVME374 shared memory.

The next exception is the STOP instruction. Since none of the MVME374 hardware uses the address or data strobes for clocking purposes, the STOP instruction is fully supported.

Another instruction is the MOVES instruction. This instruction has no effect on VMEbus cycles, since the address modifiers for VMEbus cycles come from the Address Modifier Register. If the address modifiers from a MOVES instruction indicate a CPU space cycle, a bus error results, because the only supported CPU space cycle is the Interrupt Acknowledge cycle.

Finally, any instruction (e.g., coprocessor, breakpoint) that generates CPU space cycles are terminated with a bus error after a 40 microsecond time-out. These instructions have a limited usefulness because the MVME374 does not have a local coprocessor.

4.3.2 LANCE and SIA

The AM7990 LANCE is a 48-pin DIP package operating at 10.0 MHz (provided by a separate 40 MHz oscillator, and asynchronous to the MC68020). The LANCE has a D16 peripheral interface and a D16:A24 master interface. Because the LANCE has a 16-bit data bus, latches are required to connect to the internal 32-bit memory. (The VMEbus also comes in by this same 16-bit data path.) The LANCE is restricted to doing data transfers to and from local RAM to prevent problems with data over/underrun errors, due to VMEbus activity.

The LANCE requests the local bus when it has between 2 and 8 words to transfer and is normally given the local bus after the current bus cycle is complete. If the current bus cycle is an access of the VMEbus, a retry (or bus error for RMC cycles) is forced, after 40 usec. A retry or bus error causes the local bus to be arbitrated to the LANCE before the next MPU cycle can occur. If the MPU is current VMEbus master, when the LANCE bus request occurs, the cycle is given 60 usec to finish. If the cycle is not finished in 60 usec, the current address, data, and strobes are latched on the VMEbus until a DTACK or BERR signal is received. This provides the LANCE the highest priority, and orderly access to the local memory.

The LANCE has no bus error input, and when it is the bus master does not release the bus until a 25 usec time-out when a bus fault occurs. This does not occur in normal operation, and is considered a catastrophic condition.

The AM7990 LANCE implements the IEEE 802.3 Media Access Control (MAC) sublayer protocol. It uses a powerful shared memory structure to provide the full set of MAC services as well as network monitoring and diagnostics aids. It also includes an intelligent DMA function and a 48-byte FIFO to support the MAC protocol at data rates up to 10Mbits/sec.

The AM7992B Serial Interface Adapter (SIA) interfaces the AM7990 to the off-board Ethernet transceiver. It is a 24-pin DIP VLSI chip implementation compliant with IEEE 802.3 which provides Manchester encoded data to the Ethernet and digital data to the LANCE chip. The crystal-controlled device acquires clock and data, encodes/decodes Manchester data, and uses signal-threshold limiting circuitry and transient noise-suppression circuitry in both data and collision paths to minimize false start conditions.

4.3.3 EPROM/EEPROM

Four 32-pin sockets accommodate 8K x 8, 16K x 8, 32K x 8, 64K x 8, or 128K x 8 EPROM. No mixing of device sizes is allowed, because the sockets are organized as longword-wide (32-bit) memory.

NOTE

Programmed code must be split into fourths before programming.

After reset, the first eight bytes accessed by the MPU are at locations $00000000-$00000007. The EPROM is mapped everywhere during these first two longword fetches, after which the normal memory map is restored. The first eight bytes of EPROM must contain the reset Program Counter and Interrupt Stack Pointer values.

4.3.3.1 EEPROM and Programming Consideration

EEPROM, 8K x 8 or 32K x 8, can be used in place of EPROM. EEPROM with a separate, totem pole output, status pin must have that pin lifted from the device socket. Any writes to EEPROM must be done as longword-aligned transfers only, and software must allow for the wait time between EEPROM cycles, because there is no status bit. It is suggested that the EEPROM be initially programmed in a PROM programmer (because locations $FFE80000-$FFE80007 are for reset vectors).

NOTE

The instructions used to program the EEPROM cannot be executed from the EEPROM.

4.3.4 RAM

The MVME374 has 1Mb of local shared RAM. There are eight 256K x 4 (1 megabit) DRAM chips to provide longword-wide memory and four 256K x 1 RAM chips to provide parity.

The uppermost 128 bytes of the RAM space is used as the command interrupt area from the VMEbus. Any access from the LANCE or MPU does not cause an interrupt. A write to this RAM space from the VMEbus causes a command interrupt to the processor; a read does not. The command interrupt is handled by the Multi-Function Peripheral (MFP).

Parity is accomplished by using four parity generators/checkers and four 256K x 1 DRAM chips.

DRAM speed is 100ns. RAM cycle time is four clock cycles (one wait cycle) for the MPU and one wait cycle for the LANCE.

4.3.5 Local Bus Arbiter

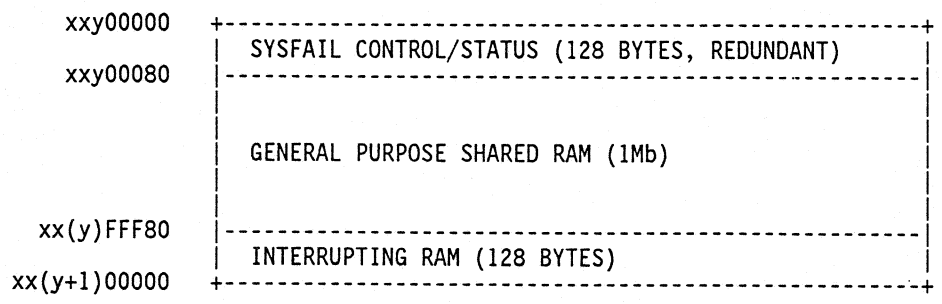
The local bus is arbitrated on a priority basis in the following order: LANCE has highest priority, RAM refresh circuitry has second highest priority, VME access is third highest priority, and the CPU has lowest priority. When a local bus request is given by the LANCE, VME, or refresh circuitry, the bus is arbitrated at the end of the current bus cycle. When the RAM refresh count reaches a critical level (three counts before the RAM refresh counter reaches the upper limit), a local bus time-out is generated, causing a retry. If the CPU is performing a VMEbus cycle, the cycle is terminated locally; while, on the VMEbus, AS*, DS0*, DS1*, Wt*, and the VMEbus address lines are latched until a DTACK* or BERR* is received.

4.3.6 VMEbus DTB Interface

The following paragraphs provide information on the Data Transfer Bus interface.

4.3.6.1 VMEbus Slave Interface

The MVME374 slave interface includes 1Mb of shared RAM with a SYSFAIL Control/Status area overlaid on the lower 128 addresses. As shown below, the slave interface can be described as three areas: SYSFAIL Control/Status, general purpose RAM, and Interrupting RAM. The VMEbus memory location of the slave interface is controlled by the Slave Base Address Header J7 as shown below:



NOTE: xxy is the value of the jumpers on the Slave Base Address Header J7. Refer to header descriptions in Chapter 2 for more information.

4.3.6.2 Interrupting RAM Area

The Interrupting RAM area is the last 128 bytes of the general purpose RAM that is specially decoded such that a write to this area, from the VMEbus, generates a level 5 interrupt to the local processor. A read of this area has no effect on the local processor interrupts. This allows other VMEbus masters (without interrupt generation capability) to interrupt the local processor. Reads or writes by the local processor also have no effect on the interrupts.

4.3.6.3 Shared RAM

Shared RAM space of 1Mb is provided to allow data to be passed directly between the host and the MVME374.

A VME host is given the local bus of the MVME374 when addressing the proper region, and when the processor has finished the cycle (or cycles, if RMC is activated), and when the refresh controller and the Local Area Network chip are not requesting or using the bus. For worst case timing (assuming 100ns RAM cycles), it could take the MC68020 0.48 us to finish a bus cycle (CAS2.L = four longwords to word-wide memory is not a valid cycle because the VMEbus has to be owned to perform this; so, a generic bus cycle is assumed), with the LANCE taking 5.4 us (8 bus cycles), and the refresh circuitry needing it for 1 us (2 refreshes), it then gets the bus for one cycle (.5 us). Therefore, it can take 6.9 us from Data Strobe being activated until DTACK* is activated, for a dual port cycle. A typical VME access to shared RAM takes about 0.75 us.

NOTE

Shared RAM allows data accesses only (supervisor or user). Any program accesses generate a global bus time-out.

4.3.6.4 SYSFAIL Control Register

This is a write-only register which uses data bit D1 to enable or disable the activation of SYSFAIL* on the VMEbus. The default condition is with SYSFAIL* enabled. This register allows the host to detect a failed board, logically remove it from the system, and possibly continue with reduced functionality, if other system modules are still functional. Data bit D3 is used to cause a reset of the MVME374 when a one is written to this bit. The bit is cleared automatically after reset. Note that if the MVME374 is system controller, the entire system gets reset. This register is a real hardware register and not a shared RAM location.

NOTE

The SYSFAIL Control/Status Register is not accessible by the local processor.

4.3.6.5 SYSFAIL Status Register

This is a read-only register which contains the state of the MVME374 internal SYSFAIL* line in D0, and the state of the SYSFAIL* enable bit from the write-only register in D1. D1 mirrors D1 on the control side. D2 shows the status of the processor HALT line (1 = HALT true, 0 = HALT false).

Both SYSFAIL Control and Status registers are redundant over 128 bytes of shared memory space (VME to shared memory only), odd byte only.

4.3.6.6 Master Interface

The MVME374 has either an A32:D16/8 or A24:D16/8 IPC-type master interface.

CAUTION

CAUTION MUST BE USED WHEN ATTEMPTING TO IMPLEMENT THE MVME374 AS A GENERIC CPU MODULE. THE ADDRESS MODIFIER CODES ACTIVATED ON THE VMEbus ARE NOT A FUNCTION OF THE MPU CODES BUT ARE CONTROLLED BY THE CONTENTS OF CONTROL REGISTER 2. THE MOVES INSTRUCTION HAS NO EFFECT ON THE ADDRESS MODIFIERS FOR A VMEbus CYCLE. ADDITIONALLY, THE GRACEFUL VMEbus CYCLE ABORT CAPABILITY OF THE MVME374 MAY CAUSE STATUS INFORMATION FROM A READ ONLY REGISTER (THAT IS CLEARED UPON READING) TO BE LOST WHEN THE VMEbus CYCLE TAKES TOO LONG AND IS RETRIED BY THE LOCAL MVME374 CPU. PROGRAM CODE SHOULD BE DOWNLOADED INTO THE LOCAL MEMORY FOR EXECUTION. THE ONBOARD MEMORY IS IN THE UPPER TWO MEGABYTES OF THE MC68020 ADDRESS SPACE, TO ALLOW THE REST OF THE MEMORY SPACE TO BE USED FOR VME ADDRESSING.

If the onboard processor is in the middle of a VMEbus cycle (with AS* and data strobes activated to the VMEbus), and it becomes critical for the LANCE to have the local bus, a graceful exit from the VMEbus cycle is necessary. In order not to violate bus specifications, when a VMEbus cycle is initiated, all address lines, address modifiers, address strobe, write, and any activated data strobes are latched until either a DTACK* or BERR* is received. Once address and data strobes are latched, the local processor cycle can be terminated with a retry and the bus arbitrated to the LANCE.

4.3.7 VMEbus Requester

The VMEbus requester operates in a Release on Local Bus Access mode. This means that the VMEbus is held until the MC68020 makes a local bus access or gives the local bus to the LANCE or refresh circuitry. Detecting a program code fetch from the MC68020 is accomplished by tying DRIVEN* (VME strobe drive enable) to cache disable. This eliminates worrying about a cache hit, and ensures that after a VMEbus access, an onboard access is performed. Ideally, this would allow a MOVEM.L of all internal registers without giving up the bus, but the refresh circuitry requests the local bus every 20 us, giving a maximum time for VMEbus ownership of 20 us (assuming bus DTACK* is being regularly received). Specifying the number of MPU registers which are moved to VME memory during a MOVEM instruction also specifies the maximum number of VMEbus cycles that the MVME374 executes prior to releasing bus mastership. This function eliminates the problem of trying to pick a single value for the maximum number of bus cycles to be executed that satisfies all applications. Although a MOVEM.L instruction can move up to 32 words, moves to the VMEbus should be limited to 8 words at a time. This 8 word limit prevents the MVME374 from monopolizing the VMEbus in a system with multiple bus masters.

4.3.8 System Controller

The MVME374 has a partial VMEbus system controller in order to reduce the number of modules in minimal system configurations. SYSRESET driver, SYSFAIL monitoring and indicating, level 3 VMEbus single level arbiter, a 77 us VMEbus time-out generator, and the 16 MHz SYSCLK are all supported.

4.3.9 VMEbus Interrupter

The MVME374 provides a programmable VMEbus compatible interrupt level and a programmable Interrupt Acknowledge vector. When the MVME374 needs to generate a bus interrupt, the local MPU writes the vector into the IRQ Vector Register and then writes the interrupt level into the IRQ Level Register; this causes the bus interrupt. After the interrupt is acknowledged, the contents of the Interrupter Register are automatically cleared, and the bus interrupt is removed. The VME Vector Register remains unchanged until the contents are re-written by the local MPU.

NOTE

USING THE INTERRUPTER TO INTERRUPT THE MPU AT LEVEL 3 (USING IRQ3* INTERRUPT) CAUSES A SPURIOUS INTERRUPT EXCEPTION.

4.3.10 Interrupt Handler

The Interrupt Handler receives interrupts from six sources. The first source is the AM7990 LANCE which generates an autovectored level 4 interrupt. The second is the MC68901 MFP (level 5), which provides a programmable Interrupt Acknowledge vector. The third, fourth, and fifth sources are autovectored at level 7 and are generated by the ABORT switch, a CPU bus error, or the DRAM parity error generator during a CPU cycle. The sixth source is VME IRQ3* (level 3), providing minimal VMEbus interrupt handling capability, as long as VMEINTEN is activated in CR1. The MFP receives inputs from various sources and provides both priority encoding and a programmable Interrupt Acknowledge vector. Sources of MFP interrupts are:

- VME command
- Tick timers
- Debug port transmitter
- Debug port receiver
- Debug port error condition
- RTS from debug port
- SYSFAIL

The Interrupt Handler checks address line A19, along with the function codes, to determine if an Interrupt Acknowledge cycle is starting. Interrupt Acknowledge is a subset of CPU space, along with Coprocessor Communication, Access Level Control, and Breakpoint Acknowledge. A19-A16 are used to differentiate between these CPU space cycles. Of all currently defined CPU space cycles, Interrupt Acknowledge is the only cycle that sets A19 = 1. All other CPU space cycles set A19 = 0.

NOTE: The MVME374 cannot interrupt itself by using the VMEbus interrupt at IRQ3* (level 3). It generates a spurious interrupt.

4.3.11 Multi-Function Peripheral (MFP)

Four onboard timers are provided through the MC68901 MFP. All timers run from a common clock but can each cause a separate interrupt and pass a unique Interrupt Acknowledge vector. For detailed information, refer to the MC68901 data sheet. The timers are assigned as follows:

Timer A - Watchdog counter, software tick timer (input can be Timer B out)
Timer B - Software tick timer (input can be Timer C out)
Timer C - Software tick timer
Timer D - Baud rate generator for the debug port

4.3.11.1 Tick Timer

Timers C and B are independently programmable general purpose delay counters. All timers share the same XTAL input clock frequency and can provide delays from 3.25 us to 41.6 ms as shown in Table 4-1.

TABLE 4-1. Tick Timer Time Delay (XTAL Frequency = 1.231 MHz)

TIMER PRESCALE COUNT	TIMER COUNT	TIME TIME DELAY = (PRESCALE) x (COUNT) x (1/XTAL FREQ)
4	01	3.25 us
10	01	8.125 us (minimum count: $01 = 1)
16	01	13.0 us
50	01	40.625 us
64	01	52.0 us
100	01	81.25 us
200	01	162.5 us
200	00	41.6 ms (maximum count: $00 = 256)

Timer B can be used in the event count mode to be cascaded off of Timer C's output. Use the following equation to calculate Timer B's interval when cascaded:

Timer B Interval = 2 x (count) x (Timer C Interval)

Timer A is used as the watchdog timer and can be used in the delay mode, or in the event count mode with Timer B's output connected to Timer A's input. In the event count mode, if Timer B is programmed, in delay mode, with a prescale = 200 and a count value = 00, the watchdog time-out value is approximately 21.3 seconds. The watchdog time is calculated as follows:

Time-out = 2 x (count) x (Timer B Interval)

If the watchdog timer is not initialized, it does not generate a reset.

The MFP has an 8-bit General Purpose Input Register (GPIO) which can be the source of a local MPU interrupt when programmed as an interrupt input or used merely as a Status Register when interrupts are disabled. On the MVME374, all I/O pins are used as inputs. The functional pinout of the GPIO Register is as follows:

D0 - System Controller enabled (high true)
D1 - Abort (low true)
D2 - VMEbus Error (low true)
D3 - CPU Parity Error (low true)
D4 - SYSFAIL (high true)
D5 - VME Command (Interrupt, low true)
D6 - Debug Port RTS (Interrupt, low true)
D7 - ACFAIL (Interrupt, low true)

4.3.11.2 Baud Rate Timer

The XTAL input to the timer is the MPU clock divided by thirteen (1.231 MHz). (The onboard firmware sets the baud rate to 9600 baud, but it may be changed by programming the MC68901 MFP.) The baud rates supported by the baud rate timer are given in Table 4-2.

TABLE 4-2. Baud Rates Supported by Timer (XTAL = 1.231 MHz)

BAUD RATE (NOTE)	NOMINAL FREQUENCY	TIMER D PRESCALE	TIMER D COUNT	ACTUAL FREQUENCY	% ERROR
9600	153600	4	1	153846	0.16
4800	76800	4	2	76921	0.16
2400	38400	4	4	38462	0.16
1200	19200	4	8	19231	0.16
600	9600	4	16	9615	0.16
300	4800	4	32	4807	0.15
150	2400	4	64	2404	0.16

NOTE: Baud Rate = Nominal Frequency / 16.

4.3.11.3 Debug Port

The MVME374 has only a partial RS-232C implementation. No facility is provided to connect it to a modem. As wired, it provides permanently true Data Set Ready (DSR), Data Carrier Detect (DCD) signals, and a programmable Clear To Send (CTS) signal. This allows the module to tell the terminal when it is ready to transmit data. The MVME374 can also detect the state of the Request To Send (RTS) signal. All of the debug port signals are routed through the P2 connector. A ribbon cable with a DB-25 connector on one end and a DIN 64-pin connector on the other can be manufactured by the customer for those who require a local debug port during their product development phase. Refer to Appendix A for details.

4.3.12 NVRAM

The party line nature of Ethernet requires an entity interfacing the cable to have a unique identity so that it can retrieve its messages from the cable traffic. This is satisfied through the use of a Station Address value, a concept somewhat analogous to a bus address. An individual MVME374, when manufactured, is assigned a unique 48-bit Station Address value which is stored, with an 8-bit checksum, in NVRAM for use by module firmware. When the node using that module is connected to the network, the module's Station Address is made known to network software and the node is identified that way from then on. The address is also on a label on the module front panel. (Refer to Table 5-4.)

There are 256 x 4 bits of NVRAM included for storing the Station Address and any other variables that would need to be saved when power is off. This is provided by an NCR52212 in conjunction with an ICL8211 power-down protection circuit. The NVRAM is an EEPROM with an overlayed static RAM. During normal reads and writes, the static RAM is accessed, speeding up the access time. In order to save the contents of the RAM, the STORE line is activated, making an image of the RAM in the EEPROM. When the RECALL line is activated at power up, an image of the EEPROM is placed in the RAM. The life of the EEPROM is 10,000 STORE cycles, and each STORE operation ties up the chip for 10 ms. Therefore, the STORE operation should only be done when necessary. A bit in Control Register 1 controls the STORE line.

4.3.12.1 Saving Data in Non-Volatile Memory (NVM)

Since the NVM cannot be accessed for 10 ms after STORE has been activated, the best way to prevent misuse of this function is to use the routines in the boot EPROM in order to store or recall the data. Because the NVM contains checksums to assure validity of data, these routines are also used to generate the checksums.

The MVME374Bug has TRAP #15 interfaces to transfer data to and from the NVRAM. Consult the MVME374Bug manual for more information.

4.3.12.2 Modifying NVRAM Fields

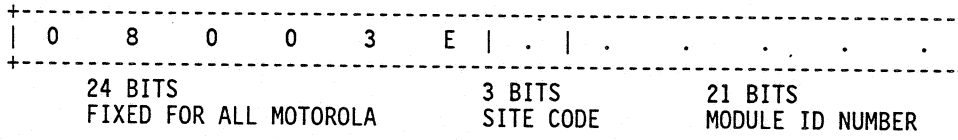
The NVRAM fields can be updated one of two ways. The first is by using the NVRAM Editor program that interacts with the local debug port. The second method is using the NVRAM editor that communicates across the VMEbus to the host console. The editor is a menu-driven program that is documented in the MicroTOP software documentation.

NOTE

Early versions of the NVRAM editor allocate fields by names that are not used on the MVME374. DO NOT change NVRAM parameters without first checking that the field does not have an alternate use. The station field address should always match the number on the station address label attached to the front panel of the module.

4.3.12.3 Ethernet Station Address Fields

The Ethernet station address uniquely identifies the individual module as being from Motorola MCD and also contains a unique network address. The format of the station address is as follows:



4.3.12.4 Power Up and Power Down Considerations

One of the primary trouble spots in non-volatile circuitry is protection from "false writes" during power up and power down. On the MVME374, an ICL8211 is used to detect when power is below an acceptable level (approximately 4.7 Vdc), and to activate the RECALL line on the NVM, which prevents changing of data during power down or power up.

4.3.12.5 Ensuring Validity of Data

Default values are stored in the boot EPROM for all parameters in the NVRAM. During power up, a checksum calculation is performed on each parameter in the NVRAM. (A 4-bit checksum for each parameter is generated each time the STORE routine is invoked.) If a checksum fails, the SYSFAIL line is not deactivated, and the FAIL LED is turned on. The default value in EPROM is loaded into NVRAM. In this way, whenever a value in NVRAM is corrupted (e.g., activating the STORE line accidentally without generating the checksum), known values are used. This also is useful when powering up the module for the first time. An 8-bit checksum, generated by adding byte-wide values in EPROM, is also generated by the STORE routine, to further ensure the values in the NVRAM. An illustration of the NVRAM memory map is shown in Figure 4-2.

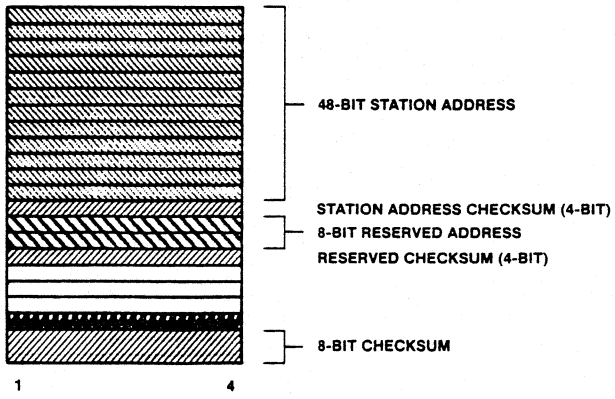


FIGURE 4-2. NVRAM Memory Map

4.3.12.6 Values Reserved in NVRAM

Refer to the MicroTOP documentation for a memory map of reserved NVRAM locations.

4.3.13 Reset Circuitry

There are five sources of CPU reset: power-up, watchdog time-out, debug RESET switch, a host CPU write to bit D3 of the SYSFAIL Control Register, or system reset. When reset occurs, Control Register 1 is set to a known state.

When the MPU executes a reset instruction, all registers and peripheral chips on the MVME374 are reset; however, a VMEbus system reset does not occur, even if the MVME374 is system controller.

4.3.14 User Interface

Motorola has developed software, called the common environment, that provides a standard means of communicating with other host processor and communications modules on the VMEbus. The MVME374 is shipped with installed common environment and debugger firmware in the four onboard EPROMs.

The common environment firmware provides the user with the capabilities of downloading software, inter-task communication, local and global resource control, and access to a real-time operating system. The inter-task feature allows MVME374 tasks to communicate with other MVME374 tasks as well as communicate with host or other offboard tasks. Local and global resource control provides buffer pool management and message passing across the VMEbus. In addition, the common environment uses the fully debugged, application proven operating system, VRTX. VRTX is supplied under license from Ready Systems, Inc., and is one of the industry's standard real-time kernels.

CHAPTER 5 - SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides interconnection signals, a parts list with parts location illustration, and schematic diagrams for the MVME374.

5.2 INTERCONNECT SIGNALS

The MVME374 interconnects with the VMEbus through connectors P1 and P2, with a debug port through P2, and with an Ethernet interface through J1 (and optionally also through P2).

5.2.1 MVME374 Connector P1 Interconnect Signals

Connector P1 is a standard DIN 41612 triple row, 96 pin male connector. All Motorola VMEbus specifications are met by the MVME374. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-1.

TABLE 5-1. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA bus (bits 0-7) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - a 16 MHz clock signal. This signal is provided by the VMEbus system controller.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - signal driven by VMEbus master that indicates a data transfer on data bus lines D08-D15.
A13	DS0*	DATA STROBE 0 - signal driven by VMEbus master that indicates a data transfer on data bus lines D00-D07.
A14	WRITE*	WRITE - signal driven by VMEbus master that specifies the direction of data transfers.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - signal driven by VMEbus slave that indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - the falling edge of this signal, driven by VMEbus master, indicates a valid address is present on the address bus.
A19	GND	GROUND
A20	IACK*	INTERRUPT ACKNOWLEDGE - signal driven by the VMEbus master that indicates a VME interrupt acknowledge cycle. A VME master has been interrupted on one of seven levels and is now acknowledging the specific interrupt with a service routine.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The IACKIN* signal is connected directly to IACKOUT*.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The IACKOUT* signal is connected directly to IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - one of the three-state lines driven by VMEbus master that provide additional information about the address bus such as size, cycle type, and/or data transfer bus master identification.
A24	A07	ADDRESS bus (bit 7) - one of 31 three-state lines driven by VMEbus master that specify an address in the memory map. Only the least significant 15 or 23 bits of the 31 associated VMEbus address lines are employed on the controller module.
A25	A06	ADDRESS bus (bit 6) - same as A07 on pin 24.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A26	A05	ADDRESS bus (bit 5) - same as A07 on pin 24.
A27	A04	ADDRESS bus (bit 4) - same as A07 on pin 24.
A28	A03	ADDRESS bus (bit 3) - one of 16 three-state lines driven by VMEbus master that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines A03-A01 are used to indicate the interrupt level that is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - same as A03 on pin A28.
A30	A01	ADDRESS bus (bit 1) - same as A03 on pin A28.
A31	-12 VDC	-12 Vdc Power - used by the logic circuits on the module.
A32	+5 VDC	+5 Vdc Power - used by the logic circuits on the module.
B1	BBSY*	BUS BUSY - An open-collector driven signal driven low by the current master to indicate that it is using the bus. When the master releases this line, the resultant rising edge causes the arbiter to sample the bus grant lines and grant the bus to the highest priority requester.
B2		Not used.
B3	ACFAIL*	AC FAILURE - input signal that indicates a power failure has occurred.
B4	BGOIN*	BUS GRANT (bit 0) IN - bus-grant-in and bus-grant-out form a daisy-chained bus grant. A grant received at the jumpered level indicates the MVME374 may become the bus master. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5	BGOOUT*	BUS GRANT (bit 0) OUT - bus-grant-in and bus-grant-out form a daisy-chained bus grant. The bus-grant-out signal indicates to the next module in the daisy-chain that it may use the DTB.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B6	BG1IN*	BUS GRANT (bit 1) IN - same as BG0IN* on pin B4.
B7	BG1OUT*	BUS GRANT (bit 1) OUT - same as BG0OUT* on pin B5.
B8	BG2IN*	BUS GRANT (bit 2) IN - same as BG0IN* on pin B4.
B9	BG2OUT*	BUS GRANT (bit 2) OUT - same as BG0OUT* on pin B5.
B10	BG3IN*	BUS GRANT (bit 3) IN - same as BG0IN* on pin B4.
B11	BG3OUT*	BUS GRANT (bit 3) OUT - same as BG0OUT* on pin B5.
B12-B15	BR0*-BR3*	BUS REQUEST (0-3) - the bus request at the jumpered level is true when the MPU requires bus mastership. When one or more bus request lines is true in the ROR mode, bus mastership is released. When the controller module is the system controller, bus request level 3 is monitored by the arbiter.
B16-B19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - same as AM4 on pin A23.
B20	GND	GROUND
B21,B22		Not used.
B23	GND	GROUND
B24-B30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - seven prioritized interrupt request inputs. Jumper enabled, level 7 is the highest priority.
B31		Not used.
B32	+5 VDC	+5 Vdc Power - same as +5 VDC on pin A32.
C1-C8	D08-D15	DATA bus (bits 8-15) - eight of sixteen three-state bidirectional data lines that provide the data path between VMEbus master and slave.
C9	GND	GROUND

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C10	SYSFAIL*	SYSTEM FAIL - An open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any board on the VMEbus.
C11	BERR*	BUS ERROR - an active low signal driven by the VMEbus slave that indicates an error has occurred during a data transfer cycle.
C12	SYSRESET*	SYSTEM RESET - the system controller provides this input signal that causes a board-level reset on the module.
C13	LWORD*	LONGWORD - three-state driven signal to indicate that the current transfer is a 32-bit transfer.
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15-C30	A23-A08	ADDRESS bus (bits 23-8) - same as A07 on pin A24.
C31	+12 VDC	+12 Vdc Power - used by the logic circuits on the module.
C32	+5 VDC	+5 Vdc Power - same as +5 VDC on pin A32.

5.2.2 MVME374 Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 triple-row, 96-pin male connector. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-2.

TABLE 5-2. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A9		Not used.
A10-A16	GND	GROUND
A17-A22		Not used.
A23	AXCLSN+	AUXILIARY TRANSFORMED COLLISION + (Input) (Ethernet) - a signal to indicate that multiple stations are contending for access to the transmission medium.
A24	AXTX+	AUXILIARY TRANSFORMED TRANSMIT + (Output) (Ethernet) - this line is intended to operate into terminated transmission lines.
A25		Not used.
A26	AXRX+	AUXILIARY TRANSFORMED RECEIVE + (Input) (Ethernet) - a data input sourced by the MAU.
A27	+12VRTN	+12 Vdc return line.
A28,A29		Not used.
A30	ABORTGND*	ABORT GROUND - ground line for ABORT switch.
A31	RESETSWNC	RESET SWITCH NC - normally closed contact for RESET switch.
A32	RESETSWNO	RESET SWITCH NO - normally open contact for RESET switch.
B1,B13, B32	+5 VDC	+5 Vdc power - used by the logic circuits on the module.
B2,B12 B22,B31	GND	GROUND
B3		RESERVED.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B4-B11	A24-A31	ADDRESS bus (bits 24-31) - Three-state driven address lines that are used in conjunction with A01-A23 to broadcast an extended address.
B14-B21, B23-B30		Not used.
C1		Not used.
C2	TXD	TRANSMIT DATA (RS-232C) - data to be transmitted is furnished on this line to the modem from the terminal.
C3	RXD	RECEIVE DATA (RS-232C) - data from the receive line is presented to the terminal by the modem.
C4	RTS	REQUEST TO SEND (RS-232C) - RTS is supplied by the terminal to the modem when it is required to transmit a message.
C5	CTS	CLEAR TO SEND (RS-232C) - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
C6	DSR	DATA SET READY (RS-232C) - DSR is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
C7	GND	GROUND
C8	DCD	DATA CARRIER DETECT (RS-232C) - sent by the modem to the terminal to indicate that a valid carrier is being received.
C9-C22		Not used.
C23	AXCLSN-	AUXILIARY TRANSFORMED COLLISION - (Input) (Ethernet) - part of a differential pair.
C24	AXTX-	AUXILIARY TRANSFORMED TRANSMIT - (Output) (Ethernet) - part of a differential pair.
C25		Not used.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C26	AXRX-	AUXILIARY TRANSFORMED RECEIVE - (Input) (Ethernet) - part of a differential pair.
C27	+12 VDC	+12 Vdc Power - used by the logic circuits on the module.
C28,C29		Not used.
C30	ABORTSWNC	ABORT SWITCH NC - normally closed contact for ABORT switch.
C31	ABORTSWNO	ABORT SWITCH NO - normally open contact for ABORT switch.
C32	RESETGND*	RESET GROUND - ground line for RESET switch.

5.2.3 MVME374 Connector J1 Interconnect Signals

Connector J1 is a DB-15 D-subminiature 15-pin female connector used to connect to Ethernet. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-3.

TABLE 5-3. Connector J1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	SHIELD	Shield for the connector.
2	XCLSN+	TRANSFORMED COLLISION + (Input) (Ethernet) - a signal to indicate that multiple stations are contending for access to the transmission medium.
3	XTX+	TRANSFORMED TRANSMIT + (Output) (Ethernet) - this line is intended to operate into terminated transmission lines.
4		Not used.
5	XRX+	TRANSFORMED RECEIVE + (Input) (Ethernet) - a data input sourced by the MAU.
6	+12VRTN	+12 Vdc return line.
7,8		Not used.
9	XCLSN-	TRANSFORMED COLLISION - (Input) (Ethernet) - part of a differential pair.
10	XTX-	TRANSFORMED TRANSMIT - (Output) (Ethernet) - part of a differential pair.
11		Not used.
12	XRX-	TRANSFORMED RECEIVE - (Input) (Ethernet) - part of a differential pair.
13	+12VOLT	+12 Vdc Power (fused) (Ethernet) - fused +12 Vdc sourced by the DTE.
14,15		Not used.

5.3 MVME374 PARTS LIST

The components of the interface module are listed in Table 5-4. The parts locations are illustrated in Figure 5-1. These parts reflect the latest issue of hardware at the time of printing.

TABLE 5-4. MVME374 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8517B01B	Printed Wiring Board, MVME374
C1-C5,C7-C14,C16-C26, C28-C39,C41, C43-C46,C48, C51-C59,C61-C65	21NW9632A03	Capacitor, ceramic, axial lead, 0.1 uF ± 20% @ 50 Vdc
C6,C15,C27, C42,C66	23NW9618A71	Capacitor, electrolytic, radial lead, 47 uF ± 20% @ 10 Vdc
C40	--	Not used.
C47	23NW9704A99	Capacitor, tantalum, radial lead, 33 uF ± 20% @ 15 Vdc
C49	23NW9618A87	Capacitor, electrolytic, radial lead, 4.7 uF ± 20% @ 25 Vdc
C50	21NW9604A39	Capacitor, ceramic, radial lead, 4700 pF ± 10% @ 50 Vdc
C60	21SW992C011	Capacitor, ceramic, 680 pF @ 50 Vdc
CR1,CR2	48NW9616A03	Diode, silicon, 1N4148/1N914
DL1	51NW9615W26	I.C. DS1000M-100
DL2	51NW9615W46	I.C. DS1000M-50
DL3	01NW9804C09	Delay module, triple, 50 ns
DS1	48NW9612A49	Indicator, LED, red, right angle
DS2	48NW9612A59	Indicator, LED, green, right angle
F1	65NW9622A26	Fuse, axial lead, micro, 1 A @ 125 Vdc
--	28NW9802E08	Connector, single socket (2 req'd) (used with F1)

TABLE 5-4. MVME374 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
J1	28NW9802H06	Connector, 15-pin, socket, right angle, D-subminiature
--	42NW9401A15	Retainer, snap slide, including screws (used with J1)
J2-J9	29NW9805C07	Pin, 0.025-inch, square, gold, auto-insert, used on J2(12), J3(6), J4(2), J5(9), J6(14), J7(16), J8(21), J9(12)
--	29NW9805B17	Jumper, insulated, shorting (25 req'd) (used with J2, J3, J5, J6, J7, J8)
P1,P2	28NW9802E51	Connector, 96-pin, plug "PWB"
--	05NW9007A26	Eyelet, 0.089-inch OD x 0.344-inch long (4 req'd) (used with P1 and P2)
R1	06SW-125A57	Resistor, fixed, film, 2.2k ohm, 5%, 1/2 W
R2,R8-R10, R13,R17,R18, R22-R24,R34-R37	51NW9626B56	Resistor network, SIP, nine 10k ohm
R3	06SW-124A23	Resistor, film, 82 ohm, 5%, 1/4 W
R4,R14	51NW9626B64	Resistor network, SIP, four 47 ohm
R5,R16	51NW9626A77	Resistor network, SIP, seven 22k ohm
R6,R7	51NW9626B48	Resistor network, SIP, five 47 ohm
R11,R15	51NW9626A48	Resistor network, SIP, four 100 ohm
R12,R38	06SW-124A49	Resistor, film, 1.0k ohm, 5%, 1/4 W
R19,R20	06SW-125A53	Resistor, fixed, film, 1.5k ohm, 5%, 1/2 W
R21	06SW-124A96	Resistor, film, 91k ohm, 5%, 1/4 W
R25	06SW-960D47	Resistor, film, 30.1k ohm, 1%, 1/8 W
R26	06SW-124A42	Resistor, film, 510 ohm, 5%, 1/4 W
R27	06SW-124A97	Resistor, film, 100k ohm, 5%, 1/4 W
R28	06SW-124A60	Resistor, film, 3.0k ohm, 5%, 1/4 W

TABLE 5-4. MVME374 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R29	06SW-124A25	Resistor, film, 100 ohm, 5%, 1/4 W
R30-R33	06SW-961A59	Resistor, film, 40.2 ohm, 1%, 1/4 W
S1,S2	40NW9801B70	Switch, push, SPDT, momentary, PC, right-angle, gold
--	38NW9404C11	Cap, switch, black, for B70 (used with S1)
--	38NW9404C12	Cap, switch, red, for B70 (used with S2)
T1	25NW9706A39	Transformer, isolation, triple, 16-pin DIP
U1-U7,U26	51NW9615W55	I.C. TC514256Z-10
U8,U27	51NW9615R84	I.C. 74F827SPC
--	09-W4659B12	Socket, I.C., SIL, 12-pin (2 req'd) (used with U27)
U9,U29,U30	51NW9615V51	I.C. IDT74FCT245AP
U10,U12, U34,U35	(NOTE)	I.C. Programmed EPROMs
--	09-W4659B16	Socket, I.C., SIL, 16-pin (8 req'd) (used with U10,U12,U34,U35)
U11,U13	51NW9615R38	I.C. SN74LS794N
U14	51NW9615S66	I.C. N8T38N
U15	51NW9615W06	I.C. IDT74FCT374P
U16,U17, U33,U37, U47	51NW9615R36	I.C. 74F543SPC
U18-U21	--	Not used.
U22-U25	51NW9615T64	I.C. MB81256-10PZ (alternate is M5M4257AL-10, part number 51NW9615Y69)
U28,U31	51NW9615K49	I.C. 74F240PC
U32	51NW9615F02	I.C. SN74LS244N
U36	(NOTE)	I.C. Programmed PAL

TABLE 5-4. MVME374 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U38-U41	51NW9615K98	I.C. 74F280PC
U42	(NOTE)	I.C. Programmed PAL
--	09-W4659B10	Socket, I.C., SIL, 10-pin (12 req'd) (used with U42,U60,U63,U75,U99,U105)
U43	(NOTE)	I.C. Programmed PAL
U44,U45	51NW9615K18	I.C. 74F373PC
U46	51NW9615K47	I.C. 74F244PC
U48	51NW9615U56	I.C. AM7990PC80
--	09-W4659B24	Socket, I.C., SIL, 24-pin (4 req'd) (used with U48,U85)
U49	51NW9615K65	I.C. 74F64PC
U50	51NW9615L74	I.C. 74F163APC
U51,U97	51NW9615K70	I.C. 74F08PC
U52	51NW9615R89	I.C. MC68020RC16E
--	09NW9811B27	Socket, I.C., pin-grid-array, 114-pin (used with U52)
U53	51NW9615J13	I.C. AM25LS2519PC
U54	51NW9615G41	I.C. SN74145N
U55,U59, U84,U94	51NW9615K66	I.C. 74F32PC
U56,U74	51NW9615R55	I.C. N74F38N
U57	51NW9615K69	I.C. 74F10PC
U58,U77	51NW9615K73	I.C. 74F00PC
U60	(NOTE)	I.C. Programmed PAL
U61,U78	51NW9615W07	I.C. IDT74FCT521AP
U62	51NW9615S63	I.C. SN74ALS243A-1N

TABLE 5-4. MVME374 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U63	(NOTE)	I.C. Programmed PAL
U64	51NW9615W41	I.C. IDT74FCT841BP
U65,U76, U88,U98, U102-U104, U107	51NW9615J39	I.C. 74F74PC
U66	51NW9615W65	I.C. XC2212AP
U67	(NOTE)	I.C. Programmed PAL
U68	51NW9615U19	I.C. IDT74FCT244P
U69	51NW9615N56	I.C. 74F174PC
U70	(NOTE)	I.C. Programmed PAL
U71	(NOTE)	I.C. Programmed PAL
U72	(NOTE)	I.C. Programmed PAL
U73	(NOTE)	I.C. Programmed PAL
U75	(NOTE)	I.C. Programmed PAL
U79	--	Not used (spare).
U80	51NW9615S83	I.C. MC145406P
U81	(NOTE)	I.C. Programmed PAL
U82,U101	51NW9615K71	I.C. 74F04PC
U83	51NW9615F38	I.C. SN74LS393N
U85	51NW9615N40	I.C. MK68901N
U86	51NW9615E93	I.C. SN74LS14N
U87	(NOTE)	I.C. Programmed PAL
U89	51NW9615K29	I.C. ICL8211CPA
U90	51NW9615J74	I.C. SN74LS74AN3
U91	51NW9615K99	I.C. 74F374PC

TABLE 5-4. MVME374 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U92	(NOTE)	I.C. Programmed PAL
U93	51NW9615U57	I.C. AM7992BPC
U95	(NOTE)	I.C. Programmed PAL
U96	51NW9615F30	I.C. DM74S05N
U99	(NOTE)	I.C. Programmed PAL
U100	(NOTE)	I.C. Programmed PAL
U105	(NOTE)	I.C. Programmed PAL
U106	(NOTE)	I.C. Programmed PAL
Y1	48AW1015B12	Crystal oscillator, 32 MHz, 0.01%
Y2	48AW1015B13	Crystal oscillator, 40 MHz, 0.01%
--	67NW9415A17	Kit, ejector handle, 6U component
--	64-W5576B01	Panel, front, MVME374 (alternate is part number 64-W5576B01A)
--	33-W5577B01	Nameplate, MVME374
--	33-W5089B01	Nameplate, Scanbe, Motorola logo
--	42NW9401B14	Captive collar screw (2 req'd)
--	03NW9004B48	Screw, captive, M2.5 (2 req'd)
--	33-W5796B01A	Label, Ethernet address (Refer to paragraph 4.3.12.)

NOTE: When ordering, use number labeled on part.

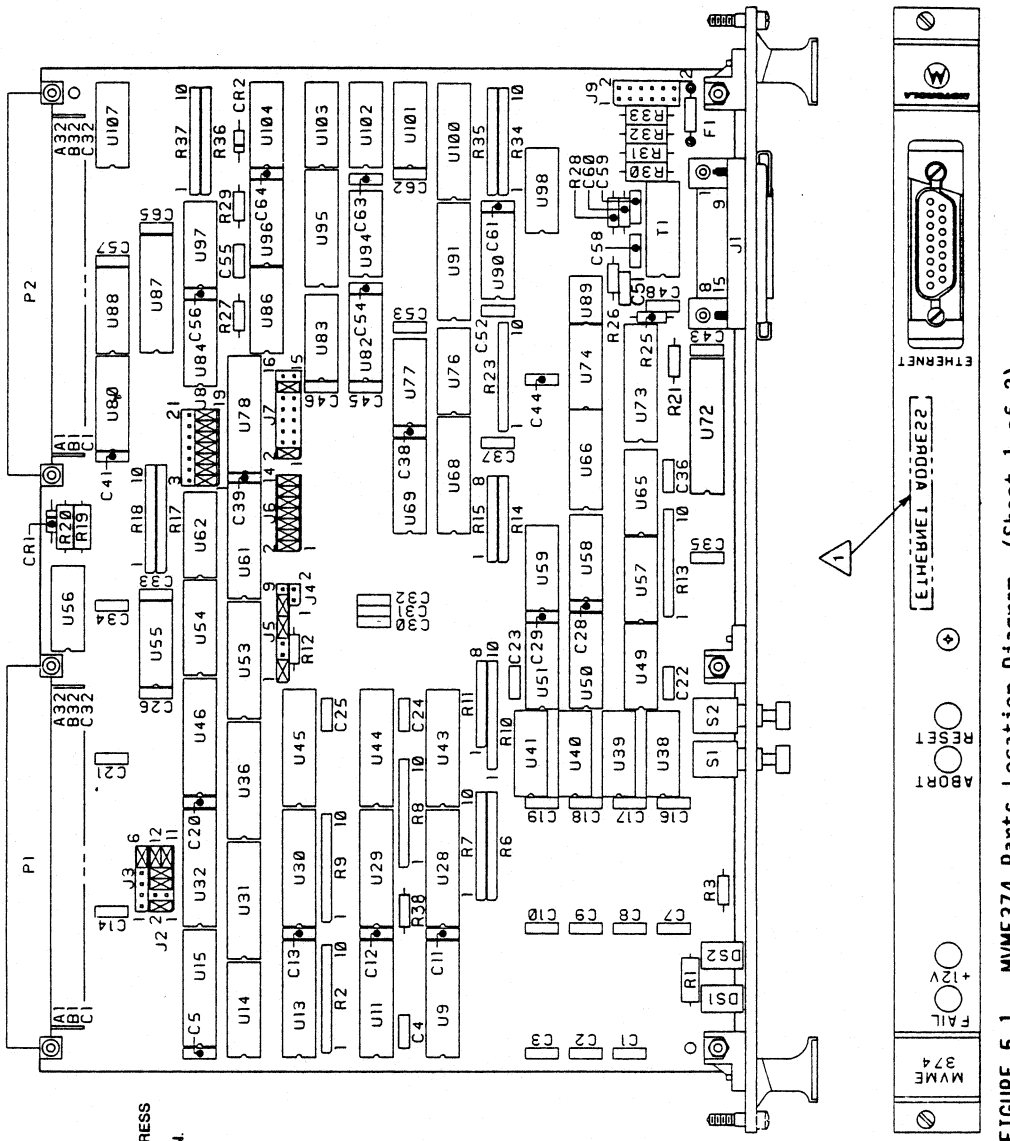


FIGURE 5-1. MVME374 Parts Location Diagram (Sheet 1 of 2)

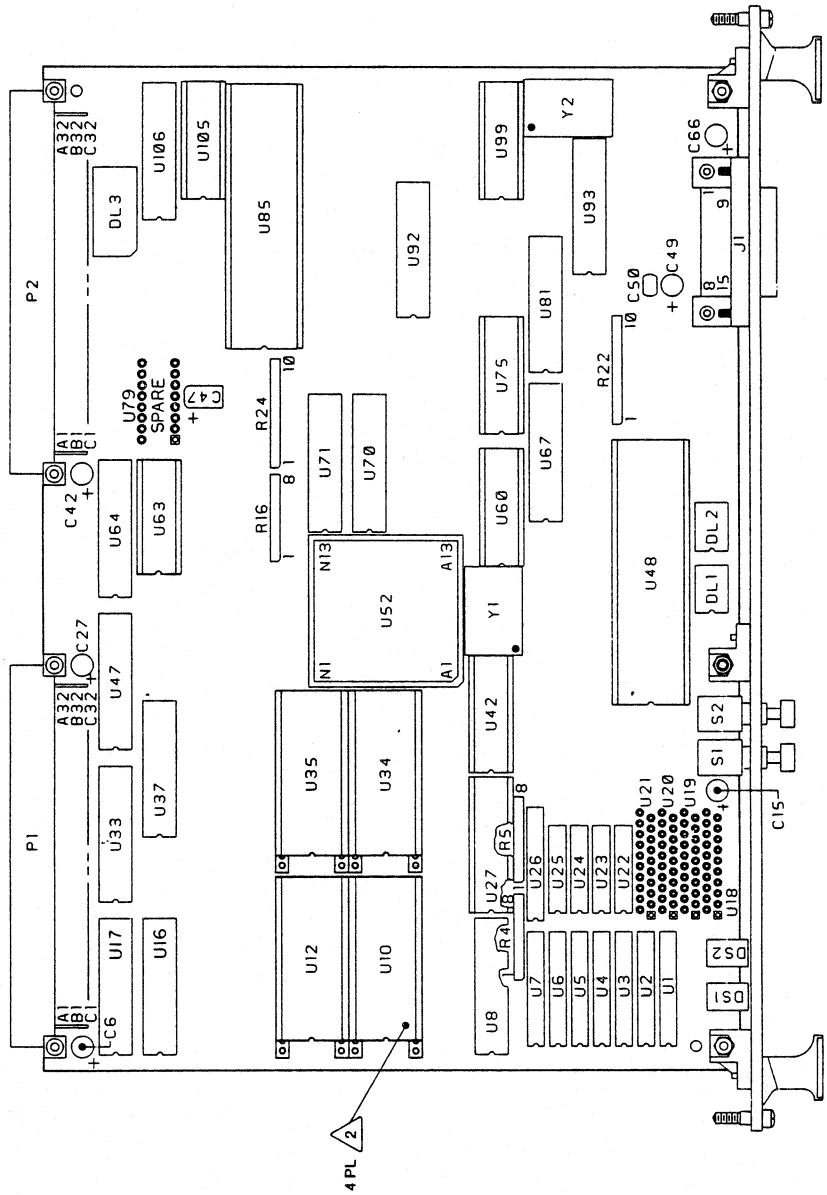


FIGURE 5-1. MVME374 Parts Location Diagram (Sheet 2 of 2)

5.4 SCHEMATIC DIAGRAMS

The schematic diagram for the MVME374 is illustrated in Figure 5-2.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3517801 CURRENT REVISION/CONFIGURATION APPLIES.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [DENOTES - ON-BOARD SIGNALS.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
7. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   (SHEET) 5 C7 (ZONE)

8. DEVICE TYPES ARE GIVEN FOR REFERENCE ONLY. 256KX4 DEVICES ARE INSTALLED.

9. DEVICE NOT INSTALLED.

REF DES	TYPE 4	GND	+5V
DL1	DELAY5M-20	4	8
DL2	DELAY5M-10	4	8
DL3	DLY2PD-50	7	14
U1	TC514100L	5	15
U2	TC514100L	5	15
U3	TC514100L	5	15
U4	TC514100L	5	15
U5	TC514100L	5	15
U6	TC514100L	5	15
U7	TC514100L	5	15
U8	F827	12	24
U9	FCT245P	10	20
U11	LS794	10	20
U13	LS794	10	20
U14	8T38	8	16
U15	FCT374	10	20
U16	F543	12	24
U17	F543	12	24
U18	M5M4C1000L	4	15
U19	M5M4C1000L	4	15
U20	M5M4C1000L	4	15
U21	M5M4C1000L	4	15
U22	M5M4256L	4	12
U23	M5M4256L	4	12
U24	M5M4256L	4	12
U25	M5M4256L	4	12
U26	TC514100L	5	15
U27	F827	12	24
U28	F240	10	20
U29	FCT245P	10	20
U30	FCT245P	10	20
U31	F240	10	20
U32	LS244	10	20
U33	F543	12	24
U36	PALSIDEC	10	20
U37	F543	12	24
U38	F280	7	14
U39	F280	7	14
U40	F280	7	14
U41	F280	7	14
U42	PALCAS	10	20
U43	PALCMMO	10	20
U44	F373	10	20
U45	F373	10	20
U46	F244P	10	20
U47	F543	12	24
U48	AM7990	1	48
		24	
U49	F64	7	14
U50	F163	8	16
U51	F08	7	14
U52	68020R12	B1	A9
		B9	D1
		C3	D2
		J3	D3
		K1	E3
		K3	M8
		L7	N8
		N7	G11
		A10	G13

REF DES	TYPE 4	GND	+5V	+12V	-12V
		F12	N13		
		G12			
		H13			
		L11			
U53	25LS2519	10	20		
U54	145	8	16		
U55	F32	7	14		
U56	F38	7	14		
U57	F10	7	14		
U58	F00	7	14		
U59	F32	7	14		
U60	PALLOCARB	10	20		
U61	FCT521	10	20		
U62	ALS243A-1	7	14		
U63	PALA32	10	20		
U64	FCT841	12	24		
U65	F74	7	14		
U66	X2212	8	18		
U67	PALINT	12	24		
U68	FCT244	10	20		
U69	F174	8	16		
U70	PALMAP	12	24		
U71	PALRAM	12	24		
U72	PALGLUE	12	24		
U73	PALANCE	10	20		
U74	F38	7	14		
U75	PALBERR	10	20		
U76	F74	7	14		
U77	F00	7	14		
U78	FCT521	10	20		
U80	MC145406	9	16	1	8
U81	PALDSACK	12	24		
U82	F04	7	14		
U83	LS393	7	14		
U84	F32	7	14		
U85	MC68901	36	11		
U86	LS14	7	14		
U87	PALVMAST	10	20		
U88	F74	7	14		
U89	ICL8211	5	8		
U90	LS74	7	14		
U91	F374	10	20		
U92	PALSELECT	12	24		
U93	AM7992B	6	18		
		7	19		
U94	F32	7	14		
U95	PALSITIME	10	20		
U96	S05	7	14		
U97	F08	7	14		
U98	F74	7	14		
U99	PALSRCTR	10	20		
U100	PALREFCNT	10	20		
U101	F04	7	14		
U102	F74	7	14		
U103	F74	7	14		
U104	F74	7	14		
U105	PALVMEOBUF	10	20		
U106	PALREQ	12	24		
U107	F74	7	14		
Y1	OSC-32MHZ	7	14		
Y2	OSC-40MHZ	7	14		

REF DES	SH
CR1	2
CR2	5
C1	2
C2	2
C3	2
C4	2
C5	2
C6	2
C7	2
C8	2
C9	2
C10	2
C11	2
C12	2
C13	2
C14	2
C15	2
C16	2
C17	2
C18	2
C19	2
C20	2
C21	2
C22	2
C23	2
C24	2
C25	2
C26	2
C27	2
C28	2
C29	2
C30	2
C31	2
C32	2
C33	2
C34	2
C35	2
C36	2
C37	2
C38	2
C39	2
C41	2
C42	2
C43	2
C44	2
C45	2
C46	2
C47	5
C48	7
C49	13
C50	13
C51	13
C52	2
C53	2
C54	2
C55	5
C56	2
C57	2
C58	13
C59	13

REF DES	SH
C60	13
C61	2
C62	2
C63	2
C64	2
C65	2
C66	2
DS2	2
DS1	5
DL2	8
DL3	16
DL3	18
F1	2
J1	3
J2*	16
J3	16
J4	19
J5	12
J6	15
J7	15
J8	15
J9	13
P1	3
P2	3
R1	2
R2	12
R2	19
R3	5
R4	8
R5	2
R5	6
R5	8
R6	8
R7	8
R8	2
R8	8
R8	11
R8	13
R9	2
R9	12
R10	2
R10	3
R10	5
R10	8
R11	5
R11	6
R12	5
R13	3
R13	6
R13	7
R13	13
R14	5
R14	9
R15	5
R16	15
R17	3
R17	6
R17	13
R17	15
R17	17

REF DES	SH
R18	2
R18	13
R18	19
R19	14
R20	14
R21	7
R22	3
R22	5
R22	7
R22	11
R22	13
R23	3
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Y1	5
Y2	13

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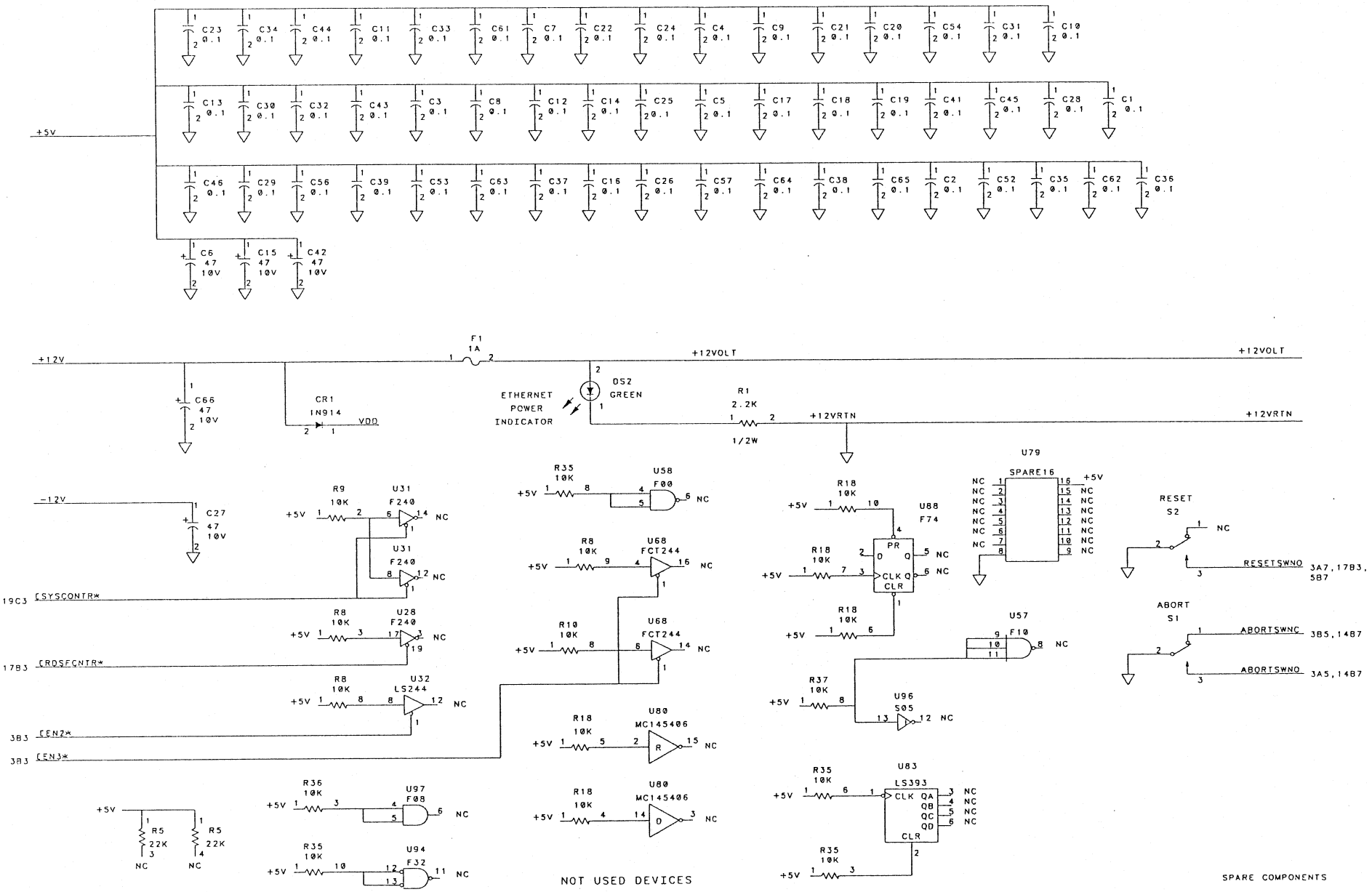

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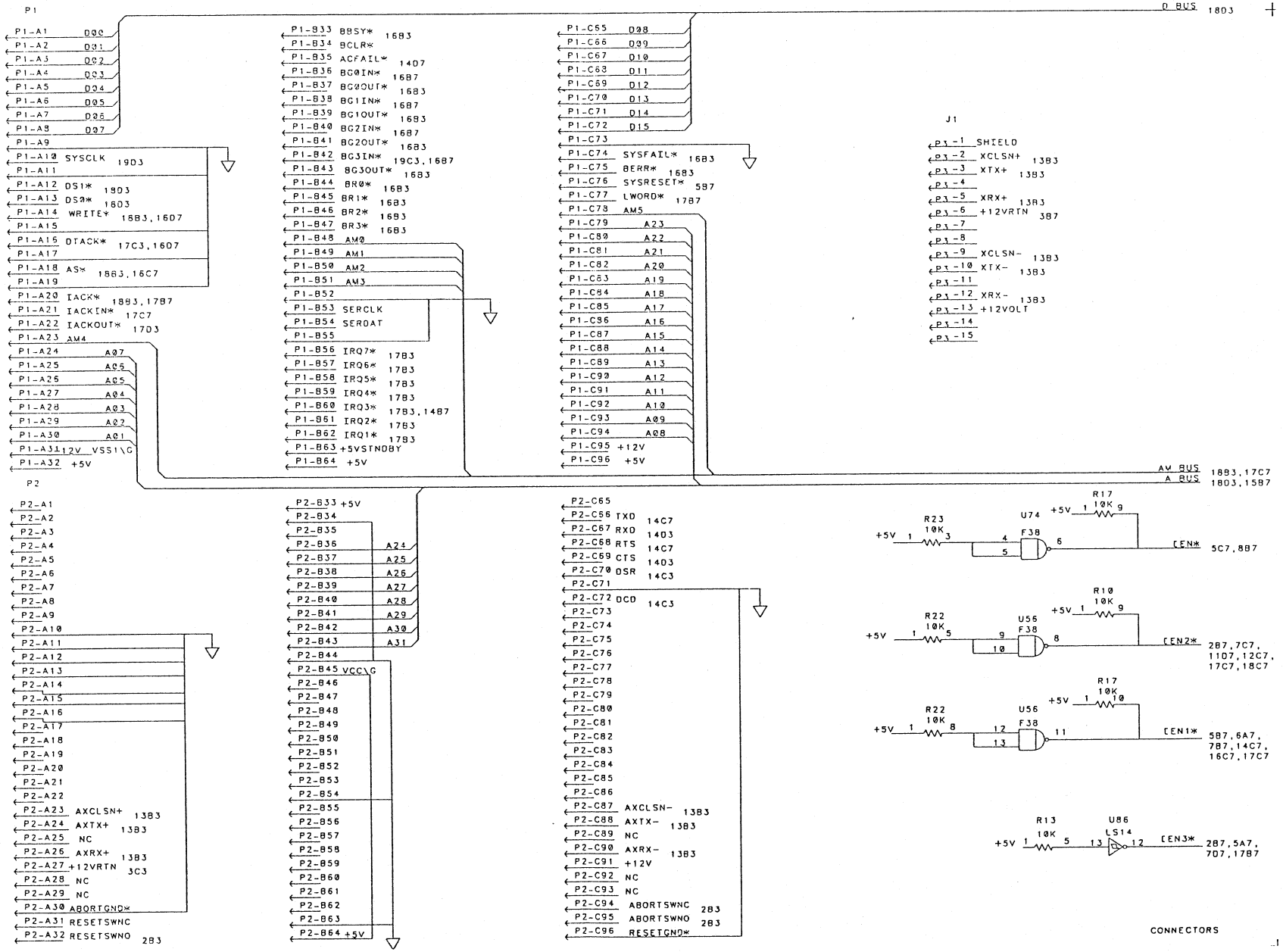


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 3 of 19)

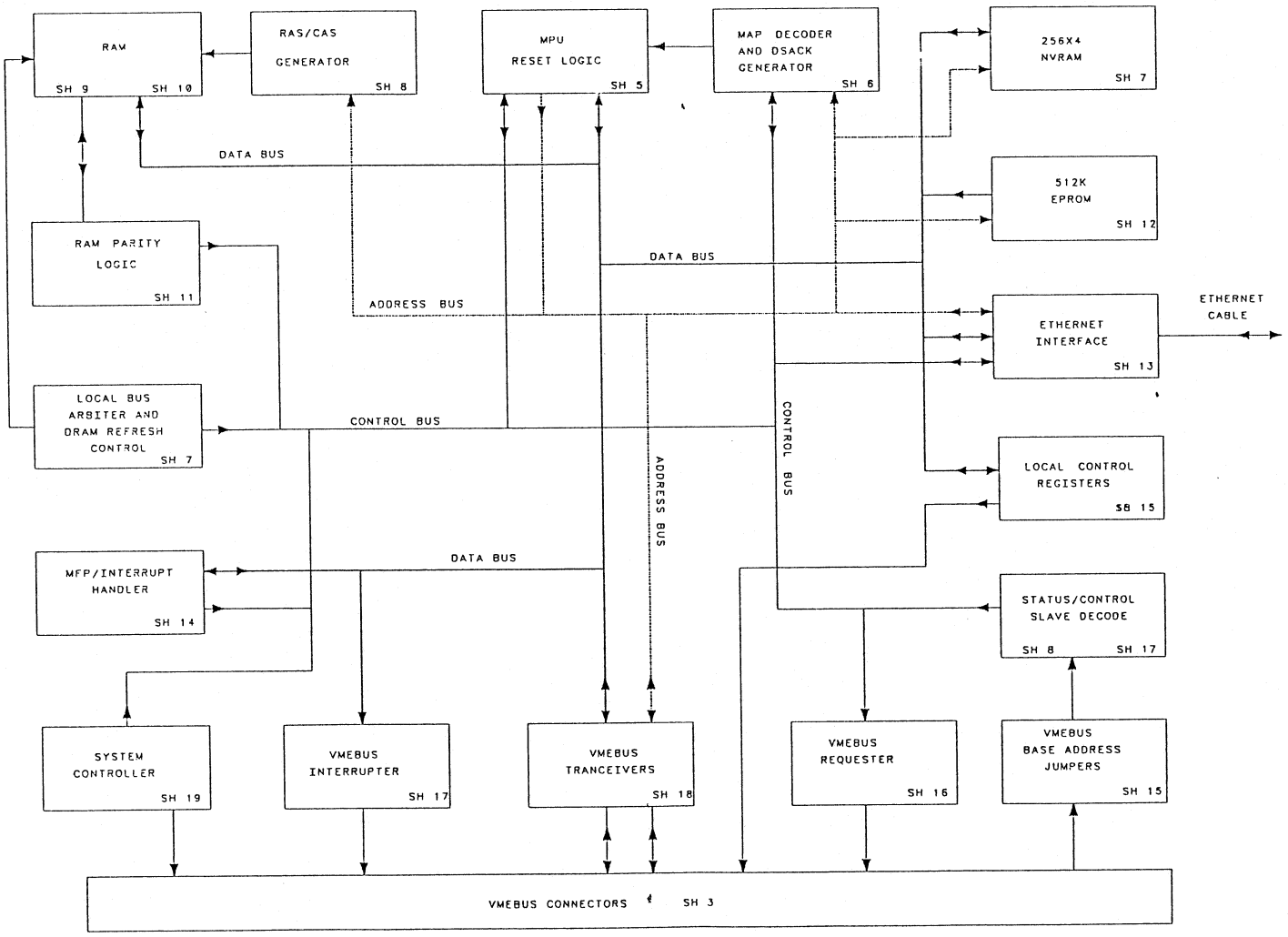


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 4 of 19)

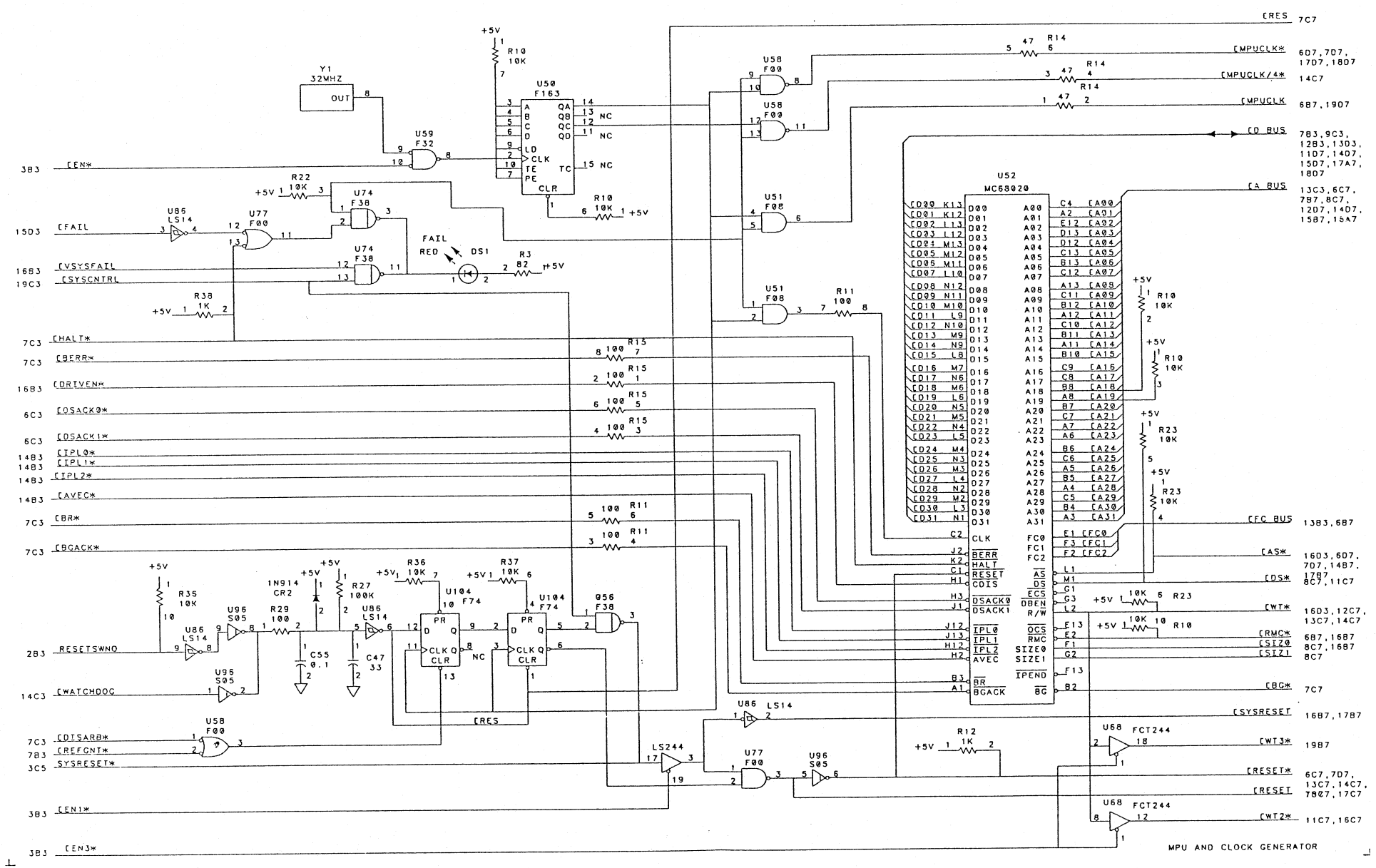


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 5 of 19)

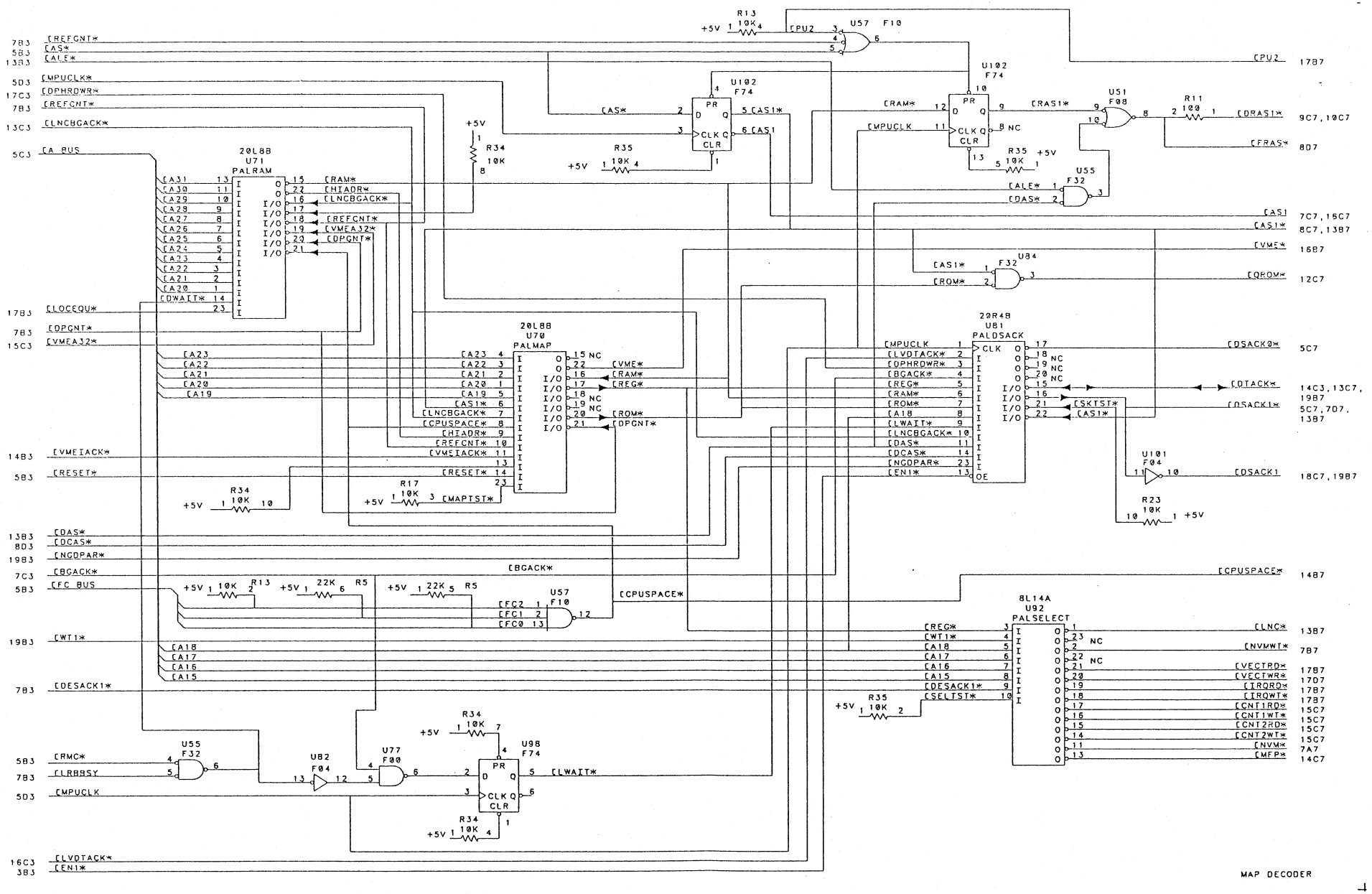


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 6 of 19)

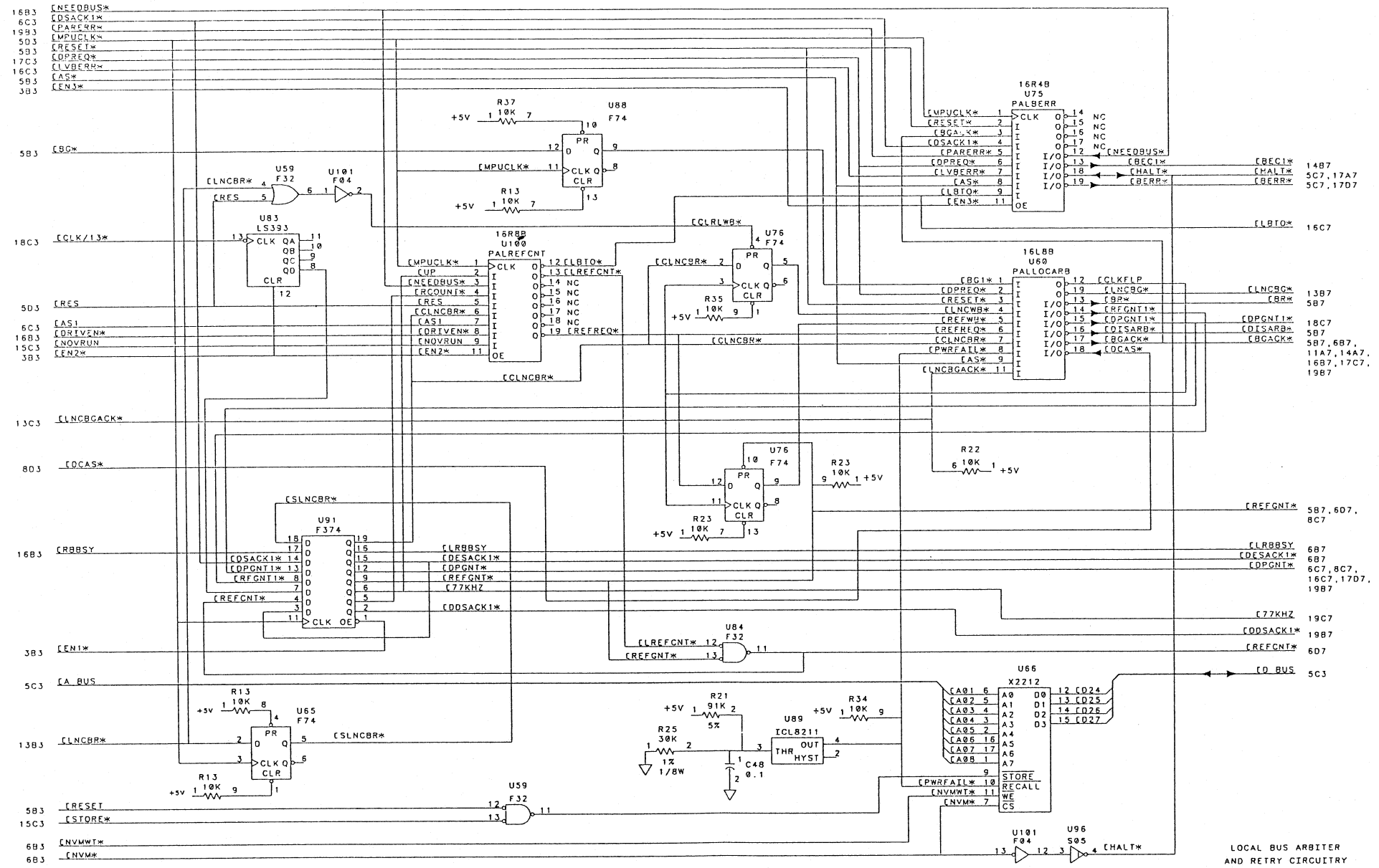


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 7 of 19)

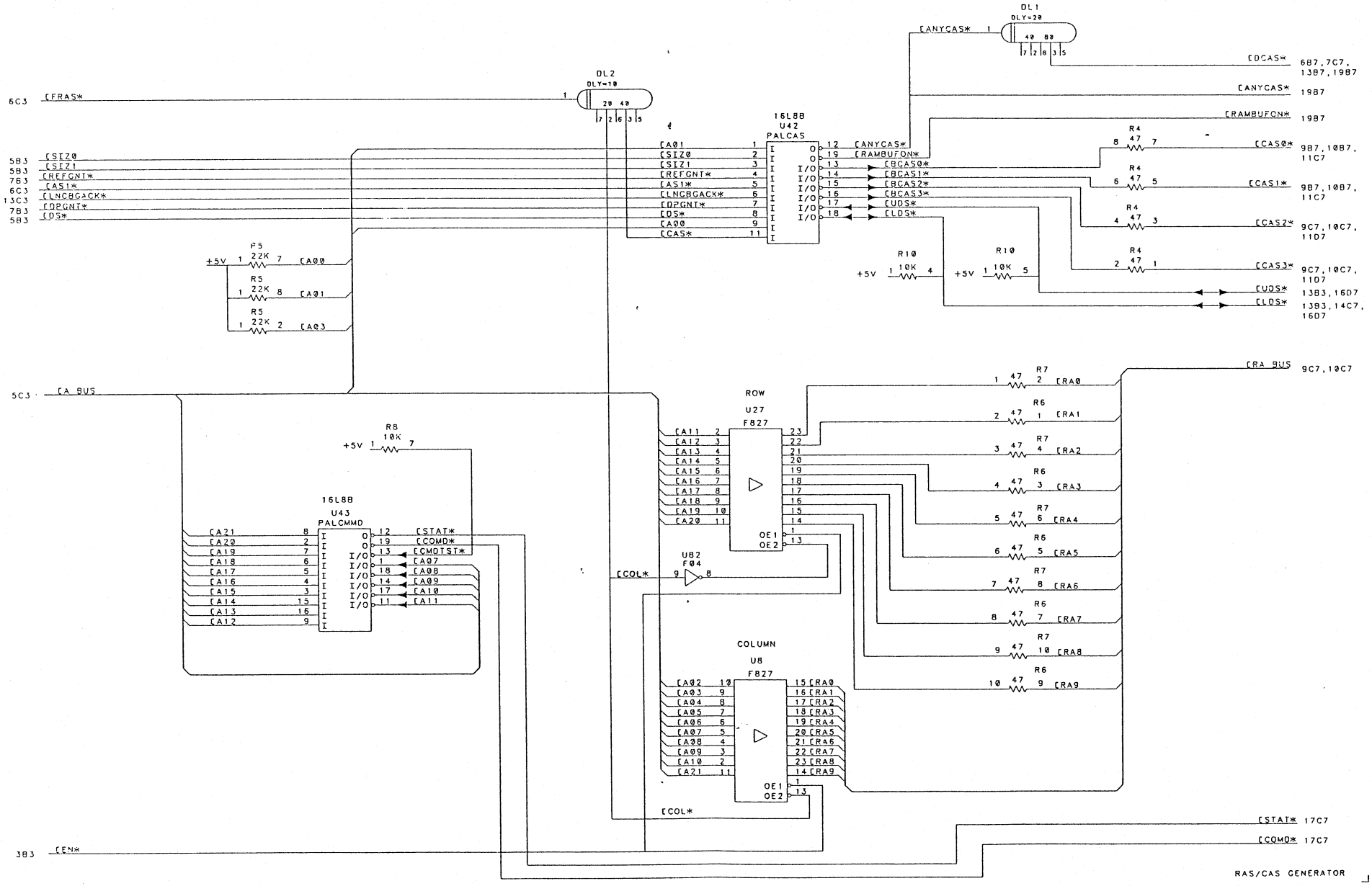
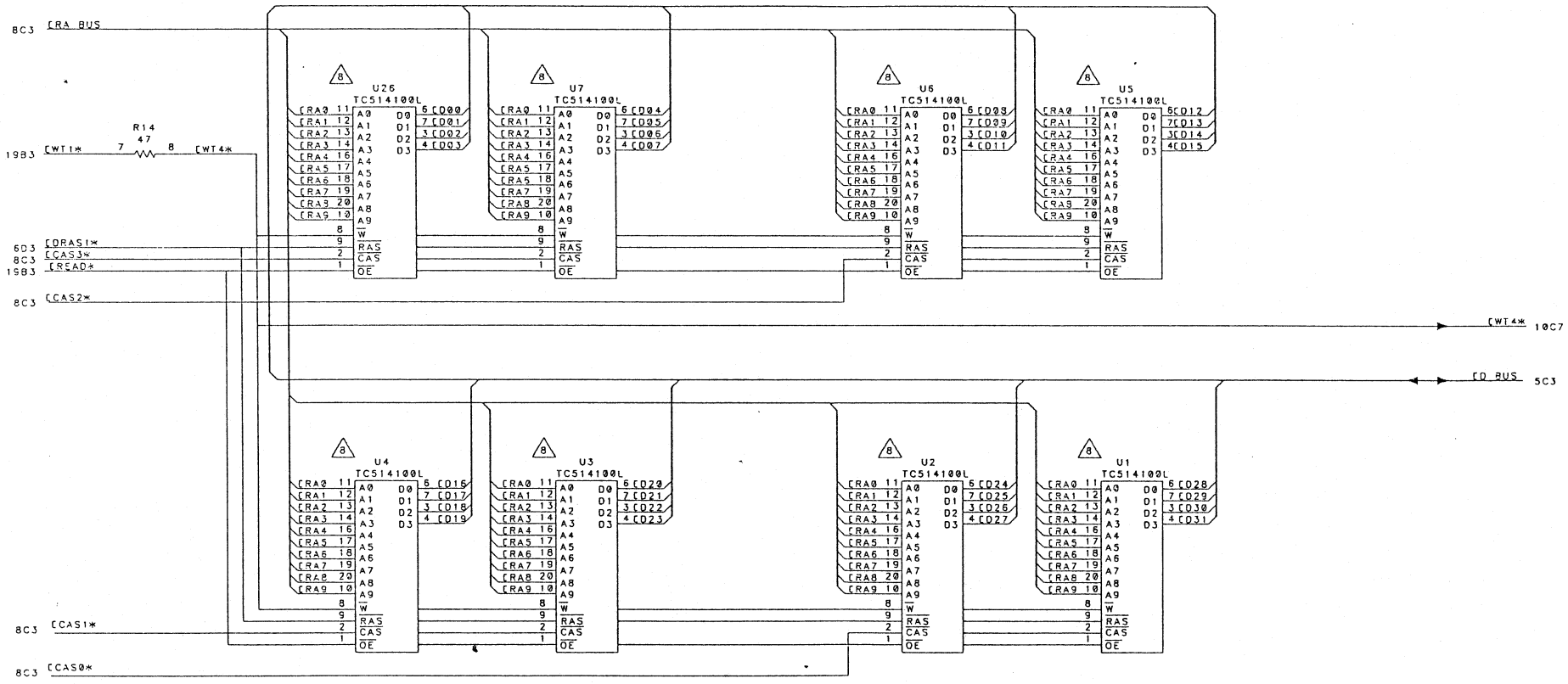


FIGURE 5-2. MVME374 Schematic Diagram (Sheet 8 of 19)



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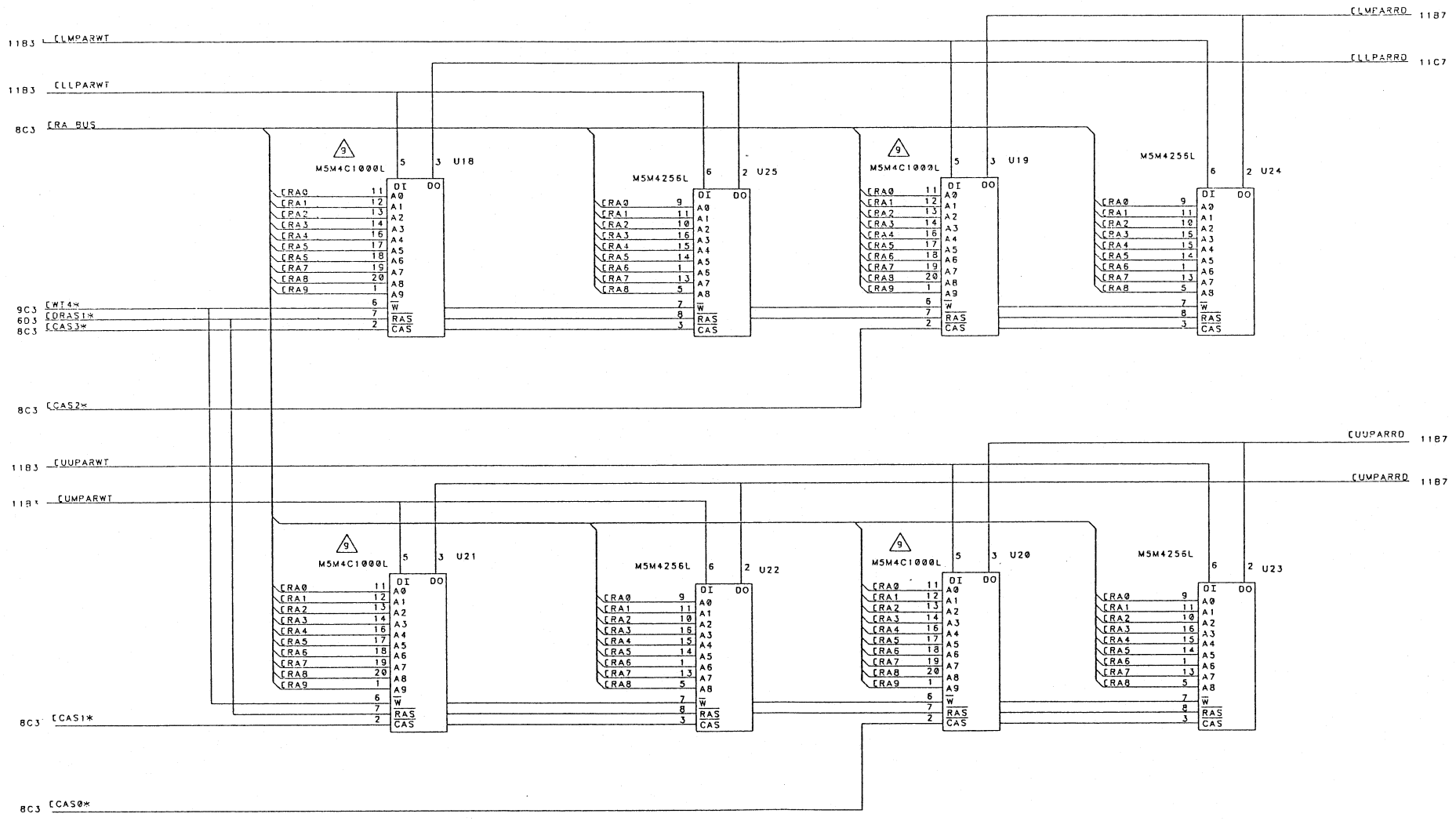

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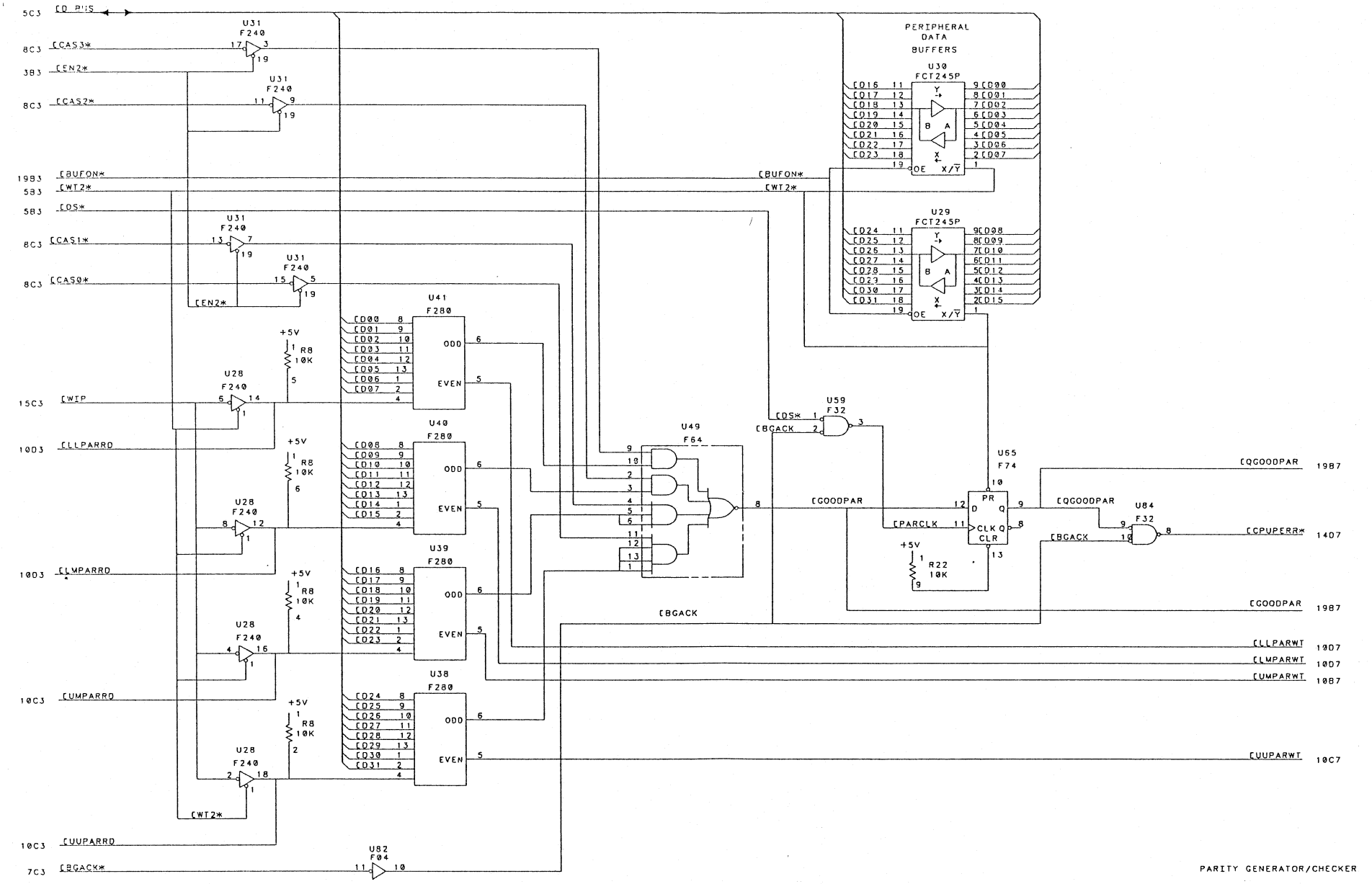

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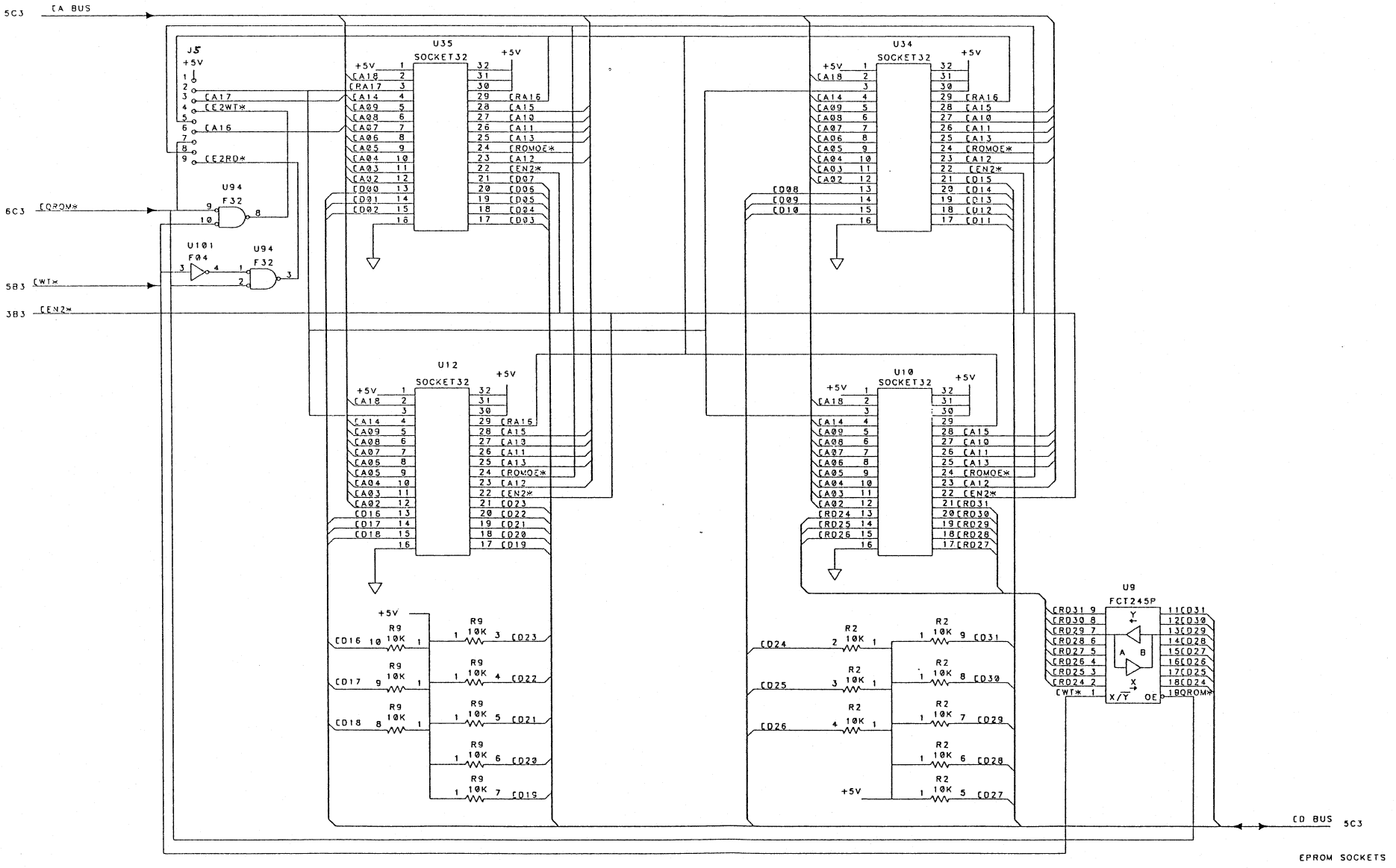

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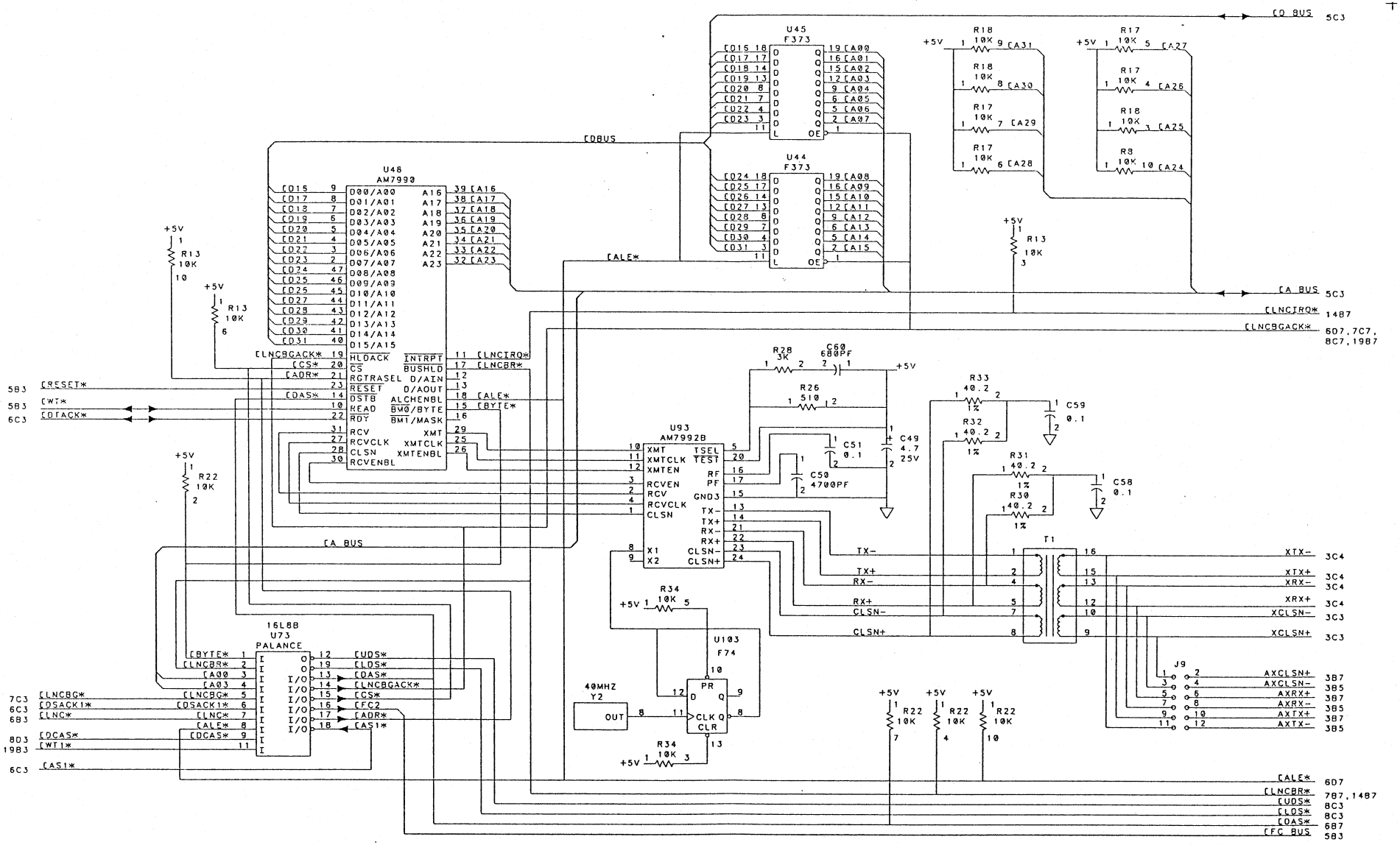

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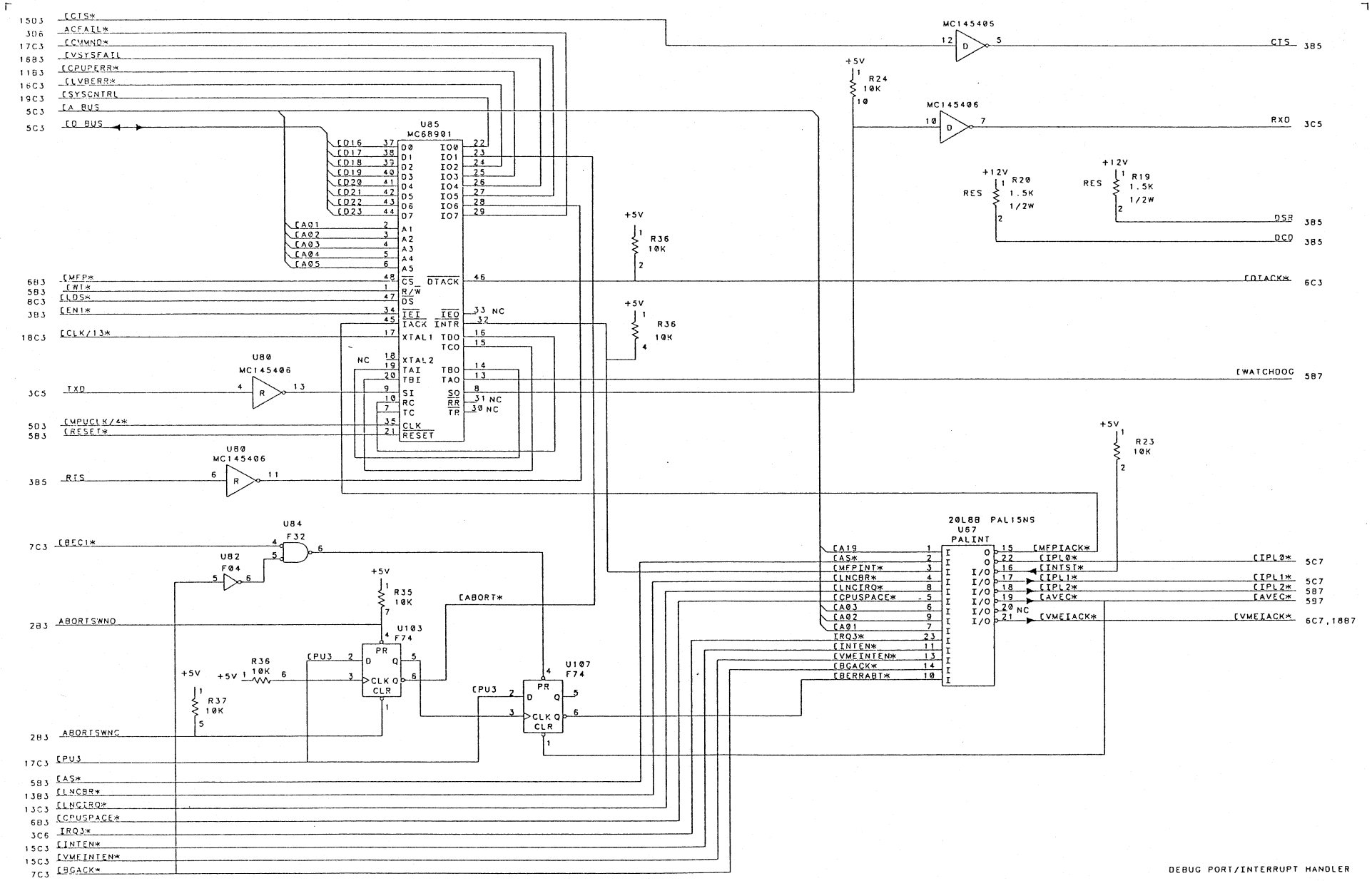

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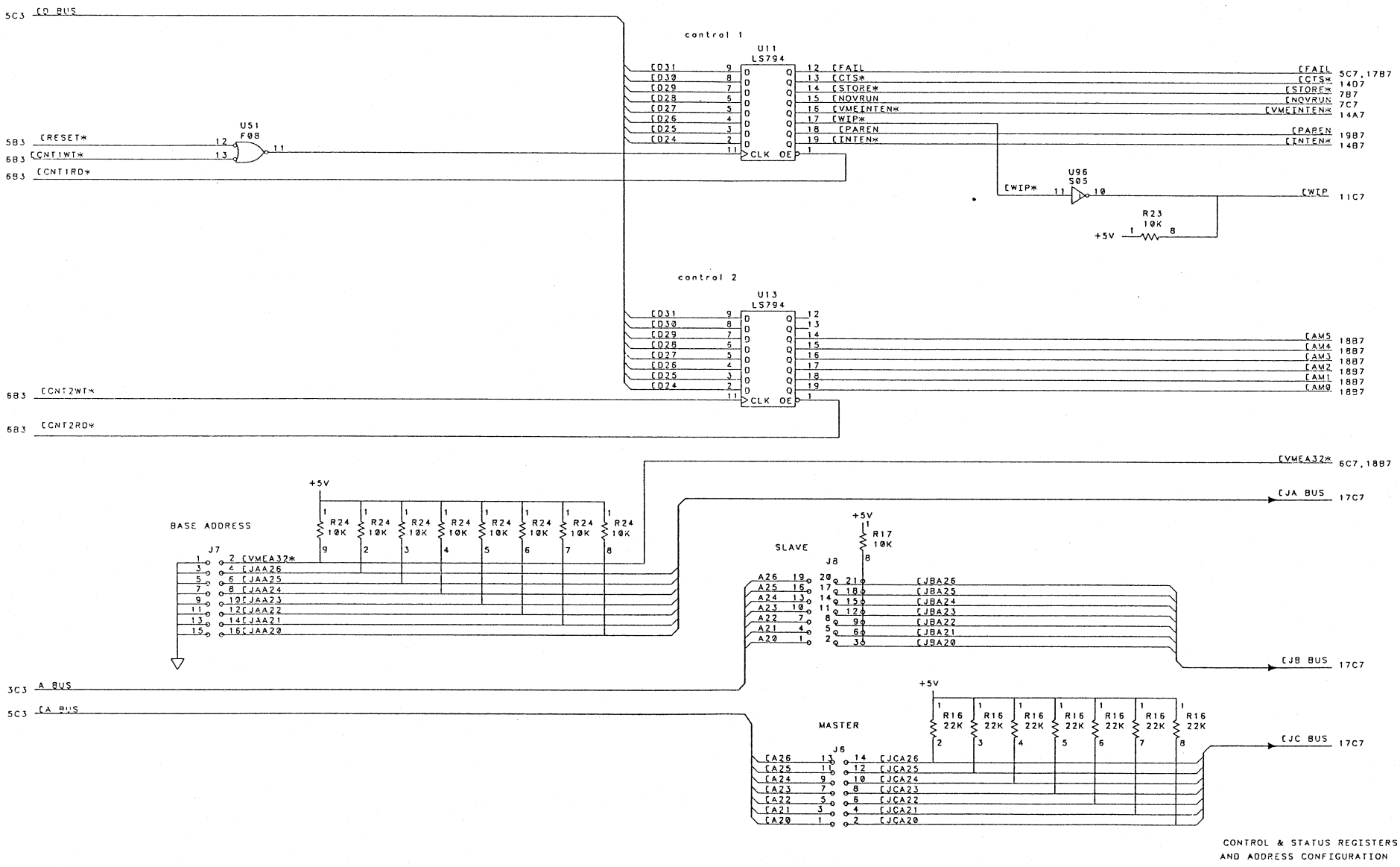

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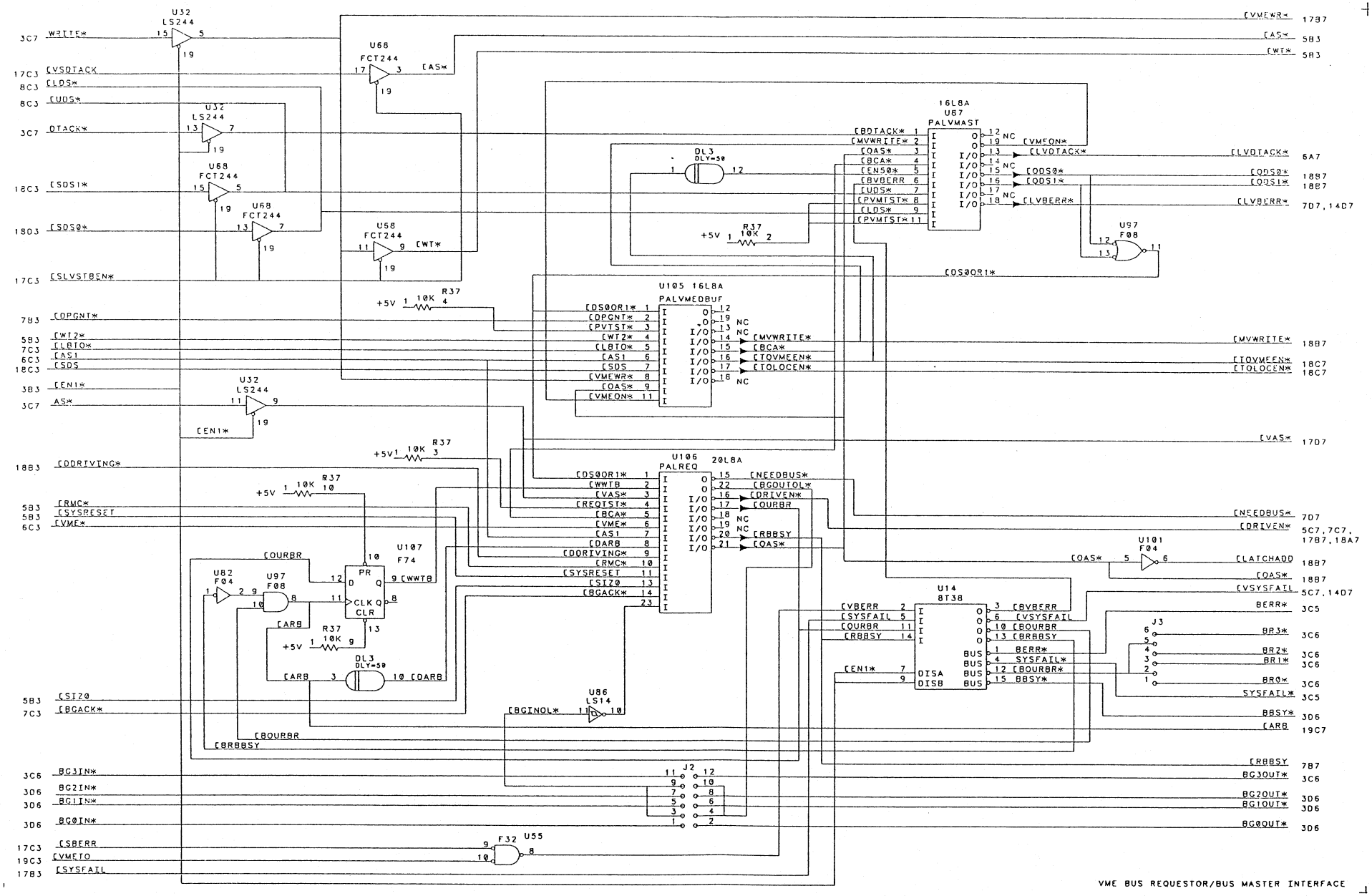

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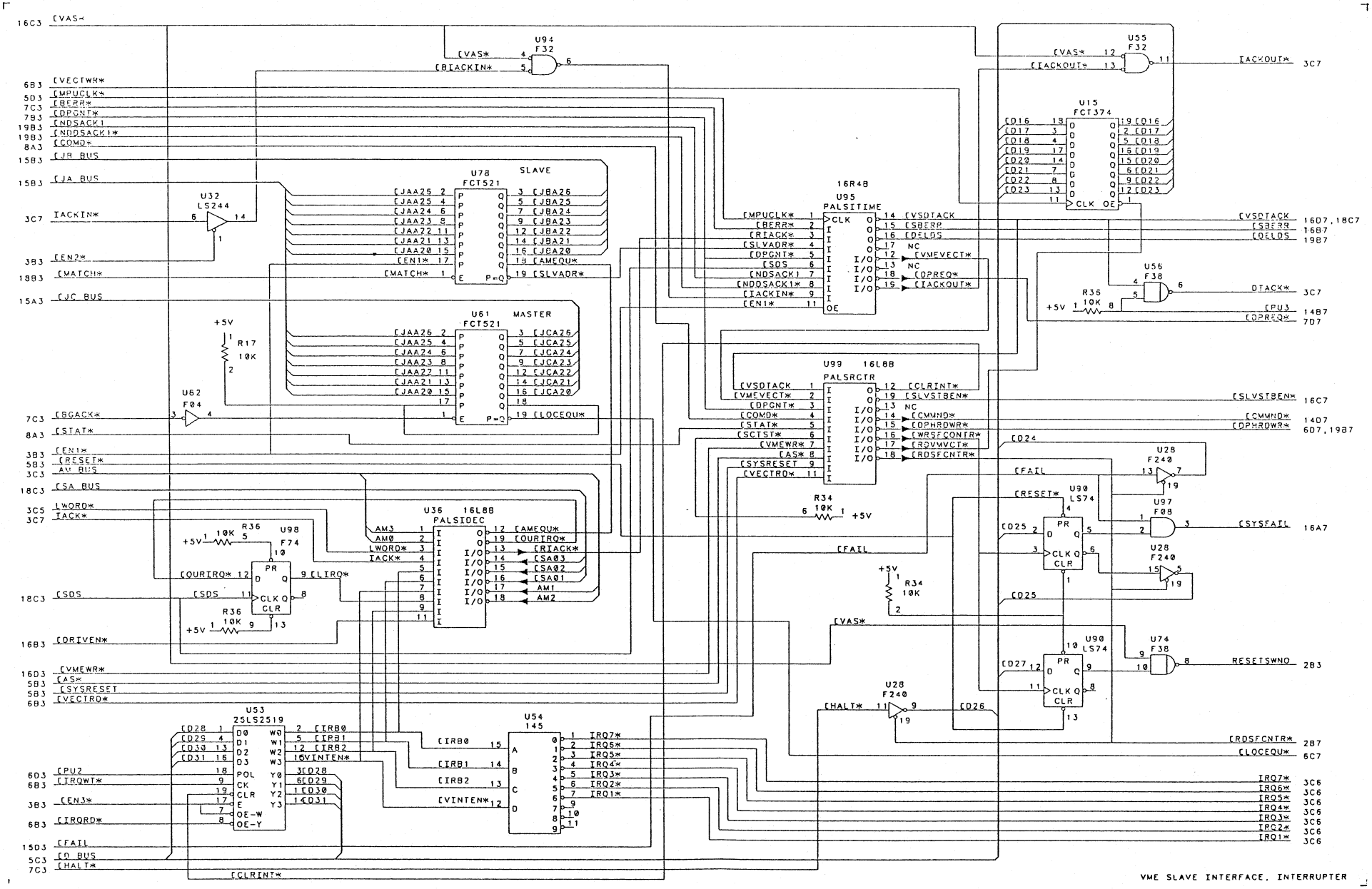

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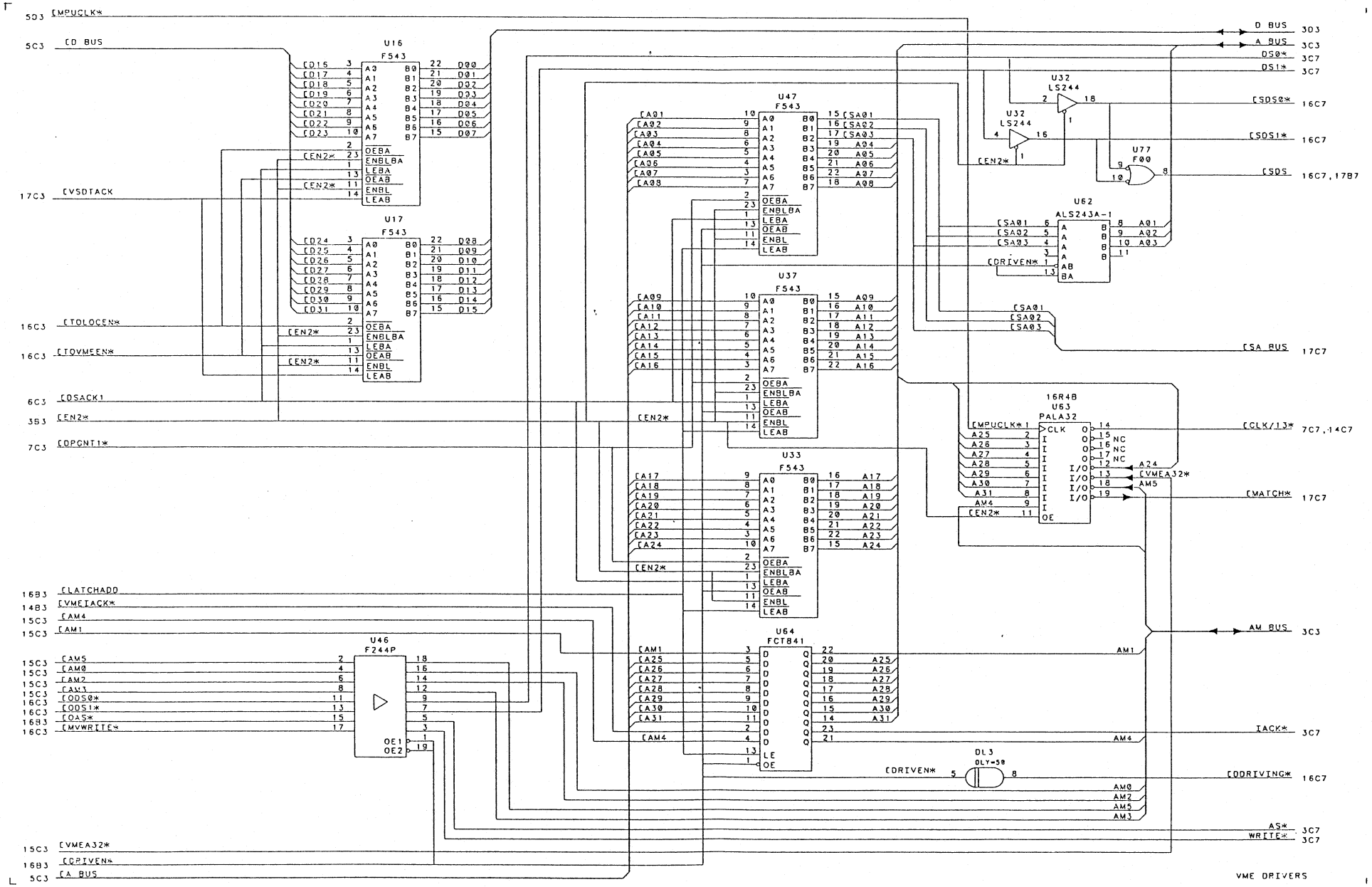

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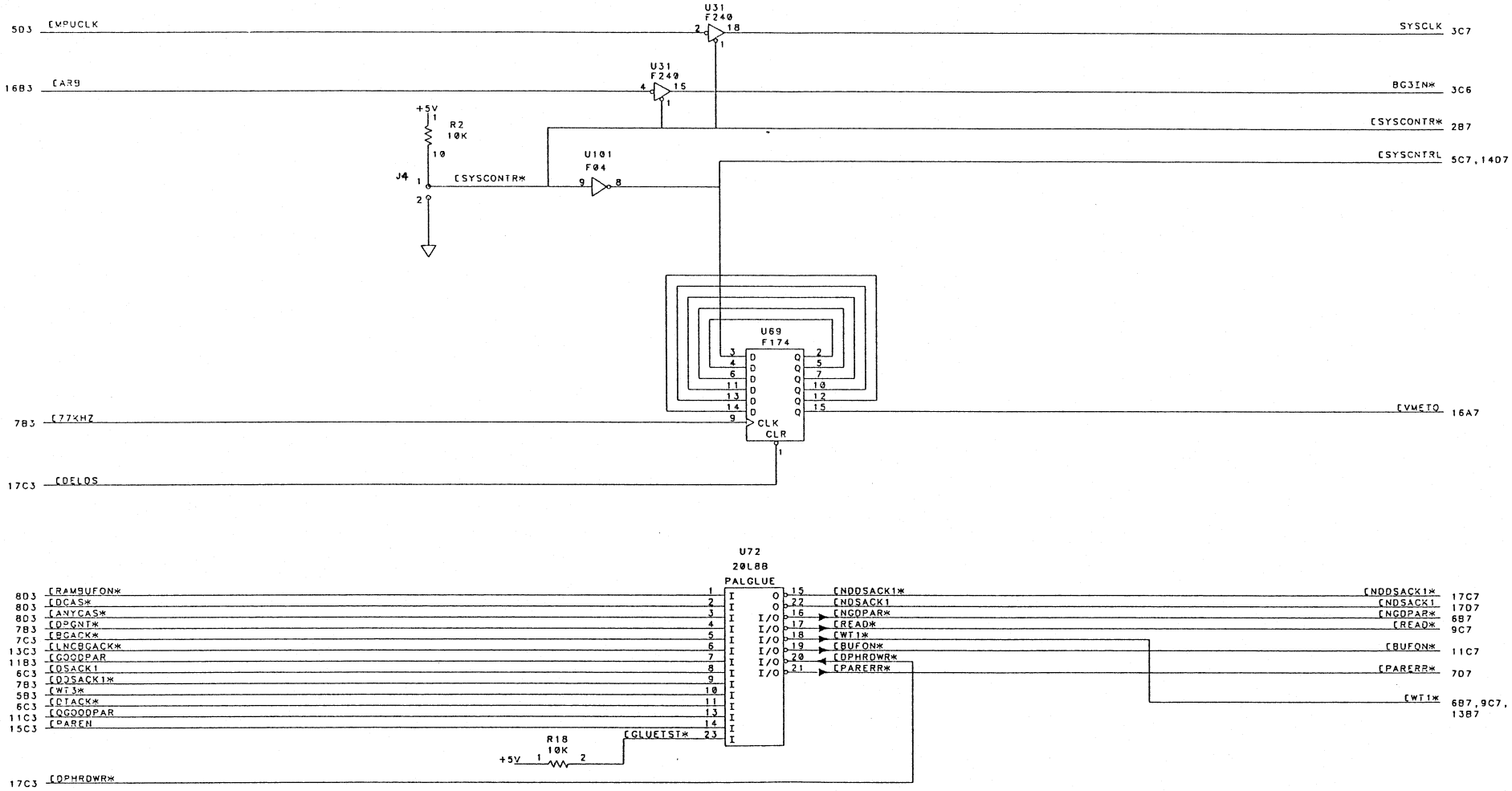

SYSTEM CONTROLLER

FIGURE 5-2. MVME374 Schematic Diagram (Sheet 19 of 19)

A

APPENDIX A - DEBUG CABLE

Parts for the debug cable are listed in Table A-1. Its parts locations are illustrated in Figure A-1. These parts are recommended, but equivalent parts may be used.

TABLE A-1. Debug Cable Parts List

ITEM NUMBER	VENDOR AND PART NUMBER	DESCRIPTION
1	Amphenol 843-191-2801-064, or 3M Co. 3365/64	Cable, flat, 64-conductor, 28 AWG, 25 inches
2	Burndy FRDS25RS-1L, or Winchester 49-1125S-0G	Connector, flat, cable, 25-pin, female
3	AMP 746603-1, or Winchester 96S-6053-0531-13	Connector, 64-position, socket
4	3M Co. Scotch 69 1.5 inch	Tape, glass cloth, white, 1.5 x 8 inches
5	Brady DAT-25-502-10	Label, white, 0.75 x 0.25 inch

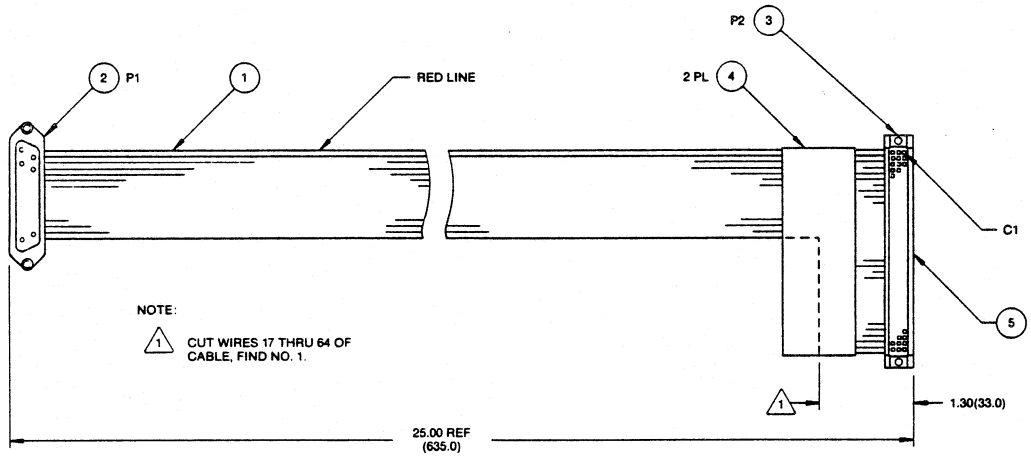

FIGURE A-1. Debug Cable Parts Location Diagram

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