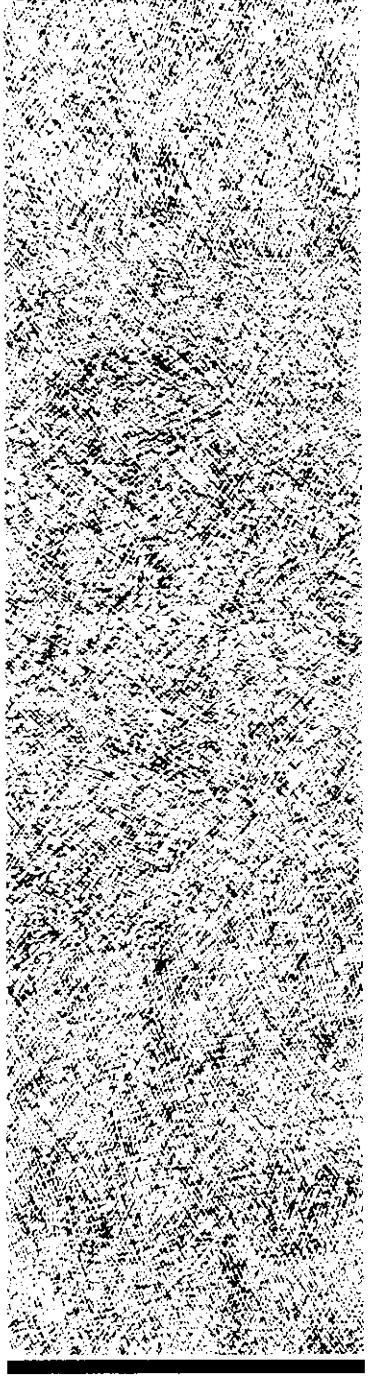
MVME050/D3

MVME050
System Controller Module
User's Manual



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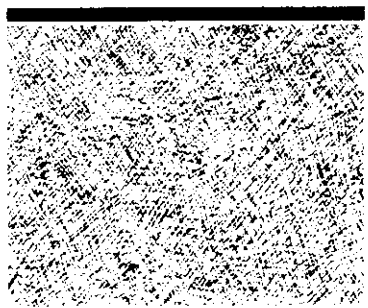

MVME050

SYSTEM CONTROLLER MODULE

USER'S MANUAL

(MVME050/D3)

PREFACE

This manual provides general information, hardware preparation, installation instructions, operating instructions, functional description, and support information for the MVME050 System Controller Module.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

Throughout this manual the paragraph headings conform to the following convention:

HARDWARE PREPARATION	(this is a main topic heading)
Controller Module Headers	(this is a subordinate topic heading under a main topic)

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

First Edition April 1989

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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CHAPTER 1 - GENERAL INFORMATION

INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME050 System Controller Module.

FEATURES

The features of the MVME050 module include:

- System controller functions:
  - 4-level priority bus arbiter
  - Power up reset/front panel reset
  - System clock and serial clock generators
  - Bus time-out generator
- Eight 28-pin sockets for EPROM/RAM
- Time-of-day clock
- Global interrupter
- User-defined/controlled front panel display
- A32/A24:D8/D16/D32 VMEbus slave interface
- Front panel RESET switch
- Front panel FAIL LED and RUN LED

SPECIFICATIONS

The MVME050 module specifications are identified in Table 1-1.

TABLE 1-1. MVME050 Module Specifications

CHARACTERISTICS	SPECIFICATIONS			
Performance	Access time		Cycle time	
	Typ	Max	Typ	Max
RAM (J26) EPROM (J27) Select Speed				
150 ns	375 ns	400 ns	455 ns	520 ns
250	475	550	555	670
350	575	675	655	785
450	650	700	730	820
Interface (I/O)				
Serial ports, printer, switches, LED	350 ns	400 ns	540 ns	650 ns
VBIM	500 ns	550 ns	580 ns	675 ns
Time-of-day clock	1100 us	1300 us	1180 us	1420 us
Bus arbitration time	Typical 75 ns		Maximum 125 ns	
Temperature				
Operating	0 degrees to 55 degrees C			
Storage	-40 degrees to 85 degrees C			
Relative humidity	5% to 90% (non-condensing)			
Physical characteristics (excluding front panel)				
Height	9.187 in. (233.35 mm)			
Depth	6.299 in. (160.00 mm)			
Thickness	0.63 in. (1.6 mm)			
Power requirements	+5 Vdc @ 3.7 A (typical) 4.4 A (max.) -12 Vdc @ 35 mA (typical) 42 mA (max.) +12 Vdc @ 140 mA (typical) 170 mA (max.)			

GENERAL DESCRIPTION

The MVME050 is a combination system controller and debug/diagnostics module for VME systems. The module is designed to offload the system controller functions from computer type modules, also to provide the typical one-per-system type features such as the time-of-day clock, printer/parallel port, and a serial port for downline loading of programs from a host system. The module is capable of holding a system diagnostics and debug monitor for end-use in-system trouble shooting and maintenance. A global interrupter provides the ability to have tightly coupled task/message passing between intelligent modules in multiprocessor systems. The controller module allows extended addressing for supporting the expanded (32 bit) VMEbus. Both 32-bit data and address are supported on EPROM/RAM sockets.

RELATED DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, the manual may be purchased from Motorola Literature Distribution Center, 616 W. 24th Street, Tempe, Arizona 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
MVME701A Transition Module	MVME701A

NOTE: Although not shown in the above list, each Motorola MCD manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); supplement bears the same number as the manual but has a suffix such as "/A1" (the first supplement to the manual).

The following publication is available from the source indicated.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017, USA.

MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the MVME050.

UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MVME050 module, certain changes may be made before installation. These changes are made through jumper arrangements on the headers. The location of the headers, LEDs, RESET switch, and connectors are illustrated in Figure 2-1. The module has been factory tested and is shipped with factory-installed jumper configurations that are also shown in the illustration. The module is operational with the factory-installed jumpers. The MVME050 module is configured to provide all the system controller functions required for a VMEbus system. It is necessary to make changes in the jumper arrangements for the following:

a. EPROM base address select (J1,J2)

b. EPROM/RAM configuration select (quad 2) (J3)

c. Bus time-out select (J4)

d. Clock damping shorting select (J5,J6)

e. System controller select (J7)

f. EPROM size select (J8)

g. RAM base address select (J9,J10)

h. EPROM/RAM configuration select (quad 1) (J11)

i. Address Modifier (AM1E) enable select (EPROM bank 1); AM16 enable select (EPROM bank 2) (J12)

j. EPROM bank enable select (J13)

k. RAM bank enable select (J14)

l. RAM size select (J15)

m. EPROM/RAM configuration select (quad 1 and 2) (J16,J17,J18,J19)

n. I/O base address select (512 byte boundaries) (J20)

o. Time-of-day clock power select and battery charge (J21)

p. SYSFAIL* or GND select for interrupt source (J22)

q. Internal/external transmit clock serial port 1 select (J23)

r. Internal/external transmit clock serial port 2 select (J24)

s. Display blanking enable select (J25)

t. RAM access time select (J26)

u. EPROM access time select (J27)

v. RESET switch disable select (J28)

w. Printer acknowledge edge select (J29)

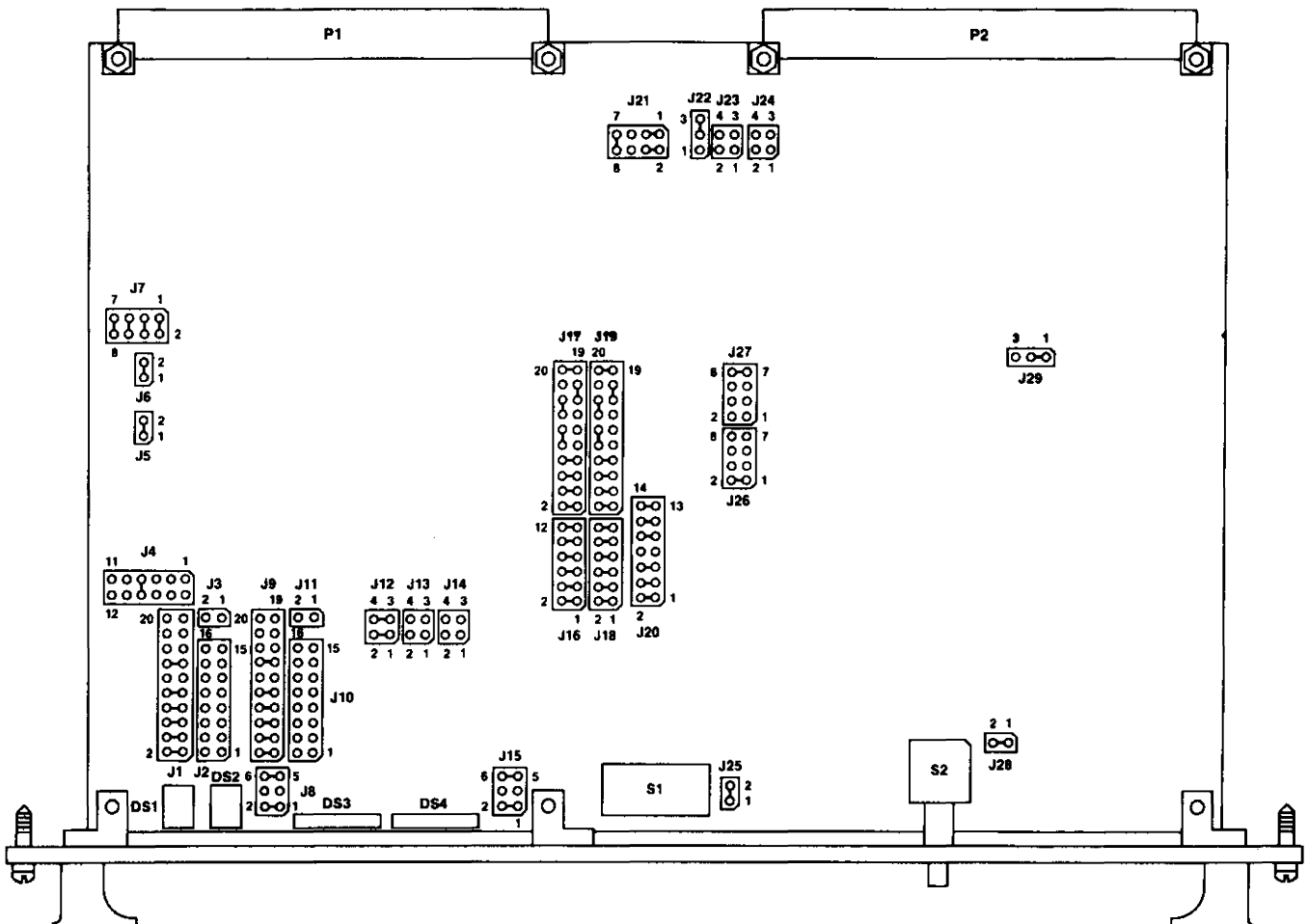


FIGURE 2-1. MVME050 Module Option Locations

The configuration options of the MVME050 module headers are discussed in the following paragraphs.

The VMEbus base address for accessing EPROM/RAM is set by jumper position on the appropriate headers. If both socket quads (refer to the *EPROM/RAM Configuration Select Headers J3, J11, J16-J19* paragraph in this Chapter) are populated with RAM, the RAM base address is set with the RAM headers (J9, J10), and the RAM addressing becomes contiguous across the socket quad boundary. The EPROM base address headers (J1, J2) are ignored. If both socket quads are populated with EPROM, the base address is set with the EPROM headers (J1, J2), and the addressing becomes contiguous across the socket quad boundary. When both RAM and EPROM populations are used, the RAM base address is set by the RAM headers (J9, J10) and the EPROM base address is set by the EPROM headers (J1, J2). If EPROM devices are installed in the high numbered socket quad (2), they are capable of being accessed when a bus master initiates a VMEbus transfer using Address Modifier (AM) code 1E (J12). If EPROM devices are installed in the low numbered socket quad (1), they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. When this type of access occurs, no other devices on the module are accessed and the EPROM base address circuitry is disabled. This feature may be disabled by removing the jumpers from J12.

EPROM Base Address Select Header (J1,J2)

The base address may be selected anywhere within the 16Mb of the system memory map with address modifier codes 39, 3A, 3D, 3E for standard addressing; or anywhere within the 4 gigabyte map with address modifier codes 09, 0A, 0D, 0E for extended addressing.

NOTE

Addressing (AM codes 09, 0A, 0D, 0E) require a backplane motherboard with a P2 connector.

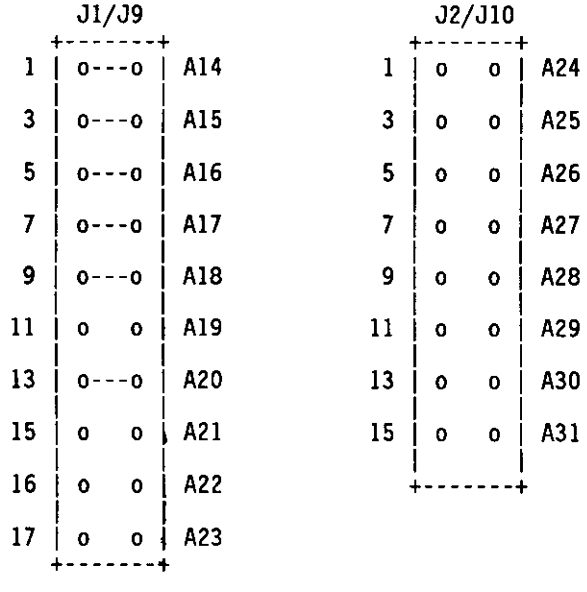
Installing a jumper enables the appropriate line. As shown below, header J1 is associated with address lines A14-A23 and header J2 with lines A24-A31. The base address selected must be on a boundary that is eight times the size of the devices used regardless of the quantity installed, as shown below.

For each quad used, a four-way split of data must be used. Let's assume the four sections of the quad were numbered as follows:

D0-D7 = 1
D8-D15 = 2
D16-D23 = 3
D24-D31 = 4

As an example, the four-way split would be:

ADDRESS	DATA	SECTION NUMBER
0	01	1
1	02	2
2	03	3
3	04	4
4	05	1
5	06	2
6	07	3
7	08	4



JUMPER IN = ADDRESS LINE LOW

DEFAULT SHOWN = E80000 24-BIT ADDRESS
FFE80000 32-BIT ADDRESS

2

DEVICE SIZE	BOUNDARY
2K x 8	16K
4K x 8	32K
8K x 8	64K
16K x 8	128K
32K x 8	256K
64K x 8	512K

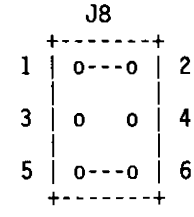
EPROM QUAD 2 RAM QUAD 1		EPROM QUAD 1 RAM QUAD 2	
XU33 D8-D15 CS2*	XU25 D0-D7 CS1*	XU16 D8-D15 CS6*	XU8 D0-D7 CS5*
XU36 D24-D31 CS4*	XU28 D16-D23 CS3*	XU19 D24-D31 CS8*	XU11 D16-D23 CS7*

RAM Base Address Select Header (J9, J10)

RAM base address is configured the same as EPROM with the exception that the headers used are J9 and J10. If RAM and EPROM devices are mixed in the sockets, do not select the same base address for RAM and EPROM. One overwrites the other. The base address defines the starting address for quad 1, and the starting address for quad 2 is offset by four times the part size. This also depends on the ROM quad enable header configuration and the RAM quad enable header configuration.

EPROM Size Select Header (J8)

Header J8 allows the user to configure the module to operate with the devices installed in the sockets. Jumpers are positioned according to the table and illustration below. The size of the device (i.e., 2K x 8) determines the position of the jumpers. Devices must all be the same size. The as-shipped configuration is shown below.



SIZE OF PART	HEADER PINS 1 TO 2	3 TO 4	5 TO 6
2K	X	X	X
4K	0	X	X
8K	X	0	X
16K	0	0	X
32K	X	X	0
64K	0	X	0

X = jumper installed

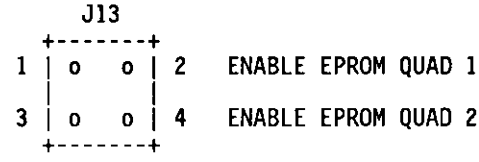
RAM Size Select Header (J15)

Refer to paragraph above. RAM size is configured the same as EPROM with the exception that the header is J15. All other information applies.

2

EPROM Quad Enable Select Header (J13)

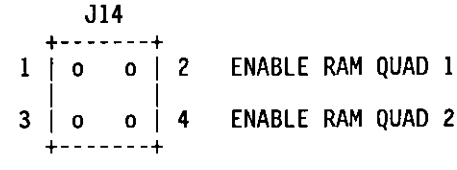
Header J13 allows the user to select quad 1 or quad 2 according to the installation of the EPROM devices. Refer to table below for quad information. To enable quad 1, install a jumper between pins 1 and 2. To enable quad 2, install a jumper between pins 3 and 4. If all EPROM in both quads, install both jumpers.



EPROM QUAD 2		EPROM QUAD 1	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

RAM Quad Enable Select Header (J14)

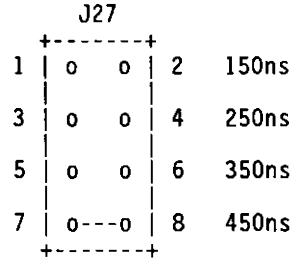
Header J14 allows the user to select quad 1 or quad 2 according to the installation of the RAM devices. Refer to the table below for quad information. To enable quad 1, install a jumper between pins 1 and 2. To enable quad 2, install a jumper between pins 3 and 4. If all RAM in both quads, install both jumpers.



RAM QUAD 1		RAM QUAD 2	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

EPROM Access Time Select Header (J27)

Header J27 is used to select the appropriate delay to compensate for the access times of the EPROM memory devices that are installed in the sockets. The access times of the EPROM devices installed should be compared with the access times in the illustration below. Install a jumper between pins that correspond to the access required by the EPROM device. Default is 450 ns as shown below:



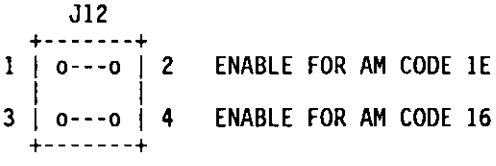
RAM Access Time Select Header (J26)

Refer to paragraph above. RAM access time is selected the same as EPROM access time except that the header is J26. All other information applies. Default is 150 ns.

2

AM1E Enable Select (Quad 2), AM16 Enable Select (Quad 1) Header (J12)

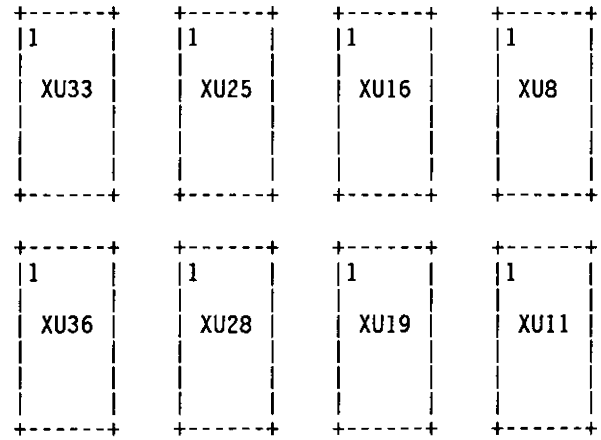
If EPROM devices are installed in EPROM quad 2, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 1E. To enable this signal, a jumper must be installed on header J12 between pins 1 and 2. See illustration and table below. If EPROM devices are installed in EPROM quad 1, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. To enable this signal, a *jumper must* be installed between pins 3 and 4.



EPROM QUAD 2		EPROM QUAD 1	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

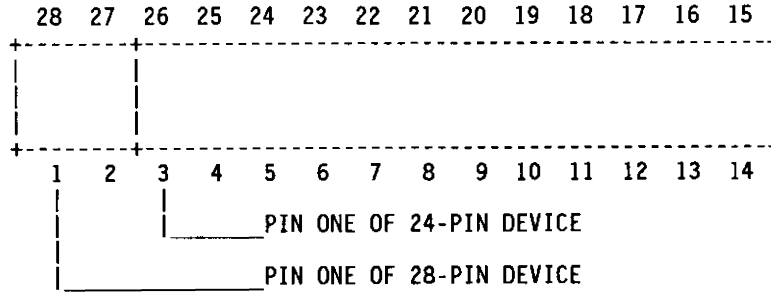
EPROM/RAM Configuration Select Headers (J3, J11, J16-J19)

Eight, 28-pin sockets may be populated by the user with 24-pin or 28-pin RAM or EPROM devices. ROM devices may be used provided the CS line is masked as true low. RAM and EPROM populations may be mixed. RAMs are installed into the sockets starting at RAM quad 1. EPROMs are installed into the sockets starting at EPROM quad 1 (refer to table in paragraph above). Configuration headers (J3,J11,J16-J19) are provided to configure each socket quad for RAM or EPROM and the type of device (i.e., 2K x 8). The socket layout on the module is illustrated below showing the corresponding headers for configuration of the sockets. Refer to the *EPROM Base Address Select Header* paragraph for four-way split information.



J11, J18, J19 J3, J16, J17

Each quad may be individually configured to accept a wide range of industry standard 24-pin and 28-pin RAM and EPROM devices. The user must provide and install the appropriate memory devices to suit the specific application intended. Devices with 28 pins are inserted with pins 1 through 28 of the device matching pins 1 through 28 of the socket. Devices with 24 pins are inserted with pins 1 through 24 of the device matching pins 3 through 26 of the socket as illustrated below.



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Associated with each socket quad are three local memory configuration headers. The headers must be configured for each quad that contains memory devices. Each figure shows the as-shipped factory configuration. The factory configuration is the same for both quads assuming 8K x 8 EPROMs.

Several RAM and EPROM devices that may be installed in the socket quads are listed in Table 2-1. The jumpering of pins on the headers for some of the configurations can be performed with the jumpers provided; other configurations may have to be done with wire wrap. Some wire wrap is necessary between pins of different headers.

TABLE 2-1. Allowable EPROM and RAM Memory Devices

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
AM2716	Advanced Micro Devices	EPROM	2K x 8	24
AM9716	Advanced Micro Devices	EPROM	2K x 8	24
HM6716	Harris	EPROM	2K x 8	24
HN462716	Hitachi	EPROM	2K x 8	24
I2716	Intel	EPROM	2K x 8	24
MBM2716	Fujitsu	EPROM	2K x 8	24
MCM2716	Motorola	EPROM	2K x 8	24
MK2716	Mostek	EPROM	2K x 8	24
MM2716	National Semiconductor	EPROM	2K x 8	24
MN2716	Panasonic	EPROM	2K x 8	24
MSM2716	OKI Electric Industry	EPROM	2K x 8	24
S4716	American Microsystems Inc.	EPROM	2K x 8	24
SM2716	Siemens	EPROM	2K x 8	24
SY2716	Synertek	EPROM	2K x 8	24
TMS2516	Texas Instruments	EPROM	2K x 8	24
TMM323	Toshiba	EPROM	2K x 8	24
UPD2716	Nippon Electric Company	EPROM	2K x 8	24

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
HN462532	Hitachi	EPROM	4K x 8	24
HN462732	Hitachi	EPROM	4K x 8	24
I2732	Intel	EPROM	4K x 8	24
MBM2732	Fujitsu	EPROM	4K x 8	24
MCM2532	Motorola	EPROM	4K x 8	24
NMC2532	National Semiconductor	EPROM	4K x 8	24
NMC2732	National Semiconductor	EPROM	4K x 8	24
TMM2732	Toshiba	EPROM	4K x 8	24
TMS2532	Texas Instruments	EPROM	4K x 8	24
UPD2732	Nippon Electric Company	EPROM	4K x 8	24
MCM68764	Motorola	EPROM	8K x 8	24
MCM68766	Motorola	EPROM	8K x 8	24
AM2764	Advanced Micro Devices	EPROM	8K x 8	28
HN2764	Hitachi	EPROM	8K x 8	28
MBM482764	Fujitsu	EPROM	8K x 8	28
MK2764	Mostek	EPROM	8K x 8	28
MSM2764	OKI Electric Industry	EPROM	8K x 8	28
NMC2564	National Semiconductor	EPROM	8K x 8	28
TMM2764	Toshiba	EPROM	8K x 8	28
TMS2564	Texas Instruments	EPROM	8K x 8	28
UPD2764	Nippon Electric Company	EPROM	8K x 8	28

2

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

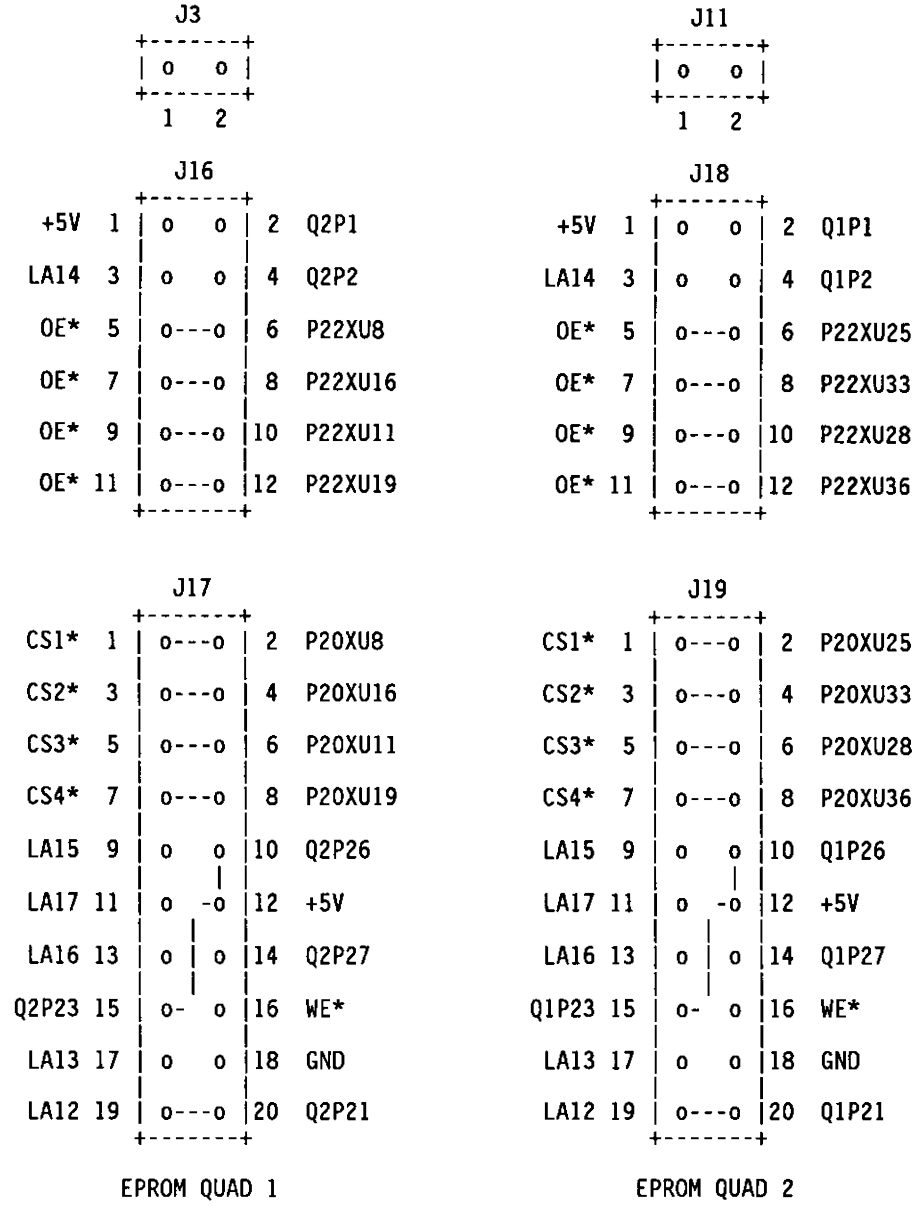
PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
AM27128	Advanced Micro Devices	EPROM	16K x 8	28
I27128	Intel	EPROM	16K x 8	28
MBM27128	Fujitsu	EPROM	16K x 8	28
TMS27128	Texas Instruments	EPROM	16K x 8	28
AM27256	Advanced Micro Devices	EPROM	32K x 8	28
I27256	Intel	EPROM	32K x 8	28
MK27256	Mostek	EPROM	32K x 8	28
TMS27256	Texas Instruments	EPROM	32K x 8	28
AM27512	Advanced Micro Devices	EPROM	64K x 8	28
I27512	Intel	EPROM	64K x 8	28
AM9218	Advanced Micro Devices	RAM	2K x 8	24
HM6116	Harris	RAM	2K x 8	24
HM6516	Harris	RAM	2K x 8	24
HM6116	Hitachi	RAM	2K x 8	24
MB2128	Fujitsu	RAM	2K x 8	24
MB8418	Fujitsu	RAM	2K x 8	24
MCM4016	Motorola	RAM	2K x 8	24
MCM65116	Motorola	RAM	2K x 8	24
MSM5116	Mitsubishi	RAM	2K x 8	24
MSM2128	OKI Electric Industry	RAM	2K x 8	24
NMC2116	National Semiconductor	RAM	2K x 8	24
SY2128	Synertek	RAM	2K x 8	24

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
TC5516	Toshiba	RAM	2K x 8	24
TC5517	Toshiba	RAM	2K x 8	24
TC5518	Toshiba	RAM	2K x 8	24
TMM2016	Toshiba	RAM	2K x 8	24
TMS4016	Texas Instruments	RAM	2K x 8	24
8148	Mostek	RAM	4K x 8	28
HM6264	Hitachi	RAM	8K x 8	28
TC5564	Toshiba	RAM	8K x 8	28
TC5565	Toshiba	RAM	8K x 8	28

2

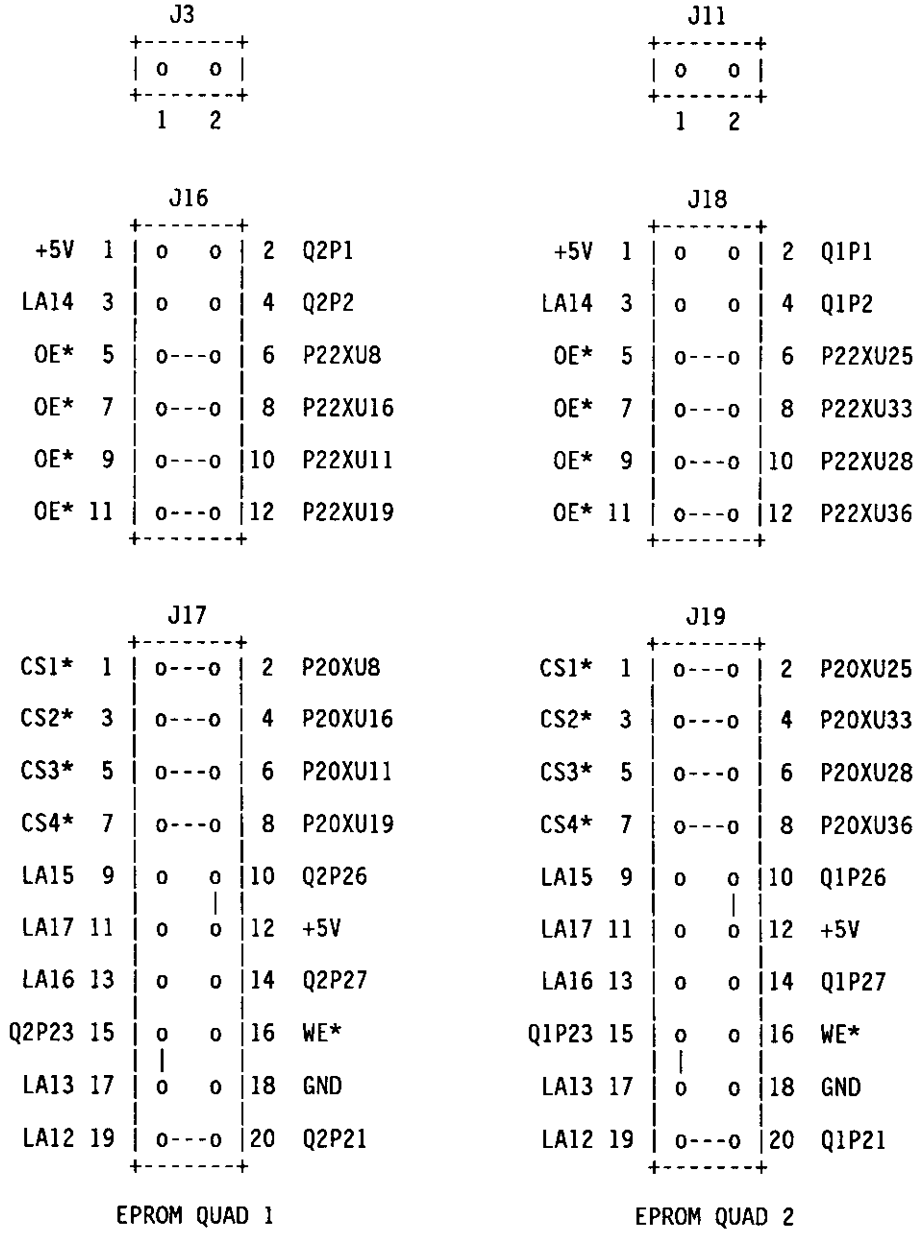
Header configuration for 2K x 8 EPROM memory devices is shown below:



EPROM QUAD 1

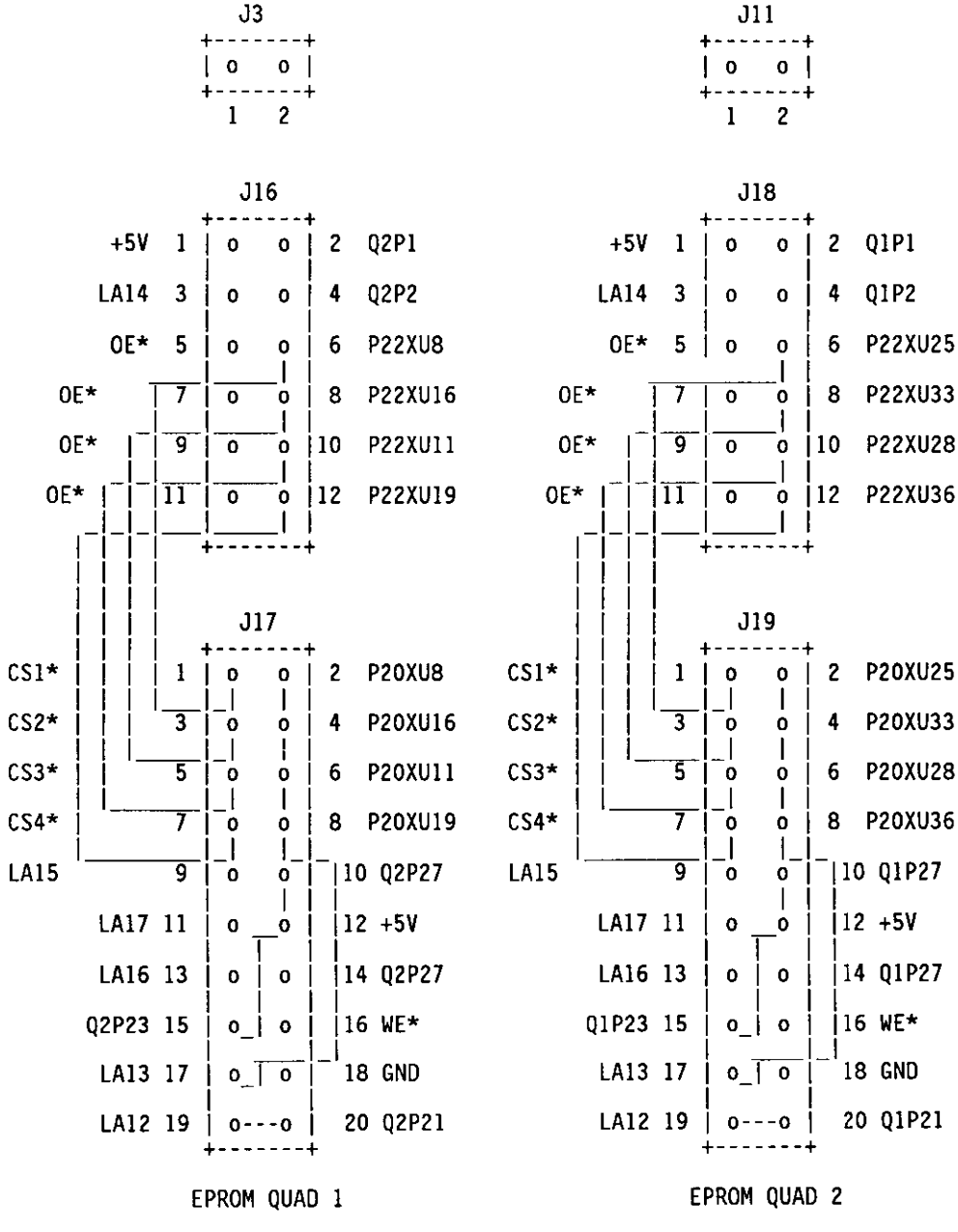
EPROM QUAD 2

Header configuration for 4K x 8 EPROM memory devices (I2732, MBM2732, NMC2732, TMM2732, UPD2732) is shown below:

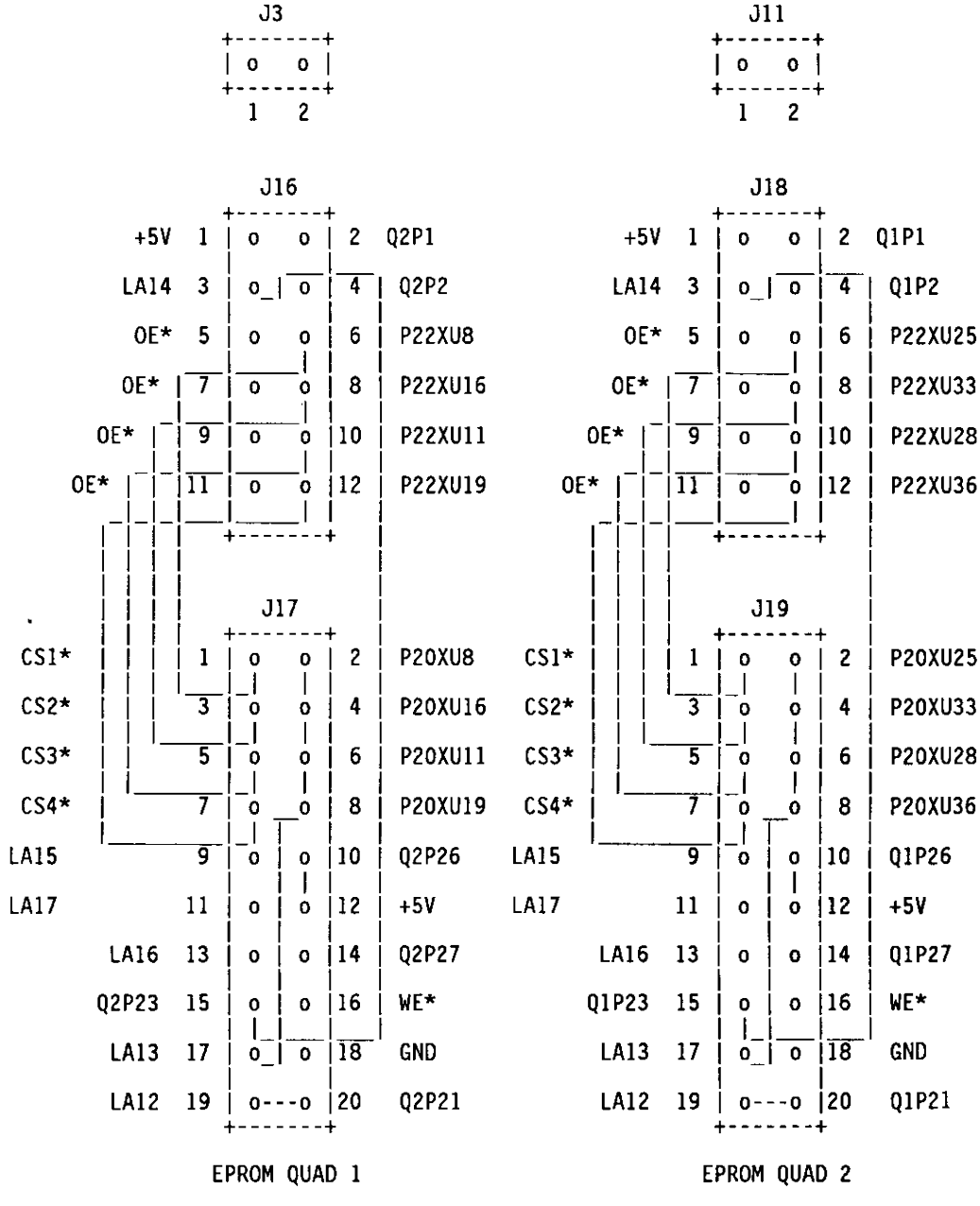


2

Header configuration for 4K x 8 EPROM memory devices (HN462532, HN462732, MCM2532, NMC2532, TMS2532) is shown below:

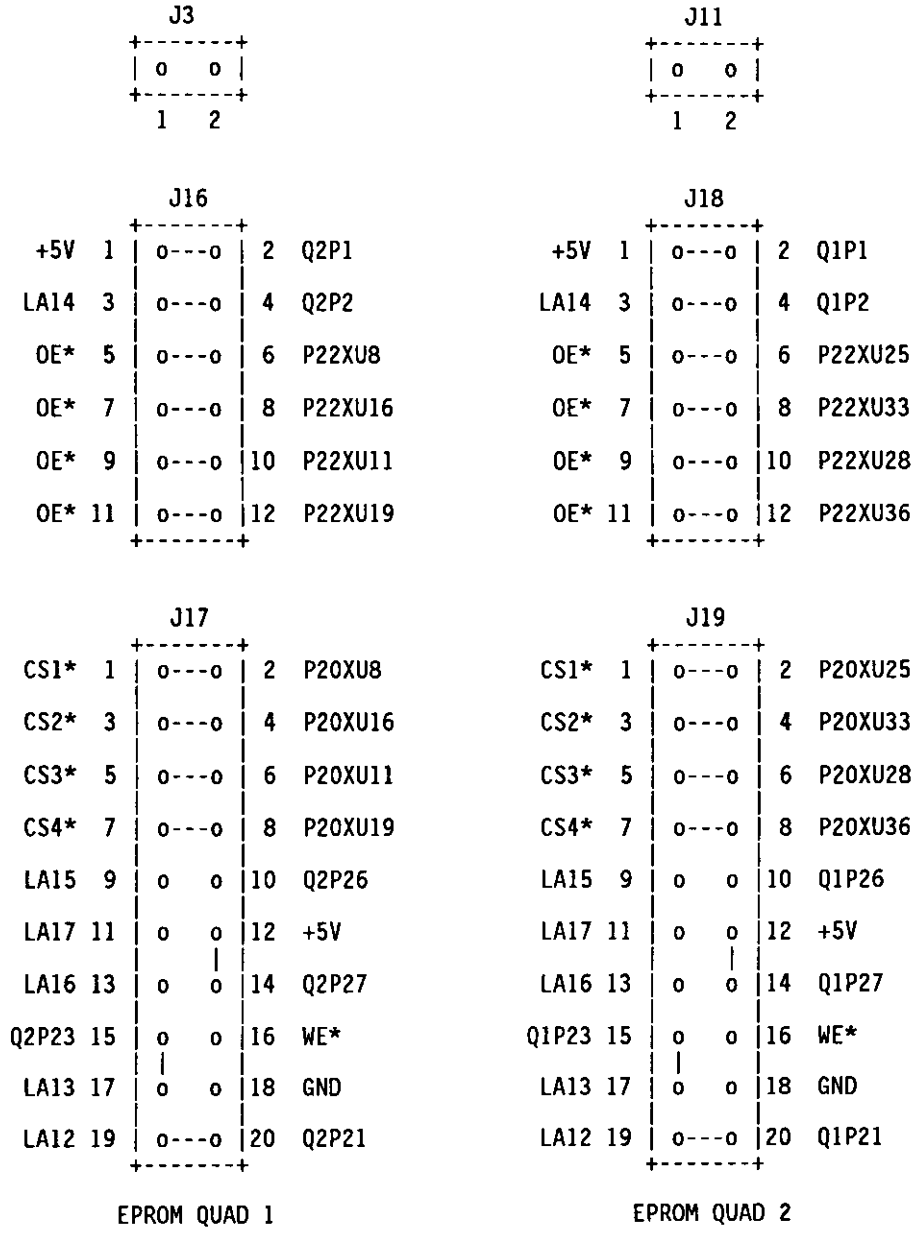


Header configuration for 8K x 8 EPROM memory devices (MCM68764, MCM68766) is shown below:

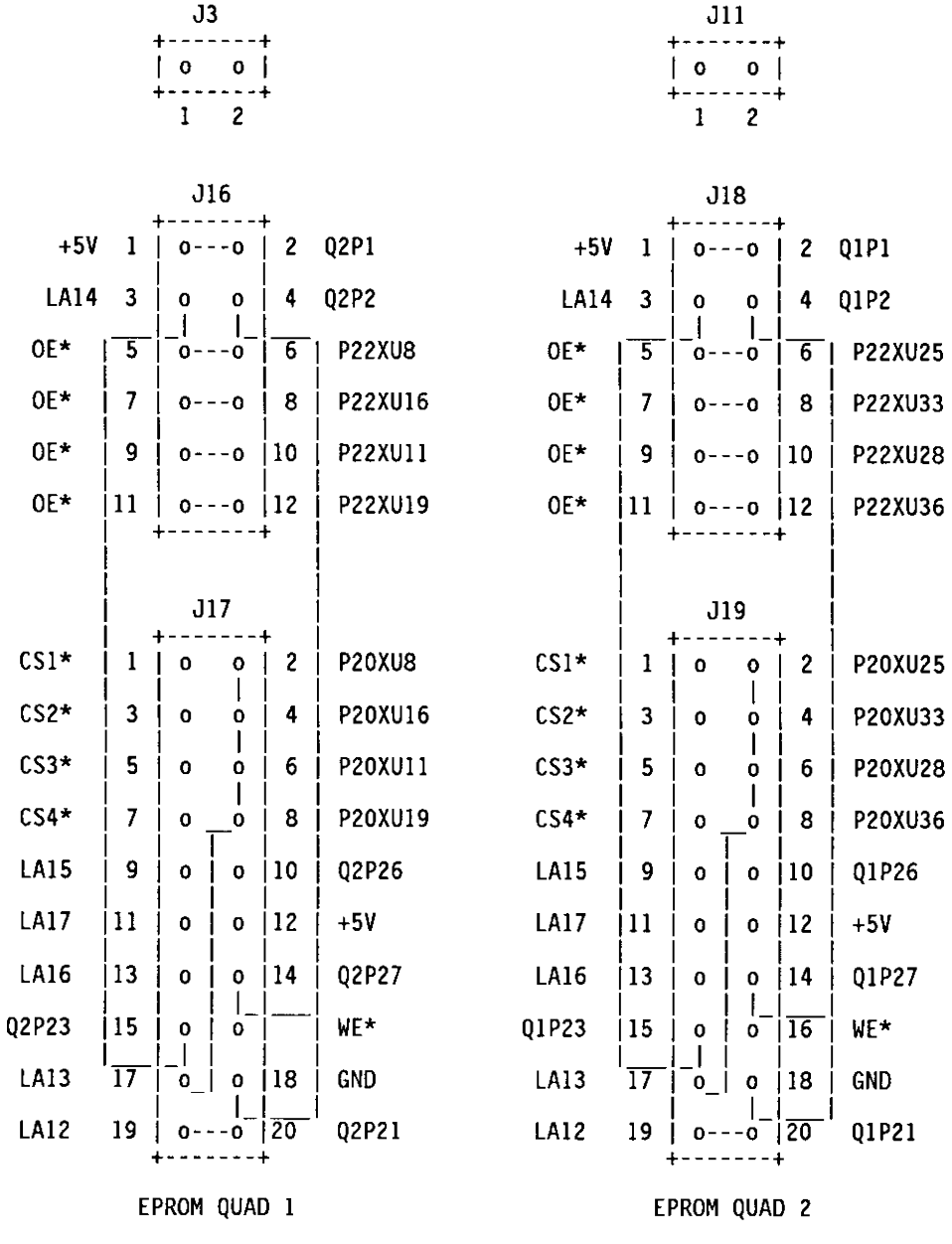


2

Header configuration for 8K x 8 EPROM memory devices (AM2764, HN2764, I2764, MBM48764, MK2764, MSM2764, TMM2764, UPD2764) is shown below:

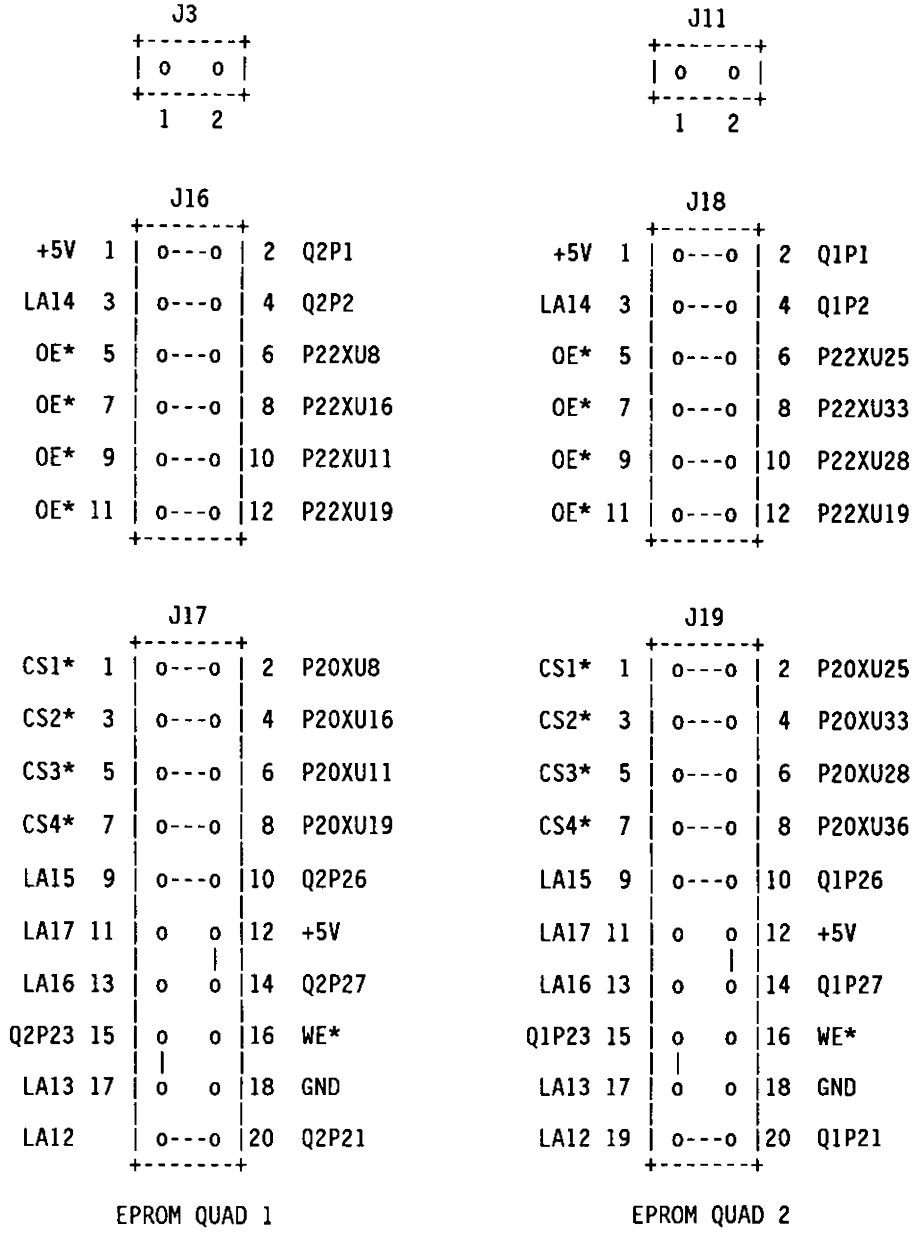


Header configuration for 8K x 8 EPROM memory devices (NMC2564, TMS2564) is shown below:

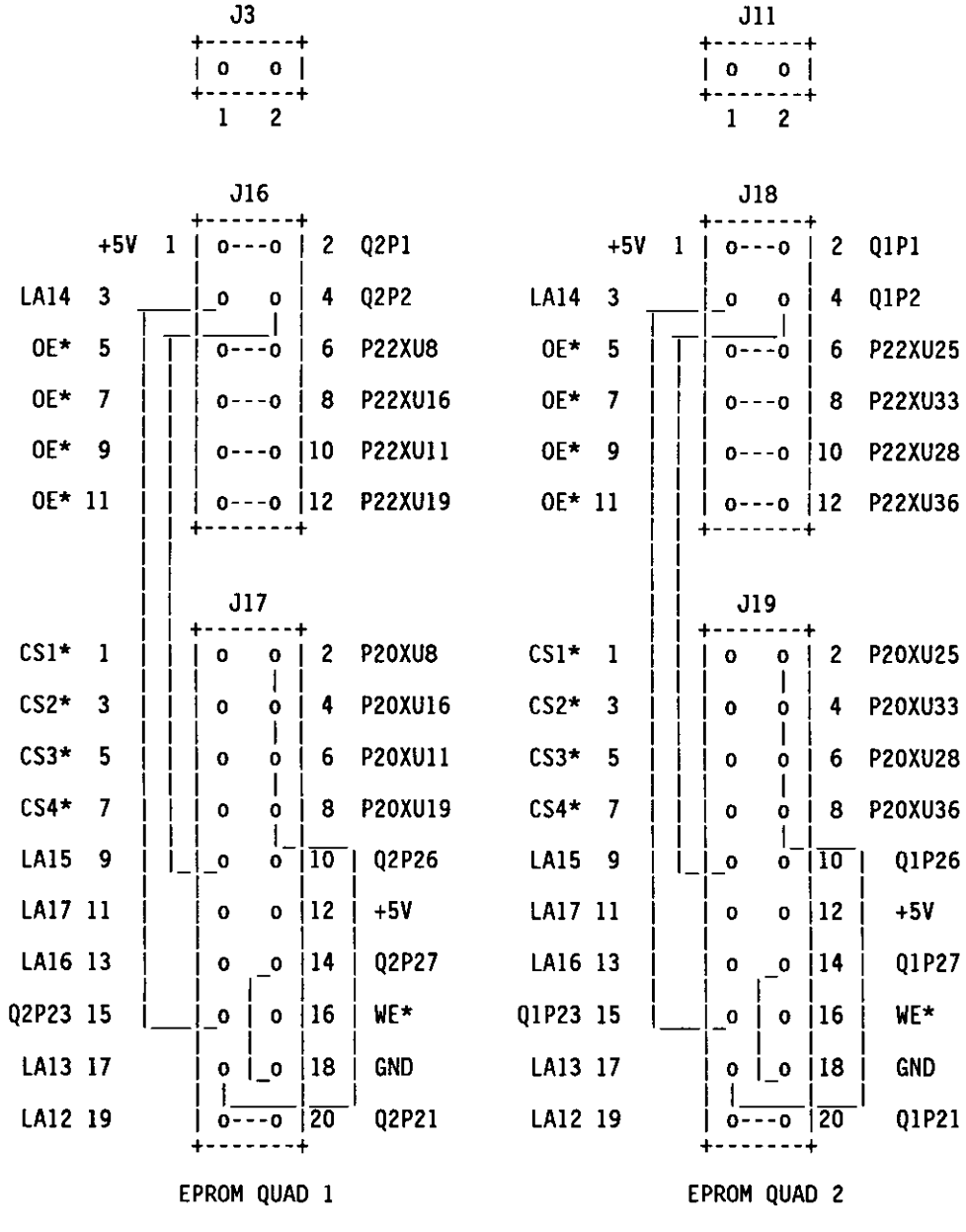


2

Header configuration for 16K x 8 EPROM memory devices (AM27128, I27128, MBM27128) is shown below:

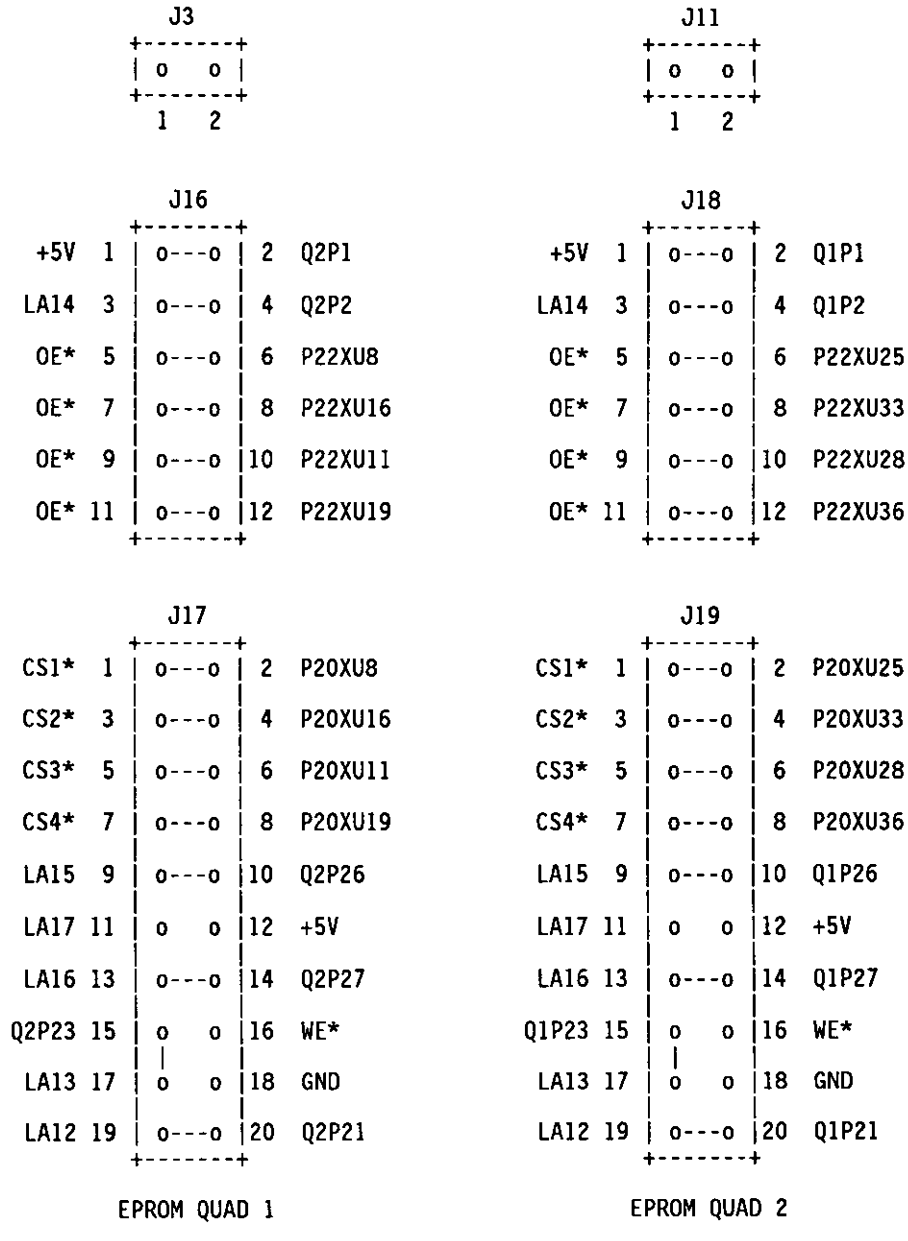


Header configuration for 16K x 8 EPROM memory devices (TMS27128) is shown below:

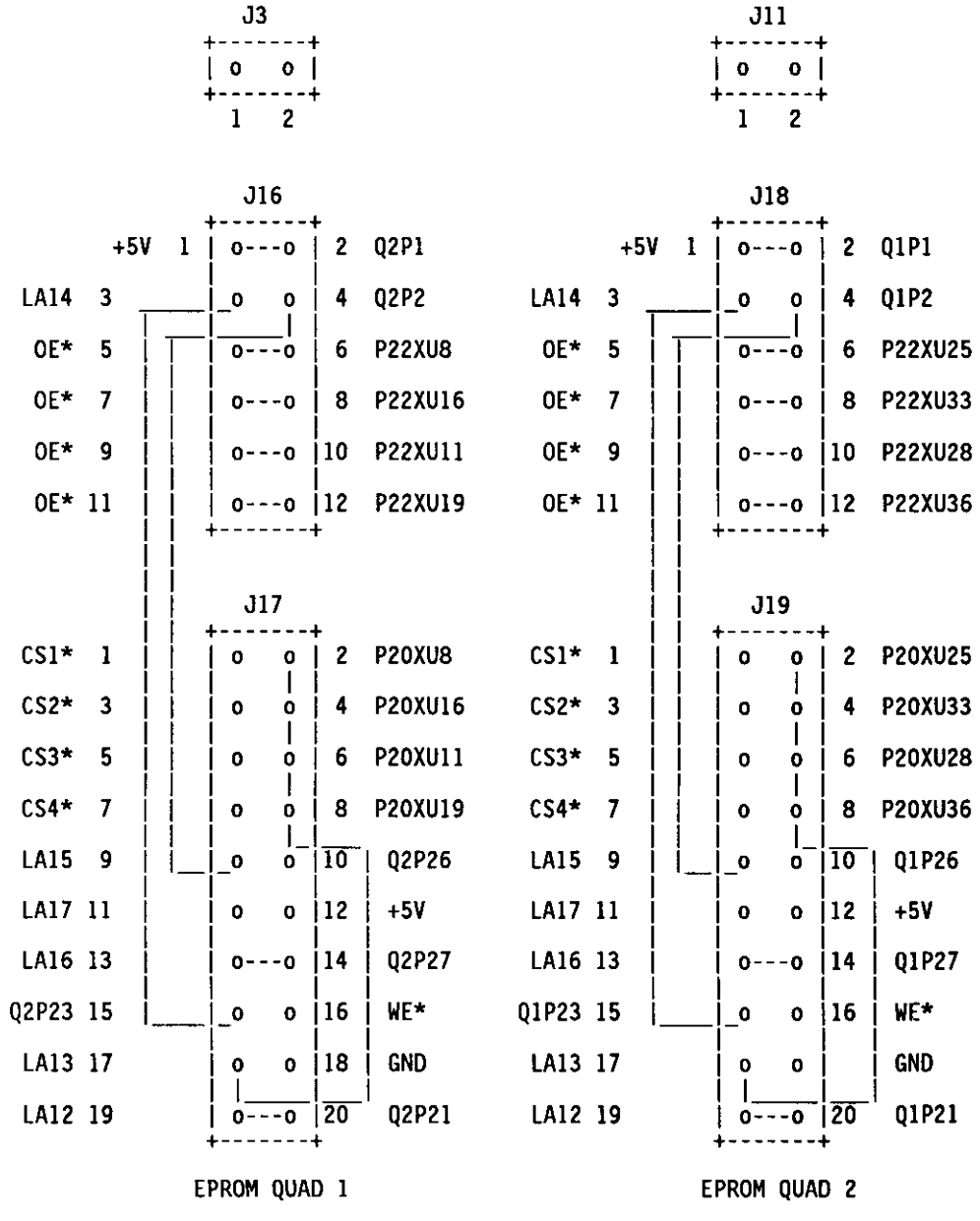


2

Header configuration for 32K x 8 EPROM memory devices (AM27256, I27256) is shown below:

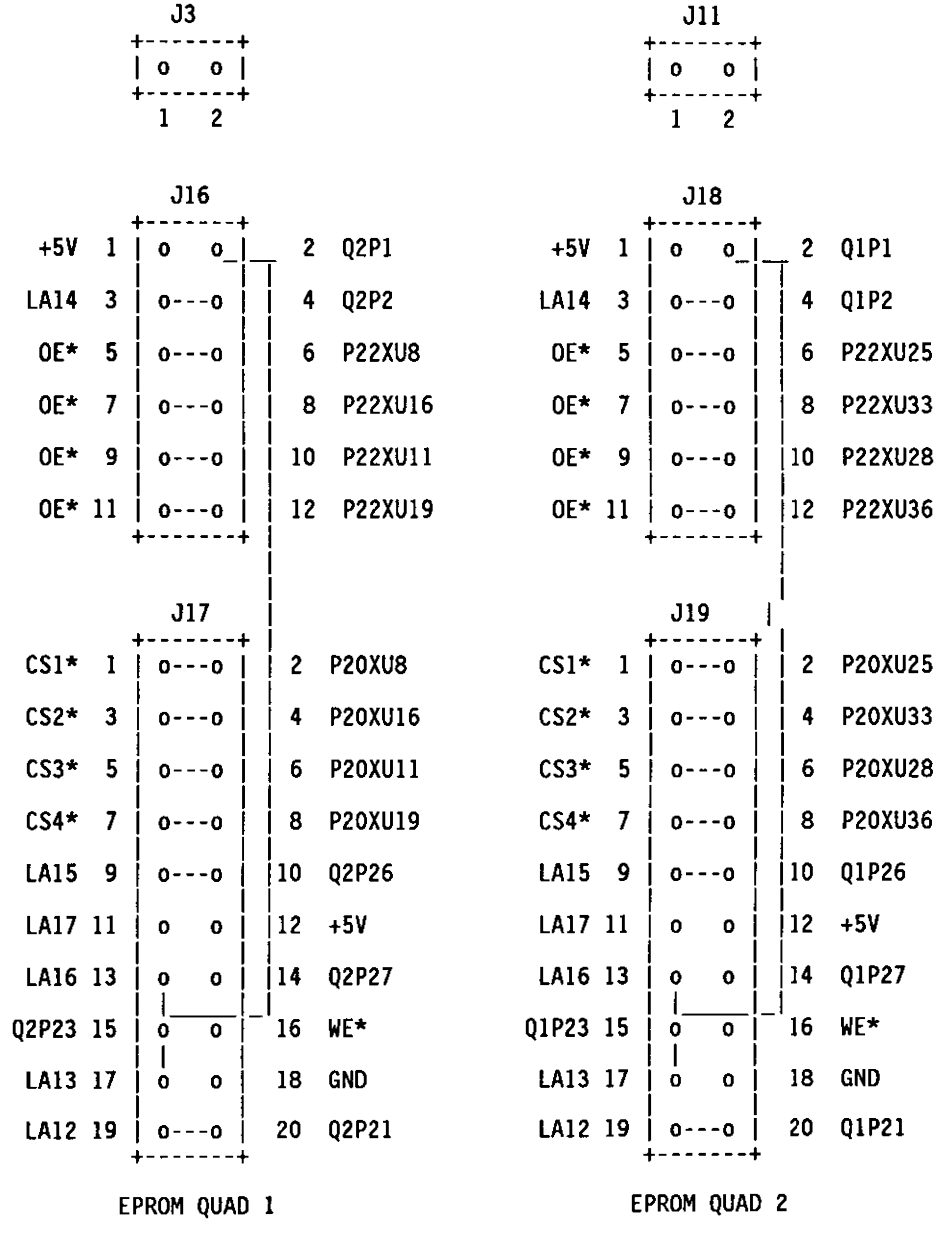


Header configuration for 32K x 8 EPROM memory devices (TMS27256) is shown below:

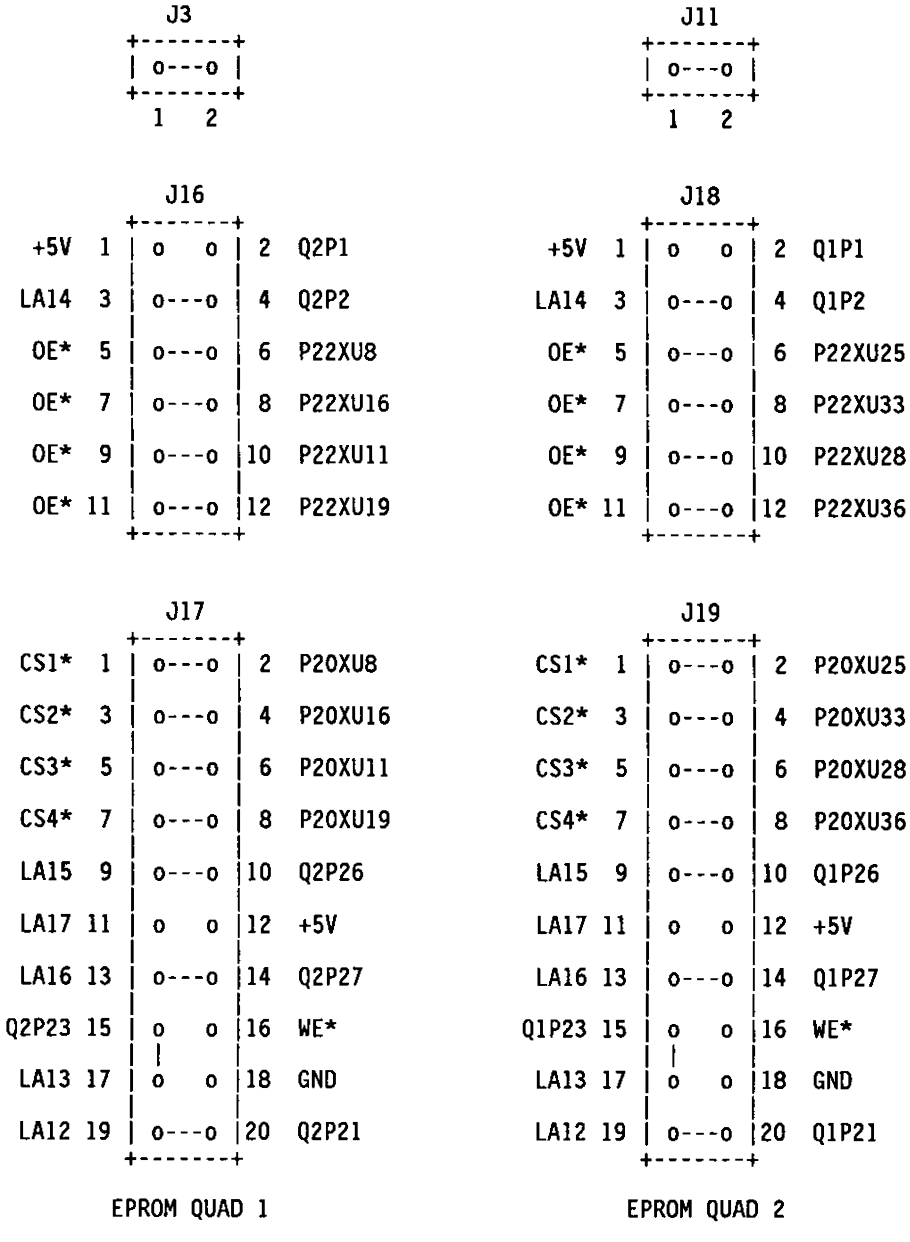


2

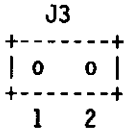
Header configuration for 32K x 8 EPROM memory devices (MK27256) is shown below:

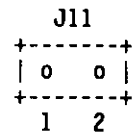


Header configuration for 64K x 8 EPROM memory devices is shown below:



Header configuration for 2K x 8 RAM memory devices is shown below:





J16

+5V	1	2	Q2P1	
LA14	3	4	Q2P2	
OE*	5	6	P22XU8	
OE*	7	8	P22XU16	
OE*	9	10	P22XU11	
OE*	11	12	P22XU19	

J18

+5V	1	2	Q1P1	
LA14	3	4	Q1P2	
OE*	5	6	P22XU25	
OE*	7	8	P22XU33	
OE*	9	10	P22XU28	
OE*	11	12	P22XU36	

J17

CS1*	1	2	P20XU8	
CS2*	3	4	P20XU16	
CS3*	5	6	P20XU11	
CS4*	7	8	P20XU19	
LA15	9	10	Q2P26	
LA17	11	12	+5V	
LA16	13	14	Q2P27	
Q2P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q2P21	

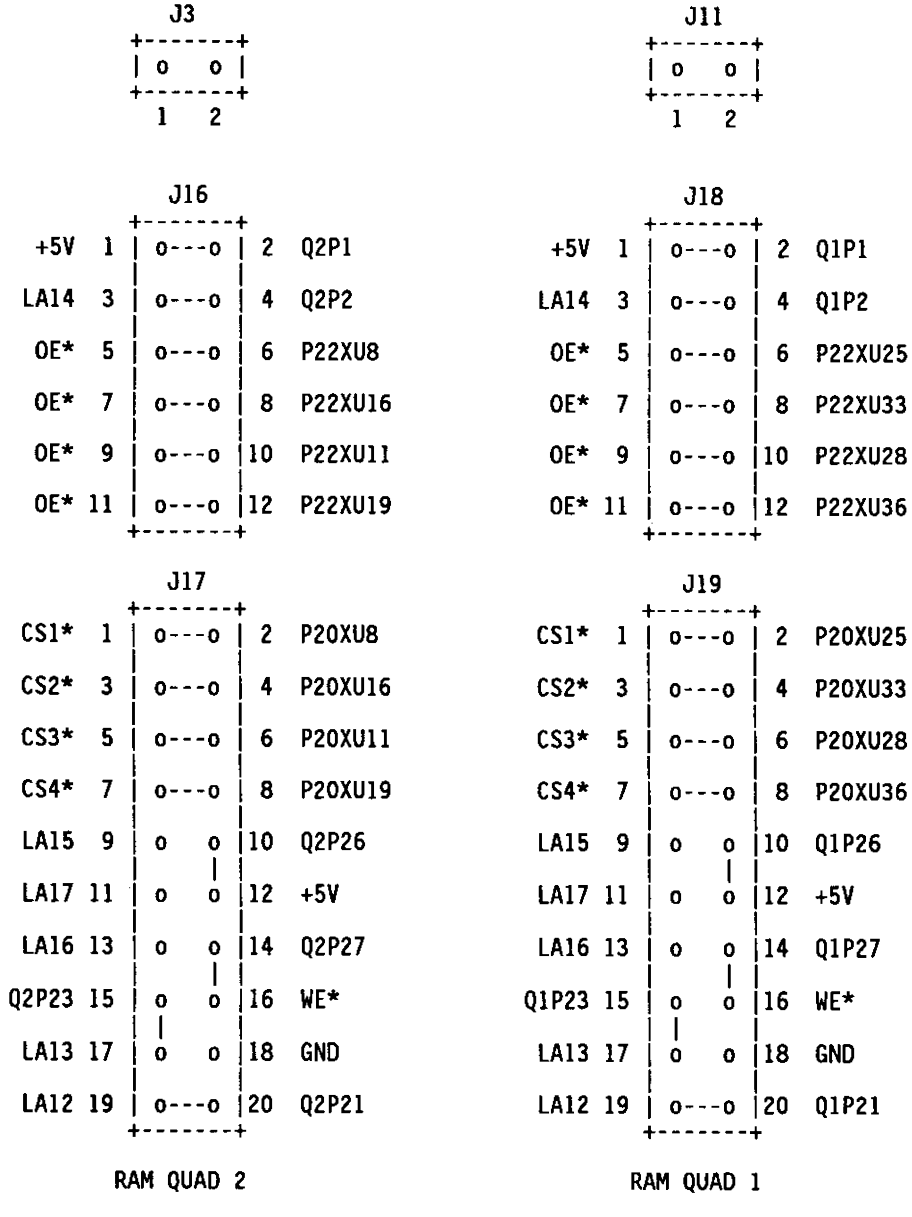
RAM QUAD 2

J19

CS1*	1	2	P20XU25	
CS2*	3	4	P20XU33	
CS3*	5	6	P20XU28	
CS4*	7	8	P20XU36	
LA15	9	10	Q1P26	
LA17	11	12	+5V	
LA16	13	14	Q1P27	
Q1P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q1P21	

RAM QUAD 1

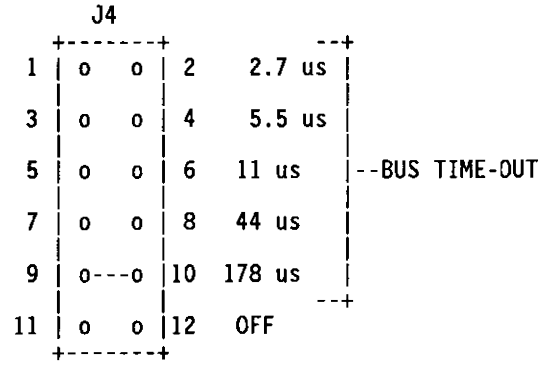
Header configuration for 8K x 8 RAM memory devices is shown below:



2

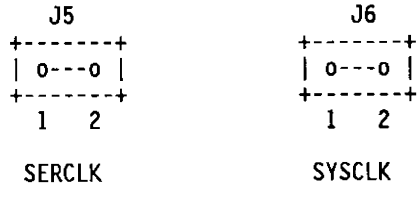
Bus Time-Out Select Header (J4)

Header J4 allows the user to select the bus time-out time after Data Strobe 0 (DS0) or Data Strobe 1 (DS1) is asserted. A time-out asserts Bus Error (BERR*). A time-out time in microseconds is selected by positioning a jumper on the desired time. Only one jumper may be installed at a time. If the controller module is not selected as the system controller, the bus time-out should be OFF. A jumper may be installed between pins 11 and 12 to turn the time-out off. Header J4 is illustrated below:



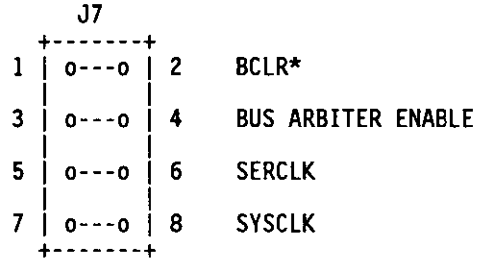
Clock Damping Shorting Select Headers (J5, J6)

An 11 ohm damping resistor may be placed in series with the driver for the Serial Clock (SERCLK) by removing the jumper from header J5. An 11 ohm damping resistor may be placed in series with the driver for the System Clock (SYSCLK) by removing the jumper from header J6. As shown below, the module is shipped with jumpers on the headers.



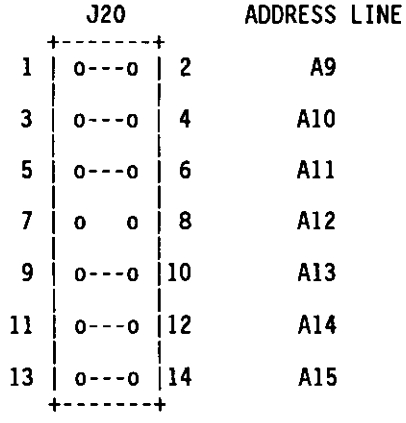
System Controller Select Header (J7)

This module may be selected as the system controller by installing all four jumpers on the header as shown below. If the module is not to be the system controller, all four jumpers must be removed from the header and header J4 pins 11 and 12 jumpered. The module is factory-configured as the system controller. If the bus arbiter is disabled, bus arbitration signals must be configured on the backplane as though the controller was an empty slot as shown in the *VMEmodule Chassis Backplane Daisy-Chained Headers* paragraph. The IACK bypass jumper must remain open.



I/O Base Address Select Header (512 Byte Boundaries) (J20)

The address line must be low to correspond with a jumper installed. As shown below, the base address is FF1000.



JUMPER IN = ADDRESS LINE LOW

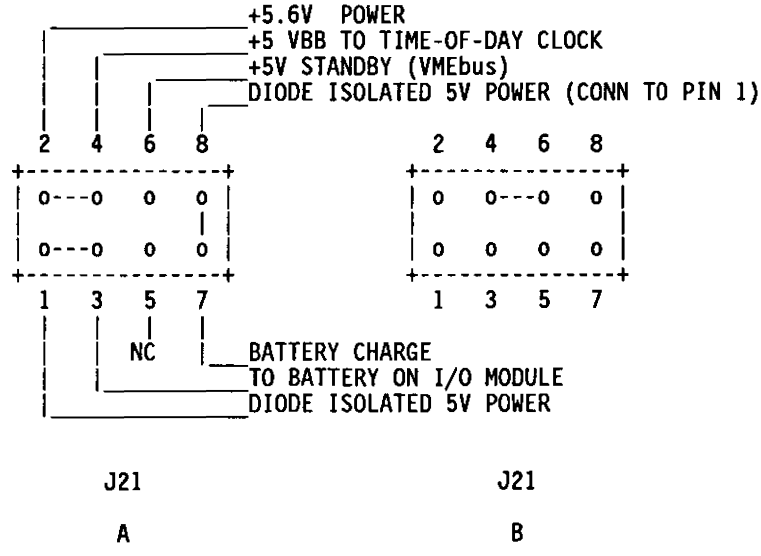
DEFAULT SHOWN = 10XX WITHIN SHORT ADDRESSING RANGE
AM CODES = 2D OR 29

Time-of-Day Clock Power Select and Battery Charge Header (J21)

Header J21 is used to select the method of powering the time-of-day clock. As shown in illustration A below, the normal configuration powers the time-of-day clock from system power while the system is ON and from the backup batteries while the system is OFF. As shown in illustration A, installing a jumper between pins 7 and 8 allow the backup batteries to be charged while the system is ON. Illustration B shows the jumper position to power the time-of-day clock from the +5V STANDBY on the VMEbus. The charge voltage is limited to 5.6 Vdc and the charge current limited to approximately 20 mA.

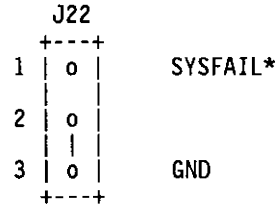
NOTE

Batteries are not supplied with the I/O module and must be supplied by the user.



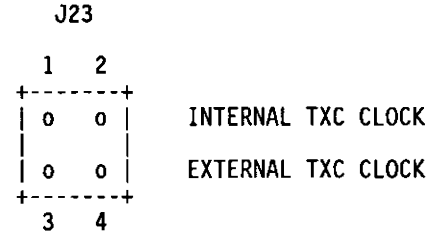
System Fail (SYSFAIL*) or GND Select for Interrupt Source Header (J22).

Header J22 allows the user to enable the input to the Bus Interrupt Module (BIM) to be held low to provide for one software controlled global interrupt. The user may select the SYSFAIL* line to generate a global system failure interrupt. When the jumper is positioned between pins 1 and 2, the SYSFAIL* line is asserted. The BIM interrupt is enabled when the jumper is positioned between pins 2 and 3. As shown below, the module is shipped with the SYSFAIL* line asserted.



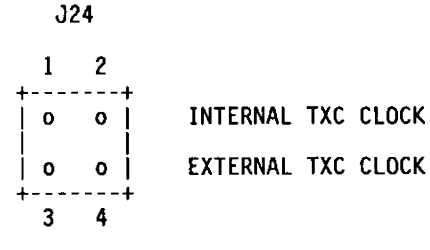
Internal/External Transmit Clock Serial Port 1 Select Header (J23)

The Transmit Clock (TxC) signal on RS-232C port 1 may be selected as an output or an input. For the signal to be an output, the jumper is positioned between pins 1 and 2. The signal is an input if the jumper is positioned between pins 3 and 4. The module is shipped without jumpers as shown below:



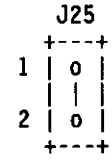
Internal/External Transmit Clock Serial Port 2 Select Header (J24)

The TxC signal on the RS-232C port 2 may be selected as an output or an input. For the signal to be an output, the jumper is positioned between pins 1 and 2. The signal is an input if the jumper is positioned between pins 3 and 4. The module is shipped without jumpers as shown below:



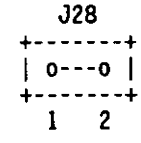
Display Blanking Enable Select Header (J25)

A two-character Light Emitting Diode (LED) display is provided on the front panel of the controller module for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register. Header J25 works with section 8 of the front panel switch. With the jumper removed from the header, the switch has no effect. With the jumper installed, if the switch is OFF (open), the displays operate normally. If the switch is ON (closed), the displays are blanked (no display). If the display is not blanked by J25 and switch section 8, software may control the blanking by writing to the blanking register -- D3 = 0 = OFF; D3 = 1 = ON. Refer to the I/O memory map for address. Reset turns the display on if blanked by software. As shown below, the module is shipped with the jumper installed.



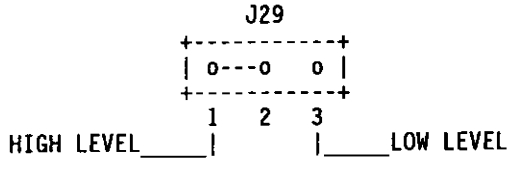
RESET Switch Disable Select Header (J28)

The front panel RESET switch on the controller module may be disabled. The switch is disabled when the jumper is removed from the header. As shown below, the module is shipped with the jumper installed.



Printer Acknowledge Level Select Header (J29)

Header J29 is provided as a means of selecting the high level or low level of the printer acknowledge signal. The module is shipped with the jumper installed between pins 1 and 2 (high level selected). The low level is selected by positioning the jumper between pins 2 and 3.



NOTE

The printer acknowledge flag register latches the acknowledge signal from the printer and must be cleared by reading the printer strobe register. If the printer is still holding the acknowledge signal, the flag does not clear. The correct sequence is: 1. clear acknowledge, 2. check acknowledge flag, 3. if not clear, go back to 1.

INSTALLATION INSTRUCTIONS

The following paragraphs discuss installation of the module into the chassis. Ensure that EPROM and/or RAM memory devices are installed and configured and that all other headers on both modules are configured for desired operation.

Module Installation

Now that the module is ready for installation, proceed as follows:

a. Turn all equipment power OFF and disconnect power cable from ac power source.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

b. Remove chassis cover as instructed in the equipment user's manual.

c. Remove the filler panel from the appropriate card slot at the front of the chassis. If the MVME050 is configured as the system controller, it must be installed in the left most card slot (slot 1) to correctly initiate the bus grant daisy-chain and the IACK daisy-chain.

d. Insert the MVME050 into the selected card slot. Be sure module is seated properly into the connectors on the backplane. Fasten the module in the chassis with the screws provided.

e. Remove IACK and BG jumpers from header on chassis backplane for card slot the MVME050 is installed in.

f. Connect any desired cables to the MVME050 module at the P2 backplane connector, to mate with optional peripherals at the RS-232C serial ports, and optional remote reset switch. These cables are user supplied unless the transition is used.

g. Replace cover and turn equipment power ON.

VMEmodule Chassis Backplane Daisy-Chained Headers

Whenever there are any empty slots between modules in the VMEmodule chassis, jumpers must be installed on the backplane headers at the empty slot locations to continue the bus arbitration signals and the acknowledge signals across the empty slot(s). Refer to the *System Controller Select Header* paragraph in this chapter for information on bus grant signals. The table below is a list of backplane pins to be daisy-chained across the empty slot(s).

BACKPLANE PIN NO.			REMARKS		
A21	to	A22	IACKIN*	to	IACKOUT*
B4	to	B5	BG0IN*	to	BG0OUT*
B6	to	B7	BG1IN*	to	BG1OUT*
B8	to	B9	BG2IN*	to	BG2OUT*
B10	to	B11	BG3IN*	to	BG3OUT*

CHAPTER 3 - OPERATING INSTRUCTIONS

INTRODUCTION

This chapter provides the necessary information to use the MVME050 module in a system configuration.

CONTROLS AND INDICATORS

The MVME050 has a RESET switch, an eight section readable switch, a FAIL indicator, a RUN indicator, and a two segment display indicator.

RESET Switch

The reset performed by the RESET switch is a system-level function. The RESET switch may be disabled by removing a jumper from header J28. Pressing the RESET switch asserts the reset signal.

Pressing the RESET switch enables the RESET signal to generate the System Reset (SYSRESET*), which is sent via the VMEbus, to the other modules in the system.

RUN Indicator

The RUN indicator is lit whenever the System Fail (SYSFAIL*) line is high and the MVME050 is operational.

FAIL Indicator

The FAIL indicator is lit whenever the MVME050 detects the SYSFAIL* line low on the VMEbus and the MVME050 is not operational.

User Status Display

The user status display indicator is provided for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register. The display may be blanked by section 8 of the readable switch or by software (refer to the *Display Blanking Enable Select Header* paragraph in Chapter 2). If blanked by software, a system reset turns the display on. D7-D4 is latched and displayed in the top display. D3-D0 is latched and displayed in the bottom display. Refer to the I/O memory map for address.

User 8-Section Software-Readable Switch

The piano type 8-section switch on the front panel is a software-readable switch. The user may include the functions of this switch in the software program. Section 8 of this switch may also function as blanking for the user status display. Refer to the I/O memory map for address.

I/O MEMORY MAP

The I/O memory is shown below:

ADDRESS	FUNCTION
FFXX00 - FFXX3F	MPCC1 64 BYTES ODD BYTES ONLY
FFXX40 - FFXX7F	MPCC2 64 BYTES ODD BYTES ONLY
FFXX80 - FFXX9F	PRINTER 32 BYTES ODD BYTES ONLY
FFXX81	(WRITE D0-D7) PRINTER DATA REGISTER
FFXX81	(READ) - PUTS FF INTO DATA OUT REGISTER
FFXX83	(WRITE D3) PRINTER STROBE REGISTER
FFXX83	(READ) - CLEARS ACKNOWLEDGE FLAG AND PRINTER IRQ
FFXX85	(WRITE) HARDWARE BUFFER CONFLICT
FFXX85	(READ) - PRINTER STATUS D0 = SELECT FROM PRINTER D1 = BUSY FROM PRINTER D2 = FAULT FROM PRINTER D7 = ACKNOWLEDGE FROM PRINTER
FFXX87	(WRITE D3) PRINTER INPUT PRIME
FFXX87	(READ) - NO OPERATION
FFXX89	(WRITE) - NO OPERATION
FFXX89	(READ D7) STATUS OF SYSFAIL* ON VMEbus
FFXX8B	(WRITE D3) BLANKING TO FRONT PANEL (0 = OFF)
FFXX8B	(READ) - NO OPERATION
FFXXA0 - FFXXBF	FRONT PANEL DISPLAY - 32 BYTES ODD ONLY (WRITE ONLY)
FFXXA0 - FFXXBF	FRONT PANEL SWITCH - 32 BYTES ODD ONLY (READ ONLY)
FFXXC0 - FFXXDF	BIM 1 - 32 BYTES ODD ONLY
FFXXE0 - FFXXFF	BIM 2 - 32 BYTES ODD ONLY
FFX100 - FFX17F	TIME-OF-DAY CLOCK - 128 BYTES ODD ONLY

XX = 00---> FE ON 512 BYTE BOUNDARIES

CHAPTER 4 - FUNCTIONAL DESCRIPTION

INTRODUCTION

This chapter provides the overall block diagram level description for the MVME050 module. The general description provides a overview of the module, followed by a detailed description of each section of the module. The block diagram of the MVME050 is shown in Figure 4-1.

GENERAL DESCRIPTION

In normal operation, the MVME050 provides all the system controller functions required for a VMEbus system. For time-of-day accesses, the system software reads the time from the time-of-day clock. Two serial ports may be used by the system software for interfacing to terminals, modems, or data links. Hard copy output is available via the Centronics-type printer port. EPROM/RAM sockets may be used as general system memory or to hold debug and/or diagnostics programs and scratch pad RAM.

In many multiprocessor systems, it is desirable for a process executing in one MPU module to interrupt a process being executed by another MPU module. The global interrupter (complete with semaphore) provides this global interrupting capability.

BLOCK DIAGRAM DESCRIPTION

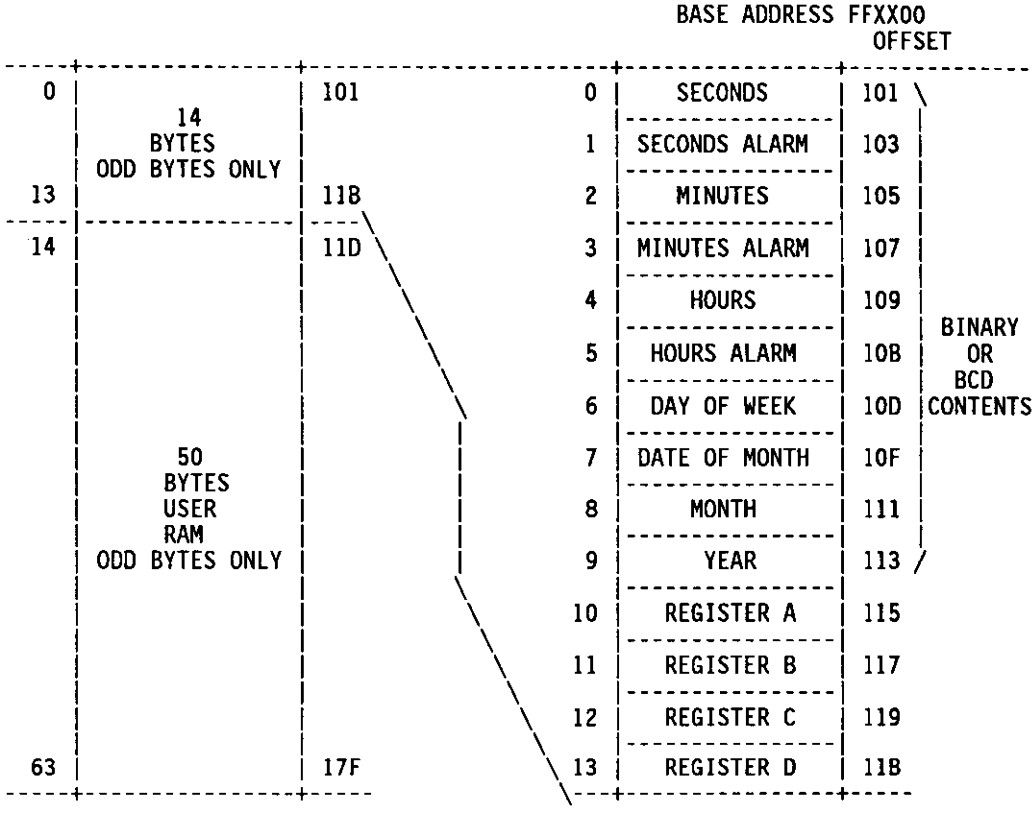
The controller operates through the following functional logic blocks.

- Time-of-day clock
- EPROM/RAM sockets
- Serial ports
- Centronics parallel printer port
- Global interrupter
- Battery backup
- Bus arbiter
- System clock generator
- Serial bus clock generator
- Bus time-out generator
- Power up reset
- RESET switch
- VMEbus interface
- User display
- Front panel lights

Time-of-Day Clock

The time-of-day clock (MC146818) provides the time keeping functions for a VME system and relieves the system software of the time keeping workload. The clock counts seconds, minutes, hours, days of the week, date, month, and year. The clock is capable of generating a VMEbus interrupt for time-of-day alarm, once-per-second to once-per-day, periodic rates from 100 microseconds to one-half second, or end-of-clock update cycle. The clock may be backed up by an external battery (located on the I/O module). The clock device also provides 50 bytes of RAM for storing system parameters during power down conditions. See address map below:

ADDRESS MAP



EPROM/RAM Sockets

Eight, 28-pin sockets may be populated by the user with 24-pin or 28-pin RAM, or EPROM devices. RAM and EPROM populations may be mixed. RAMs are loaded into the sockets starting at XU25, XU33, XU28, XU36 (RAM quad 1). EPROMs are loaded into the sockets starting at XU8, XU16, XU11, XU19 (EPROM quad 1). Socket configuration headers are provided to configure each socket quad for RAM or EPROM and the type of device.

The VMEbus base address for accessing EPROM/RAM is set by jumper position on the appropriate headers. If both socket quads are populated with RAM, the RAM base address is set with the RAM header, and the RAM addressing becomes contiguous across the socket quad boundary. The EPROM base address header is ignored. If both socket quads are populated with EPROM, the base address is set with the EPROM headers, and the addressing becomes contiguous across the socket quad boundary. When both RAM and EPROM populations are used, the RAM base address is set by the RAM header and the EPROM base address is set by the ROM/EPROM header. If EPROM devices are installed in EPROM quad 2, they are capable of being accessed when a bus master initiates a VMEbus transfer using Address Modifier (AM) code 1E. If EPROM devices are installed in EPROM quad 1, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. When this type of access occurs, no other devices on the module are accessed and the EPROM base address circuitry is disabled. This feature may be disabled by removing the jumpers at J12. Refer to the *AM1E Enable Select (Quad 1)*, *AM16 Enable Select (Quad 2) Header (J12)* paragraph in Chapter 2.

The EPROM/RAM devices supported by the MVME050 are listed in Table 2-1. Separate Data Transfer Acknowledge (DTACK*) timing headers are provided for separately timing the accesses from RAM or EPROM. This allows both fast RAMs and slow EPROM devices to be used on the same module without impacting the performance of the faster parts.

Serial Ports

Two independent, Multi-Protocol Communications Controllers (MPCC) (R68560) interface with connector P2 on the MVME050 and the RS-232C serial ports on the I/O module.

Serial ports Interrupt Request (IRQ*) line goes into Bus Interrupter Module (BIM 1) (MC68153). Interrupt (INT0) and INT1 are the BIM control register and BIM vector register as shown below:

Serial port 1	BIM	control register = FFXXC1
	BIM	vector register = FFXXC9
Serial port 2	BIM	control register = FFXXC3
	BIM	vector register = FFXXCB

Interrupts can be enabled to the VMEbus by writing to the BIM control register (refer to the MC68153 Data Sheet).

NOTE

The BIM must be initialized for external vector in control register 0 and 1 because the R68560 supplies the interrupt vector. If the BIM is initialized for internal vector, both devices supply the vector, which causes a buffer conflict.

A sample initialization procedure for asynchronous mode 9600 baud and no interrupts is shown below:

```
00---> RCR    Receiver control register
80---> TCR    Transmitter control register
C0---> SICR   Serial interface control register
1E---> PSR2   Protocol select register 2
8B---> BRDR1  Baud rate divider register 1
00---> BRDR2  Baud rate divider register 2
1D---> CCR    Clock control register
```

Now the MPCC is ready to transmit and receive characters.

The following table lists port 1 and port 2 addresses, reset values and MPCC registers.

HEX ADDRESS PORT 1	HEX ADDRESS PORT 2	RESET VALUE	ASYNCHRONOUS MODE 9600 NO INTERRUPTS	MPCC REGISTER
FFXX01	FFXX41	00		RSR
FFXX03	FFXX43	01	00	RCR
FFXX05	FFXX45			RDR
FFXX07	FFXX47	00		
FFXX09	FFXX49	0F		RIVNR
FFXX0B	FFXX4B	00		RIER
FFXX0D	FFXX4D	00		
FFXX0F	FFXX4F	00		
FFXX11	FFXX51	80		TSR
FFXX13	FFXX53	01	80	TCR
FFXX15	FFXX55			TDR
FFXX17	FFXX57	00		
FFXX19	FFXX59	0F		TIVNR
FFXX1B	FFXX5B	00		TIER
FFXX1D	FFXX5D	00		
FFXX1F	FFXX5F	00		
FFXX21	FFXX61	00		SISR
FFXX23	FFXX63	00	C0	SICR
FFXX25	FFXX65			
FFXX27	FFXX67			
FFXX29	FFXX69	0F		SIVNR
FFXX2B	FFXX6B	00		SIER
FFXX2D	FFXX6D	00		
FFXX2F	FFXX6F	00		
FFXX31	FFXX71	00		PSR1
FFXX33	FFXX73	00	1E	PSR2
FFXX35	FFXX75	00		AR1
FFXX37	FFXX77	00		AR2
FFXX39	FFXX79	01	8B	BRD1
FFXX3B	FFXX7B	00	00	BRD2
FFXX3D	FFXX7D	00	1D	CCR
FFXX3F	FFXX7F	04		ECR

XX = 00---> FE

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the baud rate divider circuit. BRDR1 contains the Least Significant Half (LSH) and BRDR2 contains the Most Significant Half (MSH). With an 8 MHz External Crystal (EXTAL) input, standard bit rates can be selected using a combination of prescaler divider (in the Clock Control Register (CCR)) and baud rate divider values shown in Table 4-1. A system reset resets the MPCC.

TABLE 4-1. Standard Baud Selection

DESIRED BAUD RATE	K VALUE	PRESCALER DIVIDER	BAUD RATE DIVIDER DECIMAL	BAUD RATE DIVIDER HEXADECIMAL MSH	LSH
			ASYNCHRONOUS MODE		
50	2	3	26,667	68	2B
75	2	2	26,667	68	2B
110	2	3	12,121	2F	59
135	2	2	14,815	39	DF
150	2	3	8,889	22	B9
300	2	2	6,667	1A	0B
1200	2	3	1,111	04	57
1800	2	2	1,111	04	57
2400	2	2	883	03	41
3600	2	2	556	02	2C
4800	2	3	278	01	16
7200	2	2	278	01	16
9600	2	3	139	00	8B
19200	2	2	104	00	68
38400	2	2	52	00	34
			ISOCHRONOUS AND SYNCHRONOUS		
50	1	3	53,333	D0	55
75	1	2	53,333	D0	55
100	1	3	24,242	5E	B2
135	1	2	29,630	73	BE
150	1	3	17,778	45	72
300	1	2	13,333	34	15
1200	1	3	2,222	08	AE
1800	1	2	2,222	08	AE
2400	1	2	1,667	06	83
3600	1	2	1,111	04	57
4800	1	3	556	02	2C
7200	1	2	556	02	2C
9600	1	3	278	01	16
19200	1	2	208	00	D0
38400	1	2	104	00	68

PRESCALER DIVIDER: 0 = DIVIDE BY 2
1 = DIVIDE BY 3

K = 1 FOR ISOCHRONOUS AND SYNCHRONOUS
2 FOR ASYNCHRONOUS

Centronics Parallel Printer Port

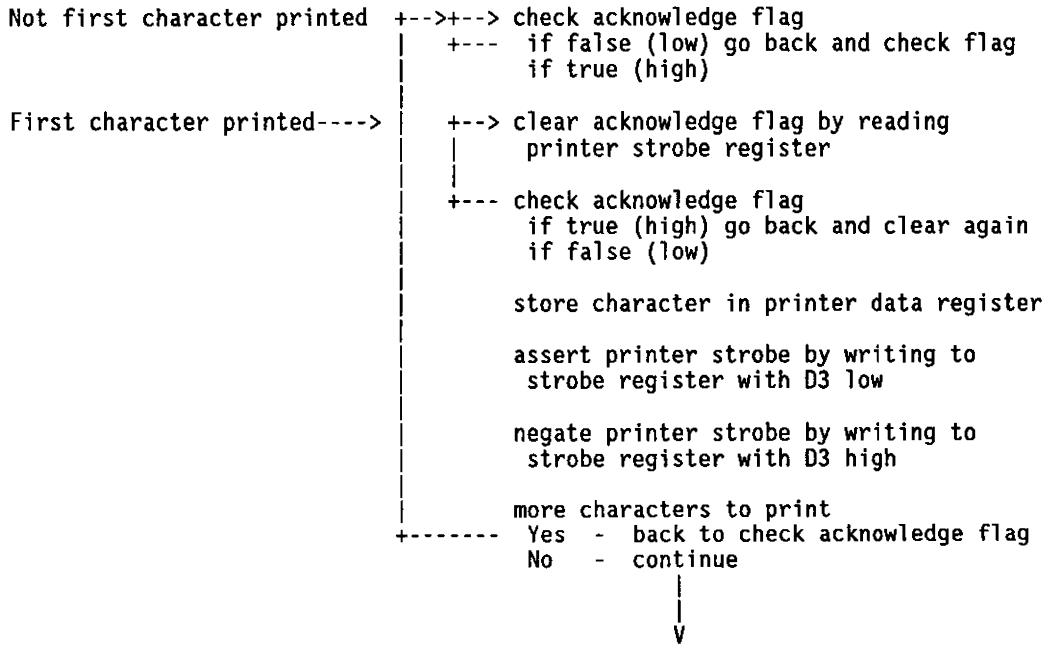
The parallel I/O port is designed to operate with a Centronics printer. The signal lines are buffered and are available at connector P2. The printer port consists of an 8-bit data register, a strobe output, an input prime, output registers, an acknowledge input, and a 4-bit status register.

The printer strobe register and the input prime register are both initialized (set high) by reset. Input prime is an input signal that clears the printer buffer and initializes the logic. Not used on all printers. The printer addresses are listed below:

```
FFXX81     (Write D0-D7) printer data register
FFXX81     (Read) - puts FF into data out register
FFXX83     (Write D3) printer strobe register
FFXX83     (Read) - clears acknowledge flag and printer IRQ
FFXX85     (Write) hardware buffer conflict
FFXX85     (Read) - printer status
              D0 = select from printer
              D1 = busy from printer
              D2 = fault from printer
              D7 = acknowledge from printer
FFXX87     (Write D3) printer input prime
FFXX87     (Read) - no operation

FFXX00   XX = 00-FE on 512 byte boundaries
```

To output a character to a printer:



NOTE

The printer acknowledge flag register latches the acknowledge signal from the printer and must be cleared by reading the printer strobe register. If the printer is still holding the acknowledge signal, the flag does not clear. The correct sequence is: 1. clear acknowledge, 2. check acknowledge flag, 3. if not clear, go back to 1.

The printer acknowledge can be selected to either edge thus permitting the use of this interface on Data Products and other printers. Refer to the *Printer Acknowledge Edge Select Header (J29)* paragraph in Chapter 2.

SYSFAIL Register

The SYSFAIL* status register (FFXX89) is provided to read the status of the VMEbus SYSFAIL* signal. D7 is low if SYSFAIL* is low. D7 is high if SYSFAIL* is high.

User Display Blanking Register

The display blanking register is a write only register to enable the user display to be blanked (turned off) by writing to FFXX8B with D3 low. A reset or writing to this register with D3 high turns the display on if it is not blanked by section 8 of switch S1 and header J25. Refer to the *Display Blanking Enable Select Header (J25)* paragraph in Chapter 2.

Global Interrupter

The global interrupter is designed using two BIM (MC68153) devices. One BIM accepts interrupt inputs from the serial ports, parallel ports, and time-of-day clock. This BIM generates VMEbus interrupts on the corresponding programmed levels. During the interrupt acknowledge cycle, the BIM provides the 8-bit interrupt vector for the interrupt, or may cause the appropriate serial port or parallel port to provide the vector (software controlled option in the BIM).

The second BIM device is used exclusively to generate global VMEbus interrupts under software control. One interrupt input to the BIM may also be jumper selected to be held low to provide for one software controlled global interrupt, or may be jumper selected to the VMEbus SYSFAIL* line to generate a global system failure interrupt.

The MC68153 register model is shown below:

MC68153 REGISTER MODEL

ADDRESS BIM1	ADDRESS BIM2	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME	BIM1	BIM2
FFXXC1	FFXXE1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0	SERIAL PORT 1	SYSFAIL/GND
FFXXC3	FFXXE3	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1	SERIAL PORT 2	GND
FFXXC5	FFXXE5	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2	TOD CLOCK	GND
FFXXC7	FFXXE7	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3	PRINTER	GND
FFXXC9	FFXXE9	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0	NOT USED	SYSFAIL/IPC
FFXXCB	FFXXEB	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1	NOT USED	IPC
FFXXCD	FFXXED	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2	TOD CLOCK	IPC
FFXXCF	FFXXEF	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3	PRINTER	IPC
		7	6	5	4	3	2	1	0	REGISTER BIT		

NOTE

When using the serial port interrupts, the BIM must be initialized for external vector in control register 0 and 1 because the R68560 supplies the interrupt vector. If the BIM is initialized for internal vector , both devices supply the vector, which causes a buffer conflict.

Battery Backup

An external battery may be connected to the MVME050 through the P2 connector to provide battery backup power for the time-of-day clock. These batteries may be located on the I/O module. Headers are provided for selecting power backup from the external batteries, +5 Vdc standby from the VMEbus, or +5 Vdc from the VMEbus. Jumper selectable battery charging is provided when system power is applied to the MVME050.

Bus Arbiter

The bus arbiter arbitrates requests and grants bus mastership on four levels. If the level of the current bus master is lower than the current bus request, the bus arbiter initiates a bus clear.

System Clock Generator

The system clock generator provides the 16 MHz system clock signal on the VMEbus. The 16 MHz clock signal is derived from the 32 MHz oscillator.

Serial Bus Clock Generator

The serial bus clock generator provides the 4 MHz nonsymmetrical serial clock for the VMEbus. The signal is derived from the 32 MHz oscillator.

Bus Time-Out Generator

The bus time-out generator monitors VMEbus data transfer activities. If a transfer takes longer than the jumper selected time, the module generates a VMEbus error signal. The time-out starts when either data strobe goes low and clears when both data strobes are high. The time-out is jumper selectable from minimum of 2 to 160 microseconds to OFF.

Power-Up Reset

When system power is turned on, this circuit provides a system reset for 300 to 800 milliseconds minimum. Power down reset is not provided. Power backed up systems require an external power monitor to generate a ACFAIL and power down reset sequence as specified in the VMEbus specification.

RESET Switch

A system RESET switch is located on the front panel of the MVME050 module. Pressing the switch generates a system reset on the VMEbus. The switch may be disabled by removing a jumper. The capability of resetting the system from a remote switch is provided through connector P2 from the I/O module.

VMEbus Interface

The VMEbus interface is slave mode only and supports 8-, 16-, and 32-bit data transfers. It also supports the 24-bit or 32-bit addressing mode. The cycle types supported are shown in Table 4-2.

User Display

A 2 character LED display is provided on the front panel for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register.

Front Panel Indicators

Front panel indicator lights display the overall system status. A red FAIL light illuminates whenever the controller module detects the SYSFAIL* line low on the VMEbus. A green RUN light illuminates when the SYSFAIL* line on the VMEbus is high.

TABLE 4-2. Supported Cycle Types

IACK*	LWORD*	AM CODE	CYCLE TYPE	ACCESSIBLE RESOURCES
X	L	X	32 bit data cycle	EPROM/RAM
L	H	X	Interrupt acknowledge	Interrupter or interrupting serial port (only D0-D7 are used)
H	X	09 0A 0D 0E	Extended addressing (32 bit) access modes	RAM/EPROM sockets - full addressing range
H	X	16 1E	User-defined mode-defined by MVME120 as alternate reset vector fetch	EPROM quad 1 EPROM quad 2
H	H	29 2D	Short I/O access	Serial ports, parallel port, time-of-day clock, global interrupter, user display (only D0-D7 are used)
H	X	39 3A 3D 3E	Standard addressing (24 bit) access mode	RAM/EPROM sockets - A24-A31 address compare is don't care

X = DON'T CARE L = LOW H = HIGH

CHAPTER 5 - SUPPORT INFORMATION

INTRODUCTION

This chapter provides the interconnection signals, parts list with parts location illustration, and schematic diagram for the MVME050.

INTERCONNECT SIGNALS

The MVME050 interconnects with the VMEbus through connector P1. Connector P2 interconnects the MVME050 with the MVME701A.

Connector P1 Interconnect Signals

Connector P1 is a standard DIN 41612 triple row, 64-pin male connector. All Motorola VMEbus specifications are met by the MVME050 module. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-1.

TABLE 5-1. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA bus (bits 0-7) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - a 16 MHz input signal used as a timing reference. This signal is provided by the VMEbus system controller.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - input signal that indicates a data transfer on data bus lines D08-D15.
A13	DS0*	DATA STROBE 0 - input signal that indicates a data transfer on data bus lines D00-D07.
A14	WRITE*	WRITE - input signal that specifies the direction of data transfers.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - this output signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - the falling edge of this input signal indicates a valid address is present on the address bus.
A19	GND	GROUND
A20	IACK*	INTERRUPT ACKNOWLEDGE - input signal that indicates a VME interrupt acknowledge cycle. The VME system controller has been interrupted on one of seven levels and is now acknowledging the specific interrupt with a service routine.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.
A23	AM4	ADDRESS MODIFIER (bit 4) - one of the three-state input lines that provide additional information about the address bus, such as size, cycle type, and/or data transfer bus master identification.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A24	A07	ADDRESS bus (bit 7) - one of 16 three-state input lines that specify an address in the memory map. Only the least significant 16 bits of the 23 associated VMEbus address lines are employed on the controller module.
A25	A06	ADDRESS bus (bit 6) - same as A07 on pin A24.
A26	A05	ADDRESS bus (bit 5) - same as A07 on pin A24.
A27	A04	ADDRESS bus (bit 4) - same as A07 on pin A24.
A28	A03	ADDRESS bus (bit 3) - one of 16 three-state input lines that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines A01-A03 are used to indicate the interrupt level that is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - same as A03 on pin A28.
A30	A01	ADDRESS bus (bit 1) - same as A03 on pin A28.
A31	-12 VDC	-12 Vdc Power - used by the logic circuits on the controller module.
A32	+5 VDC	+5 Vdc Power - used by the logic circuits on the controller module.
B1	BBSY*	BUS BUSY - This signal is driven low when the controller module is the bus master. This signal is an input to the arbiter to indicate that the bus may be arbitrated.
B2	BCLR*	BUS CLEAR - input signal that causes the release of the mastership in the RBC mode.
B3,B4		Not used.
B5	BGOOUT*	BUS GRANT 0 OUT - bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus-grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B6		Not used.
B7	BG1OUT*	BUS GRANT 1 OUT - same as BG0OUT on pin B5.
B8		Not used.
B9	BG2OUT*	BUS GRANT 2 OUT - same as BG0OUT on pin B5.
B10		Not used.
B11	BG3OUT*	BUS GRANT 3 OUT - same as BG0OUT on pin B5.
B12-B15	BR0*-BR3*	BUS REQUEST (0-3) - the bus request at the jumpered level is true when the MPU requires bus mastership. When one or more bus request lines is true in the ROR mode, bus mastership is released. When the controller module is the system controller, bus request level three is monitored by the arbiter.
B16-B19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - same as AM4 on pin A23.
B20	GND	GROUND
B21	SERCLK	SERIAL CLOCK - a high level signal used to clock the serial communication bus.
B22		Not used.
B23	GND	GROUND
B24-B30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.
B31	+5V STDBY	+5Vdc STANDBY - this line supplies +5 Vdc to devices requiring battery backup.
B32	+5 VDC	+5 Vdc Power - same as +5 VDC on pin A32.
C1-C8	D08-D015	DATA bus (bits 8-15) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
C9	GND	GROUND

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C10	SYSFAIL*	SYSTEM FAIL - reflects state of FAIL bit in MCR and fail indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - an active low output signal that indicates an error has occurred during a data transfer cycle.
C12	SYSRESET*	SYSTEM RESET - the system controller provides this input signal that causes a board level reset on the controller module.
C13	LWORD*	LONGWORD - three-state driven signal to indicate that the current transfer is a 32-bit transfer.
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15	A23	ADDRESS bus (bit 23) - same as A07 on pin A24.
C16	A22	ADDRESS bus (bit 22) - same as A07 on pin A24.
C17	A21	ADDRESS bus (bit 21) - same as A07 on pin A24.
C18	A20	ADDRESS bus (bit 20) - same as A07 on pin A24.
C19	A19	ADDRESS bus (bit 19) - same as A07 on pin A24.
C20	A18	ADDRESS bus (bit 18) - same as A07 on pin A24.
C21	A17	ADDRESS bus (bit 17) - same as A07 on pin A24.
C22	A16	ADDRESS bus (bit 16) - same as A07 on pin A24.
C23	A15	ADDRESS bus (bit 15) - same as A07 on pin A24.
C24	A14	ADDRESS bus (bit 14) - same as A07 on pin A24.
C25	A13	ADDRESS bus (bit 13) - same as A07 on pin A24.
C26	A12	ADDRESS bus (bit 12) - same as A07 on pin A24.
C27	A11	ADDRESS bus (bit 11) - same as A07 on pin A24.
C28	A10	ADDRESS bus (bit 10) - same as A07 on pin A24.
C29	A09	ADDRESS bus (bit 9) - same as A07 on pin A24.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C30	A08	ADDRESS bus (bit 8) - same as A07 on pin A24.
C31	+12 VDC	+12 Vdc Power - used by the logic circuits on the controller module.
C32	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin A32.

Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 connector. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-2.

TABLE 5-2. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1	GND	GROUND
A2	RTS1	REQUEST TO SEND (Port 1) - RTS is supplied by the terminal to the modem when it is required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
A3	DTR1	DATA TERMINAL READY (Port 1) - a signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
A4	DCD1TT	DATA CARRIER DETECT (Port 1) - furnished by the modem to the terminal to indicate that a valid carrier is being received.
A5	SUP1	PULLUP LINE (Port 1) - an active pullup line activated by jumper arrangement on headers J7 or J11.
A6	RxC1	RECEIVE CLOCK (Port 1) - this line clocks input data from a terminal to a modem.
A7,A8,A9	GND	GROUND
A10	RTS2	REQUEST TO SEND (Port 2) - same as RTS1 on pin A2.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A11	DTR2	DATA TERMINAL READY (Port 2) - same as DTR1 on pin A3.
A12	DCD2TT	DATA CARRIER DETECT (Port 2) - same as DCD1TT on pin A4.
A13	SUP2	PULLUP LINE (Port 2) - same as SUP1 on pin A5 except headers J8 and J12 apply.
A14	RxC2	RECEIVE CLOCK (Port 2) - same as RxC1 on pin A6.
A15,A16	GND	GROUND
A17-A24	D00-D07	PRINTER DATA (bits 0-7) - output data to the I/O module.
A25	PACK	PRINTER ACKNOWLEDGE - a low level input pulse indicating that the next character may be sent.
A26	PSTB*	PRINTER STROBE - an output pulse used to clock data from the system to the printer. This pulse is active low.
A27	INPRIME	PRINTER INPUT PRIME - an output signal that clears the printer buffer and initializes the logic.
A28	SEL	PRINTER SELECT - input signal indicating that the printer is selected.
A29	BUSY	PRINTER BUSY - an input signal indicating that the printer cannot receive data.
A30	FAULT	PRINTER FAULT - an input signal that indicates a printer fault condition such as paper empty, light detect, or a deselect condition.
A31	BATT	BATTERY - +5 Vdc input to the controller module for battery backup of the time-of-day clock.
A32	REMRES*	REMOTE RESET - an input for as remote switch to reset the system (normally open).
B1	+5 VDC	+5 Vdc Power - used by the logic circuits on the I/O module.
B2	GND	GROUND

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B3		Not used.
B4-B11	A24-A31	VME ADDRESS bus (bits 24-31) - eight three-state input lines that specify an address in the memory map.
B12	GND	GROUND.
B13	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin B1.
B14-B21	D16-D23	VME DATA bus (bits 16-23) - eight three-state bidirectional data lines.
B22	GND	GROUND
B23-B30	D24-D31	VME DATA bus (bits 24-31) - eight three-state bidirectional data lines.
B31	GND	GROUND
B32	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin B1.
C1	TxD1	TRANSMIT DATA (Port 1) - data to be transmitted is furnished on this line to the modem from the terminal.
C2	RxD1	RECEIVE DATA (Port 1) - data that is demodulated from the receive line is presented to the terminal by the modem.
C3	CTS1	CLEAR TO SEND (Port 1) - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of the message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
C4	DCD1IN	DATA CARRIER DETECT (Port 1) - furnished by the modem to the terminal to indicate that a valid carrier is being received.
C5	DSR1	DATA SET READY (Port 1) - DSR is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
C6,C7	GND	GROUND
C8	TxC1	TRANSMIT CLOCK (Port 1) - this line clocks output data to the modem from the terminal.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C9	TxD2	TRANSMIT DATA (Port 2) - same as TxD1 on pin C1.
C10	RxD2	RECEIVE DATA (Port 2) - same as RxD1 on pin C2.
C11	CTS2	CLEAR TO SEND (Port 2) - same as CTS1 on pin C3.
C12	DCD2IN	DATA CARRIER DETECT (Port 2) - same as DCD1IN on pin C4.
C13	DSR2	DATA SET READY (Port 2) - same as DSR1 on pin C5.
C14,C154	GND	GROUND
C16	TxC2	TRANSMIT CLOCK (Port 2) - same as TxC1 on pin C8.
C17-C32	GND	GROUND

5

PARTS LIST

The components of the MVME050 are listed in Table 5-3. The parts locations are illustrated in Figure 5-1. These parts reflect the latest issue of hardware at the time of printing.

TABLE 5-3. MVME050 Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8452B01	Printed wiring board
CR1,CR2	48NW9607A29	Rectifier, 1N5818
CR3	48NW9616A03	Diode, 1N4148/1N914
C1-C19,C21-C26,C28,C29,C31-C35,C38-C40,C42,C43,C45,C48-C50,C52-C59	21NW9632A03	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc

TABLE 5-3. MVME050 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
C20	21NW9632A02	Capacitor, fixed, ceramic, 1.0 uF @ 50 Vdc
C27,C36	23NW9618A22	Capacitor, electrolytic, 50 uF @ 16 Vdc
C30	23NW9618A43	Capacitor, electrolytic, 6.8 uF @ 35 Vdc
C37	23NW9618A67	Capacitor, electrolytic, 10 uF @ 35 Vdc
C44,C46	21NW9710A01	Capacitor network, SIP, 7/470 pF
C47	20NW9628A04	Capacitor, trimmer, 5.5-18 pF
C51	21NW9629A18	Capacitor, fixed, mica, 56 pF @ 500 Vdc
DS1	48NW9612A49	Indicator, LED, red
DS2	48NW9612A59	Indicator, LED, green
DS3,DS4	72NW9624A03	Display, LED readout
J1-J29	29NW9805C07	Pin, autoinsert (244 required)
P1,P2	28NW9802E51	Connector, 96-pin
Q1	48NW9610A22	Transistor, MPS2222
R1	51NW9626B64	Resistor network, SIP, 4/47 ohm
R2	51NW9626B93	Resistor network, SIP, 4/22 ohm
R3,R6,R11	06SW-124A20	Resistor, fixed, film, 62 ohm, 5%, 1/4 W
R4,R14,R34	51NW9626B56	Resistor network, SIP, 9/10k ohm
R5,R10,R30-R33,R36	51NW9626B55	Resistor network, SIP, 9/4.7k ohm
R7	51NW9626B57	Resistor network, SIP, 9/1k ohm
R8,R9,R17,R29	06SW-124A65	Resistor, fixed, film, 4.7k ohm, 5%, 1/4 W
R13	06SW-125A27	Resistor, fixed, carbon, 120 ohm, 5%, 1/2 W
R15	51NW9626B51	Resistor network, SIP, 5/1k ohm

TABLE 5-3. MVME050 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R16,R19,R21	51NW9626B53	Resistor network, SIP, 7/4.7k ohm
R18,R22	51NW9626B54	Resistor network, SIP, 7/39k ohm
R20	06SW-124A87	Resistor, fixed, film, 39k ohm, 5%, 1/4 W
R23	06SW-124B50	Resistor, fixed, film, 15 megohm
R25	06SW-124B22	Resistor, fixed, film, 1.0 megohm
R26	06SW-124A25	Resistor, fixed, film, 100 ohm, 5%, 1/4 W
R27	06SW-124A41	Resistor, fixed, film, 470 ohm, 5%, 1/4 W
R28	06SW-124A75	Resistor, fixed, film, 12k ohm, 5%, 1/4 W
R35	51NW9626A53	Resistor network, SIP, 7/4.7k ohm
S1	40NW9801B35	Switch, 8-section, DIP, SPST, piano
S2	40NW9801B70	Switch, pushbutton, SPDT, momentary contact
U1,U15	(NOTE)	I.C. programmed
U2	51NW9615F38	I.C. SN74LS393N
U3,U5,U55, U61,U92	51NW9615J39	I.C. 74F74PC
U4,U7,U81, U87	51NW9615H89	I.C. SN74LS645-1N
U6	51NW9615F79	I.C. SN74S240N
U9,U17,U26, U34,U42	51NW9615H41	I.C. SN74LS682N
U10	51NW9615E77	I.C. SN74LS27N
U12,U44	51NW9615F02	I.C. SN74LS244N
U13	(NOTE)	I.C. programmed
U14,U90	51NW9615E95	I.C. SN74LS240N
U18,U27	51NW9615N56	I.C. 74F174PC

TABLE 5-3. MVME050 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U20,U29	51NW9615E86	I.C. SN74LS151N
U21,U22,U30, U31,U74	51NW9615E98	I.C. SN74LS373N
U23	51NW9615F85	I.C. SN74S38N
U24	51NW9615D93	I.C. SN74S30N
U32		Not used.
U35,U78,U85	51NW9615C21	I.C. SN74LS04N
U37	51NW9615H83	I.C. SN74LS641-1N
U38-U40	(NOTE)	I.C. programmed
U41,U46	51NW9615S88	I.C. MC68153P
U43,U63	51NW9615C22	I.C. SN74LS08N
U45	51NW9615E67	I.C. SN74S260N
U47,U79	51NW9615K71	I.C. 74F04PC
U48	51NW9615C56	I.C. SN74S08N
U49,U54,U62	51NW9615N32	I.C. 74F164PC
U50	(NOTE)	I.C. programmed
U51	51NW9615D32	I.C. SN74S02N
U52,U64	51NW9615D27	I.C. SN74S32N
U53	51NW9615F05	I.C. SN74LS20N
U56,U89	51NW9615E91	I.C. SN74LS00N
U57,U67	51NW9615P40	I.C. R68560P
U58,U60,U68	51NW9615B30	I.C. MC1489AP

TABLE 5-3. MVME050 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U59,U69,U70	51NW9615B29	I.C. MC1488P
U65	51NW9615E88	I.C. SN74LS10N
U66,U76	51NW9615C24	I.C. SN74LS32N
U71	51NW9615B56	I.C. MC14528CP
U72	51NW9615D91	I.C. SN74S139N
U73	(NOTE)	I.C. programmed
U75	51NW9615F41	I.C. SN74LS164N
U77	51NW9615E99	I.C. SN74LS374N
U80,U86	51NW9615H11	I.C. SN74LS645N
U82	51NW9615H35	I.C. MC146818P
U83	51NW9615J38	I.C. SN74LS646NT
U84	51NW9615H54	I.C. SN74LS12N
U88	51NW9615H93	I.C. SN74LS641N
VR1,VR2	48NW9608A31	Diode, zener, 5.6V, 1N5339B
VR3	51NW9615J93	I.C. LM317LZ
Y1	48AW1014B14	Crystal oscillator, 32 MHz
Y2	48AW4206B02	Crystal, 4.194304 MHz, 0.001%
	09NW9811A88	Socket, DIL, right angle (use at DS3,DS4)
	09NW9811A78	Socket, DIL, 20-pin (use at U1,U13,U15,U38,U40, U50,U73)
	09-W4659B14	Socket, DIL, 14-pin (use at U8,U11,U16,U19,U25, U28,U33,U36)
	09NW9811B01	Socket, DIL, 24-pin (use at U39)

TABLE 5-3. MVME050 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	09-W4659B20	Socket, SIL, 20-pin (use at U41,U46,U57,U67)
	09-W4659B12	Socket, SIL, 12-pin (use at U82)
	09NW9811A46	Socket, 4 lead crystal oscillator
	64-W5091B01	Panel, front
	29NW9805B17	Jumper, shorting, insulated (use at J1,J4-J9, J12,J15-J22,J25-J29)

NOTE: When ordering, use number labeled on part.

SCHEMATIC DIAGRAM

The schematic diagram for the MVME050 is illustrated in Figure 5-2.

APPENDIX A - TIME-OF-DAY CLOCK COMPENSATION

The time-of-day clock function is controlled by crystal Y2. This is a 4.194304 MHz, 0.001% device specified over the temperature range of 0-70 degrees C. Assuming the crystal parameters of CO and CL are met by the particular circuit configuration, this time base provides the time-of-day clock with an inherent accuracy of +/- 5.26 minutes per year. While these parameters can be exactly matched for any selected module, matching many modules would require different values of tuning capacitance to compensate for varying circuit capacitance. Module capacitance, because of the crystal holder, MC146818 socket, etc., would possibly cause the frequency of Y2 to change beyond its tolerance, thus affecting long term clock accuracy.

An obvious method of performing this tuning would be through the use of an onboard trimmer capacitor. While this would be a method tuning, it could also introduce variation because of temperature, life degradation, and shock, as well as ease of accessibility.

A better method of time base adjustment would be to adjust any clock inaccuracies through a software compensation method. An example of this would be to allow the module to run in the final environment and determine how fast or how slow the clock device (MC146818) is actually running over a known period of time. A software update could then be made periodically to add or subtract the proper amount of seconds. The MC146818 alarm function might be used to generate a daily interrupt, with the corresponding interrupt service routine performing the adjustment.

Located next to the reset switch on the controller module, a trimmer capacitor (C47) is provided to adjust the frequency of the time-of-day clock, instead of the method listed above.

The time-of-day clock should be adjusted periodically to maintain its accuracy. For this procedure it is assumed the clock is powered from the VMEbus power supply. To adjust the time-of-day clock, proceed as follows:

a. Turn all equipment power OFF.

CAUTION

REMOVING/INSERTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Remove the controller module from the chassis.

c. Install controller module on a VME compatible extender card and install in chassis.

d. Connect a frequency counter to pin 21 of the MC146818 device located at the lower front corner of the module.

e. Turn equipment power ON.

f. Adjust capacitor C47 until frequency reading is 1.048576 MHz.

g. Turn equipment power OFF, remove counter, remove extender card, install controller module in chassis, and turn equipment power ON, if desired.

This completes the adjustment of the time-of-day clock.

APPENDIX B - RS-232C INTERCONNECTIONS

The RS-232C standard is the most widely used interface between terminals and computers or modems, and yet it is not fully understood. This is because all the lines are not clearly defined, and many users do not see the need to conform for their applications. A system should easily connect to any other. Many times designers think only of their own equipment, but the state-of-the-art is computer-to-computer or computer-to-modem operation.

The RS-232C standard was originally developed by the Bell System to connect terminals via modems. Therefore, several handshaking lines were included. In many applications these are not needed, but since they permit diagnosis of problems, they are included in many applications.

The standard RS-232C interconnections are listed in Table B-1. To interpret this information correctly it is necessary to know that RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of them must be configured as a terminal and the other as a modem. Because computers are normally configured to work with terminals, they are said to be configured as a modem. Also, the signal levels must be between +3 and +15 volts for a high level, and between -3 and -15 volts for a low level. Any attempt to connect units in parallel may result in out of range voltages and is not allowed by the RS-232C specification.

TABLE B-1. RS-232C Interconnections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	TxD	TRANSMIT DATA - data to be transmitted is furnished on this line to the modem from the terminal.
3	RxD	RECEIVE DATA - data which is demodulated from the receive line is presented to the terminal by the modem.
4	RTS	REQUEST TO SEND - RTS is supplied by the terminal to the modem when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.

TABLE B-1. RS-232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
5	CTS	CLEAR TO SEND - CTS is a function supplied to the terminal by the modem which indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	DATA SET READY - data set ready is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	SIG-GND	SIGNAL GROUND - common return line for all signals at the modem interface.
8	DCD	DATA CARRIER DETECT - sent by the modem to the terminal to indicate that a valid carrier is being received.
9-14		Not used.
15	TxC	TRANSMIT CLOCK - this line clocks output data to the modem from the terminal.
16		Not used.
17	RxC	RECEIVE CLOCK - this line clocks input data from a terminal to a modem.
18,19		Not used.
20	DTR	DATA TERMINAL READY - a signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
21		Not used.
22	RI	RING INDICATOR - RI is sent by the modem to the terminal. This line indicates to the terminal that an incoming call is present. The terminal causes the modem to answer the phone by carrying DTR true while RI is active.
23		Not used.
24	TxC	TRANSMIT CLOCK - Same as TxC on pin 15.

TABLE B-1. RS232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
25	BSY	BUSY - A positive EIA signal applied to this pin causes the modem to go off-hook and make the associated phone busy.

NOTES: 1. High level = +3 to +15 volts. Low level = -3 to -15 volts.

2. RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of the computers must be configured as a modem and the other as a terminal.

There are several levels of conformance that are appropriate for typical RS-232C interconnections. The bare minimum requirement is the two data lines and a ground . The full version of RS-232C requires 12 lines and accommodates automatic dialing, automatic answering, and synchronous transmission. A middle-of-the-road approach is illustrated in Figure B-1.

One set of handshaking signals frequently implemented are RTS and CTS. CTS is used in many systems to inhibit transmission until the signal is high. In the modem application, RTS is turned around and returned as CTS after 150 microseconds. RTS is programmable in some systems to work with the older type 202 modem (half duplex). CTS is used in some systems to provide flow control to avoid buffer overflow. This is not possible if modems are used. It is usually necessary to make CTS high by connecting it to RTS or to some source of +12 volts such as the resistors shown in Figure B-1. It is also frequently jumpered to an MC1488 gate which has its inputs grounded (the gate is provided for this purpose). Another signal used in many systems is DCD. The original purpose of this signal was to tell the system that the carrier tone from the distant modem was being received. This signal is frequently used by the software to display a message like CARRIER NOT PRESENT to help the user to diagnose failure to communicate. Obviously, if the system is designed properly to use this signal, and it is not connected to a modem, the signal must be provided by a pullup resistor or gate as described before (see Figure B- 1). Many modems expect a DTR high signal and issue a DSR. These signals are used by software to help prompt the operator about possible causes of trouble. The DTR signal is used sometimes to disconnect the phone circuit in preparation for another automatic call. It is necessary to provide these signals in order to talk to all possible modems (see Figure B-1.). Figure B-1 is a good minimum configuration that almost always works. If the CTS and DCD signals are not received from the modem, the jumpers can be moved to artificially provide the needed signal. A way that an RS-232C connector can be wired to enable a computer to connect to a basic terminal with only three wires is shown in Figure B-2. This is because most terminals have a DTR

signal that is ON, and that can be used to pullup the CTS, DCD, and DSR signals. Two of these connectors wired back-to-back can be used. It must be realized that all the handshaking has been bypassed and possible diagnostic messages do not occur. Also the Tx and Rx lines may have to be crossed since Tx from a terminal is outgoing but the Tx line on a modem is an incoming signal.

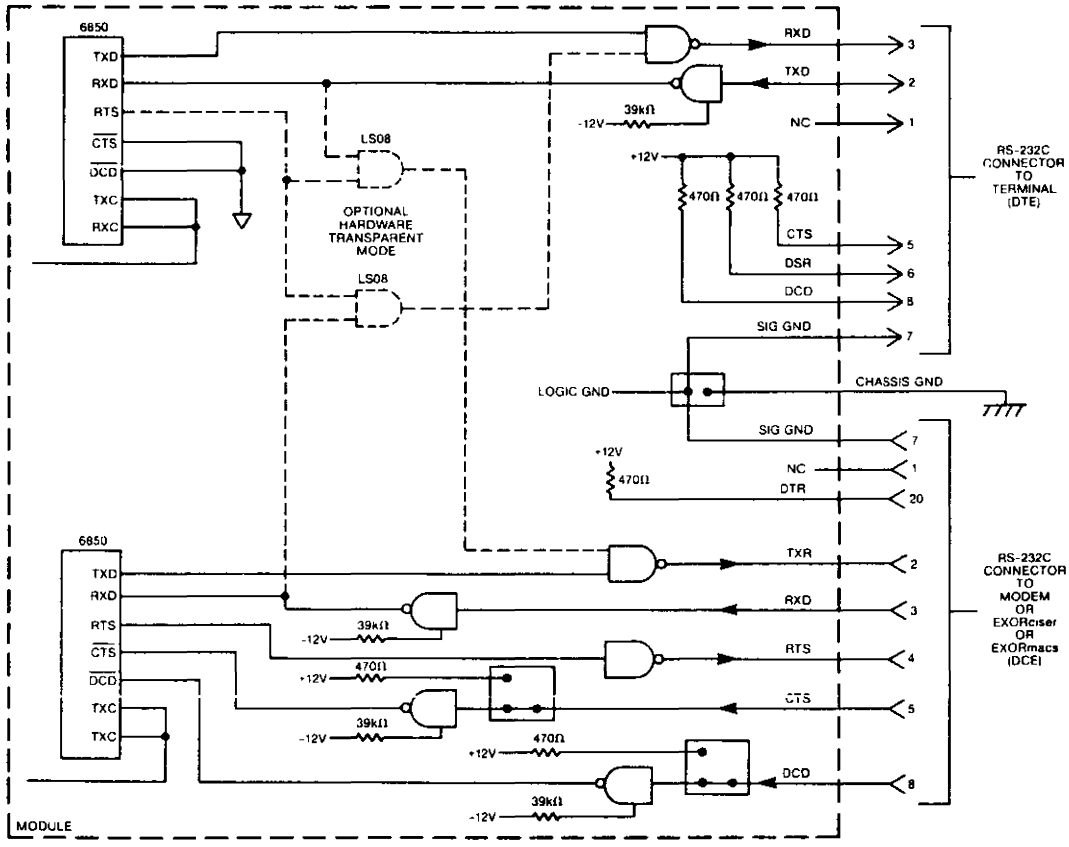


FIGURE B-1. Middle-of-the-Road RS-232C Configuration

Another subject that needs to be considered is the use of ground pins. There are two pins labeled GND. Pin 7 is the SIGNAL GROUND and must be connected to the distant device to complete the circuit. Pin 1 is the CHASSIS GROUND, but it must be used with care. The chassis is connected to the power ground through the green wire in the power cord and must be connected to the chassis to be in compliance with the electrical code. The problem is that when units are connected to different electrical outlets, there may be several volts difference in ground potential. If pin 1 of the devices are interconnected

with a cable, several amperes of current could result. This not only may be dangerous for the small wires in a typical cable, but could result in electrical noise that could cause errors. That is the reason that Figure B-1 shows no connection for pin 1. Normally, pin 7 should only be connected to the CHASSIS GROUND at one point, and if several terminals are used with one computer, the logical place for that point is at the computer. The terminals should not have a connection between the logic ground return and the chassis.

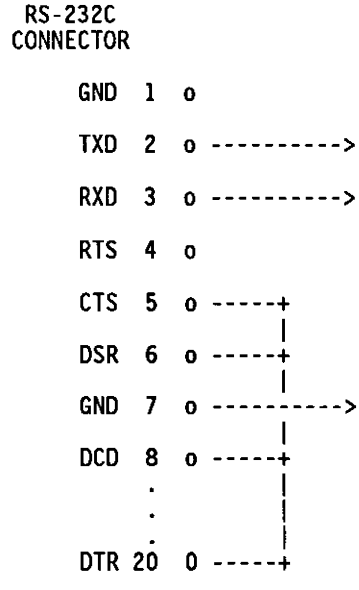


FIGURE B-2. Minimum RS-232C Connection

APPENDIX C - PROGRAMMABLE ARRY LOGIC

Programmable Array Logic (PAL) source code for the various devices on the MVME050 is listed in the following pages. In the upper left corner of each page is the PAL number (PAL16L8B), the device reference designation (U108), and the schematic sheet number (SHEET 6). The pages are arranged in sheet number order.

AM PROM

TBP28S42 U38 SHEET 4

INPUTS			OUTPUTS		
PIN	PROM FUNCTION	SIGNAL	PIN	PROM FUNCTION	SIGNAL
1	A0	AM0	6	Q1	RRAM*
2	A1	AM1	7	Q2	IOAM*
3	A2	AM2	8	Q3	AM1E*
4	A3	AM3	9	Q4	AM16*
5	A4	AM4	11	Q5	EXTAM*
16	A5	AM5	12	Q6	NC
17	A6	LIACK*	13	Q7	NC
18	A7	GND	14	Q8	NC
19	A8	GND			
15	CS*	LOW			

The output RRAM* is used to qualify the EPROM or RAM address decoding on sheet 5 and 6 of the schematic.

The signal RRAM* will go true if:

LIACK* is HI (false) and an address modifier code of 09, 0A, 0D, 0E, 39, 3A, 3D, 3E is true.

The outout IOAM* is used to qualify the IO address decoding on sheet 4 of the schematic.

The signal IOAM* will go true if:

LIACK* is HI (false) and an address modifer code of 29, or 2D is true.

The output AM1E* is used to enable EPROM quad one when a VME 120 board puts out the address modifier code of 1E during its reset vector fetch.

The signal AM1E* will go true if:

LIACK* is HI (false) and an address modifer code of 1E is true.

The output AM16* is used to enable EPROM quad two when a VME 120 board puts out the address modifier code of 16 during its reset vector fetch.

The signal AM16* will go true if:

LIACK* is HI (false) and an address modifer code of 16 is true.

The output EXTAM* is used to enable the address decoding circuit for the address lines A24 through A31. If this signal is false, these address lines are "dont cared".

The signal EXTAM* will go true if:

LIACK* is HI (false) and an address modifer code of 0A, 0B, 0D, 0E is true.

```
PALIOD   51AW4644B02        D093
825153
U40 SHEET 4 VME 050    5 MAR 83

NOTE: a / in the pin definition means LOW true signal

LA05 LA06 LA07 LA08 /ENIO /WRITE DIOACK QC /ACKIO GND                PIN
/IOSEL /TODSEL /BIM2 /BIM1 /SWITCH /LED /PNTR /MPCC2 /MPCC1 VCC      Definition

NOTE: a / in the output equations means FALSE
      a * in the output equations means AND
      a + in the output equations means OR

IF (VCC) MPCC1 =       /LA06*/LA07*/LA08*ENIO* WRITE*QC  ;READ
               +       /LA06*/LA07*/LA08*ENIO*/WRITE*/DIOACK*QC ;WRITE

IF (VCC) MPCC2 =       LA06*/LA07*/LA08*ENIO* WRITE*QC  ;READ
               +       LA06*/LA07*/LA08*ENIO*/WRITE*/DIOACK*QC ;WRITE

IF (VCC) PNTR  = /LA05*/LA06*LA07*/LA08*ENIO* WRITE*QC  ;READ
               + /LA05*/LA06*LA07*/LA08*ENIO*/WRITE*/DIOACK*QC ;WRITE

IF (VCC) LED   =
               + LA05*/LA06*LA07*/LA08*ENIO*/WRITE*/DIOACK*QC ;WRITE

IF (VCC) SWITCH =  LA05*/LA06*LA07*/LA08*ENIO* WRITE*QC  ;READ

IF (VCC) BIM1  = /LA05*LA06*LA07*/LA08*ENIO*QC  ;READ
               + /LA05*LA06*LA07*/LA08*ENIO*QC ;WRITE

IF (VCC) BIM2  =  LA05*LA06*LA07*/LA08*ENIO*QC  ;READ
               +  LA05*LA06*LA07*/LA08*ENIO*QC ;WRITE

IF (VCC) TODSEL = /LA07*LA08*ENIO*QC  ;READ OR WRITE

IF (VCC) IOSEL  =       /LA06*/LA07*/LA08*ENIO*QC  ;MPCC1
                +        LA06*/LA07*/LA08*ENIO*QC  ;MPCC2
                + /LA05*/LA06*LA07*/LA08*ENIO*QC   ;PNTR
                +  LA05*/LA06*LA07*/LA08*ENIO*QC   ;LED
                +  LA05*/LA06*LA07*/LA08*ENIO*QC   ;SWITCH
                + /LA05* LA06*LA07*/LA08*ENIO*QC   ;BIM1
                +  LA05*LA06*LA07*/LA08*ENIO*QC    ;BIM2
                +           /LA07*LA08*ENIO*QC     ;TODSEL
                +   LA05*LA06*LA07*/LA08*ENIO*QC   ;REDUNDANT

IF (VCC) ACKIO =        /LA06*/LA07*/LA08*ENIO*WRITE*QC          ;READ MPCC1
               +        /LA06*/LA07*/LA08*ENIO*/WRITE*DIOACK*QC ;WRITE
               +         LA06*/LA07*/LA08*ENIO*WRITE*QC          ;READ MPCC2
               +         LA06*/LA07*/LA08*ENIO*/WRITE*DIOACK*QC ;WRITE
               +  /LA05*/LA06*LA07*/LA08*ENIO*WRITE*QC           ;READ PNTR
               +  /LA05*/LA06*LA07*/LA08*ENIO*/WRITE*DIOACK*QC  ;WRITE
               +   LA05*/LA06*LA07*/LA08*ENIO*/WRITE*DIOACK*QC  ;WRITE LED
               +   LA05*/LA06*LA07*/LA08*ENIO*WRITE*QC          ;READ SWITCH
               +   /ACKIO*QC  ; feedback term to hold ACKIO
                             , true untill QC goes away
```

C

This is the I/O decoder for all the enables of the I/O functions.

Output Signal	Address	Function
MPCC1	FFXX00	Chip enable for first serial port (MPCC)
MPCC2	FFXX40	Chip enable for second serial port (MPCC)
PNTR	FFXX80	Chip enable for printer port
LED	FFXXA0	Chip enable for user display (write only)
SWITCH	FFXXA0	Chip enable for user readable switch (read only)
BIM1	FFXXC0	Chip enable for first BIM (no dtack on even bytes)
BIM1	FFXXE0	Chip enable for second BIM (no dtack on even bytes)
TODSEL	FFX100	Chip enable for time of day clock (no dtack on even bytes)

The output IOSEL (low true) turns on the data bus buffers and will go true if any I/O is selected

The output ACKIO (low true) starts the DTACK timing only for the I/O devices which cant generate a dtack. NOTE the BIMs and the time-of-day circuit generate their own dtack signal.

C

```
ADDRESS COMPARITOR   VME-050  51AW4644B01        97D3
82S153
U1 & U15 SHEETS 5 & 6     15 MAR 84

The following list of signals is the pin definition for this PAL.  The
first signal is for pin 1 and the next is for pin 2 etc.

The / before a signal means low true signal.

LA1 LA16 LA15 LA14 J4 J3 J2 J1 /OUTEQ GND
/LSIZE5 SIZE5 SZ0 SZ1 SZ2 NC16 NC17 NC18 NC19 VCC

The following list is the output equations for each output in human
readable form.  The last listing lists the fuse numbers for programming
a part.

The / before a signal means FALSE.
The + means OR

IF (VCC) OUTEQ
         = 1 LOW TRUE                                                    AND T
                                                    * S2  */S1  * S0      00
+                                                   * S2  */S1  */S0      01
+  LA17                     * J4                    */S2  * S1  * S0      02
+ /LA17                     */J4                    */S2  * S1  * S0      03
+  LA17* LA16               * J4  * J3              */S2  * S1  */S0      04
+ /LA17* LA16               */J4  * J3              */S2  * S1  */S0      05
+  LA17*/LA16               * J4  */J3              */S2  * S1  */S0      06
+ /LA17*/LA16               */J4  */J3              */S2  * S1  */S0      07
+  LA17* LA16* LA15         * J4  * J3  * J2        */S2  */S1  * S0      08
+  LA17* LA16*/LA15         * J4  * J3  */J2        */S2  */S1  * S0      09
+  LA17*/LA16* LA15         * J4  */J3  * J2        */S2  */S1  * S0      10
+  LA17*/LA16*/LA15         * J4  */J3  */J2        */S2  */S1  * S0      11
+ /LA17* LA16* LA15         */J4  * J3  * J2        */S2  */S1  * S0      12
+ /LA17* LA16*/LA15         */J4  * J3  */J2        */S2  */S1  * S0      13
+ /LA17*/LA16* LA15         */J4  */J3  * J2        */S2  */S1  * S0      14
+ /LA17*/LA16*/LA15         */J4  */J3  */J2        */S2  */S1  * S0      15
+  LA17* LA16* LA15* LA14*  J4  * J3  * J2  * J1    */S2  */S1  */S0      16
+  LA17* LA16* LA15*/LA14*  J4  * J3  * J2  */J1    */S2  */S1  */S0      17
+  LA17* LA16*/LA15* LA14*  J4  * J3  */J2  * J1    */S2  */S1  */S0      18
+  LA17* LA16*/LA15*/LA14*  J4  * J3  */J2  */J1    */S2  */S1  */S0      19
+  LA17*/LA16* LA15* LA14*  J4  */J3  * J2  * J1    */S2  */S1  */S0      20
+  LA17*/LA16* LA15*/LA14*  J4  */J3  * J2  */J1    */S2  */S1  */S0      21
+  LA17*/LA16*/LA15* LA14*  J4  */J3  */J2  * J1    */S2  */S1  */S0      22
+  LA17*/LA16*/LA15*/LA14*  J4  */J3  */J2  */J1    */S2  */S1  */S0      23
+ /LA17* LA16* LA15* LA14*/J4  * J3  * J2  * J1    */S2  */S1  */S0      24
+ /LA17* LA16* LA15*/LA14*/J4  * J3  * J2  */J1    */S2  */S1  */S0      25
+ /LA17* LA16*/LA15* LA14*/J4  * J3  */J2  * J1    */S2  */S1  */S0      26
+ /LA17* LA16*/LA15*/LA14*/J4  * J3  */J2  */J1    */S2  */S1  */S0      27
+ /LA17*/LA16* LA15* LA14*/J4  */J3  * J2  * J1    */S2  */S1  */S0      28
+ /LA17*/LA16* LA15*/LA14*/J4  */J3  * J2  */J1    */S2  */S1  */S0      29
+ /LA17*/LA16*/LA15* LA14*/J4  */J3  */J2  * J1    */S2  */S1  */S0      30
+ /LA17*/LA16*/LA15*/LA14*/J4  */J3  */J2  */J1    */S2  */S1  */S0      31
```

C

```
IF (VCC) SIZE5 = S2 */S1 *S0
     HIGH TRUE

IF (VCC) LSIZE5 = S2 */S1 *S0
       LOW TRUE
```

This PAL is a programmable comparitor simular to the function of the 74LS682's execpt that the three size inputs are used to determine how many of the address lines and jumpers to compare. If the size is zero, (all three size inputs low) the logic level of all of the address lines LA17 through LA14 must match the jumper levels J4 through J1 for the output OUTEQ to go true (low). There are sixteen possible combinations that the match may occur for size zero. If the size is set to one, the address line LA14 and the jumper J4 are dont cared so there are eight possible combinations that may match and assert the output OUTEQ. For size two, the address lines LA14 and LA15 and jumpers J1 and J2 are dont cared, and four possible combinations for a match. Size three will have address lines LA14, LA15, LA16 and jumpers J1, J2, J3 dont cared, and two possible combinations for a match. Size four has all the address lines and all the jumper inputs dont cared and the signal OUTEQ is held true. Size five also has the signal OOTEQ held true and the signal SIZE5 will be true (high) and the signal LSIZE5 will also be true (low).

```
PAL20L8
U39 VME-050   51AW4697B03   FB8C
RAM / ROM CHIP SELECT PAL FOR VME-050  SHEET 7  01 JUNE 84

/ROMEN2 /ROMEN1 /BDS0 LA01 ROMA /BDS1 /LLWORD /AM1E /AM16 NC /STB GND
/RAMEN2 /RAMEN1 /CS8 /CS7 /CS6 /CS5 /CS4 /CS3 /CS2 /CS1 RAMA VCC

IF (VCC) CS1 = STB*ROMEN2*ROMA*LA01*BDS0*/LLWORD ; D0 - D7
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*LA01*BDS0*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*LA01*BDS0*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS2 = STB*ROMEN2*ROMA*LA01*BDS1*/LLWORD  ; D8 - D15
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*LA01*BDS1*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*LA01*BDS1*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS3 = STB*ROMEN2*ROMA*/LA01*BDS0*/LLWORD  ; D16 - D23
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*/LA01*BDS0*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*/LA01*BDS0*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS4 = STB*ROMEN2*ROMA*/LA01*BDS1*/LLWORD  ; D24 - D31
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*/LA01*BDS1*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*/LA01*BDS1*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS5 = STB*ROMEN1*/ROMA*LA01*BDS0*/LLWORD ; D0 - D7
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*LA01*BDS0*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*LA01*BDS0*/LLWORD
   + STB*AM1E*/ROMA*LLWORD

IF (VCC) CS6 = STB*ROMEN1*/ROMA*LA01*BDS1*/LLWORD ; D8 - D15
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*LA01*BDS1*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*LA01*BDS1*/LLWORD
   + STB*AM1E*/ROMA*LLWORD

IF (VCC) CS7 = STB*ROMEN1*/ROMA*/LA01*BDS0*/LLWORD ; D16 - D23
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*/LA01*BDS0*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*/LA01*BDS0*/LLWORD
   + STB*AM1E*/ROMA*LLWORD
```

C

```
IF (VCC) CS8 = STB*ROMEN1*/ROMA*/LA01*BDS1*/LLWORD ; D24 - D31
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*/LA01*BDS1*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*/LA01*BDS1*/LLWORD
   + STB*AM1E*/ROMA*LLWORD
```

****

ROM QUAD 2		ROM QUAD 1	
RAM QUAD 1		RAM QUAD 2	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

C

****

The / means low true in the pin definitions.

In the output equations:

The * means AND

The / means FALSE

The + means OR

```
PAL16L8
U13 VME 050  51AW4281B12   46EE
FOUR LEVEL VME BUS ARBITOR  SHEET 11     5 MAR 84

PSBR0 PSBR1 PSBR2 PSBR3 NSBR0 NSBR1 NSBR2 NSBR3 LOW GND
/DGP /GP /BBSY /RESET /CLR /BG3OUT /BG2OUT /BG1OUT /BG0OUT VCC

IF (DGP) BG3OUT = PSBR3

IF (DGP) BG2OUT = /PSBR3*PSBR2

IF (DGP) BG1OUT = /PSBR3*/PSBR2*PSBR1

IF (DGP) BG0OUT = /PSBR3*/PSBR2*/PSBR1*PSBR0

IF (VCC) CLR = RESET
             + NSBR3*/PSBR3*BBSY
             + /PSBR3*NSBR2*/PSBR2*BBSY
             + /PSBR3*/PSBR2*NSBR1*/PSBR1*BBSY
             + /PSBR3*/PSBR2*/PSBR1*NSBR0*/PSBR0*BBSY


IF (VCC) GP =  /RESET*/BBSY*NSBR3
            +  /RESET*/BBSY*NSBR2
            +  /RESET*/BBSY*NSBR1
            +  /RESET*/BBSY*NSBR0

DESCRIPTION:   VME 050 FOUR LEVEL BUS ARBITOR PAL

   The BUS GRANT OUT'S  are priortised so that grant 3 has the hightest
   priotity   BG3OUT* will be asserted if PSBR3 is true and DLYGNTPND* is
   true   BG2OUT* will be asserted if PSBR2 is true and PSBR3 is false and
   DLYGNTPND* is true.  BG1OUT* will be asserted if PSBR1 is true and PSBR2
   is false and PSBR3 is false and DLYGNTPND* is true.  BG0OUT will be asserted
   if PSBR0 is true and PSBR1 is false and PSBR2 is false and PSBR3 is false
   and DLYGNTPND* is true.

  BUSCLR* will be asserted if BSYSRST* is asserted or if the next state of
  BR3 (NSBR3) is true and the present state of BR3 (PSBR3) is false and
  BBSY* is true ( this means the bus is still busy by the current bus master).
  likewise for the other levels

  Grant pending ( GNTPEND* ) is asserted when BSYSRST* is false and BBSY*
  is false and there is a bus request pending.  note normally BBSY*
  will be the last signal of this term to cause the output to true.

*****************************************************************

The / means low true in the pin definitions

In the output equasions.

     The * means AND

     The / means FALSE
```

```
PAL16L8
050   SHEET 11 VME 050  15 AUG 84      51AW4804B03     86E8
NEW SERIAL CLOCK & TIMEOUT CLOCK GENERATOR

/PSA /PSB /PSC /PSD /PSE /ROM2 /A1E /A16 /STB GND
/ROM1 /ROMOE /NC13 /NSE /SC /NSD /NSC /NSB /NSA VCC

IF (VCC) NSE = PSE*/PSC
             + PSE*/PSB*/PSA
             + PSE*/PSD*PSB
             + PSE*PSB*/PSA
             + PSE*PSD*/PSB
             + /PSE*PSD*PSC*PSB*PSA

IF (VCC) NSD = PSD*/PSC
             + PSD*PSB*/PSA
             + PSD*/PSB
             + /PSD*PSC*PSB*PSA

IF (VCC) NSC = /PSC*PSB*PSA
             + PSC*PSB*/PSA
             + PSC*/PSB*/PSA
             + /PSE*PSC*/PSB
             + PSD*PSC*/PSB

IF (VCC) NSB = /PSC*/PSB*PSA
             + PSB*/PSA
             + /PSE*PSC*/PSB*PSA
             + PSD*PSC*/PSB*PSA

IF (VCC) NSA = /PSA

IF (VCC) SC  = /PSE*/PSD*PSC*PSB*/PSA
             + /PSE*PSD*/PSC*PSB*/PSA
             + PSE*/PSD*/PSC*/PSB*PSA
             + PSE*/PSD*PSC*/PSB*PSA

IF (VCC) ROMOE = ROM1*STB
               + ROM2*STB
               + A1E*STB
               + A16*STB

DESCRIPTION: SERIAL CLOCK PAL FOR VME 050    6-1-3-1 SEQUENCE
```

C

```
PRINTER
82S153              19 MAR 83
U 73 VME050     51AW4644B03   D050

The following list of signals is the pin definition for this PAL. The
first signal is for pin 1 and the next is for pin 2 etc.

The / before a signal means low true signal.

BD03 /PNTR3 /PNTR7 /RESET /WRITE /PACK /FAILSN /SFAIL A01 GND
/SW8 /LEDBI  FFLED FFPS FFIP BD07 PNTACK PSTB /INPRIM VCC

The following list is the output equations for each output in human
readable form. The last listing lists the fuse numbers for programming
a part.

The / before a signal means FALSE.
The + means OR
The * means AND


IF (VCC) FFLED  = FFLED RESET WRITE
       hi true
                + /A01 FFLED  RESET

                + FFLED  FAILSN  RESET

                + A01 /BD03 /WRITE /FAILSN


IF (VCC)  LEDBI = A01 LEDBI  RESET /WRITE /FAILSN
        hi true
                + /SW8

                + FFLED  RESET  WRITE

                + /A01 FFLED  RESET

                + FFLED  RESET  FAILSN

The above terms make a D type flip-flop. See diagram.


IF (/A01 WRITE /FAILSN)  BD07 = SFAIL
                       HI TRUE

These are the terms to read the status of SYSFAIL* on the VMEbus.


IF (VCC) /PNTACK= /PNTACK /ACK
        LOW TRUE
                + /PNTR3 WRITE

                + /RESET

The above terms make a set-reset type flip-flop.
```

C

```
IF (VCC) /FFPS =  /FFPS  PNTR3
      LOW TRUE
                + /FFPS WRITE
                + /RESET
                +  BDO3 /PNTR3 /WRITE

IF (VCC) /PSTB  = /PSTB /PNTR3 /WRITE
                + /FFPS WRITE
                + /RESET
                + /FFPS PNTR3
```

The above terms make a D type flip-flop with the D input tied high.

```
IF (VCC) /FFIP  = /FFIP PNTR7
      LOW TRUE
                + /FFIP WRITE
                + /RESET
                +  BDO3 /PNTR7 /WRITE

IF (VCC) /INP   = /INP /PNTR7 /WRITE
     LOW TRUE
                + /FFIP WRITE
                + /RESET
                + /FFIP PNTR7
```

The above terms make a D type flip-flop.

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U

V

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