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SUBJECT: SENSING WINDING GEOMETRY AND INFORMATION PATTERNS

To: N. H. Taylor

From: J. I. Raffel

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Abstract: Two properties of the sensing winding used in the Whirlwind I and MTC core memories are common to a large class of winding configurations. These are: 1) maximum partial cancellation of core "noise" 2) no inductive coupling between drive and sense wires. A new winding is suggested to replace the present zig-zag geometry. This should prove easier to implement and preliminary tests on a plane containing both old and new sense windings indicate that the two are electrically equivalent. Since core "noise" is a function of information and sense winding geometry, a different checkerboard pattern exists for this new winding.

In general, checkerboard patterns used for production testing should not be called "worst" patterns since no attempt is made to guarantee the disturbed states of the cores, and these have a considerable effect on sense winding outputs.

For a core memory using a two-dimensional read and consisting of n rows and n columns, all that is required in order to have a "cancelling" winding with respect to "noise" signals from half-selected cores is that the winding pass through half the cores of each row and of each column in one direction and through the remaining halves in the other direction. Consider a square array shown in Figure 1. Each of the first n/2 rows can be made of any of the $nC_{n/2}$ combinations of n/2 pluses and n/2 minuses. (Plus and minus refer to core polarity with respect to sense winding.) If the next n/2 rows contain the complement configuration to that of the top half, the conditions for a cancelling winding as defined above are fulfilled. Figure 1 shows a typical example of a winding belonging to this class. The MTC-type sense winding has a distribution like that of Figure 2. It is seen to satisfy the necessary conditions also. Another possible geometry which suggests itself is shown in Figure 3. This appears to be the physically simplest configuration which satisfies the necessary conditions for partial concellation of core "noise".

It is now necessary to consider the problem of inductive pick-up. For this the cores can be neglected entirely and only the large closed loops of wire comprising the sense winding need be considered. The requirement for a non-inductive winding, if we neglect end effects and consider the drive wires as infinitely long, is that the $\int \frac{1}{r} dA$ be zero where r is the perpendicular distance between a drive line and a differential area dA as shown in Figure 4. The integral over A in Figure 4 would be made up of the two components A_1 and A_2 of opposing sign following the usual polarity convention for evaluating surface integrals.* The simplest way of guaranteeing this is that the net enclosed are (algebraic sum) at a given distance from any row or column wire is zero. The present sense winding uses two overlapping loops which have equal and opposite components of area with respect to any horizontal or vertical driving line. This has a map as shown in Figure 5 where solid areas and cross-hatched areas refer to loop areas of opposing polarity. If we consider the map of Figure 6 any "checkerboard" pattern of the type shown having an even number of squares on a side will be non-inductive. Here, as with core-noise cancellation, all that is required is that n/2 rows be "half and half" and the other n/2 rows be the complement of the upper half. It is to be emphasized, however, that here we refer to areas comprised of closed loops of wire and not to cores. The winding of Figure 3 is therefore seen to be both cancelling and non-inductive. This winding may be thought of most simply as being composed of four digit-plane type windings, (a single section links all cores in the same direction) connected in series so that adjacent quadrants of the plane are of opposite polarity. In building larger arrays and/or utilizing printed wiring techniques, this type of winding may prove to be much simpler to install than the old zig-zag.

The problem of delta noise has been considered in E-488, M-2351 and M-2568. These analyses show that a so-called "worst" pattern (that is, a condition under which ONEs are smallest and ZEROs largest) results from having one type of information on the positive half of the sense winding and another on the negative half of the sense winding. Using Freeman's terminology** half the cores should be in the "w_1" state and the other half in the "r_z" state on the selected row and column. That is, half the cores should be in the write-disturbed ONE state and half in the read-disturbed ZERO state. In the past no attempt has been made to guarantee that cores had been properly read-disturbed or write-disturbed, the emphasis being placed merely on inserting the proper pattern of ONE's and ZEROs in the array. For production testing of planes this type of test is probably sufficient for obtaining comparisons, but in no case should the results from such tests be used as any absolute indicator of margins and the term "worst" pattern should probably not be used where the disturb condition is not taken into account.

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*Osgood Advanced Calculus -

**Pulse Response of Ferrite Memory Cores - M-2568

A test plane containing the old zig-zag type of sense winding was wound with an additional winding of the type shown in Figure 3. The experimental results obtained with the new winding of Figure 3 indicated no inductive pick-up, as expected, but in rastering through the array extremely large ZEROs were encountered at certain places. These ZEROs were reduced to normal size by the addition of the post-write disturb pulse and were therefore seen to be attributable to the core output and not pickup.

It next became necessary to determine why this effect was only encountered when testing the new sense winding with its corresponding checkerboard pattern and not when testing the old with its pattern. In each case the memory is filled with a pattern which places ZEROs on one half (the half shown with minuses for instance) the sense winding and ONEs on the other (pluses). The only difference which arises for the two windings is that the halves are composed of different groupings of cores (see Figures 2 and 3). In each case the array is addressed cyclically, a row at a time, starting from the lower left-hand corner. The difference in outputs between the two windings is clearly the result of the difference in information sequencing which results in differences in the <u>disturbed</u> state of the cores in the array. In other words, in both cases we have half the cores in the ONE state and half in the ZERO but no consideration has been given to whether the ZEROs are read-disturbed and the ONEs write-disturbed. A glance at the old checkerboard pattern, Figure 2, indicates that since no more than two ONEs are written consecutively almost all of the cores in the array are, in fact, going to be in the read-disturbed state, having been placed there by the digit-plane driver used for writing ZEROs and therefore there is not even a remote possibility of having the ONEs write-disturbed by chance somewhere in the array.

An examination of the sequence for the new checkerboard pattern, Figure 3, indicates two inherent characteristics which tend to guarantee the proper disturbed conditions for many more cores: 1)Long strings of consecutive ONEs and of consecutive ZEROs are placed in the array at a time. 2) Successive rows (except for the middle pair) have the same information. The results can be best demonstrated by considering two adjacent rows as shown in Figure 7. Writing the last ZERO of the bottom row read-disturbs all the cores in the array (digit-plane-driver pulse). Writing the series of ONEs to finish out the line write-disturbs columns directly above each ONE and hence leaves the ONEs in the second row write-disturbed. (Incidentally, the ZEROs of the bottom row are also write-disturbed.) The first ZERO of the second row is now about to be read out and the ZEROs in its row have been read-disturbed and the ONEs write-disturbed. It is therefore quite reasonable to expect an unusually large noise output. It should be pointed out that even now the disturb condition of <u>all</u> the cores has not been guaranteed. Only the <u>row</u> containing the selected core has been disturbed properly, no attention has been paid to the <u>column</u>, and indeed the cores here are all read-disturbed (except for the one core in the previous row) because the last excitation these cores saw was the digit-plane-driver pulse which occurred when writing ZEROs in the previous row. The ZERO output is therefore still far from the worst case. Figure 8 shows a sketch of the output from the array for this pattern.

Note that the peak value of the maximum ZERO has become alarmingly large, but at strobe-time discrimination is still excellent.

Another effect which has not been sufficiently evaluated is the size of the voltage induced in the sense winding by the digit-plane-driver pulse. This is greatest when all the cores in the plane are in the proper w_1 and r_2 states, and under a true worst condition might very well be large enough to cause the sense-amplifier to block.

The new sense winding seems to work well and the experimental results obtains with it have served to emphasize the need for a thorough experimental investigation of theoretically predicted "noisy" patterns. The term worst pattern which was previously used rather loosely to describe checkerboard patterns regardless of the disturbed condition of the cores should be avoided in the future. These patterns are worthwhile as standard tests but by no means represent the most adverse conditions which could be encountered in computer operation. It is hoped that this point has been made sufficiently clear to avoid the necessity of periodic re-discoveries that our test patterns do not give the worst signal-to-noise ratios.

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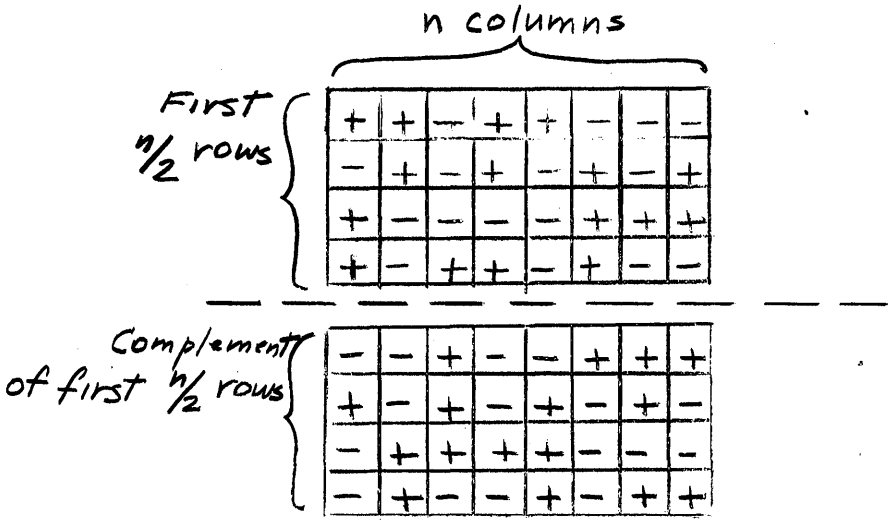


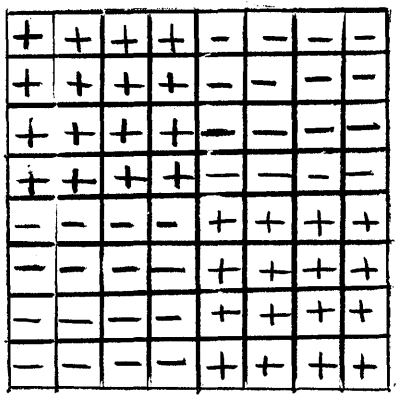
Typical Winding With Core-Noise Cancellation

Fig. 1

−	+	+	−	−	+	+	−
+	−	−	+	+	−	−	+
+	−	−	+	+	−	−	+
−	+	+	−	−	+	+	−
−	+	+	−	−	+	+	−
+	−	−	+	+	−	−	+
+	−	−	+	+	−	−	+
−	+	+	−	−	+	+	−

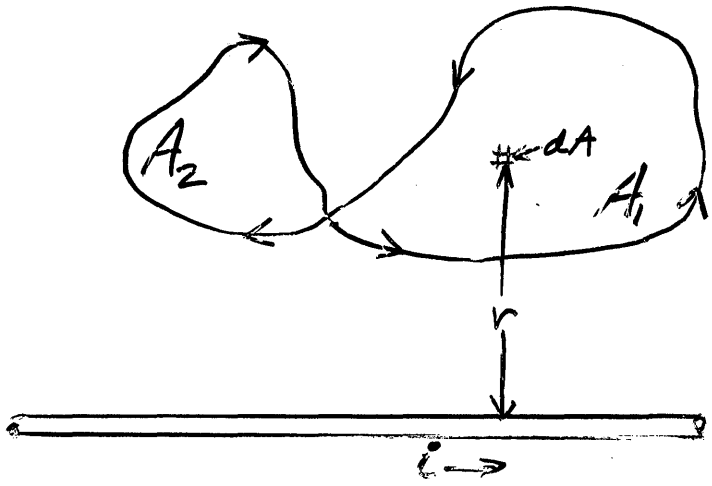
MTC-type Core-Noise Cancellation

Fig. 2



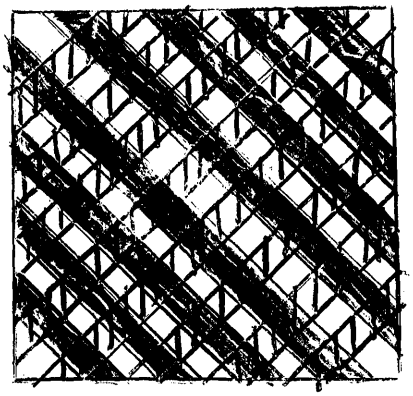
Proposed Cancelling Winding

Fig. 3



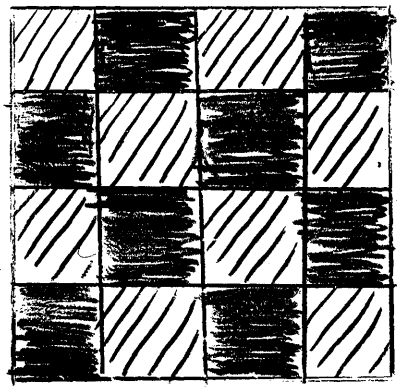
Voltage Induction by Current-Carrying Conductor

Fig. 4



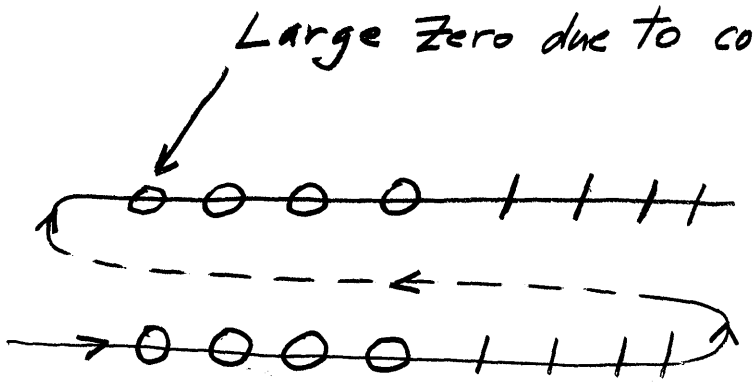
Loop-Area Map For MTC-type Winding

Fig. 5



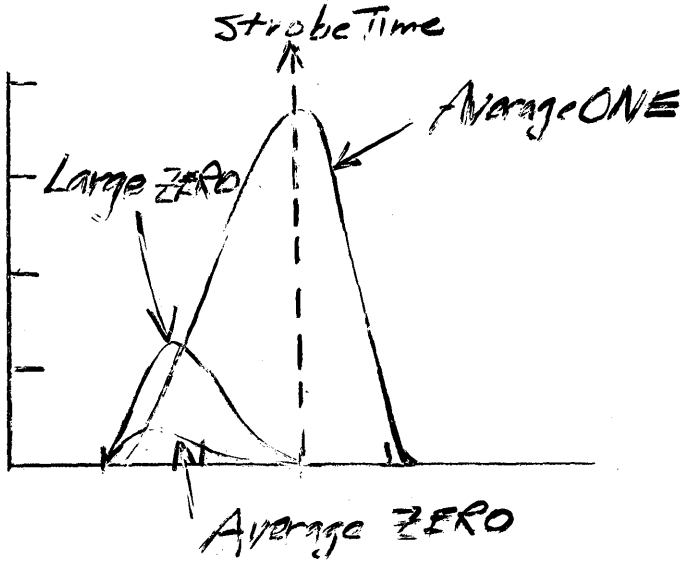
Loop-Area Map For Checkerboard Type

Fig. 6



Sequence For New Winding

Fig. 7



Sketch Showing Relative Sizes of ONEs and ZEROs

Fig. 8