Paul G. Griffith
September 29, 1955

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: THE APPLICATION OF TRANSISTORS TO MULTIPOSITION SELECTION SWITCHES

BRIEF STATEMENT OF THE PROBLEM:

A transistor multiposition selection switch is to be designed, constructed, and analyzed which will receive a coded binary input from n-pairs of terminals controlled by flip-flops, and which has a selected output on one of 2^n output lines. The selected output may in turn control the equipment necessary to obtain random access to a magnetic memory.[1,2,3] With the coming of larger memories (e.g. 256 x 256 x 37) and transistorized computers, the present diode matrix switches[4,5] are not practical. A possible solution to this problem is a dynamic switch designed around surface barrier transistors to provide operation at faster rise and fall times and with lower power requirements.

HISTORY OF THE PROBLEM:

The first multiposition switch where n-pairs of inputs selects one of 2^n outputs was conceived independently by Jan Rajchman and Perry Crawford during 1941. This first switch,[6,7] has been generalized to many different forms as will be shown in the following discussion.

Resistance Matrix Switch

A typical resistance matrix switch is shown in Figure 1. This switch has three input pairs and eight output lines (the number of things taken three at a time is eight and in general n-pairs of inputs have 2^n outputs).

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1. Superscripts refer to the bibliography at the end of the proposal.

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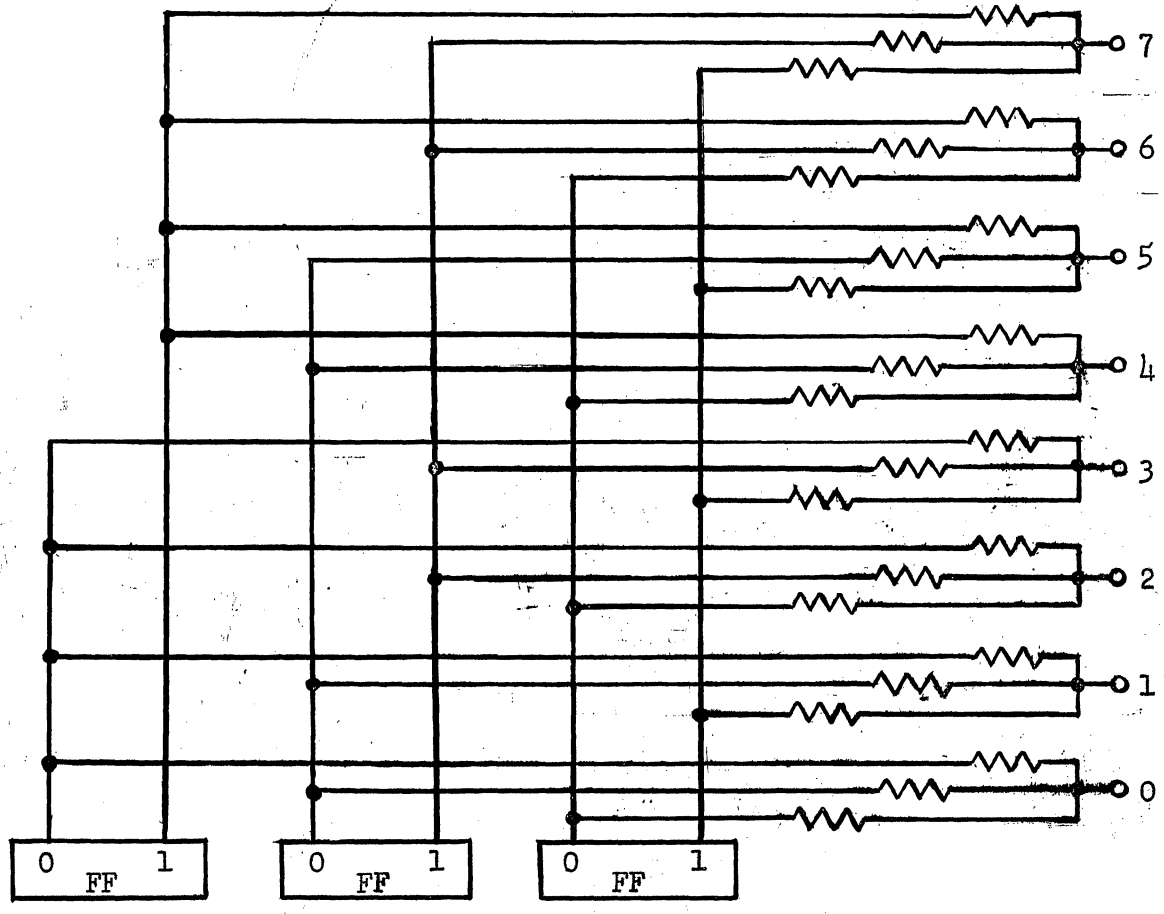
The operation can be explained as follows: Assume that the voltage at each input pair is either zero or E volts and the selected output terminal is number 7. Then the selection switches must be set to 111 and the selected terminal will be at E volts. Terminals 3, 5, and 6, will be at 2E/3 volts; terminals 1, 2, and 4, will be at E/3 volts; and terminal 0 will be at zero volts. In general, there are (n+1) possible output voltages, E, $\frac{n-1}{n}E$, $\frac{n-2}{n}E$, ..., 0. The distribution of output terminals among these voltages is given by the (n+1) row of the Pascal triangle. The output voltage, which is at E volts, must have some type of discriminator to reject the other voltages on the nonselected terminals. The effective switching voltage, $E-\left(\frac{n-1}{n}\right)E$, equals E/n. As n becomes large, it is apparent that selection becomes more difficult and thus the practical size of switches of this type is limited.



RESISTANCE MATRIX SWITCH
FIGURE 1.

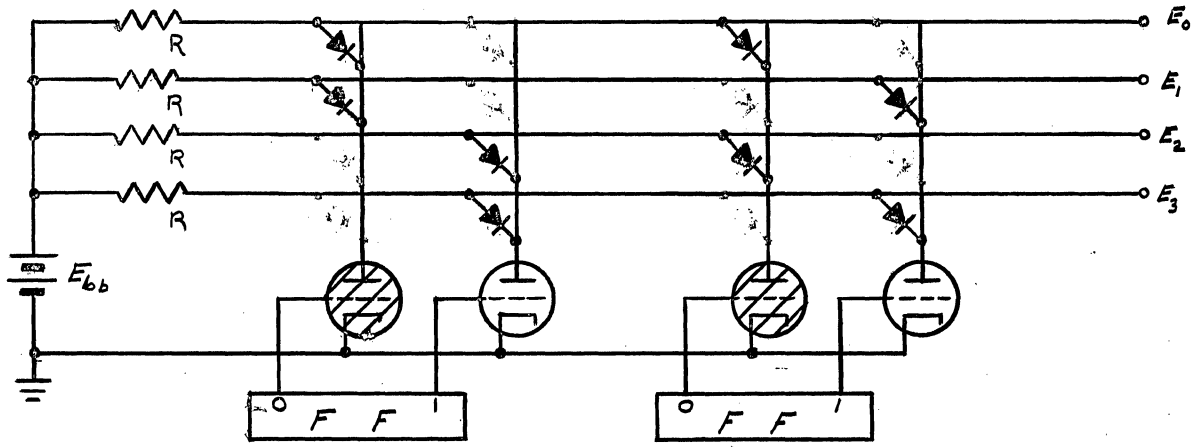
Diode Matrix Switch

By replacing the resistors in the matrix of Figure 1 with crystal diodes, as shown in Figure 2a, a circuit is obtained which can have a larger effective switching voltage. Plate current through the buffer amplifiers must flow through the resistors, R. The crystal matrix is connected so that current always flows through all the resistors but one. The terminal associated with that resistor, being at the higher voltage than the other terminals, is the selected terminal. In order to make the explanation easily understood, assume that the crystal-rectifier has a forward resistance, R_f, and a back resistance, R_b, which are independent of the magnitude of the current through the rectifier. To determine whether a crystal rectifier may be represented by R_f or R_b, the polarity of the voltage across the rectifier can be established by inspection of the circuit. An "on" buffer amplifier may be represented by the static plate resistance of the tube, r_p, and an "off" buffer amplifier by an infinite resistance. The equivalent circuit can be represented as shown in Figure 2b; and if R_f is assumed to be much smaller than R, the equivalent circuit can be simplified to that of Figure 2c (this is a very good approximation provided that R is at least ten times greater than R_f). The general equivalent circuit for the above assumptions is shown in Figure 2d. The effective switching voltage from this equivalent circuit becomes

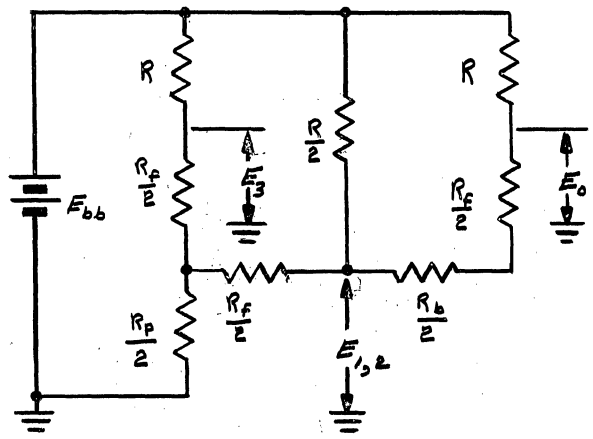
$$\Delta E = \frac{R R_b E_{bb}}{(2^n-1)(2^{n-1}-1)} \Big/ \left[R_p\left(R + \frac{R}{2^n-1} + \frac{R_b}{(2^{n-1}-1)n}\right) + \frac{R}{2^n-1}\left(\frac{R_b}{2^{n-1}-1} + Rn\right) \right]$$

The simplified equivalent circuit shows that ΔE will decrease as n increases or R_b decreases; however, this type of switch allows one to have

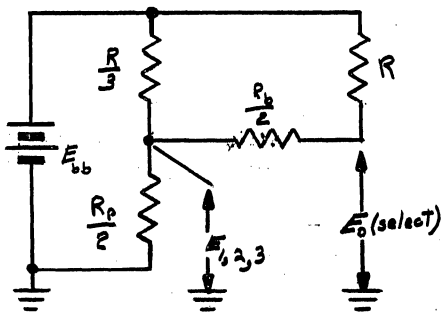
much greater switching voltages compared to a resistance switch of the same size. 64-position switches of this type are presently being used in the MTC digital computer at Lincoln Laboratory. Switches of this magnitude, however, require large amounts of power to drive them, i.e., transmitting tubes, in order that the voltage at the output terminals will rise rapidly (e.g. one-half microsecond). Thus, in larger sizes this type of switch becomes uneconomical, not due to the cost of the diodes, which are relatively inexpensive, but due to the required complexity of driving equipment.



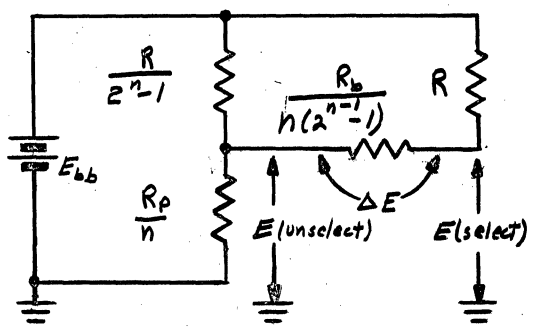
(a)



(b)



(c)

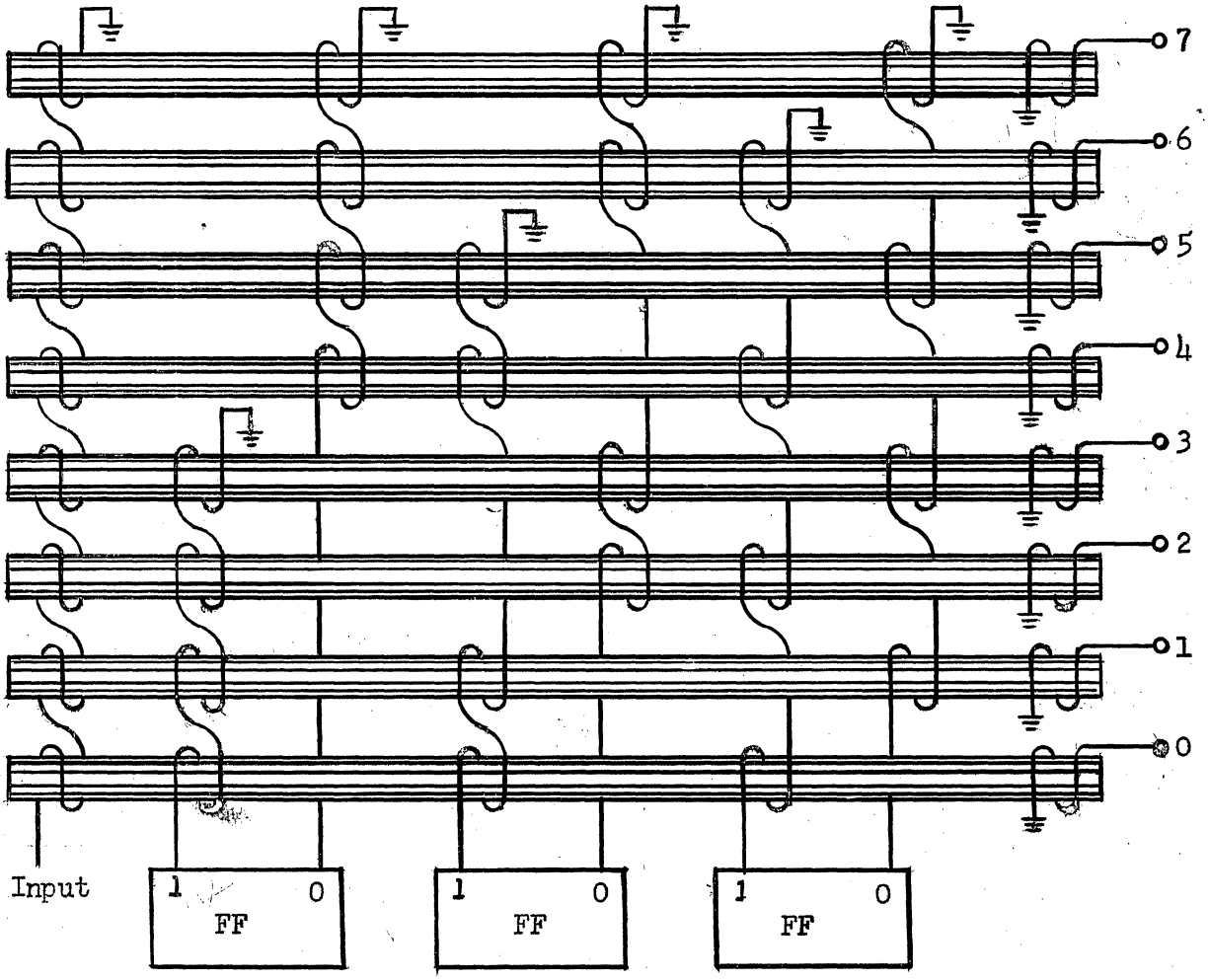


(d)

FIGURE 2.

Magnetic Matrix Switch[8,9,10]

The structure of the magnetic matrix switch (Figure 3) is similar to the diode matrix switch just discussed. Output selection is made possible by the use of saturable cores which have rectangular hysteresis loops. It is assumed that the output current of each flip-flop is great enough that the presence of an input pulse will cause a net flux change only in the selected core. Each core has an output winding and an input winding as in a transformer. The primary disadvantages of this type of switch are slow operating speeds and undesirable noise levels.

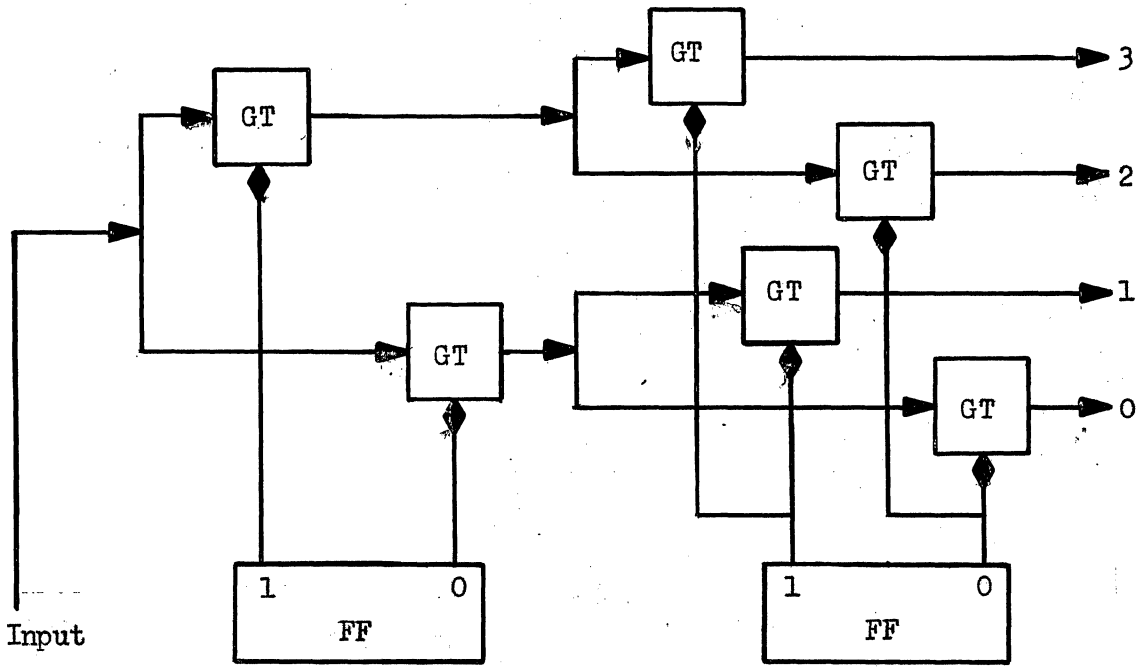


MAGNETIC MATRIX SWITCH
FIGURE 3.

Gate Tube Whiffle-Tree Switch

Gate tubes can be connected to form multiposition switches. Figure 4 is a 4-position gate tube whiffle-tree switch. A two digit order is applied to the two input flip-flops. The output will be determined by the series of gate tubes that are selected. For example, to select output number 1, the coded input to the flip-flops would be 01. Input pulses pass through the series of gate tubes that complete a path to the selected output. The disadvantages of this type of switch are the delay inherent in each gate unit and the large number $(2^{n+1} - 2)$ of gate tubes required to make a moderately large switch.

A gate tube with multiple control grids[11] to eliminate these difficulties has been suggested. However, gate tubes with n control grids have not been developed with an n much larger than 3 which restricts the maximum practical size of this type switch.



GATE TUBE WHIFFLE-TREE SWITCH
FIGURE 4.

PROPOSED PROCEDURE

Transistor Switching

In the past five years transistor switching circuitry has been investigated for computer work and is now beginning to play an important role in the computer field; however, multiposition selection switches have not been investigated. It is anticipated that an all-transistor multiposition selection switch can eliminate many of the difficulties found in the other types of switches. One promising transistor for this particular application is the Philco surface barrier transistor currently under mass production. This study will center about several switching configurations of surface barrier transistors as outlined in the Probable Procedure.

Probable Procedure

1. Transistor "and" and "or" circuits will be analyzed with regards to speed, rise and fall times, power considerations and limitations, maximum size, etc. Shown in Figure 5 are typical "and" and "or" circuits with their respective transmissions, according to the Boolean Algebra notation (the output is at zero volts).

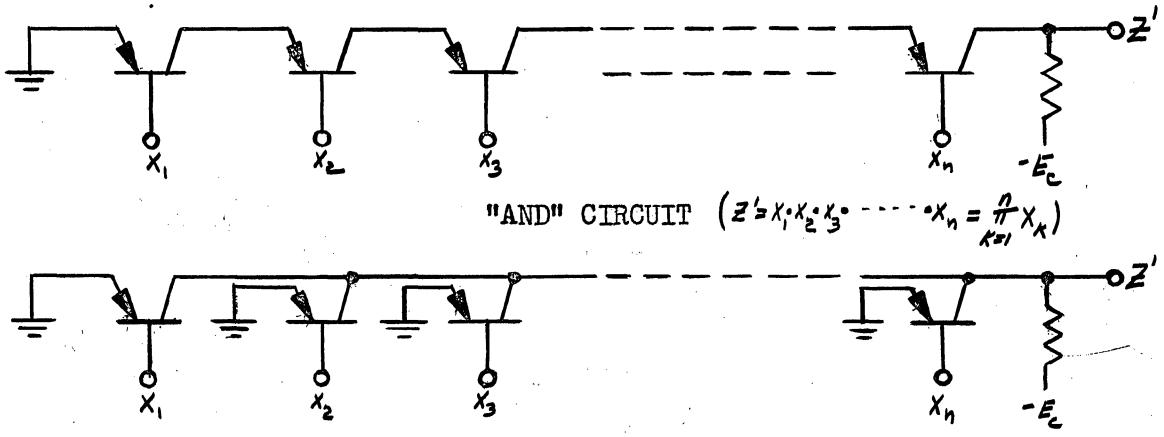
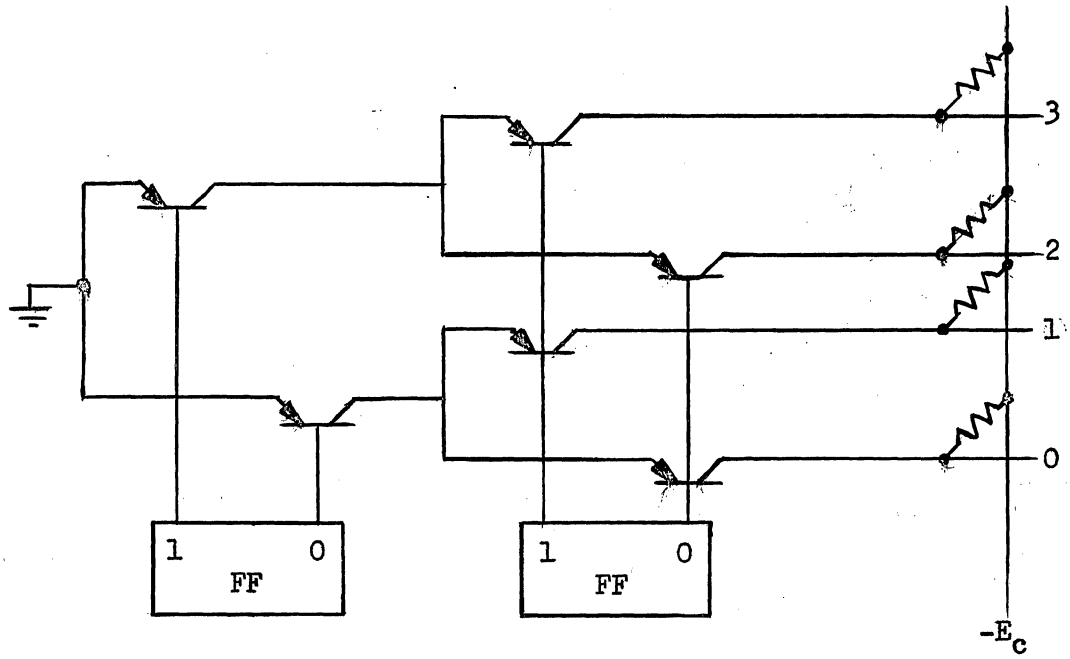
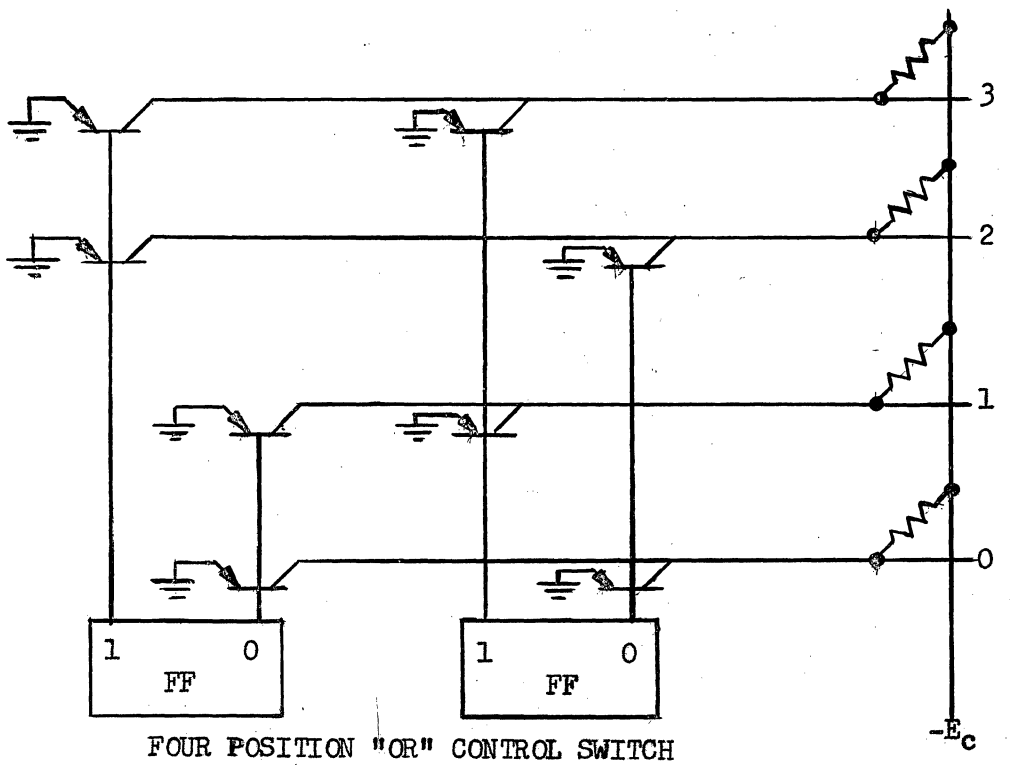


FIGURE 5.

2. Transistor switches employing the use of "and" and "or" circuits will be investigated. These switches will also be referred to as control switches for reasons which will become apparent later. Shown in Figure 6 are typical "and" and "or" types of control switches.



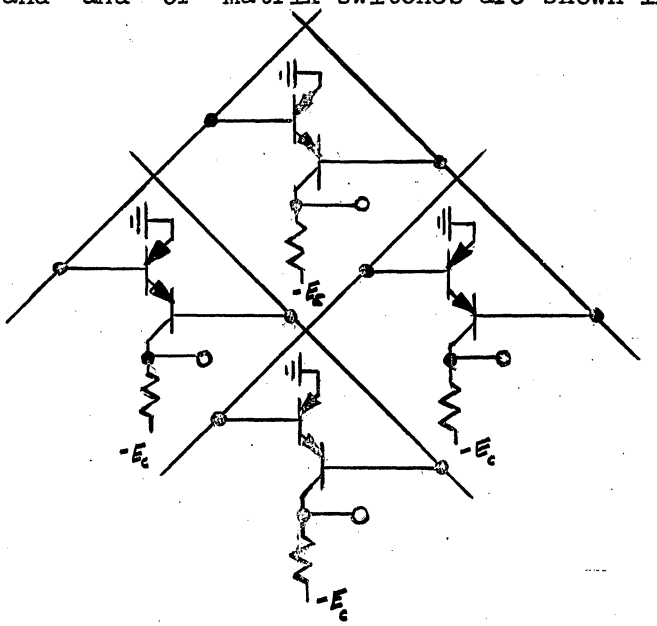
FOUR POSITION "AND" CONTROL SWITCH



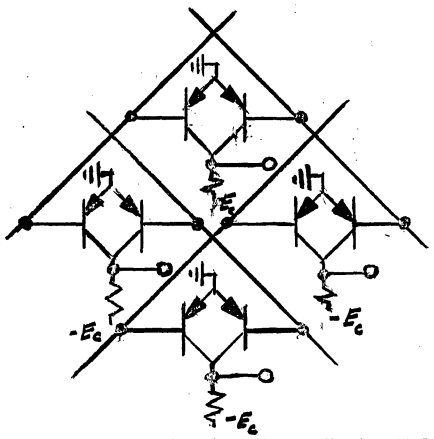
FOUR POSITION "OR" CONTROL SWITCH

FIGURE 6.

3. Transistor "and" and "or" types of matrix switches will be analyzed. Two typical "and" and "or" matrix switches are shown in Figure 7.



FOUR OUTPUT "AND" MATRIX SWITCH

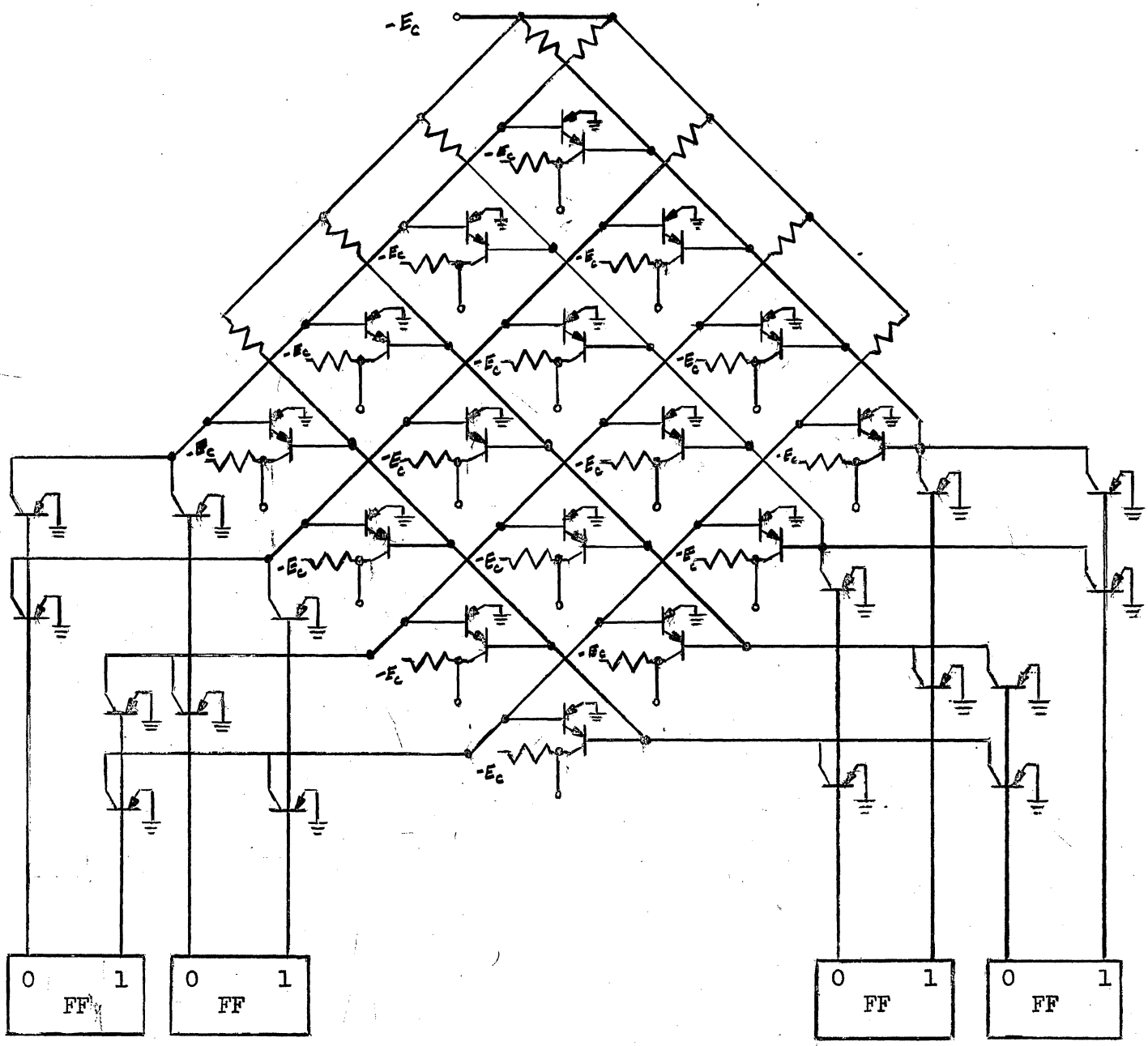


FOUR OUTPUT "OR" MATRIX SWITCH

FIGURE 7.

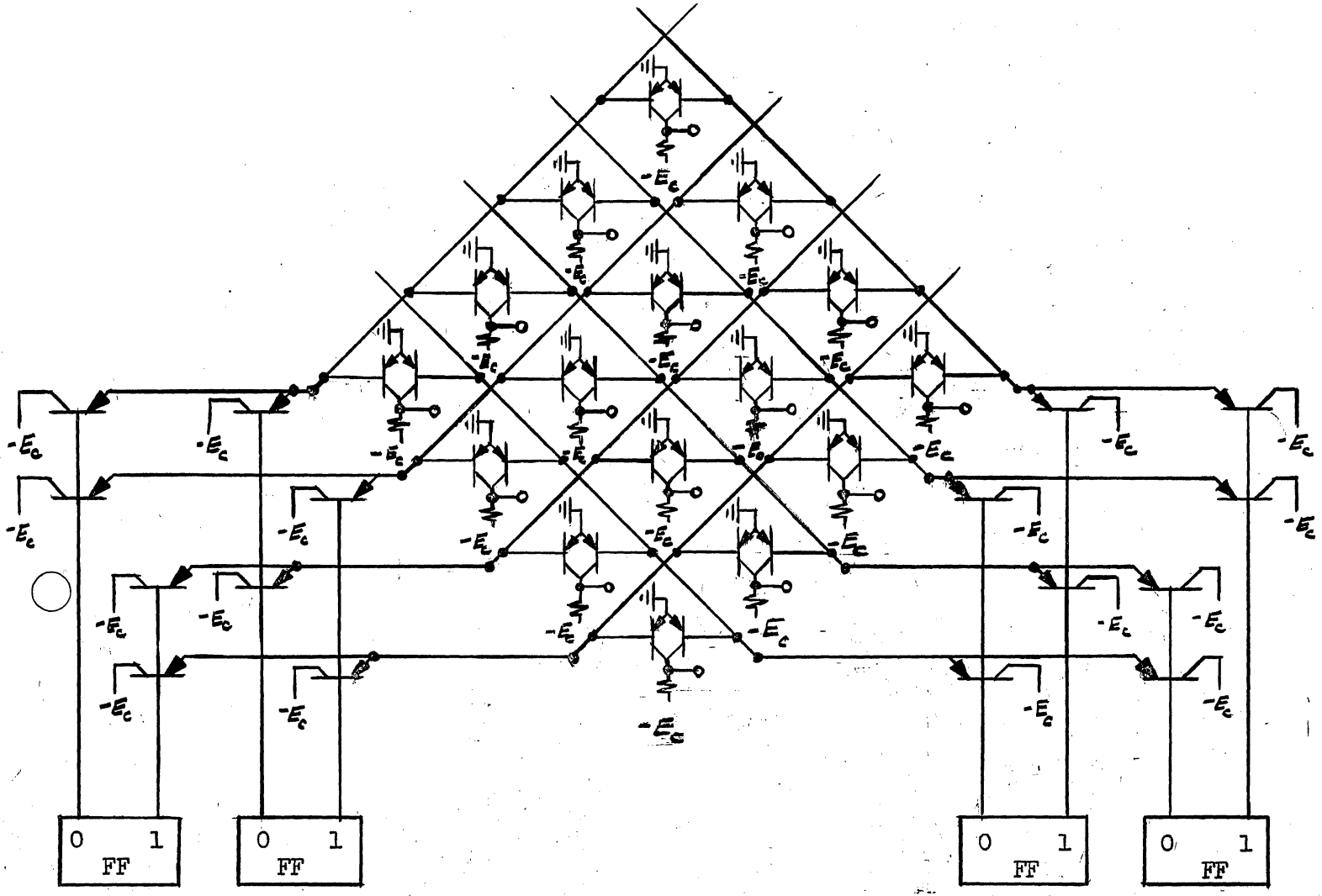
4. A transistor multiposition selection switch consisting of a matrix type switch controlled by two control switches will be designed, constructed, and analyzed. Shown in Figures 8 and 9 are typical multiposition switches. Static and dynamic analysis with consideration of economy will be studied for optimum design procedures.

Thought will be given to the type of load to be driven from the output of this switch which will include either driving the grid of a vacuum tube or perhaps a transistor selection switch.[12]



SIXTEEN OUTPUT MULTIPOSITION SWITCH (ZERO SELECT)

FIGURE 8.



SIXTEEN OUTPUT MULTIPOSITION SWITCH ($-E_c$ SELECT)

FIGURE 9.

EQUIPMENT NEEDED:

Lincoln Laboratory will supply the test equipment and components necessary for this thesis. This equipment will primarily be composed of the Burrough's Standard Test Equipment.

ESTIMATED DIVISION OF TIME:

1.	Preparation of the proposal.	50 hours
2.	Further study of the literature.	25 hours
3.	Experimental work and analysis.	150 hours
4.	Correlation of results and formulation of deductions and conclusions.	75 hours
5.	Preparation of the thesis report.	100 hours
	Total	400 hours

SIGNED: Paul G Griffith
Paul G. Griffith

Date: September 29, 1955

SUPERVISION AGREEMENT:

In my opinion this problem is adequate for a Master's thesis; therefore, I am willing to jointly supervise the research and evaluate the thesis.

APPROVED: William K. Linvill
W. K. Linvill
Associate Professor of
Electrical Engineering

APPROVED: Dudley A. Buck
D. A. Buck
Instructor in
Electrical Engineering

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BIBLIOGRAPHY

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12. Davidson, George A., "A Transistor Selection System for a Magnetic-Core Memory," Lincoln Laboratory, Memorandum 6M-3717, June 1955.