LITTON L-304

MICROSYSTEM DIGITAL COMPUTER

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INTRODUCTION

The Litton L-304 Computer is a high-speed, militarized, general-purpose digital computer which is highly reliable, small in size, light in weight, and consumes little power. These characteristics are achieved by full micro-miniaturization and use of advanced techniques in memory design, interconnection, heat removal, digital circuitry, and power supplies. The L-304 Computer is shown in Figure 1.

Figure 1. L-304 Computer

An extensive list of 62 instructions includes several for special comparison and data handling operations. Programming is simplified and operating time shortened by use of these special instructions for programs containing functions such as correlation, association, tracking, list processing, coordinate transformation, display generation, and communication. Multiprogramming in the L-304 Computer is facilitated by the availability of 64 program levels with eight multipurpose process registers per program level. These process registers, usable either as accumulators or index registers, account in part for the high speed of the computer.

Additional characteristics of the L-304 Computer are:

- Parallel, binary operation
- 32-bit instruction word
- 16- or 32-bit data word, including sign bit
- 2-microsecond memory read-write cycle
- Memory expandable in 4096-word modules from 4096 to 32, 768 words
- 8. 5-megacycle clock rate
- 7 addressing modes
- Accommodation of up to 64 input-output devices
- Predicted mean time between failures greater than 8000 hours
- Predicted availability greater than 99. 99 percent
- Compatible with American Standard Code for Information Interchange (ASCII)
- Real-time clock
- Multiprogramming and multiprocessing capabilities

More detailed information on the L-304 Computer, as well as information on the higher-speed L-305 and L-306 Computers, is contained in the Litton document, Litton L-300 Microsystem Digital Computers. That document also provides information on the multiprogramming and multiprocessing capabilities of the L-304, L-305, and L-306 Computers.

SYSTEM ORGANIZATION

A block diagram of the L-304 Computer is shown in Figure 2. The L-304 is divided into five modular sections: central computer, micromemory, input-output, control console, and power supply. Within the central computer section, the number of flip-flop registers has been minimized and multiple use is made of each of the registers in the L-304 Computer. This organization reduces size, weight, and power consumption, and minimizes cost by decreasing the number of components.

Additional features of the system organization are:

(1) 62 basic instructions

(2) 512 multipurpose process registers

(3) Seven addressing modes

(4) Special Move and Gated Comparison instructions

(5) 64 program interrupt levels

(6) 64 input-output channels

Each of these features will be separately described.

INSTRUCTION REPERTOIRE

The L-304 instruction word, shown in Figure 3, is divided into the following six fields:

(1) E (Control Designator)—A "one" in this bit position automatically causes the next instruction in sequence to be skipped, unless an illegal arithmetic operation, such as overflow, occurs, in which case the next instruction in sequence is performed.

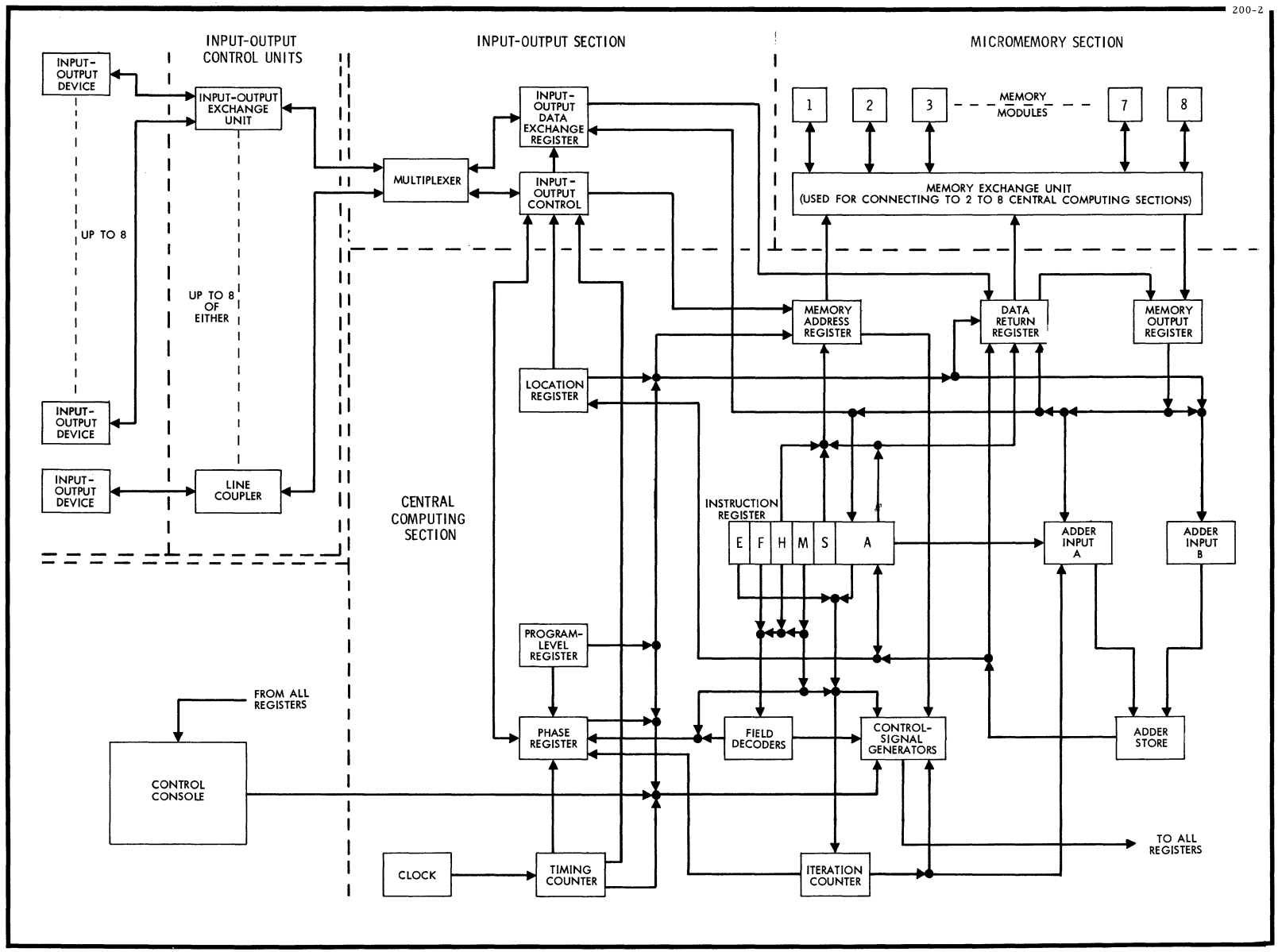

Figure 2. L-304 Block Diagram

FIELD	E	F						H			M			S			A													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BITS	1	6						3			3			3			16															

Figure 3. Instruction Word Format

(2) F (Function Code)—This 6-bit field, consisting of two octal digits, determines the operation to be performed.

(3) H (Accumulator Designator)—This 3-bit field specifies which of the eight process registers is to function as an accumulator.

(4) M (Addressing Mode Designator)—This 3-bit field designates which of the seven addressing modes is to be used.

(5) S (Index Register Designator)—This 3-bit field specifies which of the eight process registers is to function as an index register.

(6) A (Address)—This 16-bit field, nominally the address field, has its contents specified by the addressing mode. The 16 bits permit the selection of any one of the 65,536, 16-bit half-words in memory.

The 62 basic instructions are listed in the Appendix.

MULTIPURPOSE PROCESS REGISTERS

There are eight addressable 16-bit process registers for each of the 64 computer input-output channels. Each of these registers is multipurpose; it may be used as an accumulator, an index register, or for list processing purposes. The registers to be used by an instruction are specified in the instruction word by the H and S fields, as indicated above.

The use of multipurpose process registers provides programming ease and greatly reduces the need to move data between working registers and the memory. Furthermore, the fact that the same registers have more than one purpose further reduces time in many instances. For example, a number generated in a register used as an accumulator may be used directly for a table look-up operation merely by next designating that register as an index register. On the other hand, an index register may be modified or compared as easily as an accumulator merely by next designating the register as an accumulator. Additional flexibility has been provided for these process registers by assigning normal memory addresses to them, thus simplifying interregister operations.

A further feature of the process registers is that they may sometimes be regarded as register pairs. A register pair can be loaded from memory or stored into memory with a single instruction. In addition, a Shift Long Left instruction will shift data from one register to the next.

ADDRESSING MODES

The seven addressing modes included in the L-304 Computer provide a great degree of power and flexibility in the ways in which data can be referenced in memory. These addressing modes are:

(1) Direct — The operand is in the location specified by the A field of the instruction word.

(2) Direct with Indexing — The operand is in the location specified by the sum of the A field of the instruction word and the contents of the index register specified by S.

(3) Literal—The operand is the A field of the instruction word.

(4) Literal with Indexing—The operand is the sum of the A field of the instruction word and the contents of the index register designated by S.

(5) Indirect—The A field of the instruction word contains the address of the word in memory which contains the address of the operand.

(6) Indirect with Direct Indexing—The A field of the instruction word is added to the designated index register. The result is the address of the word in memory, which contains the address of the operand.

(7) Indirect with Indirect Indexing—The A field of the instruction word contains the address of a word in memory, the contents of which are added to the designated index register. The result is the address of the operand.

Literal addressing permits rapid access to constants and can reduce memory requirements by allowing a constant to be stored within an instruction itself. The three indirect addressing modes are important aids in programs which utilize list processing techniques, particularly those programs which involve not only association and correlation problems, but also those concerned with sorting and searching operations.

SPECIAL INSTRUCTIONS

Two special types of instructions, the Move instructions and the Gated Comparison instructions, are provided in the L-304 instruction repertoire. Both instructions are valuable in a variety of programs.

The two Move instructions allow any number of bits in one register to be addressed by means of a mask and moved to any position in another process register. One of the two instructions allows the bits to be stored in the second register without disturbing the remaining contents of that register. The second instruction permits storage of the bits in the second register and sets the remainder of that register to zero. This capability

greatly facilitates the handling of "packed" data, i.e., data that are stored to minimize memory requirements by packing several short items in a single word.

The four Gated Comparison instructions allow comparisons to be made between a value in memory and the contents of one of the process registers plus or minus a designated gate value. This gate value must be stored in a specific process register prior to the execution of the gated comparison. The program can be made to branch if the value in memory falls inside the gate range, outside the range, outside and less than the range, or outside and greater than the range. These instructions are extremely useful where values are known only approximately or where some tolerance is allowed on either side of an expected value.

PROGRAM INTERRUPT LEVELS

A significant feature of the L-304 Computer is the availability of 64 program interrupt levels. Each level may contain an independent program or an integrated portion of a larger program. Each level has eight process registers, including a location register, and time-shares the arithmetic section and memory output register with the other 63 levels. Each level has an assigned priority, but only operates if the level is the highest priority "active" level. An interrupt level may be designated "active" either by instruction or by interrupts from the input-output section. Interrupts may thus be processed immediately without program provision for temporary storage of the process register contents.

Automatic switching from one program level to another, without the required intercession of an executive routine, is of utmost importance in real-time computing. In many instances, the time constraints are such that a requirement to branch to an executive routine prior to changing program levels will consume more time than is allowed for execution of the object program itself. Executive routines do play an important role in setting up program priorities prior to entry into a critically timed real-time operation. Flexibility in the assignment of program level priorities has therefore been provided in the L-304 Computer.

INPUT-OUTPUT CHANNELS

Extensive, versatile input-output capabilities are provided in the L-304 Computer. Each computer may communicate with up to 64 input-output devices through a system which uses line couplers and input-output exchange units as shown in Figure 2. Once a transfer of data is initiated, transmission between the computer memory and the input-output device is accomplished independently of the computer program.

The maximum rate of data transfer over all 64 input-output channels with the L-304 Computer is 62, 500, 8-bit characters per second or 62, 500, 32-bit words per second.

PHYSICAL CHARACTERISTICS

The L-304 Computer is compact, light in weight, and consumes little power. The dimensions, weight, and power consumption of the L-304 are indicated in Table 1.

Table 1. L-304 Computer Physical Characteristics

Memory Size (32-bit words)	Dimensions (inches)			Weight (pounds)	AC Line Power Consumption (watts)
	Length	Width	Height		
4,096	10-1/2	9	3-1/2	20	160
8,192	10-1/2	9	4-1/2	26	195
16,384	10-1/2	9	6-1/2	37	255
32,768	10-1/2	9	10-1/2	60	380

The power input to the computer is approximately 80 percent of that shown in Table 1. The microminiature power supply accounts for the remaining 20 percent of the power consumption. The computer is capable of operating from +28 vdc power in accordance with MIL-STD-704 or 208/120 vac, 400-cps, 3-phase power. A 115-vac, 60-cps, single-phase power pack is available when operation from commercial 60-cps power is required.

FABRICATION TECHNOLOGY

CIRCUITRY

There are various advantages to the use of microelectronic circuits. These advantages include a reduction in overall equipment cost, size, weight, and power consumption, and an increase in overall reliability.

The circuitry used in the L-304 Computer consists of semiconductor integrated circuits, in the form of NAND (an inverted logical AND) gates, interconnected by multilayer laminated boards. The Litton integrated NAND circuits (LINCs) are of two types: an eight-input NAND gate, and a dual, four-input NAND gate. Both LINCs measure 0.250 by 0.175 by 0.065 inch, excluding leads, and 0.325 by 0.375 by 0.065 inch, including leads.

These LINCs—developed for use in the TFX aircraft, Phoenix missile fire control computer—are obtainable from multiple sources of supply. The LINCs, thoroughly tested and highly reliable in operation, were the result of an intensive Litton development program. Since only two types of LINCs are used in the computer, supply and maintenance are simplified and facilitated.

MODULES

The modular construction of the L-304 Computer offers certain distinct advantages over conventional construction. Automated fabrication techniques can be used to significantly reduce construction cost, and system adaptability and expandability are easily achieved. As system requirements change, the L-304 Computer is designed to accommodate varying quantities and combinations of modules. Increased memory capacity or conversion from a single to a multicomputer is accomplished merely by adding modules.

The modules in the L-304 Computer are in the form of drawers, which plug into the computer housing. These drawers are shielded assemblies, consisting of 18 patchboards, 9 mounted on each side of a master board. The patchboard, which measures 1.9 by 2.5 inches and accommodates 30 LINCs, is shown in Figure 4.

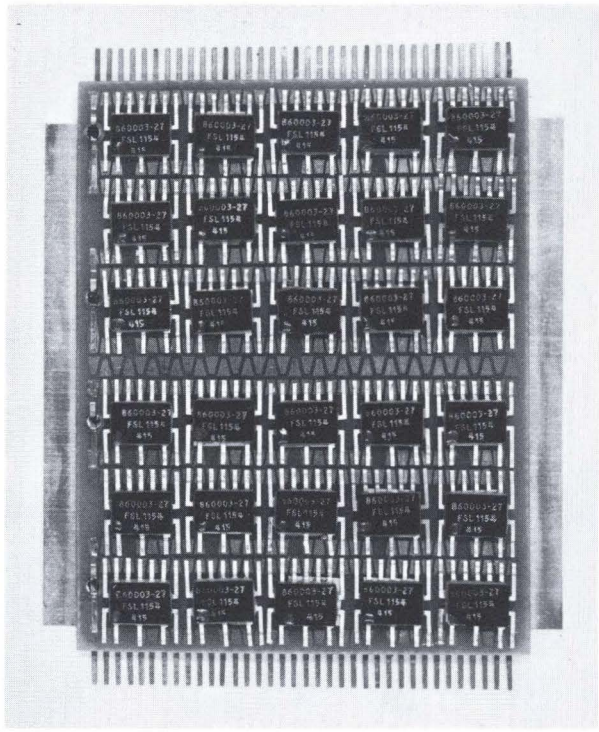

Figure 4. Patchboard

MILITARIZATION

The L-304 Computer is planned for a military environment, and does not require air conditioning or heating. It is designed to meet the applicable sections of the following environmental specifications:

Altitude	MIL-E-5400F
Temperature range	-55°C to +125°C; MIL-STD-169, MIL-E-5400F, and MIL-E-16400E
Humidity	MIL-STD-170 and MIL-E-5400F
Vibration	MIL-E-5400F
Shock	MIL-S-901C
Orientation	MIL-E-16400E
Radio frequency interference	MIL-I-6181D, MIL-I-11748D, and MIL-I-16910A
Sand and dust	MIL-STD-810
Salt spray	MIL-E-16400E
Fungus	Nonnutrient
Drip-proofing	MIL-STD-108

RELIABILITY

Reliability in the L-304 Computer is achieved through:

- Use of conservatively designed integrated and thin-film hybrid microcircuits, with complete control maintained over all details of their production, transportation, test, storage, and handling.
- Use of highly reliable multilaminar boards for microcircuit interconnection.
- Redundancy of memory modules, central computers, and input-output channels.
- Computer monitoring of the entire system with programmed automatic switchover to another memory module, central computer, or input-output channel in the event of failure.

Microcircuits of the semiconductor integrated and thin-film hybrid types, as used in the L-304 Computer, have inherently greater reliability than conventional component circuitry for two principal reasons: (1) the number of separate point connections is considerably reduced, and (2) the overall reliability of the system is not dependent upon the individual reliabilities of each component but is instead a function of the reliabilities of component groups. The large reduction in point connections is highly beneficial to overall system reliability since each connection is a potential source of failure. Groups of components, rather than separate components, are used in the determination of reliability figures for integrated microcircuits since all similar electrical elements (for example, capacitors) of these microcircuits are fabricated simultaneously. This fabrication method results in fewer steps and increased reliability for individual circuit elements.

Thin-film hybrid microcircuits are used for those circuits which must operate either at higher speed or higher power than is possible with semiconductor integrated microcircuits.

The predicted mean time between failures (MTBF) for the L-304 Computer will vary depending on the modules included within the computer. This prediction is based on a series functional relationship of individual module failure rates. The L-304, with 4096 words of micromemory would require three power supply units. The predicted MTBF for such a combination would be 8500 hours.

MAINTAINABILITY

Although the need for maintenance will be infrequent because of the high MTBF of the L-304 Computer, the predicted availability figure of better than 99.99 percent for this computer requires that maintenance be easily performed when necessary. Availability is equal to the MTBF divided by the sum of the MTBF and the mean time to repair.

Computer faults in the field are automatically isolated to specific plug-in drawers by the use of the computer self-test feature. Programmed isolation of faults to specific areas of the drawers will be possible at the repair depot level. A hand-held microcircuit tester with self-contained power will also be available for use at depot level. Diodes are used to isolate the microcircuits so that faults may be diagnosed without the need to detach a microcircuit.

APPENDIX. INSTRUCTION LIST

Instruction*	Mnemonic Code	Function Code	Timing (microseconds)
Add	ADD	10	7
Add Absolute	ADA	14	7
Add Unsigned	ADN	16	7
Compare, Jump if Equal	CJE	51	7
Compare, Jump if Greater	CJG	53	7
Compare, Jump if Less	CJL	50	7
Compare, Jump if Unequal	CJU	52	7
Divide	DIV	31	38
Decrement RH by One, Transfer if RH ≠ 0	DOX	33	5
Decrement RH by Two, Transfer if RH ≠ 0	DTX	32	5
Exchange	EXC	02	8
Exchange Double	EXD	03	8
Exclusive OR	EOR	20	7
Execute	EXE	01	2
Gated Comparison, Jump if Inside	GCI	54	10
Gated Comparison, Jump if Outside	GCO	55	10
Gated Comparison, Jump if Outside and Greater	GCG	57	10
Gated Comparison, Jump if Outside and Less	GCL	56	10
Halt	HLT	77	2
Inclusive OR	IOR	21	7
Interrogate Status	INS	75	11 to 26
Jump Three Way	JTW	37	7
Load Double	LDD	06	6
Load RH	LDR	04	6
Logical AND	AND	22	7
Move and Insert	MVI	70	7 + n
Move and Zero	MVZ	71	8 + n
Multiply	MPY	30	28 to 38

*Refer to notes at end of Appendix.

APPENDIX. INSTRUCTION LIST (Continued)

Instruction*	Mnemonic Code	Function Code	Timing (microseconds)
No Operation	NOP	00	2
Normalize Long Left	NLL	45	9 + p
Prepare to Receive	PRC	74	9
Prepare to Transmit	PTM	73	9
Reflect	RFT	47	6 + p
Replace Add	RAD	12	7
Replace Exclusive OR	RER	24	7
Replace Inclusive OR	RIR	25	7
Replace Logical AND	RAN	26	7
Replace Subtract	RUB	13	7
Reset Lower Bit	RBL	62	5
Reset Upper Bit	RBU	63	5
Set Lower Bit	SBL	60	5
Set Upper Bit	SBU	61	5
Shift and Count	SNC	46	7 + p + m
Shift Long Left	SLL	44	6 + p
Special Device Command	SDC	76	10
Store All Zeros	STZ	72	5
Store Double	STD	07	6
Store RH	STR	05	6
Subtract	SUB	11	7
Subtract Absolute	SBA	15	7
Subtract Unsigned	SBN	17	7
Test Lower Bit, Jump if 0	TLZ	64	5
Test Lower Bit, Jump if 1	TLF	66	5
Test Upper Bit, Jump if 0	TUZ	65	5
Test Upper Bit, Jump if 1	TUF	67	5
Transfer if RH = 0	XEZ	40	5
Transfer if RH ≠ 0	XNZ	41	5

*Refer to notes at end of Appendix.

APPENDIX. INSTRUCTION LIST (Continued)

Instruction	Mnemonic Code	Function Code	Timing (microseconds)
Transfer if RH is Negative	XNG	42	5
Transfer if RH is Positive	XPS	43	5
Transfer on Console Transfer Switch	XSW	36	2
Transfer Unconditional	XFR	34	2
Transfer Unconditional and Store Link	XLK	35	4

NOTES:

1. Add 2 microseconds for indexed or indirect addressing. Add 4 microseconds for indexed and indirect addressing. Subtract 2 microseconds for literal addressing.

2. RH = process register

3. m = number of 1's in count

4. n = number of right shifts required for alignment

5. p = number of bit positions shifted

DATA SYSTEMS DIVISION OF LITTON INDUSTRIES