PUB. NO.	OLD REV.	NEW REV.	TITLE
29-526	R02	R03	M83-Series Model 8/32 Processor Customer Installation Manual

This revision includes changes reflecting:

ECNs 3701

SCNs

Briefly, the changes are as follows:

This Package Consists Of:

This Instruction Sheet

New Title Sheet

Page Revision Status Sheet

Sheets iii, iv, 5 thru 27

A159

METRIC

M83-SERIES
MODEL 8/32 PROCESSOR
CUSTOMER INSTALLATION MANUAL

PERKIN-ELMER

Interdata Division
2 Crescent Place
Oceanport, N.J. 07757

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-526

TITLE Model 8/32 Customer Installation Manual

REVISION R03   DATE August 1978

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
i/ii	R02	5/78						
iii	R03	8/78						
iv	R03	8/78						
1	R02	5/78						
2	R00	1/78						
3	R00	1/76						
4	R00	1/76						
5								
thru								
27/28	R03	9/78						

TABLE OF CONTENTS

FIGURES

TABLES

4. POWER SUPPLY INSTALLATION

4.1 Introduction

This section describes the installation of the Model 8/32 Power Supply. Mounting information and cabling instructions are provided for the Power Supply in various configurations. Power Supply types 34-023 and 34-033 are currently available. Older supplies are referenced where appropriate.

4.2 Mounting

The power supplies mount directly behind the Processor and Expansion chassis (see Figure 8). They are attached to the right mounting upright (viewed from the rear). There is adequate slack in the power supply cable to allow the power supply to swing out. To prevent the cable from being pinched between the power supply and chassis support rails, a service loop is required. Power Supply 34-023 mounting varies slightly. Refer to Publication Number 29-452 for details.

<p align="center">WARNING</p>

<p align="center">BEFORE SWINGING OUT THE POWER SUPPLIES, THE RACK
LEVELING FEET SHOULD BE LOWERED. UP TO FIVE POWER
SUPPLIES CAN BE SWUNG OUT AT ONE TIME AFTER THE
LEVELERS ARE IN CONTACT WITH THE FLOOR SURFACE.</p>

The power supplies may be swung in or out on their mounting pivots for easy access to the back plane. When they are in operating position, they are secured by two 10-32 screws which attach to the left mounting upright (viewed from the rear).
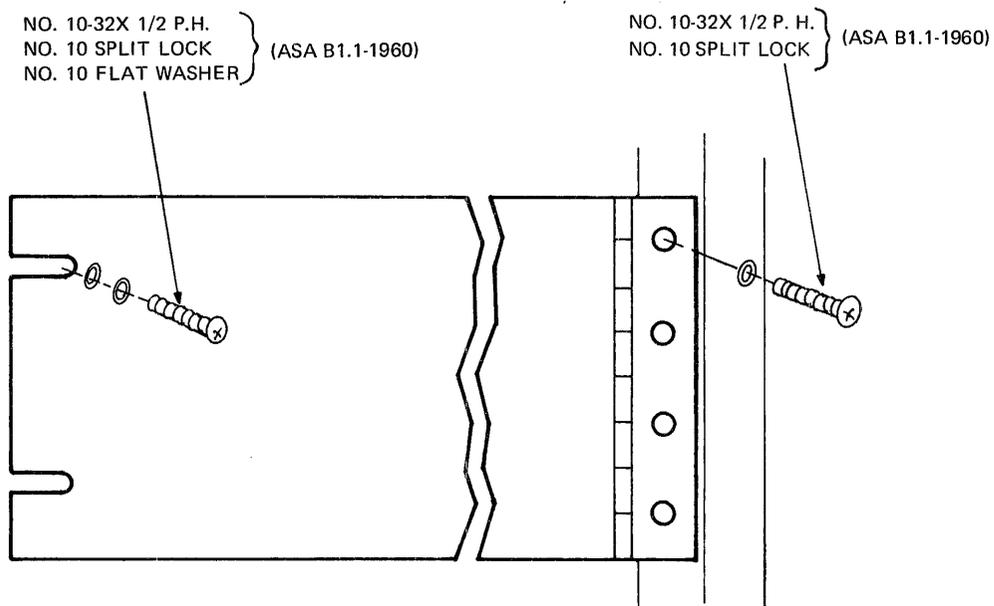
Figure 8. 34-033 Power Supply Mounting

4.3 Power Supply/Chassis Cabling

4.3.1 <u>System Voltages</u>. The Model 8/32 System requires three system voltages:

Mnemonic	Voltage
P5	+5V
P15	+16.5V
N15	−16.5V

Any other voltages locally generated are not considered system voltages.

4.3.2 System Power Supply. The standard INTERDATA Power Supply is used for all power requirements in the Model 8/32 System. All three outputs (P5, N15, and P15) are short circuit protected, and regulated to +1% when normally loaded. P15 and N15 are overvoltage protected. On the 34-033 Power supply, P5 is also overvoltage protected.

Refer to the appropriate Power Supply Manual for installation and operating details. Refer to Figures 9 and 10 for power control set up for additional power supplies.

4.3.2.1 Power Supply Manuals

The following chart indicates the appropriate maintenance manual for various power supplies.

POWER SUPPLY	MANUAL NUMBER
34-026 34-027 34-029	29-437
34-023	29-452
34-033	29-595

NOTE: ALL OF THE ABOVE POWER SUPPLIES ARE FUNCTIONALLY EQUAL.
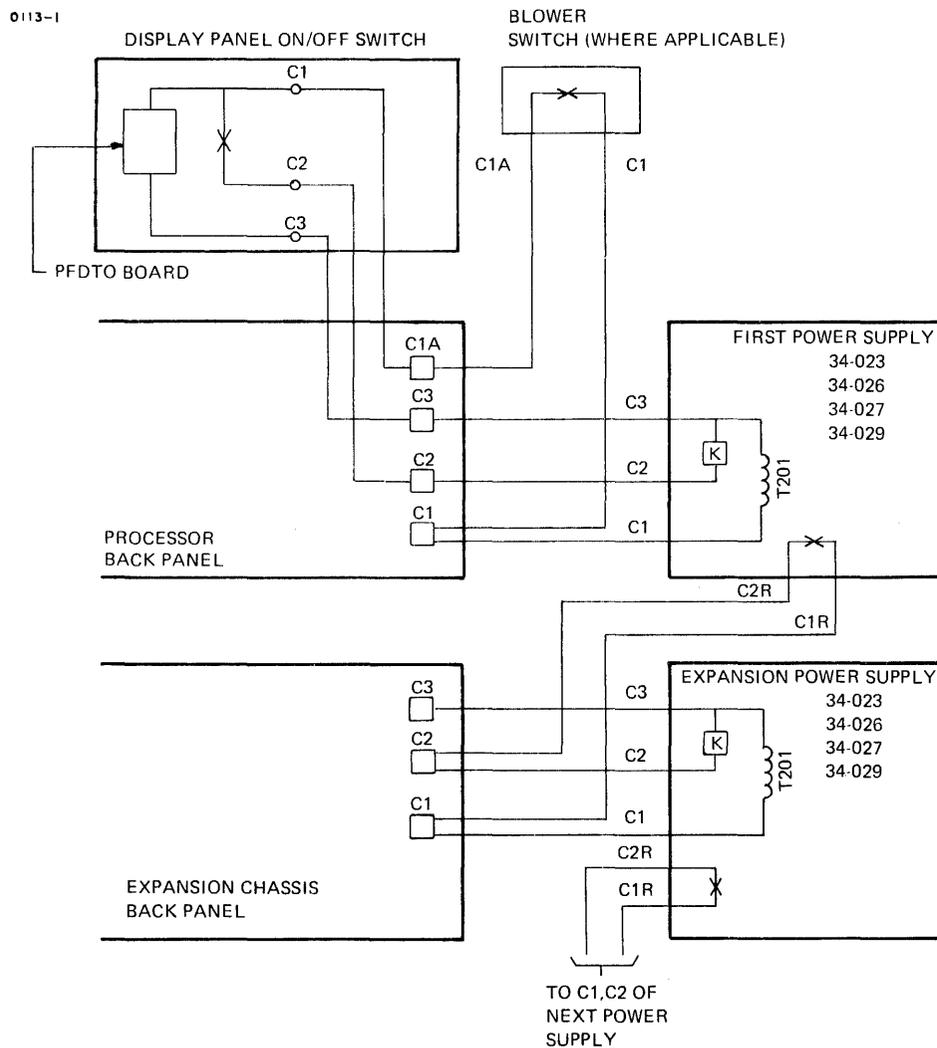
Figure 9. Set Up for Additional Power Supplies
(34-023, 34-026, 34-027, 34-029)

6

DISPLAY PANEL ON/OFF SWITCH

BLOWER SWITCH (WHERE APPLICABLE)
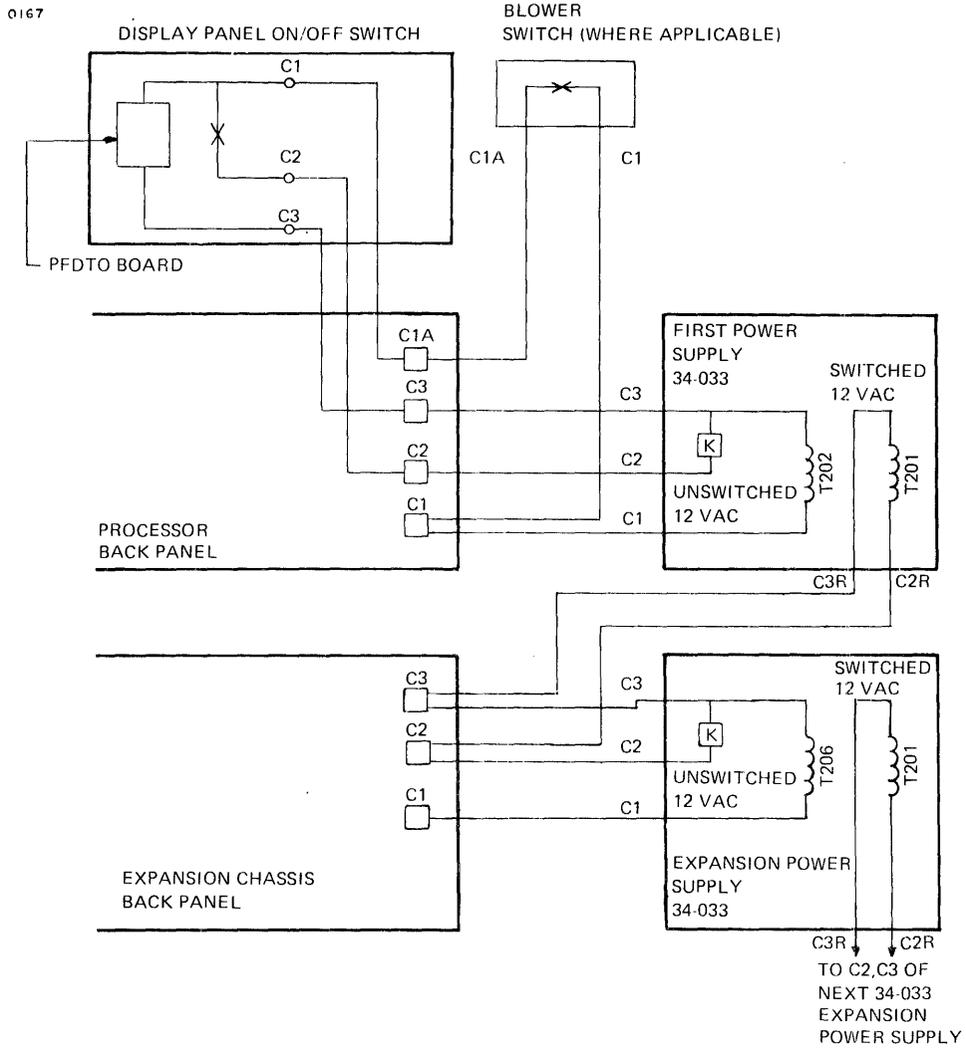
Figure 10. Set Up for Additional Power Supplies (34-033)

4.3.3 Primary Power Requirements. The Power Supply is limited to operating at 115VAC or 230VAC + 10%, 47 to 63 Hz.

NOTE

All supplies which power the Processor and memory expansion chassis must receive AC power of the same phase from a single circuit breaker.

The maximum power requirements for each Power Supply are:

Input Line	34-023	34-033
115 VAC	7.5 Amperes	6.5 Amperes
230 VAC	3.75 Amperes	3.25 Amperes

4.3.4 Conversion Procedure from 115 to 230 VAC Operation. The Power Supply is shipped from the factory strapped for 115 VAC. To switch to 230 VAC operation, refer to the appropriate power supply manual.

4.3.5 <u>Adjustments.</u> All power system adjustments are made at the factory and should not require readjustment in the field. If readjustment becomes necessary, the recommended settings are given below.

Voltage Adjustments:

Mnemonic	Voltage Setting
P5	+ 5.1 Volts
P15	+16.5 Volts
N15	−16.5 Volts

Voltages should always be measured at the backpanel when making adjustments. These adjustments are made after disconnecting the tracking thermistors and placing a 1 K ohm ±5% resistor across the thermistor terminals.

4.3.6 Configuration. In a Model 8/32 System, the minimum system configuration consists of one twin chassis and two standard INTERDATA Power Supplies. Figure 11 shows the power distribution of the basic system.

4.3.7 <u>Installation.</u> The installations for the various power systems are:

1. Connect the cables to the twin chassis; referring to one of the following figures, depending upon the configuration:

   – Basic 8/32 Processor with 128KB Memory (Figure 11).
   – Basic 8/32 Processor and First Memory Expansion Chassis with 256KB Memory (Figure 12).
   – Basic 8/32 Processor and First Memory Expansion Chassis with 384KB and 512KB Memory (Figure 13).
   – Basic 8/32 Processor, First and Second Memory Expansion Chassis with 640KB to 1024KB Memory (Figure 14).
   – Basic 8/32 Processor with Double Floating Unit and/or Writable Control Store (Figure 15).

   Note that the memory expansion backpanel contains two sets of +15 and -15 VDC power busses, and in some configurations it is necessary to connect the busses with jumper cables.

2. Cables from the front of the chassis may be routed through the 44.5 mm (1¾") space between chassis (see Figure 3). If there are any unused connectors, secure them to prevent shorting.

POWER SUPPLY LEADS	POWER SUPPLY NO. 1	POWER SUPPLY NO. 2				
CHASSIS BACK PANEL DESIGNATION						
P15	B	B				
N15	B	B				
(4) P5	A	B				
(3) GND	A	B				
GND (+15)	B	B				
TA	A	B				
TB	A	B				
C1	B	B				
C2	B	B				
C3	B	T. B.				
+L	A	T. B.				
LGND	A	T. B.				
FAN POWER	*T. B.	T. B.				

* T. B. — TIE BACK WIRE

BACK PANEL DESIGNATION
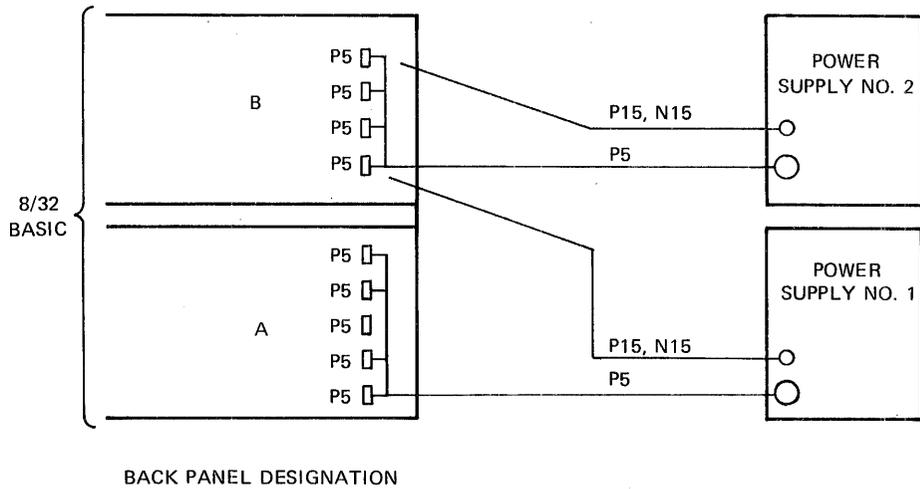
Figure 11. Basic 8/32 with 128 KB Memory Power Distribution

POWER SUPPLY LEADS	POWER SUPPLY NO. 1	POWER SUPPLY NO. 2	POWER SUPPLY NO. 3			
CHASSIS BACKPANEL DESIGNATION						
P15	T. B.	C	D			
N15	T. B.	C	D			
GND (I15)	T. B.	C	D			
P5	A	B	C			
P5	A	B	C			
P5	A	B	D			
P5	A	B	D			
GND	A	B	C			
GND	A	B	D			
GND	A	B	D			
TA	T. B. Note 2	C	D			
T.B.	T. B. Note 2	C	D			
C1 Note 1	B	B	D			
C2 Note 1	B	B	D			
C3	B	T. B.	T. B.			
+L	A	T. B.	T. B.			
LGND	A	T. B.	T. B.			
FAN POWER	T. B.	T. .B.	T. B.			

* T. B. — TIE BACK WIRE

NOTES

1. Connect C1 and C2 on "B" backpanel to C1 and
   C2 on "D" backpanels with jumper wires 17-182.

2. P15 and N15 voltages on this Power Supply
   must be adjusted to within a range of 15 to
   17.5 volts to prevent crowbars from triggering.
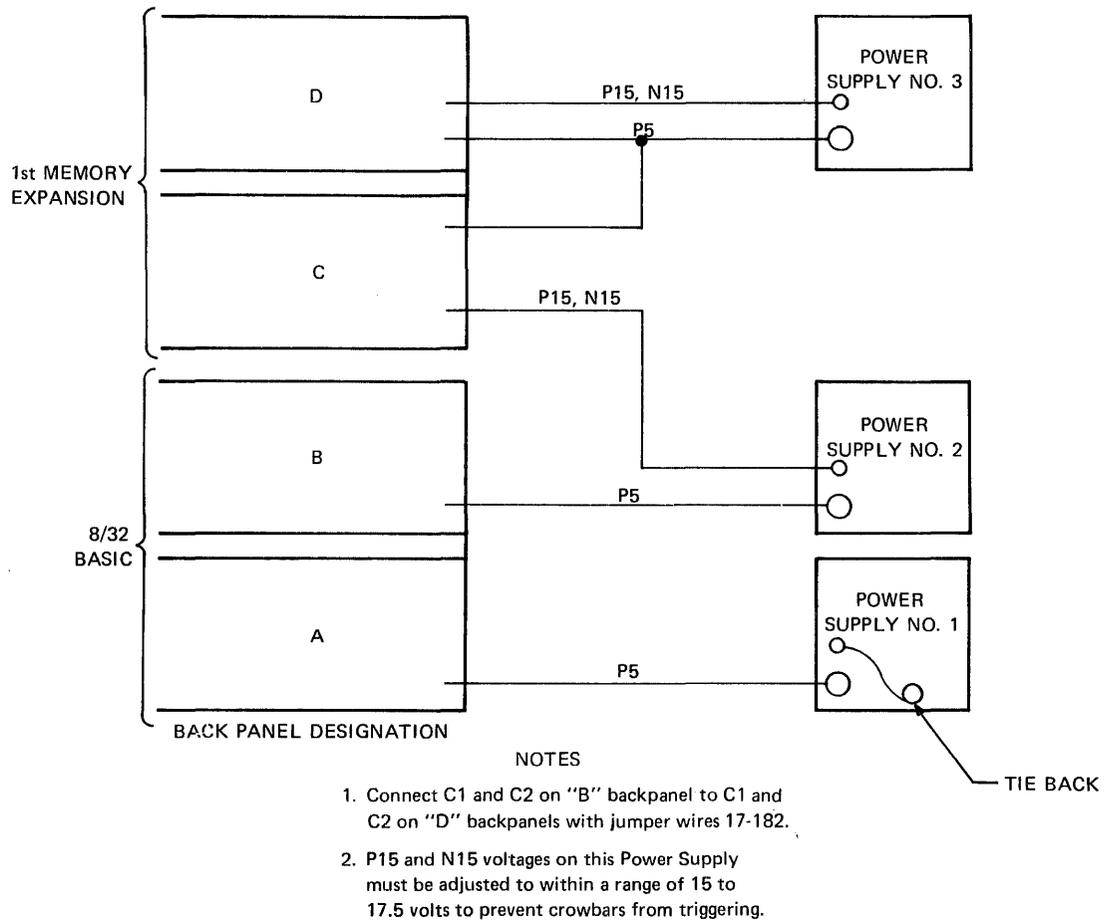
Figure 12. Model 8/32 with 256 KB Memory Power Distribution

POWER SUPPLY LEADS	POWER SUPPLY NO. 1	POWER SUPPLY NO. 2	POWER SUPPLY NO. 3	POWER SUPPLY NO. 4		
CHASSIS BACKPANEL DESIGNATION						
P15	C	C	D	D		
N15	C	C	D	D		
GND (I15)	C	C	D	D		
P5	A	B	D	C		
P5	A	B	D	C		
P5	A	B	D	C		
P5	A	B	D	C		
GND	A	B	D	C		
GND	A	B	D	C		
GND	A	B	D	C		
TA	C	C	D	D		
TB	C	C	D	D		
C1 Note 1	B	B	D	C		
C2 Note 1	B	B	D	C		
C3	B	T. B.	T. B.	T. B.		
+L	A	T. B.	T. B.	T. B.		
LGND	A	T. B.	T. B.	T. B.		
FAN POWER	T. B.	T. B.	T. B.	T. B.		

* T. B. — TIE BACK WIRE

Figure 13. Model 8/32 with 384 KB and 512 KB Memory Power Distribution
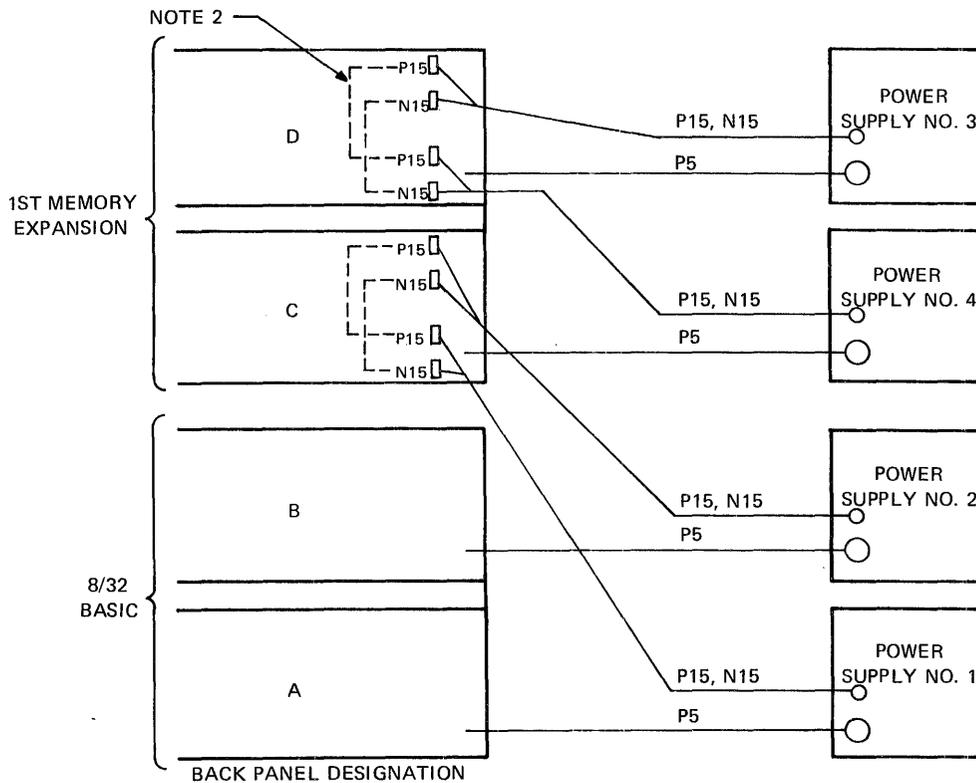
NOTES

1. Connect C1 and C2 on "B" backpanel to C1 and C2 on "C" and "D" backpanels with jumper wires 17-182.

2. Remove P15 and N15 jumpers on backpanel "C" and "D".

POWER SUPPLY LEADS	POWER SUPPLY NO. 1	POWER SUPPLY NO. 2	POWER SUPPLY NO. 3	POWER SUPPLY NO. 4		
	CHASSIS BACK PANEL DESIGNATION					
P15	F	C	D	E		
N15	F	C	D	E		
GND (+15)	F	C	D	E		
P5	A	B	D	E		
P5	A	B	D	E		
P5	A	B	C	F		
P5	A	B	C	F		
GND	A	B	D	E		
GND	A	B	C	F		
GND	A	B	C	F		
TA	F	C	D	E		
TB	F	C	D	E		
C1	B	B	D	E		
C2	B	B	D	E		
C3	B	T. B.	T. B.	T.B.		
+L	A	T. B.	T. B.	T.B.		
LGND	A	T. B.	T. B.	T.B.		
FAN POWER	*T. B.	T. B.	T. B.	T.B.		

*T.B. – TIE BACK WIRE
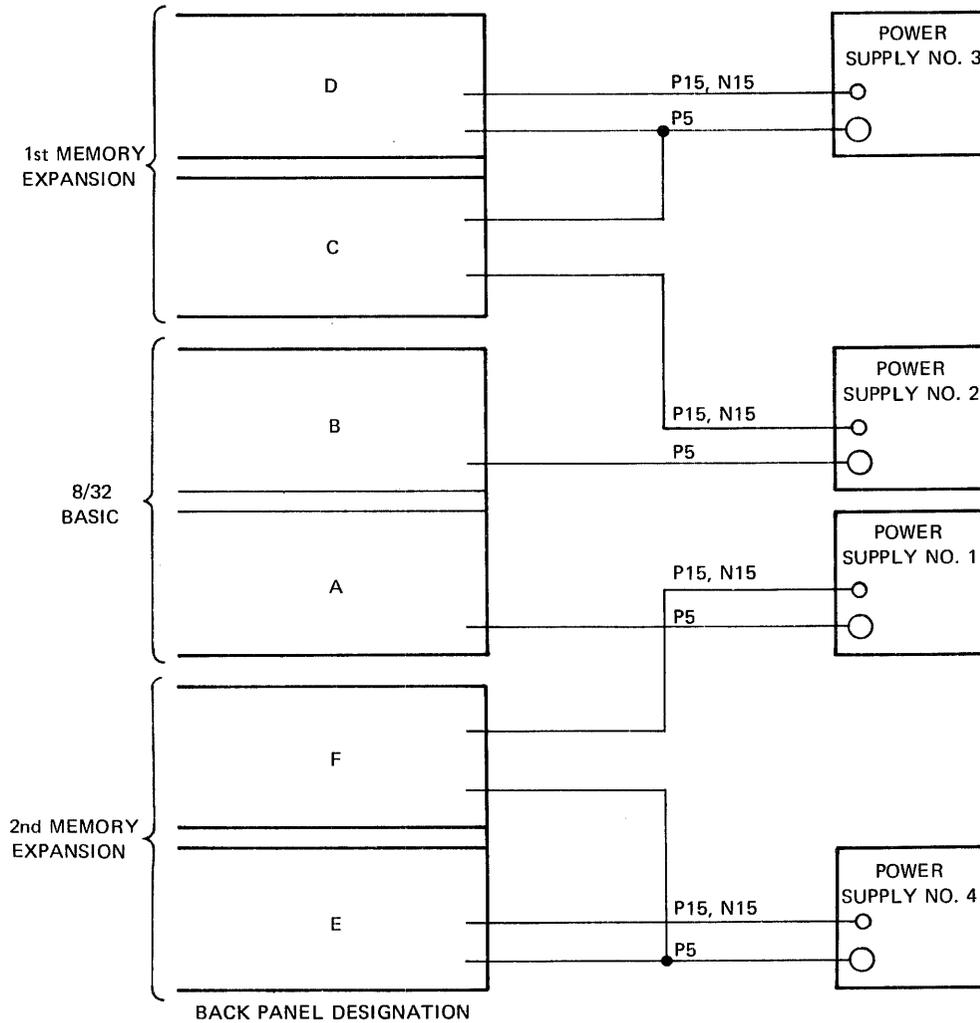
NOTE

Connect C1 and C2 on "B" backpanel to C1 and C2
on "D" and "E" backpanels with jumper wires 17-372.

Figure 14. Model 8/32 Power Wiring for 640KB to 1024KB Power Distribution

POWER SUPPLY LEADS	POWER SUPPLY NO. 1	POWER SUPPLY NO. 2	POWER SUPPLY NO. 3	POWER SUPPLY NO. 4	POWER SUPPLY NO. 5	
CHASSIS BACKPANEL DESIGNATION						
P15					T. B.	
N15					T. B.	
GND(I15)					T. B.	
P5					A	
P5					A	
P5					A	
P5					A	
GND					A	
GND					A	
GND					A	
TA					T. B. Note 1	
TB					T. B. Note 1	
C1					B	
C2					B	
C3					T. B.	
+L					T. B.	
LGND					T. B.	
FAN POWER					T. B.	

* T.B. — TIE BACK WIRE
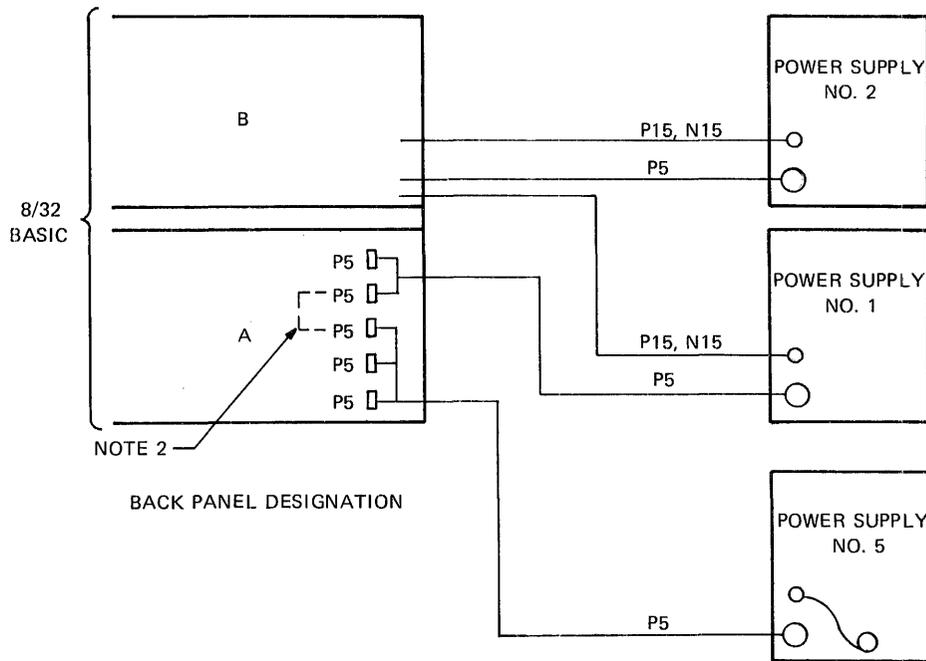
NOTES

1. P15 and N15 voltages on this Power Supply must be adjusted to within a range of 15 to 17.5 volts to prevent crowbars from triggering.

2. Remove P5 jumper on backpanel "A".

Figure 15. Model 8/32 Basic with Double Floating Unit and/or Writable Control Store Power Distribution

5. PROCESSOR AND EXPANSION CHASSIS INSTALLATION

5.1 Installation

For different memory expansions, it is possible to have from one to three 356 mm (14") twin chassis in the Model 8/32 System (located as shown in Figure 3). Figures 11 through 15 show the three possible configurations.

Prior to mounting the chassis, replace the appropriate solid covers on the plenums with perforated covers (see Section 3.2).

The 8/32 Basic System and its memory expansions must always be mounted in a cabinet that is equipped with a blower and plenum. It must be configured as shown in Figure 3. These chassis do not have chassis fans. 178 mm and 356 mm (7" and 14") chassis with fans are not to be used . When 178 mm (7") I/O chassis without fans are to be mounted in this cabinet, they must be installed in positions where duct covers are located (see Figure 3).

CAUTION

IF A CABINET OTHER THAN AN 09-069 INTERDATA CABINET IS USED, THE USER MUST SUPPLY HIS OWN FORCED AIR COOLING SYSTEM.

To mount a chassis, slide the chassis into the rack on the chassis support rails from the front of the rack (see Figures 1 and 2).

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A RACK CABINET OTHER THAN AN INTERDATA IS USED, CONSULT THE RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The chassis support rails are fastened to the mounting uprights of the front and rear of the rack. The Expansion and Processor chassis are screwed in place at the mounting uprights in front of the rack.

5.2 Basic Processor Configuration and Cabling

The basic Model 8/32 with 128KB of memory is comprised of:

1.	4 each 32-198 32KB core modules	Upper Slots 2, 4, 5, and 7
2.	2 each 35-534 LMI	Upper Slots 3 and 6
3.	1 each 35-535 MBC	Upper Slot 1
4.	1 each 35-536 CPA	Upper Slot 0
5.	1 each 35-537 CPB	Lower Slot 7
6.	1 each 35-555 CPC	Lower Slot 6
7.	1 each 35-538 ALU	Lower Slot 4
8.	1 each 35-539 IOU	Lower Slot 3

All chassis are designed to accept 381 mm x 381 mm (15" x 15") printed circuit boards. Lower Slots 0, 1, and 2 are reserved for I/O. Either full or halfboard I/O may be plugged into these slots. One or two 178 mm (7") halfboards may be inserted into the 356 mm (14") chassis via the 16-398 Half Board Adaptor Kit (see Figure 16). The Half Board Adaptor Kit may hold two active 178 mm (7") boards or one active and one blank board, depending on requirements. A 254 mm (10") I/O Controller (provided it does not use Connector 1) may be inserted via the 02-234 I/O Adaptor Kit (see Figure 17). No wiring takes place between the boards and the adaptors. The adaptors are assigned such that the connectors on the boards plug directly into the chassis.

Figure 18 is a configuration of the Basic Processor chassis as viewed from the Display Panel side. It correlates applicable cables to the associated Processor connectors and Table 1 lists the function of each cable.

Figure 19 depicts the Basic Processor Chassis as viewed from the back plane. Shown here are the 35-578 Local Memory Bus (LMB) Terminator, the 35-596 Control Address (CA) Terminator, the 17-336 EDMA Cable Assembly, and the 35-569 Processor Terminator. Note that one end of the 17-336 Cable Assembly has a terminator card. This end of the cable must always be installed on upper Slot 1, Connector 1 side. The other end of 17-336 is shown connected to lower Slot 2, Connector 1 side but may also be connected to lower Slots 0 or 1.
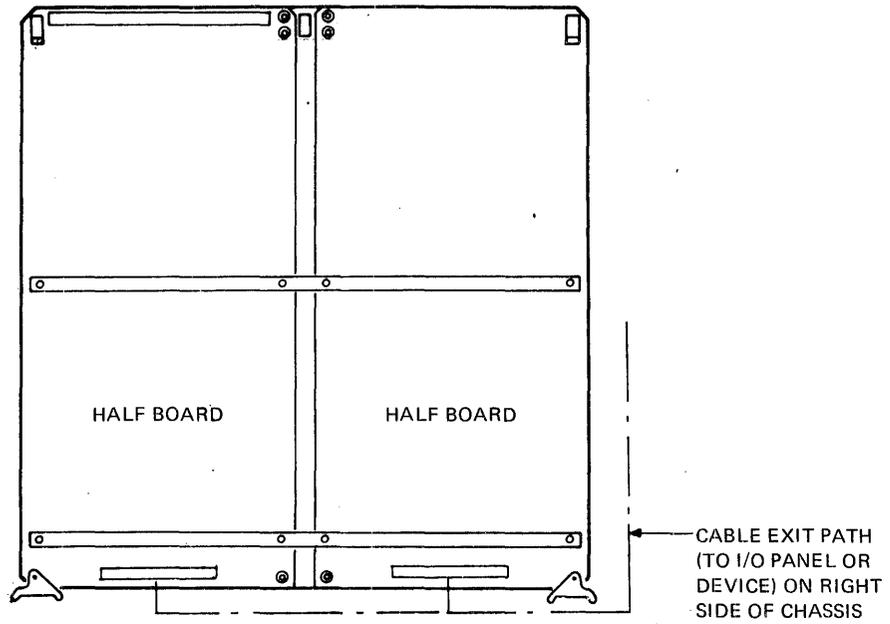
NOTE

35-398 half board can be located on either side.

Figure 16. 16-398 Half Board Adapter
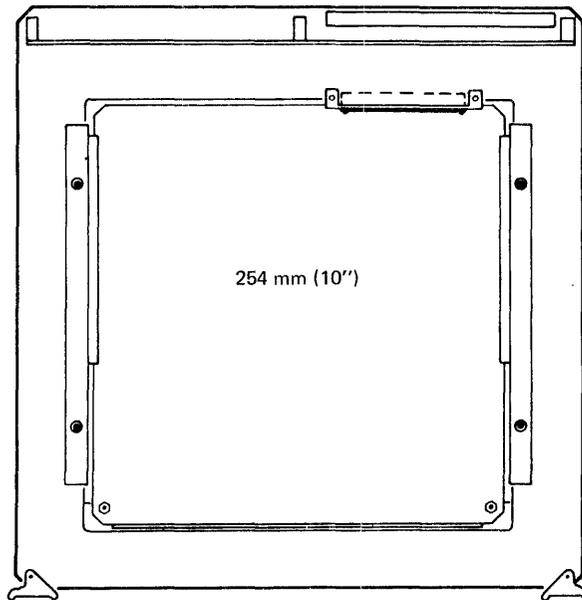
Figure 17. 02-234 I/O Adapter (Top View)

07	────────────	MEM
06	────────────	LMI
05	────────────	MEM
04	────────────	MEM
03	────────────	LMI
02	────────────	MEM
01	────────────	MBC
00	A ... B	CPA
07	NOTE ...	CPB
06	C ... D	CPC
05		UNUSED
04		ALU
03	E ... F	IOU
02		(I/O)
01		(I/O)
00		(I/O)
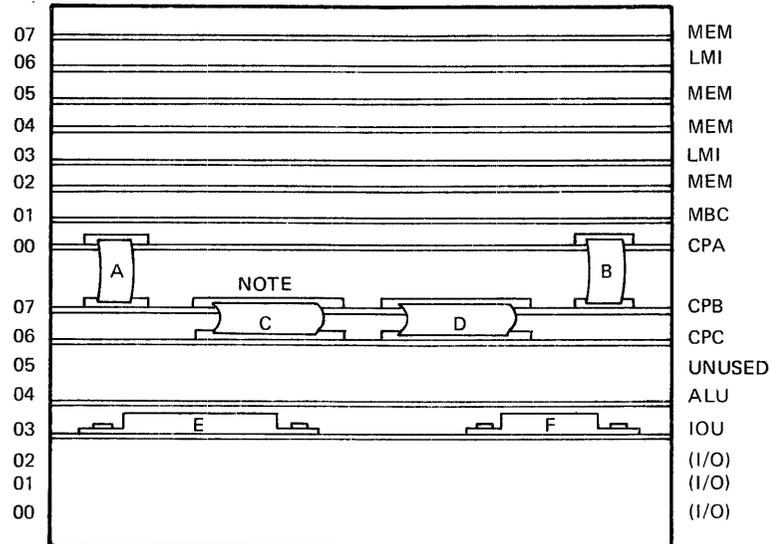
NOTE
Optional on Writable Control Storage (WCS)

Figure 18. Basic Processor; Front View

TABLE 1. PROCESSOR CABLES

LOC.	CONNECTOR #	CABLE	FUNCTION	TYPE
A	CPU5	17-361	USER SOURCE/DEST. REG. ADDR.	RIBBON
B	CPU2	17-361	B.S. REG. ADDR.: MC FIELD	RIBBON
C	CPU4	17-360	CONTROL STORE DATA	RIBBON
D	CPU3	17-360	CONTROL STORE ADDR.; A,B,S	RIBBON
E	IOU3	17-152 ASSY.	DISPLAY	BUNDLED WIRE
F	IOU2	17-180	TTY	BUNDLED WIRE

5.3   Processor Strap Options

Several Processor boards have strappable options which are described in the following paragraphs. Refer to Section 7 for information on memory system strap options.

5.3.1 35-536 CPA; Base Register Selection. The Base Register (BR) address is selected via three straps at IC location 05J on the CPA board. The following table indicates the possible starting locations and their respective strapping instructions. The standard address is X'300'.

STARTING LOCATION	05J11 TO	05J13 TO	05J15 TO
X'300'	05J06	05J03	05J01
X'500'	05J05	05J04	05J01
X'700'	05J06	05J04	05J01
X'900'	05J05	05J03	05J02

5.3.2 35-537 CPB; Privileged/Illegal Straps. Depending upon system options, one of three straps must be included to properly service the illegal instruction interrupt. The straps are located at IC location 03D and the following table indicates the proper strap for each option. The standard strap is 03D02 to 03D14.

OPTION	03D02 TO
BASIC 8/32	03D15
SGL. PREC. FLT. PT.	03D14
DBL. PREC. FLT. PT.	03D13

16

If the Writable Control Store (WCS) option is added, a different PRIV/ILLEG ROM must be used; however, the straps are the same.

Clock Switches. The Processor runs with two clock speeds and CPB is equipped with an octal switch at IC location 15E to accommodate marginal testing, nominal or normal mode, and extender board testing. Switch Positions 1 through 4 are for the faster Processor clock and Positions 5 through 8 for the slower clock. The following table indicates the use of each switch position. Boards should normally have Position 2 and Position 6 closed.

SWITCH POSITION	USE
1	MARGINS
2	NOMINAL
3	SLOW NOMINAL
4	EXTENDER BOARD
5	MARGINS
6	NOMINAL
7	EXTENDER BOARD
8	SLOW NOMINAL

5.3.3 35-538 ALU Clock. There are four wire wrap stakes located at the front of the ALU board which provide for three ALU clock speeds. The following diagram and table indicate the location of the stakes and the approximate clock rates for each tap respectively. The ALU should normally be strapped for nominal clocks (60 + 2 nanoseconds).

100 - 6	CLK		
101 - 6	MRG	MRG	56 nanoseconds
102 - 6	NOM	NOM	60 nanoseconds
103 - 6	NOMA	NOMA	62 nanoseconds
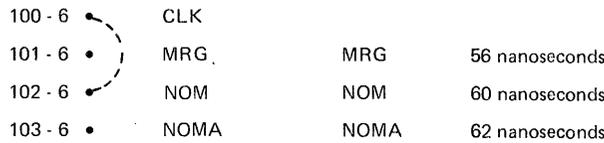
TTY Address. Normally strapped for X'02', the TTY address may be modified to X'82'. The following table correlates the strap position to the TTY address.

TTY ADDR	03J10 TO
X'02'	03J11
X'82'	03J09

6. DISPLAY PANEL INSTALLATION

The Model 8/32 Display Panel is electrically tied to the Processor via a connector and Faston lugs. The connector is installed on Connector 3 of the 35-539 IOU board and the terminal lugs mate into a terminal strip on the left side of the Processor chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. The Display Console is physically mounted to the brackets provided on the Processor chassis.

7. MEMORY INSTALLATION AND EXPANSION

7.1 First Memory Expansion (up to 512KB)/Cabling

Memory may be expanded beyond 128KB, in increments of 128KB, up to 512KB in one Expansion chassis. Each 128KB increment requires the addition of four 32-198 32KB memory modules. If expansion beyond 512KB is desired, a second Expansion chassis is required.

Refer to Figure 20. All memory modules up to a maximum of 512 KB are installed in the Expansion chassis above the Basic Processor chassis. The MBC is installed in upper Slot 1 of the Processor chassis and the two LMI modules are installed in upper Slots 3 and 6 of the Processor chassis. Upper Slots 2, 4, 5, and 7 remain blank. The first Memory Expansion chassis accommodates memory of 256KB, 384KB, and 512KB.

7.2 Second Memory Expansion

A second Memory Expansion chassis is required for memory size greater than 512KB. Up to 1MB of memory may be accommodated with two Expansion chassis.

Refer to Figure 14. All memory modules are installed in the two Memory Expansion chassis, one located above and one below the Basic Processor chassis. The MBC module is installed in upper Slot 1 of the Processor chassis and the two LMI modules are installed in upper Slots 3 and 6 of the Processor chassis. Upper Slots 2, 4, 5 and 7 remain blank.
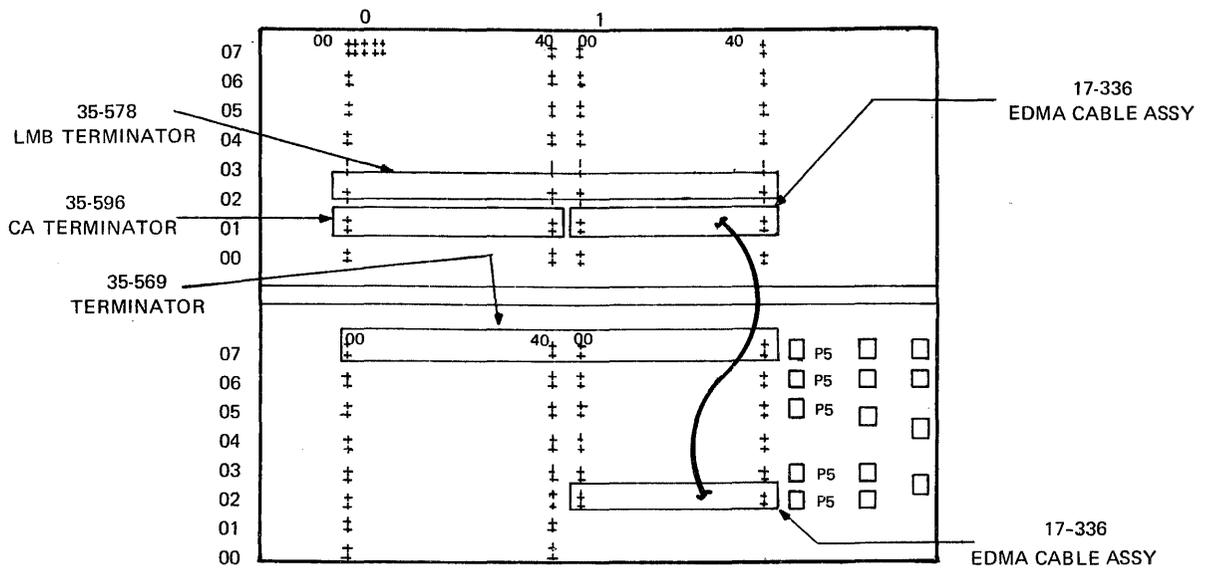
Figure 19. Basic Processor — Rear View

35-578 LMB TERMINATOR
35-596 CA TERMINATOR
35-569 TERMINATOR
17-336 EDMA CABLE ASSY
17-336 EDMA CABLE ASSY

	256KB	384KB	512KB

LMI
LMI
MBC
CPA
CPB
CPC
UNUSED
ALU
IOU
(I/O)
(I/O)
(I/O)
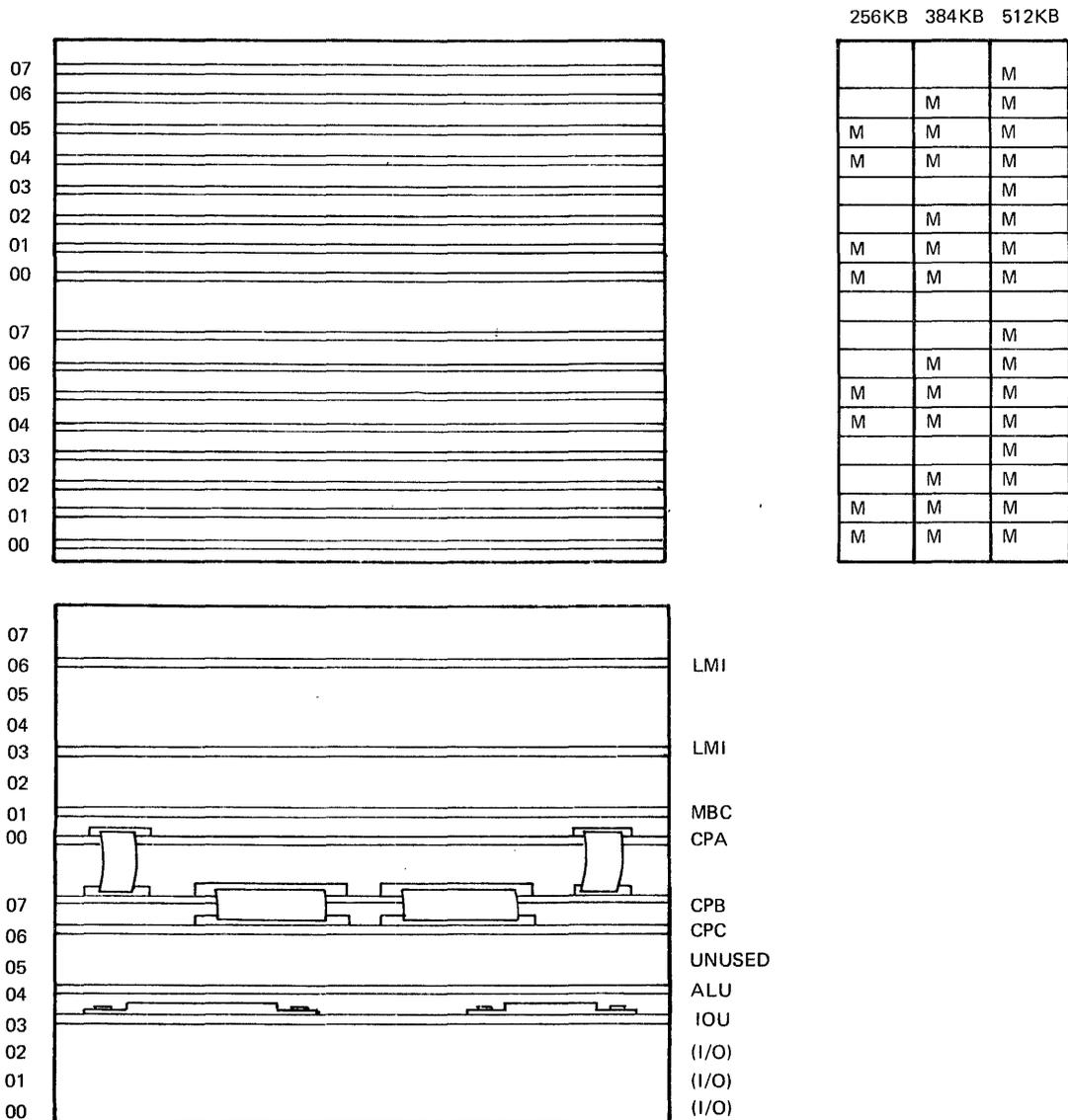
Figure 20. Front View of Processor Configuration with First Memory Expansion

Figure 21. Front View of Processor Configuration with First and Second Memory Expansion

1st MEMORY EXPANSION

Row	640KB	768KB	896KB	1024KB
07				M
06			M	
05		M	M	
04	M	M	M	
03	M	M	M	
02	M	M	M	
01	M	M	M	
00	M	M	M	
07				
06			M	
05		M	M	
04	M	M	M	
03	M	M	M	
02	M	M	M	
01	M	M	M	
00	M	M	M	M

8/32 BASIC

Row	Label
07	LMI
06	
05	
04	LMI
03	
02	MBC
01	CPA
00	CPB
07	CPC
06	UNUSED
05	ALU
04	IOU
03	(I/O)
02	(I/O)
01	(I/O)
00	

2nd MEMORY EXPANSION

Row	640KB	768KB	896KB	1024KB
06	M	M	M	M
05	M	M	M	
04	M	M	M	
03	M	M	M	
02	M	M	M	
01		M	M	
00			M	
07				
06	M	M	M	
05	M	M	M	
04	M	M	M	
03	M	M	M	
02	M	M	M	
01		M	M	
00			M	
				M

8. CONFIGURATION

8.1 Basic Chassis I/O

The Processor Multiplexor Bus is capable of driving 14 loads (not including the built-in Teletype and Display interfaces). The overall length of the bus is not to exceed the three copper slots available in the basic chassis, plus a 914 mm (36") cable, plus 16 copper slots, plus a 17-183 or a 17-224 or a 127 mm (15") cable.

Within the Basic 8/32 chassis three I/O slots are available (lower Slots 0, 1, and 2). These have been defined as follows:

> The Connector 1 side is reserved for private I/O only.
> The Connector 0 side may contain half-board I/O, ESELCH, or Mux Bus Buffer.

Up to two ESELCHs/MBFRs may be installed in these three slots. However, if an ESELCH is installed in Slot 2, the controller must be installed in Slot 1. If an ESELCH is installed in Slots 1 and/or 0, the controllers may be anywhere within reach of a 914 mm (36") cable.

Note that within the basic chassis, a fullboard I/O cannot run off of the Processor Mux Bus.

8.2 System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system Expansion chassis must be mounted below the basic Processor chassis, or in an adjacent rack.
2. All chassis must be contiguous.
3. All 356 mm (14") system Expansion chassis must be mounted above any 254 mm (10") Expansion chassis.
4. Multiboard peripheral device controllers (on 254 mm (10") circuit boards) can only be used in the 254 mm (10") system Expansion chassis.

8.3 Circuit Board Distribution

Model 8/32 Digital Systems may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system Expansion chassis.

1. The Extended Selector Channel can be placed in Slots 6, 4, 2, or 0 of the system Expansion chassis, or Slots 0, 1, or 2 of the Basic Processor chassis. Use only the 35-508M00R12 or the 35-508M01R00 ESELCH Card.

2. All slots on Connector 1 below the position where the ESELCH is inserted become ESELCH Bus slots. (This only applies within the back panel containing the ESELCH.) The ESELCH Bus extends down the right side connectors (rear view). Note that all device controllers on 254 mm (10") adapter boards connect the Multiplexor Bus from left side connectors (rear view). Therefore, these device controllers may be inserted in vacant ESELCH Bus slots, but are not on the ESELCH Bus. This also applies to all 178 mm (7") boards on adapters, installed on the left side.

3. The ESELCH Bus can be extended by cable to any even numbered slot in an I/O chassis. In this case, the I/O Multiplexor Bus must be cut between the even numbered slot and the slot above it.

4. All device addresses are hard-wired on the device controller cards, (device addresses may be changed at option) so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain" and convenience.

5. The 178 mm (7") system Expansion chassis, and the Basic Processor chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. For multi-board 254 mm (10") device controllers, the 254 mm (10") system Expansion chassis must be used.

6. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to 8.3 Interrupt Priority Back Panel Wiring to determine which physical location has what priority. When deciding which devices should have a higher or lower priority, devices that must be serviced in a specific amount of time or loss of data access occurs, should be given a higher priority than a device with a high interrupt rate but no data loss if not serviced.

8.4 Interrupt Priority Back Panel Wiring

The Acknowledge Control line from the Processor carries the interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with interrupt control circuits. Back plane wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK(TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has an interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back plane at that position.

On the IOU board location in the Processor chassis, the daisy-chain starts at one of 127-0, 128-0, 129-0 or 130-0 terminals (Slot 3) and normally goes to the Console TTY RACK0, Terminal 137-1 of the same slot. The TTY TACK0 (237-1) is wired to Pin 122-0 at Slot 2 and continued through the I/O slots as described previously.

Figure 22 shows the standard interrupt priority wiring to resolve conflicts in attention requests, queued on the same RACK0/TACK0 "daisy chain." The arrows indicate the direction of priority from the highest priority to the lowest. By changing the wires crossing from Side 0 to Side 1 of the Processor and/or Expansion panels, interrupt priorities may be rearranged. An example of this is shown in Figure 23, Modified Interrupt Priority. Slot 3 on Side 1 of the Processor panel has the highest priority. When Extended Selector Channels (ESELCHs) are installed, the standard interrupt priority must be modified. Refer to Figure 24 Interrupt Priority with ESELCH installed. The Multiplexor Bus may be restored to the remaining slots on Side 1 that are not used for the private ESELCH Bus. This may be accomplished by using the 17-183 cable. To prevent this, install the ESELCH as low as possible in the chassis.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

8.5 Terminators

35-433: I/O Bus Terminator. Install one on the transmit end of a 914 mm (36") cable and install one at the end of the Processor Mux Bus.
35-548: EDMA Bus Terminator, Connector 1. Install at the end of the EDMA Bus.
35-572: EDMA Bus Terminator, Connector 1. Install at the end of the EDMA Bus.

8.6 Multilevel External Interrupts

1. The 8/32 is capable of acknowledging four levels of external interrupts. Associated with each interrupt level is an Attention (ATN) line and a priority chain (RACK0/TACK0).

2. The four Attention lines (ATN000:030) located on CPB (lower Slot 7) are wired to the OR-tied Attention lines of the device controllers (or external Processor).

3. The four Acknowledge lines (ACK000:030) located on the IOU (lower Slot 3) are the source of the priority chain.

4. ATN/ACK levels must not be crossed. That is, ATN000 must be OR-tied to ATN line of those devices in the ACK000 priority chain. Similarly, ATN010 must be in the ACK010 priority chain, etc.

5. Standard 8/32 backplane wiring is as follows:

   — ATN000 on CPB is wired to ATN0 on IOU
   — ACK000 on IOU is wired to TTY RACK0 on IOU
   — TTY TACK0 on IOU is wired to RACK0 on Connector 0, I/O Slot 2

NOTE

ATN0 from I/O slots must be wired to one of ATN00:03 on CPB slot. (137-1, 138-1 or 237-1, 238-1).

For example: ATN01 must be used if ACK01 is used for driving RACK0/TACK0 "daisy chains".

4
3
2
1
0

7
6
5
4
3
2
1
0

PROCESSOR CHASSIS

IOU SLOT
(ACK00) 127
(ACK01) 128
(ACK02) 129
(ACK03) 130

122
222

(TTY) 137
(RACK0) 122
(TACK0) 222

237

IOU

122
222

134

7
6
5
4
3
2
1
0
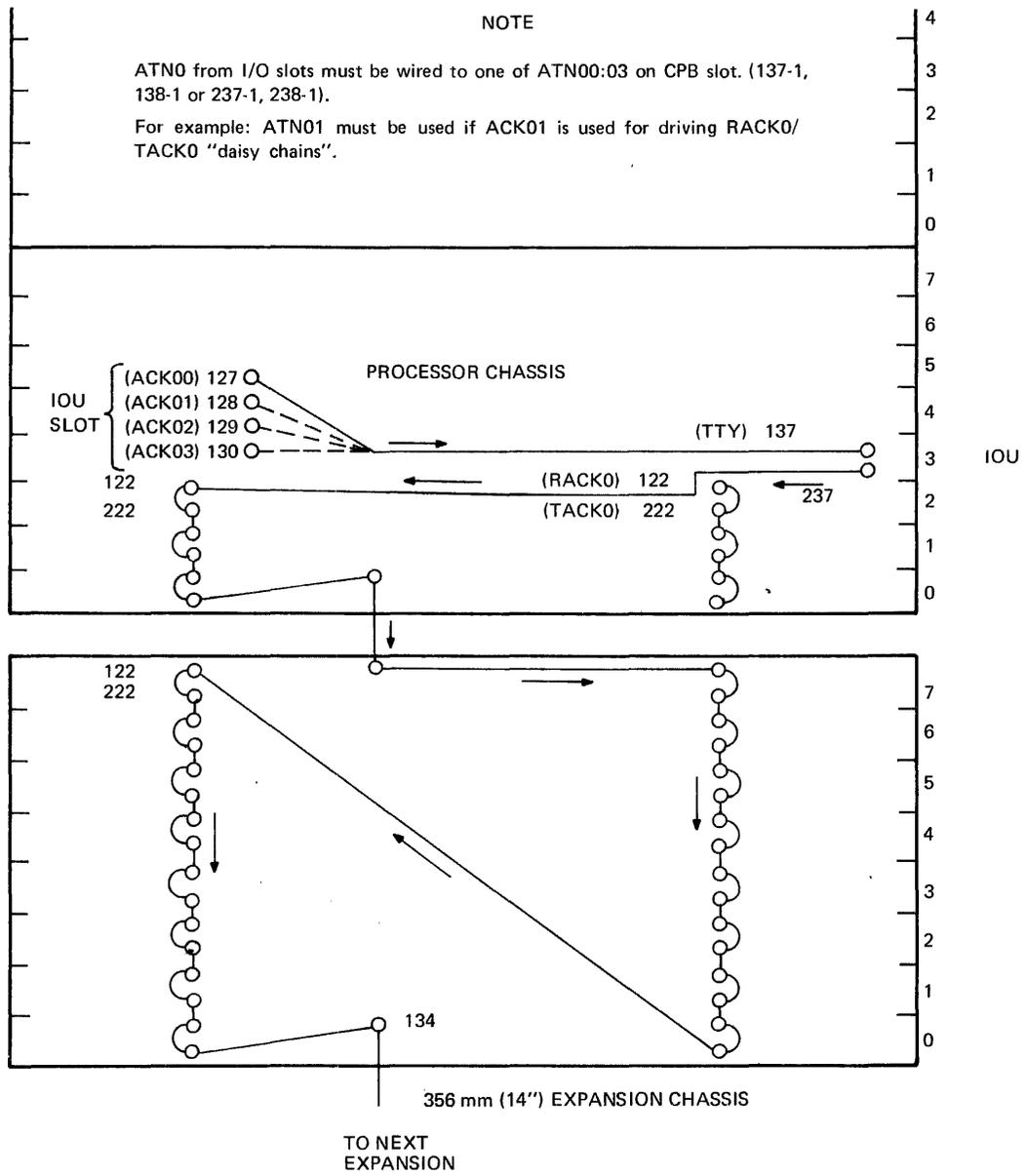
356 mm (14") EXPANSION CHASSIS

TO NEXT
EXPANSION

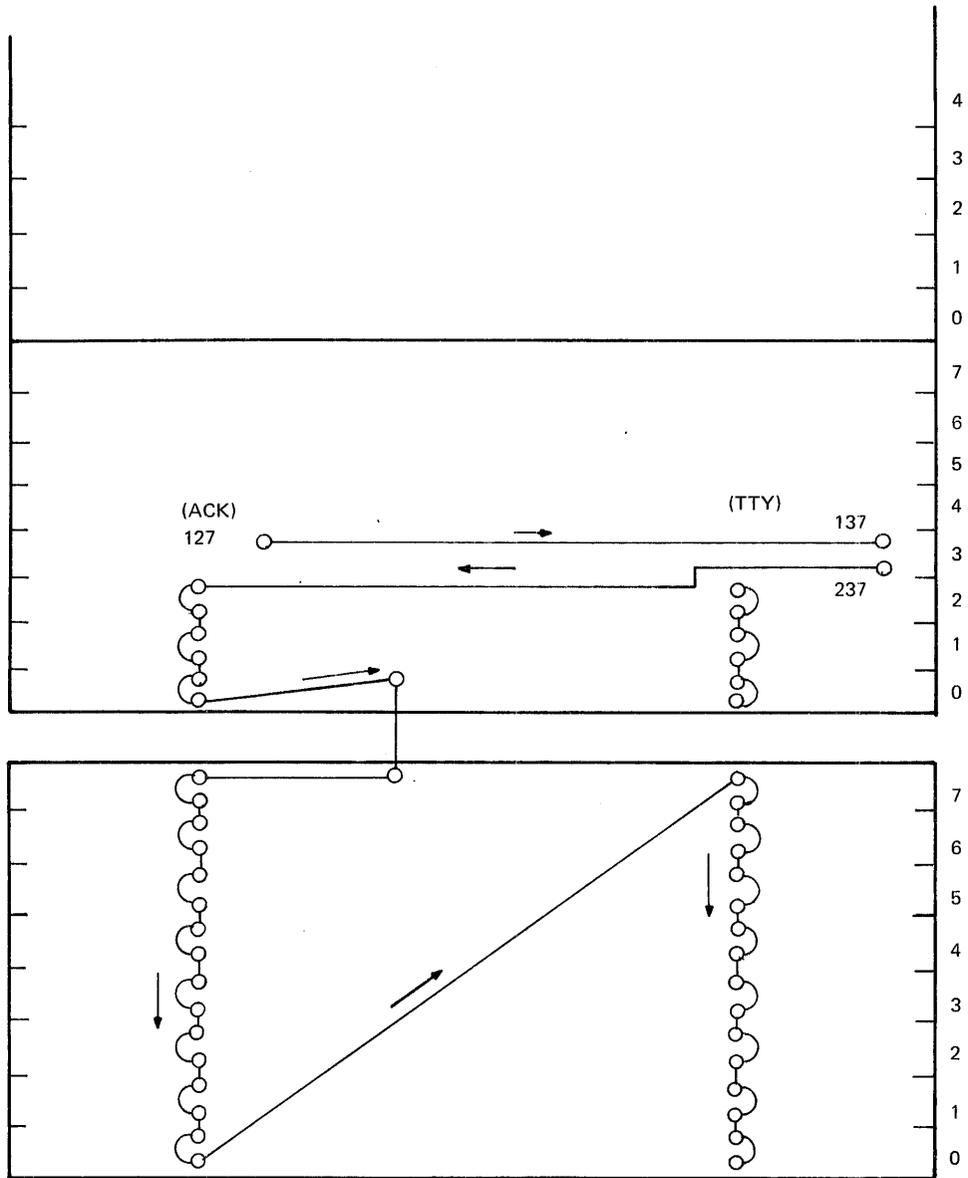**Figure 22. Standard Interrupt Priority**
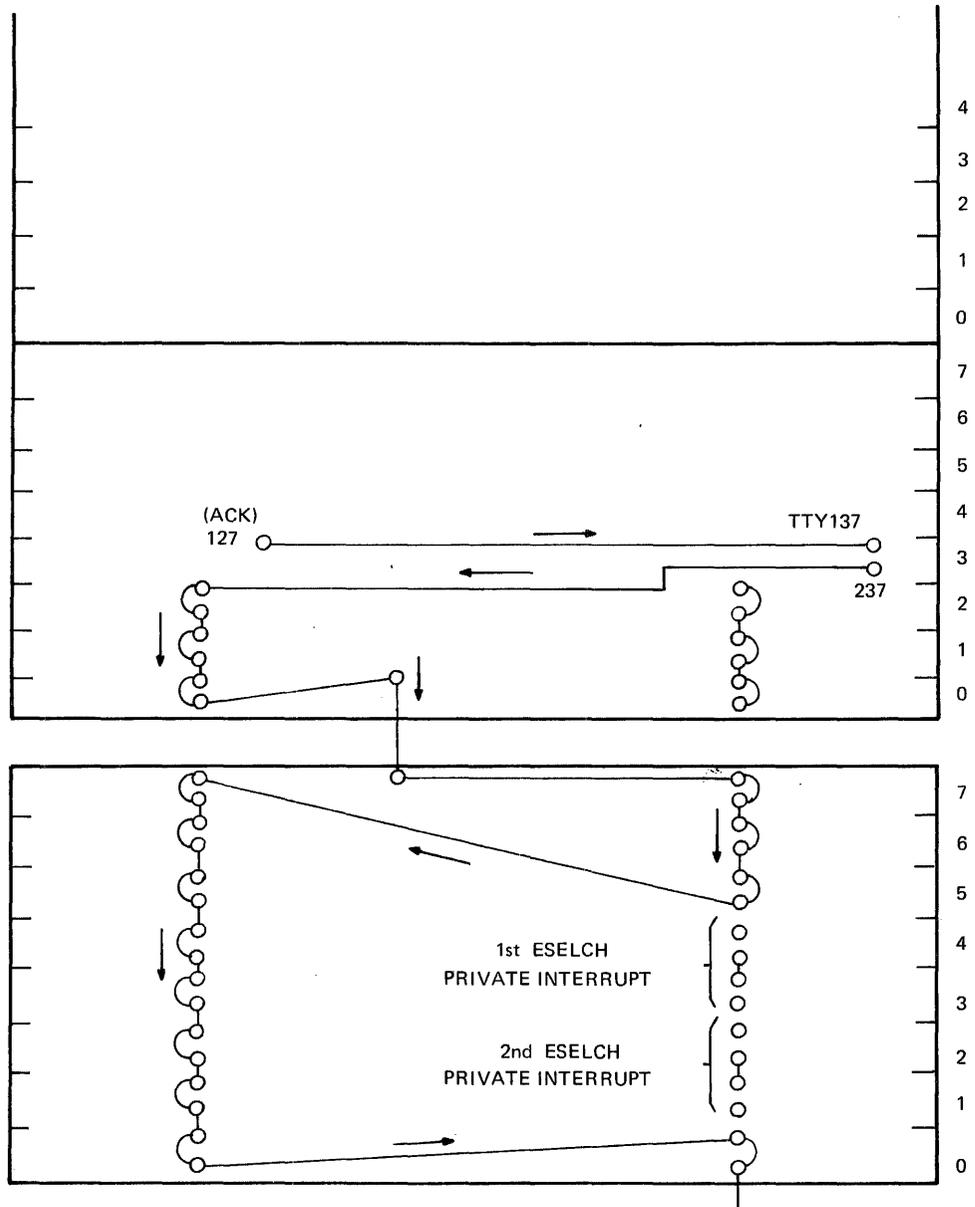
Figure 23. Modified Interrupt Priority

Figure 24. Interrupt Priority with ESELCH Installed

9. CABLES

9.1 Power Cable

The standard INTERDATA cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a three-wire, twist-lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel #2610) plug. A three-wire grounding, 30 Ampere, 125 VAC receptable (Hubbel #2611 or equivalent) is required to accept this plug.

9.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of the INTERDATA Expansion chassis discussed in Section 4. The choice of cables is dependent upon system configuration. The following cables are always used in pairs:

1. 17-193: I/O Expansion Cable, Connector 0.

   This cable is used to connect the "0" connector field between two adjacent 356 mm (14") chassis.

2. 17-194: I/O Expansion Cable

   This cable is used to connect the "1" connector I/O fields between two adjacent 356 mm (14") chassis.

3. 17-216: I/O Expansion Cable, 914 mm (36 ") long

   This is a 914 mm (36") long cable. It can be used to connect two 356 mm (14") chassis that are not adjacent.

4. 17-214: 356 mm (14") to 254 mm (10") Expansion Cable

   This cable is used to connect the "0" connector field of a 356 mm (14") chassis to a lower adjacent 254 mm (10") chassis. It provides an 8-bit I/O bus to the 10 inch card file.

5. 17-166: 356 mm (14") to 254 mm (10") I/O Expansion Cable 914 mm (36") long

   This cable is used to connect the "1" side of a 356 mm (14") expansion chassis to a 254 mm (10") expansion chassis. It provides an 8-bit I/O bus to a 254 mm (10") chassis. It must not be connected to the Basic Processor Multiplexor Bus. It may be driven either by an Extended Selector Channel or a bus buffer. It can be used on the older 254 mm (10") chassis.

6. 17-183: "0" to "1" Connector

   This cable can be used to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 356 mm (14") chassis.
   There is no RACK0/TACK0 wire in this cable.
   It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

7. 17-215: 254 mm (10") I/O Expansion Cable

   This cable is used to connect two adjacent 254 mm (10") chassis.

8. 17-326: EDMA/I/O Connector 0

9. 17-327: EDMA/I/O Connector 1

10. 17-328: EDMA only Connector 0, 914 mm (36")

11. 17-329: EDMA only Connector 1, 914 mm (36")

12. 17-336: EDMA Connector 1

13. 17-335: Memory Data/Memory Sense Cable

14. 17-334: Memory Address Expansion Cable

15. 17-359: EDMA/I/O Connector 1, 914 mm (36")

16. 17-360: Processor Connector 2/5

17. 17-361: Processor Connector 3/4

18. 17-374: I/O/EDMA, Connector 0, 914 mm (36")

9.3 Typical Configurations

Refer to Figure 25 for typical system configuration.

10. TESTING

10.1 Standard Test Software

The following software is supplied with the basic Processor to insure that the system is operational:

1. Processor Test Programs   06-154, 155, 178
2. Memory Test Program   06-156 (F01, F02, F03)
3. Floating Point Test   DR320005
4. TTY Test Program   06-004
5. MAC Test Program   06-160 (F01 and F02)

10.2 Additional Software

In addition to the test software mentioned above, appropriate test software is supplied with each peripheral.

NOTES

1. The Processor Mux Bus is contiguous and is terminated at each end on the Connector 0 side.
2. The Expansion chassis may be mounted within the 8/32 cabinet or in an adjacent cabinet.
3. The EDMA Bus is terminated at the end of the bus.
4. Provision has been made for the installation of a MBFR if future expansion is necessary.

0   1   2
1
0

8/32 BASIC
17- 336
7
6
5
4
3

UCLK   35-433   2
LSU   1   CONNECTOR 1 PRIVATE I/O NOT USED.
PTRP   0

17-374   17 - 329

ESELCH   7   REROUTE RACK0/TACK0 TO
40MB   6   CONNECTOR 0 SIDE
40MB   5 ◄— CUT MUX BUS
ESELCH   EXPANSION 1   4
MAG   3 ◄— CUT MUX BUS
ESELCH   2
         17-216   35- 548   1 ◄— CUT MUX BUS
(MBFR)   35-433   35- 572   0

ULI1   7
ULI2   6
ULI3   5
                 4
         EXPANSION 2   3
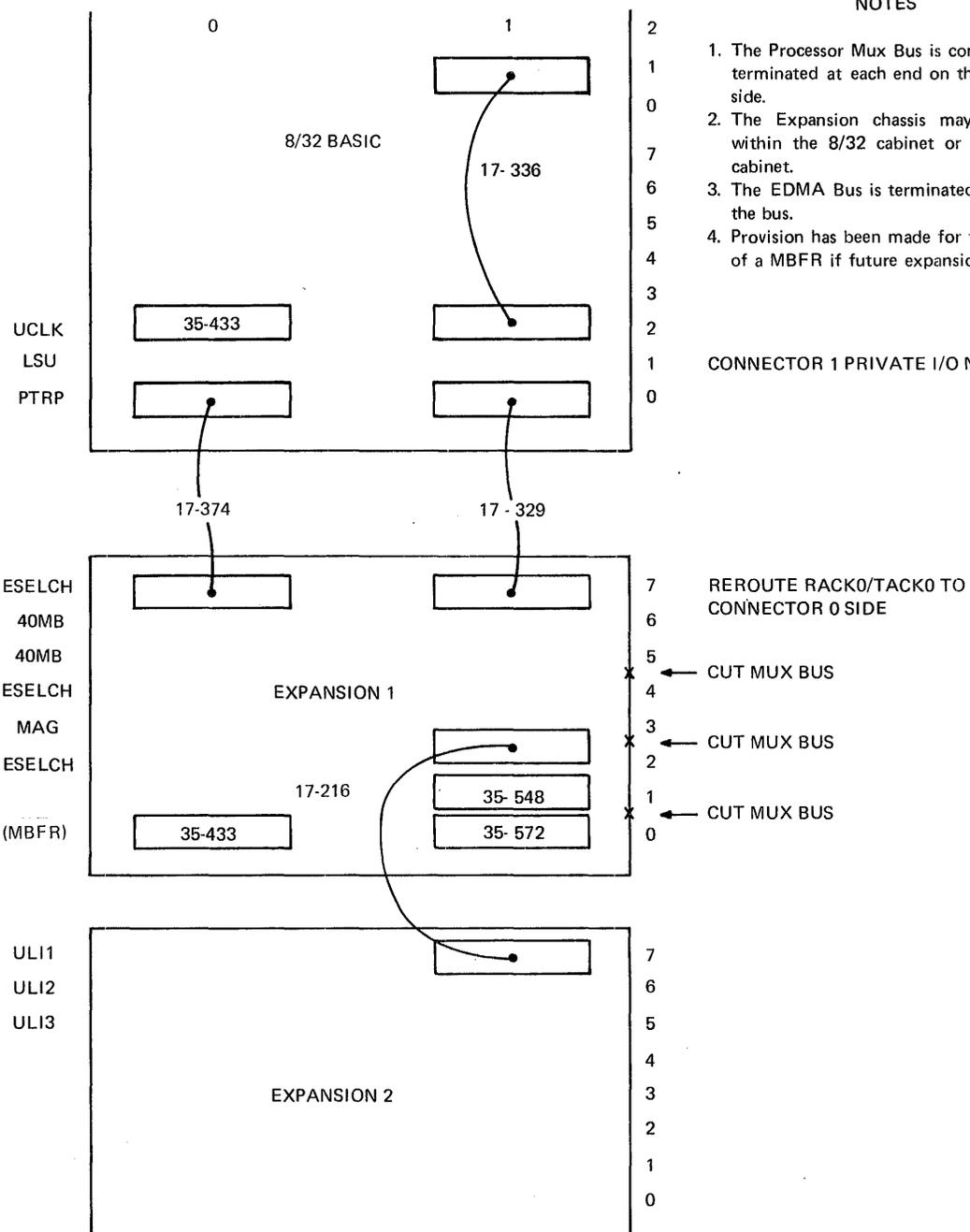   2
                 1
                 0

Figure 25. Typical System Configuration (Back Panel)