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32 KB CORE MEMORY INSTALLATION MANUAL

INTERDATA®
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32 KB CORE MEMORY INSTALLATION MANUAL

INTRODUCTION

This manual provides the information necessary to install a 32KB Core Memory Module into INTERDATA Models M70, M74, 7/16, 6/16, 7/32, and 8/32 Systems.

INTERDATA Part Numbers 02-409F01 and 02-409F02 designate the 32KB Memory Modules with a cycle time of 0.75 microsecond and 02-409F03 and 02-409F04 designate the 32-206 32KB Memory Modules with a cycle time of 1.0 microsecond.

INTERDATA Part Numbers 02-409F01 or 02-409F03 and 02-409F02 or 02-409F04 designate the 32-206 32KB Core Memory Modules with a parity bit and without a parity bit, respectively.

The 32KB Memory Module has a maximum access time of 275 nanoseconds. For additional functional and circuit details, refer to *32KB Core Memory Maintenance Manual,* Publication Number 29-493 or 29-513.

PHYSICAL CHARACTERISTICS

The Memory Module consists of one 15 inch mother-board which contains a plug in core stack of 16K x 17 bits (32K bytes with parity) or 16K x 16 bits (32K bytes without parity). This Module is pluggable into standard INTERDATA chassis with 0.75 inch center to center spacing.

Table 1 provides the power requirements of the 32KB Core Memory Module.

TABLE 1. POWER REQUIREMENTS

VOLTAGE			
MODE	NAME	NOMINAL VALUE (V)	MAX. CURRENT DRAIN (AMPS.)
OPERATING	P15 N15 P5	16.5 -16.5 5.0	2.4 @ 0°C 2.0 @ 0°C 4.0
STAND-BY (EACH MODULE)	P15 N15 P5	16.5 -16.5 5.0	0.020 0 3.0

UNPACKING

When the 32KB Core Memory Module is shipped with a system, it is installed at the factory and requires no special unpacking procedure.

If the Module is shipped separately, it should be unpacked with care and inspected for damage prior to installation.

CONFIGURATIONS

General

Power Supply Voltage Temperature Programming.

The 32-206, 32KB Core Memory Module can be mixed with the 32-198 (32KB M01), 35-491 (16KB), and 35-456 (8KB) Memory Modules.

In such configurations, the 32-206 Memory Module is installed in the slot containing terminals TEMP A and TEMP B.

If the 32-206 Module is mixed with a 32-200 (64 KB Core Memory Module) or is installed without any of the previously mentioned memory modules, the connections to TA and TB from the power supply, which normally lead to backplane Pins 128-1 (TEMP A) and 227-1 (TEMP B), are terminated across a fixed resistor value of 1K ohm, ±5%, ¼ Watt (21-001F09).

Address Coding and Parity

Each 32KB module is strapped for address coding and parity (PARO) indication. Detailed installation information is given as it applies to each particular system and module.

For parity (PAR0) option strapping refer to *32KB Core Memory Maintenance Manual,* Publication Number 29-493 or 29-513. In the 32-206F02 or 32-206F04 Module, the parity (PAR0) option is deactivated by connecting A97, Pin 09 (Tie Point "B") to ground (Tie Point "C").

In the 32-206F01 or 32-206F03 Module, the parity (PAR0) option is activated by connecting A97, Pin 09 Tie Point "B") to A97, Pin 10 (Tie Point "A"). PAR0 strapping is done on the component side of the printed circuit board.

Data Unavailable (DUA0) Signal.

The DATA UNAVAILABLE (DUA0) signal is activated (if required) by connecting A97, Pin 02 (Tie Point "F") to A97, Pin 01 (Tie Point "E").

All strap connections are made on the component side of the printed circuit board.

Model 70

The 32-206 Module can be installed in place of or with 16KB (Series 6) and 8KB (Series 5) Memory Modules in any Model 70 Processor or 50/55 Communications Processor that has the 35-387M02 Memory Control Board (R03 or higher revision) printed circuit board.

The 32-206 Module requires on board wiring for address codings. Address coding strapping is described in Tables 2 and 3.

The 32-206F03 or 32-206F04 Modules require on board strapping for a memory cycle time of 1.0 microsecond by removing the wire strap connection from Tie Point "S" to Tie Point "R" and connecting A91 Pin 01 (Tie Point "S") to A73 Pin 02 (Tie Point "T").

The first 32KB Module (Module 0) in the Model 70 Processor or 50/55 Communications Processor must be installed in the Processor Slot 3. The second 32KB Module (Module 1) can be installed in an adjacent slot for a total of 64K bytes.

TABLE 2. 32KB MEMORY ADDRESS CODE STRAPPING: MODULE 0
MODEL 70, MODEL 74, 7/16 BASIC, 7/16 HSALU, 6/16

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000		1	2	3	4
		108-0	208-0	106-0					
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2								●
	M2							●	
	N2			●					
	P2								
	L3								
	M3					●			
	N3					●			
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

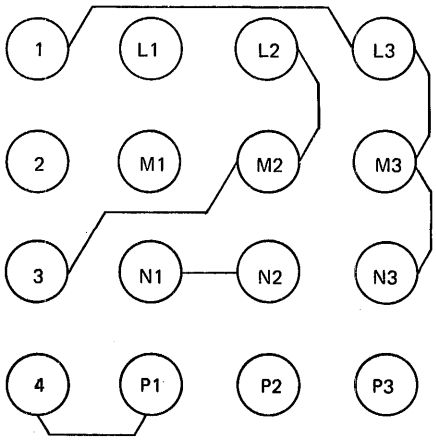
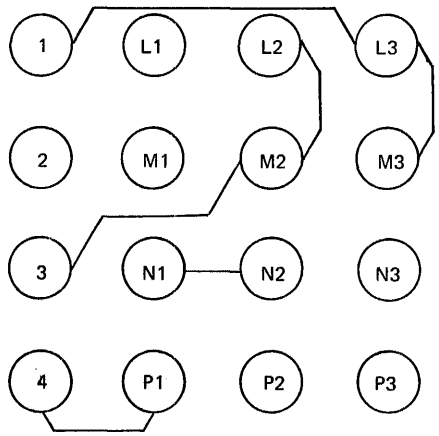


TABLE 3. 32KB MEMORY ADDRESS CODE STRAPPING: MODULE 1
MODEL 70, MODEL 74, 7/16 BASIC, 7/16 HSALU, 6/16

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000		1	2	3	4
		108-0	208-0	106-0					
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2								●
	M2							●	
	N2			●					
	P2								
	L3						●		
	M3					●			
	N3								●
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:



8KB (Series 5), 16KB (Series 6), and 32KB Combination Configurations

The 8KB (Series 5) and 16KB (Series 6) Memory Modules can be combined with a 32KB Memory Module to add 8KB and/or 16KB to a 32KB boundary. Slot 3 in the Processor chassis must be used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first memory module, unless the Processor chassis and Expansion chassis are powered by an INTERDATA 34-020 power supply. The 8KB (Series 5), 16KB (Series 6), and 32KB Memories are configured at the factory per user requirements. Refer to Table 4.

TABLE 4. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULE COMBINATION CONFIGURATIONS

MEMORY	MEMORY MODULE	SLOT (S)	CPU OR EXPANSION
32KB	1 32KB	3	CPU
40KB	1 32KB 1 SERIES 5	3 7	CPU EXPANSION
48KB	1 32KB 1 SERIES 6	3 2, 1, OR 0	CPU
	1 32KB 2 SERIES 5	3 7-6 OR 7-1	CPU EXPANSION
56KB	1 32KB 1 SERIES 6 1 SERIES 5	3 7 5 OR 2	CPU EXPANSION EXPANSION
	1 32KB 3 SERIES 5	3 7-6-5 OR 7-1-2	CPU EXPANSION
64KB	2 32KB	3-2,3-1,3-0	CPU
	1 32KB 2 SERIES 6	3 2-1, 1-0	CPU
	1 32KB 4 SERIES 5	3 7-6-5-4 OR 7-1-2-3	CPU EXPANSION
	1 32KB 1 SERIES 6 2 SERIES 5	3 7 4-5 OR 2-3	CPU EXPANSION EXPANSION

NOTES

1. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULES CONFIGURED AT THE FACTORY PER USER REQUIREMENT
2. SLOT 3 IN THE PROCESSOR (CPU) CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE
3. SLOT 7 IN THE EXPANSION CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE, UNLESS THE PROCESSOR (CPU) CHASSIS AND EXPANSION CHASSIS ARE POWERED BY A BULK POWER SUPPLY, INTERDATA PART NUMBER 34-020

If the 32KB Memory Module is the expansion to a system already configured, the 32KB Memory Module must be placed in Slot 3, the first 32KB of core address, 0000 - 7FFE, in the Model 70 Processor chassis.

Refer to Table 5 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries. For example, for 40KB of memory, one 32KB Memory Module must be installed in Slot 3 of the Processor chassis and one 8KB (Series 5) Memory Module must be installed in Slot 7 of the Expansion chasis.

TABLE 5. 8KB (SERIES 5) MEMORY ADDRESS BOUNDARIES

SLOT	MEMORY ADDRESS	MEMORY	
3	0000 - 1FFE	8KB	MODEL 70 CPU MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS
2	2000 - 3FFE	16KB	
1	4000 - 5FFE	24KB	
0	6000 - 7FFE	32KB	
7	8000 - 9FFE	40KB	UNIVERSAL EXPANSION CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS
6	A000 - BFFE	48KB	
5	C000 - DFFE	56KB	
4	E000 - FFFE	64KB	
3	E000 - FFFE	64KB	
2	C000 - DFFE	56KB	
1	A000 - BFFE	48KB	
0	8000 - 9FFE	40KB	

NOTES

1. IF THE 32KB MEMORY IS THE EXPANSION TO A SYSTEM ALREADY CONFIGURED, THE 32KB MEMORY MUST BE IN SLOT 3, THE FIRST 32KB OF CORE ADDRESS, 0000 - 7FFE, IN THE MODEL 70 PROCESSOR (CPU) CHASSIS

2. SLOT MEMORY ADDRESS BOUNDARY DESIGNATIONS PERTAIN TO 8KB (SERIES 5) MEMORY MODULE ONLY (TABLE 5)

3. REFER TO TABLE 5 FOR THE APPROPRIATE SLOT IN WHICH TO INSTALL 8KB (SERIES 5) MEMORY MODULES RELATIVE TO MEMORY ADDRESS BOUNDARIES. FOR EXAMPLE; FOR 40KB OF MEMORY, ONE 32KB MUST BE INSTALLED IN SLOT 3 OF THE PROCESSOR (CPU) CHASSIS AND ONE 8KB (SERIES 5) MUST BE INSTALLED IN SLOT 7 OF THE EXPANSION CHASSIS

Model 74

32KB (32-206) Memory Module Configuration

The 32KB (32-206) Memory Module requires on-board wiring for address coding as described in Tables 2 and 3.

The 32-206F03 or 32-206F04 Modules require on board strapping for a memory cycle time of 1.0 microsecond by removing the wire strap connection from Tie Point "S" to Tie Point "R" and connecting A91 Pin 01 (Tie Point "S") to A73 Pin 02 (Tie Point "T").

The first 32KB Memory Module (Module 0) in the Model 74 must be installed in the Processor Slot 5. Refer to Table 6 for 32KB configuration. The second 32KB Memory Module (Module 1) may be installed in an adjacent slot for a total of 64K bytes.

The 32KB Memory Modules must only be installed in Model 74 Processors that have a 35-446R02 (CPU-HI) or higher revision printed circuit board. The 32KB Memory Module can be installed in place of, or with, 16KB (Series 6) and 8KB (Series 5) Memory Modules.

8KB (Series 5), 16KB (Series 6), and 32KB Combination Configurations

The 8KB (Series 5) and 16KB (Series 6) Memory Modules can be combined with a 32KB Memory Module to add 8KB and/or 16KB to a 32KB boundary. Slot 5 in the Processor chassis must be used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first memory module, unless the Processor chassis and Expansion chassis are powered by an INTERDATA 34-020 power supply.

The 8KB (Series 5), 16KB (Series 6), and 32KB Memories are configured at the factory per user requirements. Refer to Table 7.

TABLE 6. 32KB MEMORY MODULE CONFIGURATIONS

MEMORY	MEMORY MODULE	CPU SLOT (S)
32KB	0	5
64KB	1	4 SLOT 5 AND ANY REMAINING SLOT 4:0
—	—	3
—	—	2
—	—	1
—	—	0

NOTES

1. THE 32KB MEMORY MODULE CAN BE INSTALLED IN ANY MODEL 74 WITH 35-446R02 (CPU-HI) OR HIGHER PRINTED CIRCUIT BOARDS
2. THE FIRST 32KB MEMORY MODULE MUST BE INSTALLED IN SLOT 5
3. THE MODEL 74 CPU CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS ARE SHOWN IN TABLE 8

TABLE 7. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULE COMBINATIONS CONFIGURATIONS

MEMORY	MEMORY MODULE	SLOTS	CPU OR EXPANSION
32KB	1 32KB	5	CPU
40KB	1 32KB 1 SERIES 5	5 1	CPU
48KB	1 32KB 1 SERIES 6	5 4,3,2,1 OR 0	CPU
	1 32KB 2 SERIES 5	5 0-1	CPU
56KB	1 32KB 1 SERIES 6 1 SERIES 5	5 7 5 OR 2	CPU EXPANSION EXPANSION
	1 32KB 3 SERIES 5	5 7-6-5 OR 7-1-2	CPU EXPANSION
64KB	2 32KB	5-4,5-3,5-2,5-1, 5-0	CPU
	1 32KB 2 SERIES 6	5 4-3,3-2,2-1,1-0	CPU
	1 32KB 1 SERIES 6 2 SERIES 5	5 7 5-4 OR 2-3	CPU EXPANSION EXPANSION
	1 32KB 4 SERIES 5	5 7,6,5,4 OR 7,1,2,3	CPU EXPANSION

NOTES

1. 8KB (SERIES 5), 16KB, (SERIES 6), AND 32KB MEMORY MODULES CONFIGURED AT THE FACTORY PER USER REQUIREMENT
2. SLOT 5 IN THE CPU CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE
3. SLOT 7 IN THE EXPANSION CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE, UNLESS THE CPU CHASSIS AND EXPANSION CHASSIS ARE POWERED BY A BULK POWER SUPPLY, INTERDATA PART NUMBER 34-020

If the 32KB Memory Module is the expansion to a system already configured, the 32KB Memory Module must be placed in Slot 5, the first 32KB of core address, 0000 = 7FFE, in the Model 74 Processor chassis.

Refer to Table 8 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries. For example, for 40KB of memory, one 32KB Memory Module must be installed in Slot 5 and one 8KB (Series 5) Memory Module must be installed in Slot 1 of the Processor chassis.

TABLE 8. 8KB (SERIES 5) MEMORY MODULE BOUNDARIES

SLOT	MEMORY ADDRESS	MEMORY
5	0000 - 1FFE	8KB
4	2000 - 3FFE	16KB
3	4000 - 5FFE	24KB
2	6000 - 7FFE	32KB
1	8000 - 9FFE	40KB
0	A000 - BFFE	48KB

MODEL 74 MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

7	8000 - 9FFE	40KB
6	A000 - BFFE	48KB
5	C000 - DFFE	56KB
4	E000 - FFFE	64KB
3	E000 - FFFE	64KB
2	C000 - DFFE	56KB
1	A000 - BFFE	48KB
0	8000 - 9FFE	40KB

UNIVERSAL EXPANSION CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

NOTES

1. IF THE 32KB MEMORY IS THE EXPANSION TO A SYSTEM ALREADY CONFIGURED, THE 32KB MEMORY MUST BE IN SLOT 5, THE FIRST 32KB OF CORE ADDRESS, 0000 - 7FFE, IN THE MODEL 74 CPU CHASSIS
2. SLOT MEMORY ADDRESS BOUNDARY DESIGNATIONS PERTAIN TO 8KB (SERIES 5) MEMORY MODULES ONLY (TABLE 8)
3. REFER TO TABLE 6 FOR THE APPROPRIATE SLOT IN WHICH TO INSTALL 8KB (SERIES 5) MEMORY MODULES RELATIVE TO MEMORY ADDRESS BOUNDARIES. FOR EXAMPLE; FOR 40KB OF MEMORY, ONE 32KB MUST BE INSTALLED IN SLOT 5 AND ONE 8KB (SERIES 5) MUST BE INSTALLED IN SLOT 1 OF THE CPU CHASSIS

Model 7/16 Basic, 7/16 HSALU, 6/16

32 KB Memory Configurations

The 32-206 32KB Memory Module requires on-board wiring for address coding. For strapping information refer to Tables 2 and 3.

The 32-206F03 or 32-206F04 Modules require on board strapping for a memory cycle time of 1.0 microsecond by removing the wire strap connection from Tie Point "S" to Tie Point "R" and connecting A91 Pin 01 (Tie Point "S") to A73 Pin 02 (Tie Point "T").

The first 32KB Memory Module (Module 0) in the 7/16 Basic Processor must be installed in Slot 5 of the Processor chassis (refer to Table 9). The first 32KB Memory Module (Module 0) in the 7/16 HSALU must be installed in Slot 3 of the Processor chassis, (refer to Table 10).

TABLE 9. 32KB MEMORY MODULE CONFIGURATIONS (7/16 BASIC)

MEMORY	MEMORY MODULE	CPU SLOT (S)
32KB	0	5
64KB	1	SLOT 5 AND ANY 4 REMAINING SLOT 4:0
–	–	3
–	–	2
–	–	1
–	–	0

NOTES

1. THE 32KB MEMORY MODULE CAN BE INSTALLED IN ANY MODEL 7/16 BASIC 35-520R02 (CPU-HI) OR HIGHER PRINTED CIRCUIT BOARDS
2. THE FIRST 32KB MEMORY MODULE SHALL BE INSTALLED IN SLOT 5
3. THE MODEL 7/16 BASIC CPU CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS ARE SHOWN IN TABLE 13

TABLE 10. 32KB MEMORY MODULE CONFIGURATIONS (7/16 HSALU)

MEMORY	MEMORY MODULE	CPU SLOT (S)
32KB	0	3
64KB	1	SLOT 3 AND ANY ONE 2 REMAINING SLOT 2:0
		1
		0

NOTES

1. THE 32KB MEMORY MODULE CAN BE INSTALLED IN ANY MODEL 7/16 HSALU
2. THE FIRST 32KB MEMORY MODULE SHALL BE INSTALLED IN SLOT 3
3. THE MODEL 7/16 HSALU CPU CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS ARE SHOWN IN TABLE 14

The 32KB Memory Module must only be installed in 7/16 Basic Processors that have a 35-446R02 (CPU-HI) or higher revision level.

The 32KB Memory Modules can be installed in place of, or with, 8KB (Series 5) Memory Modules and 16KB (Series 6) Memory Modules in the 7/16 Basic and the 7/16 HSALU Processor Systems.

8KB (Series 5), 16KB (Series 6), and 32KB Combination Configurations

The 8KB (Series 5) and 16KB (Series 6) can be combined with a 32KB Memory Module to add 8KB and/or 16KB to a 32KB boundary. If the total memory configuration exceeds 64KB (two 32KB Memory Modules), 8KB (Series 5) Memory Modules may not be used in that configuration.

On the 7/16 Basic Processor, Slot 5 in the Processor chassis must be used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first memory module.

On the 7/16 HSALU, Slot 3 in the Processor chassis must be used for the first 32KB Memory Module. Slot 7 in the Expansion chassis, if required, must be used for the first Memory Module.

The 8KB (Series 5), 16KB (Series 6), and 32KB Memory Modules are configured at the factory per user requirements. Refer to Table 11 for the 7/16 Basic Processor system, and Table 12 for the 7/16 HSALU Processor system.

TABLE 11. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULE COMBINATIONS CONFIGURATIONS (7/16 BASIC)

MEMORY	MEMORY MODULE	SLOTS	CPU OR EXPANSION
32KB	1 32KB	5	CPU
40KB	1 32KB 1 SERIES 5	5 1	CPU
48KB	1 32KB 1 SERIES 6	5 4,3,2,1 OR 0	CPU
	1 32KB 2 SERIES 5	5 0-1	CPU
56KB	1 32KB 1 SERIES 6 1 SERIES 5	5 7 5 OR 2	CPU EXPANSION EXPANSION
	1 32KB 3 SERIES 5	5 7-6-5 OR 7-1-2	CPU EXPANSION
64KB	2 32KB	5-4,5-3,5-2,5-1, 5-0	CPU
	1 32KB 2 SERIES 6	5 4-3,3-2,2-1,1-0	CPU
	1 32KB 1 SERIES 6 2 SERIES 5	5 7 5-4 OR 2-3	CPU EXPANSION EXPANSION
	1 32KB 4 SERIES 5	5 7,6,5,4 OR 7,1,2,3	CPU EXPANSION

NOTES

1. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULES ARE CONFIGURED AT THE FACTORY PER USER REQUIREMENT
2. SLOT 5 IN THE 7/16 BASIC CPU CHASSIS SHALL BE USED FOR THE FIRST MEMORY MODULE
3. SLOT 7 IN THE EXPANSION CHASSIS SHALL BE USED FOR THE FIRST MEMORY MODULE WHENEVER MEMORY IS CONFIGURED INTO THE EXPANSION CHASSIS

TABLE 12. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULE COMBINATION CONFIGURATIONS (7/16 HSALU)

MEMORY	MEMORY MODULE	SLOT (S)	CPU OR EXPANSION
32KB	1 32KB	3	CPU
40KB	1 32KB 1 SERIES 5	3 7	CPU EXPANSION
48KB	1 32KB 1 SERIES 6	3 2, 1, OR 0	CPU
	1 32KB 2 SERIES 5	3 7-6 OR 7-1	CPU EXPANSION
56KB	1 32KB 1 SERIES 6 1 SERIES 5	3 7 5 OR 2	CPU EXPANSION EXPANSION
	1 32KB 3 SERIES 5	3 7-6-5 OR 7-1-2	CPU EXPANSION
64KB	2 32KB	3-2,3-1,3-0	CPU
	1 32KB 2 SERIES 6	3 2-1, 1-0	CPU
	1 32KB 4 SERIES 5	3 7-6-5-4 OR 7-1-2-3	CPU EXPANSION
	1 32KB 1 SERIES 6 2 SERIES 5	3 7 4-5 OR 2-3	CPU EXPANSION EXPANSION

NOTES

1. 8KB (SERIES 5), 16KB (SERIES 6), AND 32KB MEMORY MODULES ARE CONFIGURED AT THE FACTORY PER USER REQUIREMENT
2. SLOT 3 IN THE 7/16 HSALU CPU CHASSIS SHALL BE USED FOR THE FIRST MEMORY MODULE
3. SLOT 7 IN THE EXPANSION CHASSIS MUST BE USED FOR THE FIRST MEMORY MODULE, WHENEVER MEMORY IS CONFIGURED INTO THE EXPANSION CHASSIS

If the 32KB Memory Module is the expansion to a system already configured, all memory modules that are not 32KB Memory Modules must be reconfigured such that they become the top of available memory. Note that if the final memory configuration exceeds 64KB, 8KB (Series 5) Memory Modules may not be used.

Refer to Table 13 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries for the 7/16 Basic Processor system.

TABLE 13. 8KB (SERIES 5) MEMORY MODULE BOUNDARIES (7/16 BASIC)

SLOT	MEMORY ADDRESS	MEMORY
5	0000 - 1FFE	8KB
4	2000 - 3FFE	16KB
3	4000 - 5FFE	24KB
2	6000 - 7FFE	32KB
1	8000 - 9FFE	40KB
0	A000 - BFFE	48KB

MODEL 7/16 BASIC MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

7	8000 - 9FFE	40KB
6	A000 - BFFE	48KB
5	C000 - DFFE	56KB
4	E000 - FFFE	64KB
3	E000 - FFFE	64KB
2	C000 - DFFE	56KB
1	A000 - BFFE	48KB
0	8000 - 9FFE	40KB

UNIVERSAL EXPANSION CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

NOTES

1. IF THE 32KB MEMORY IS THE EXPANSION TO A SYSTEM ALREADY CONFIGURED, THE 32KB MEMORY SHALL BE IN SLOT 5, THE FIRST 32KB OF CORE ADDRESS, 0000 - 7FFE, IN THE MODEL 7/16 BASIC CPU CHASSIS
2. SLOT MEMORY ADDRESS BOUNDARY DESIGNATIONS PERTAIN TO 8KB (SERIES 5) MEMORY MODULES ONLY (TABLE 13)
3. REFER TO TABLE 13 FOR THE APPROPRIATE SLOT IN WHICH TO INSTALL 8KB (SERIES 5) MEMORY MODULES RELATIVE TO MEMORY ADDRESS BOUNDARIES. FOR EXAMPLE: FOR 40KB OF MEMORY, ONE 32KB SHALL BE INSTALLED IN SLOT 5 OF THE 7/16 BASIC CPU CHASSIS AND ONE 8KB (SERIES 5) SHALL BE INSTALLED IN SLOT 1 OF THE CPU CHASSIS

Refer to Table 14 for the appropriate slot in which to install 8KB (Series 5) Memory Modules relative to memory address boundaries for the 7/16 HSALU Processor system.

The 32KB Module in the 6/16 Processor may be installed in Slot 6 only.

The 32KB Module address strapping per installation in 6/16 is equivalent to Module 0 in Table 2.

The 6/16 Processor requires the DATA UNAVAILABLE (DUA0) signal to be active during each memory cycle. The 32-206 must be strapped to activate this signal, by connecting A97, Pin 01 (Tie Point "F") to A97, Pin 02 (Tie Point "E").

This connection is made on the component side of the printed circuit board.

TABLE 14. 8KB (SERIES 5) MEMORY ADDRESS BOUNDARIES (7/16 HSALU)

SLOT	MEMORY ADDRESS	MEMORY
3	0000 -1FFE	8KB
2	2000 - 3FFE	16KB
1	4000 - 5FFE	24KB
0	6000 - 7FFE	32KB

MODEL 7/16 HSALU MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

7	8000 - 9FFE	40KB
6	A000 - BFFE	48KB
5	C000 - DFFE	56KB
4	E000 - FFFE	64KB
3	E000 - FFFE	64KB
2	C000 - DFFE	56KB
1	A000 - BFFE	48KB
0	8000 - 9FFE	40KB

UNIVERSAL EXPANSION CHASSIS MEMORY ADDRESS BOUNDARY SLOT DESIGNATIONS

NOTES

1. IF THE 32KB MEMORY IS THE EXPANSION TO A SYSTEM ALREADY CONFIGURED, THE 32KB MEMORY SHALL BE IN SLOT 3, THE FIRST 32KB OF CORE ADDRESS, 0000 - 7FFE, IN THE MODEL 7/16 HSALU CPU CHASSIS
2. SLOT MEMORY ADDRESS BOUNDARY DESIGNATIONS PERTAIN TO 8KB (SERIES 5) MEMORY MODULE ONLY (TABLE 14)
3. REFER TO TABLE 14 FOR THE APPROPRIATE SLOT IN WHICH TO INSTALL 8KB (SERIES 5) MEMORY MODULES RELATIVE TO MEMORY ADDRESS BOUNDARIES. FOR EXAMPLE: FOR 40KB OF MEMORY, ONE 32KB SHALL BE INSTALLED IN SLOT 3 OF THE 7/16 HSALU CPU CHASSIS AND ONE 8KB (SERIES 5) SHALL BE INSTALLED IN SLOT 7 OF THE EXPANSION CHASSIS

Model 7/32

32KB Memory Configurations

The 32KB Memory Module requires on-board address code strapping. Address code strapping information is shown on Tables 15 through 22.

The 32-206F03 or 32-206F04 Modules require on board strapping for a memory cycle time of 1.0 microsecond by removing the wire strap connection from Tie Point "S" to Tie Point "R" and connecting A91 Pin 01 (Tie Point "S") to A73 Pin 02 (Tie Point "T").

The first 32KB Memory Module in the 7/32 Processor must be installed in Slot 3 of the Processor chassis, refer to Table 10.

Memory blocks must be configured in adjacent descending slots.

Slot 7 in the Expansion chassis, if required, must be used for the first memory module.

If the 32KB Memory Module is the Expansion to a system already configured, all memory modules that are not 32KB memory modules must be reconfigured such that they become the top of available memory. Note that if the final memory configuration exceeds 64KB, 8KB (Series 5) memory modules may not be used.

For 7/32 Processor system 8KB (Series 5) memory module variations, refer to the 01-087A20 Installation Specification provided in the *Model 7/32 Maintenance Manual,* Publication Number 29-403 for details.

TABLE 15. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (1ST MEMORY) MODEL 8/32 (EIGHTH 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000		1	2	3	4
		108-0	208-0	106-0					
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3					●			
	M3					●			
	N3						●		
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

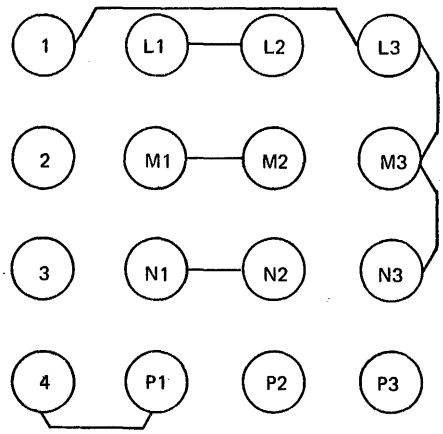


TABLE 16. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (2ND MEMORY) MODEL 8/32 (SEVENTH 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000		1	2	3	4
		108-0	208-0	106-0					
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3					●			
	M3					●			
	N3							●	
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

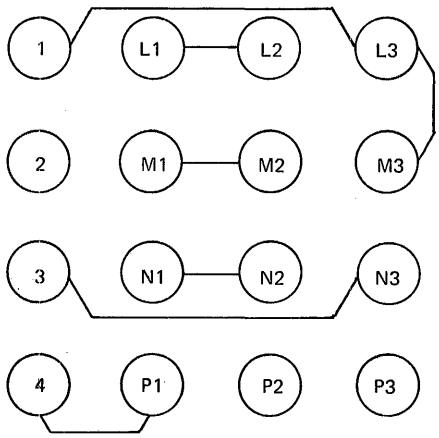


TABLE 17. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (3RD MEMORY) MODEL 8/32 (SIXTH 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000					
		108-0	208-0	106-0		1	2	3	4
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3							●	
	M3					●			
	N3					●			
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

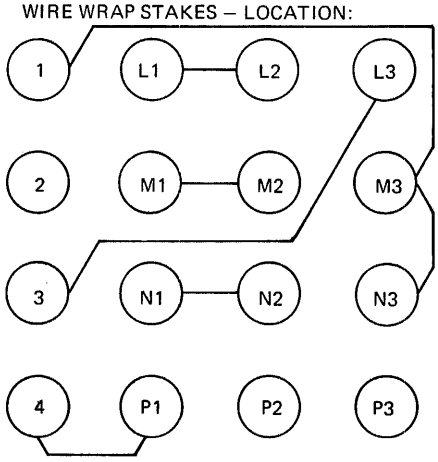


TABLE 18. 32KB MEMORY ADDRESS CODE STRAPPING:
MODEL 7/32 (4TH MEMORY)
MODEL 8/32 (FIFTH 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000					
		108-0	208-0	106-0		1	2	3	4
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3							●	
	M3					●			
	N3							●	
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

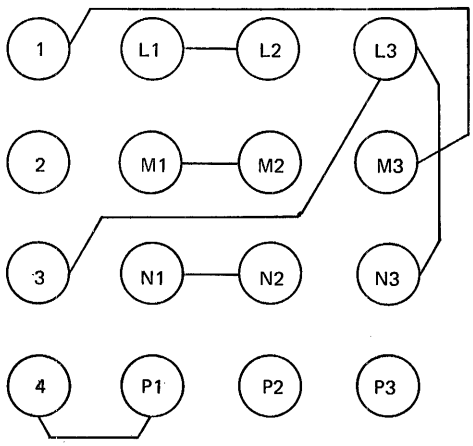


TABLE 19. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (5TH MEMORY) MODEL 8/32 (FOURTH 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000		1	2	3	4
		108-0	208-0	106-0					
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3					●			
	M3							●	
	N3					●			
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

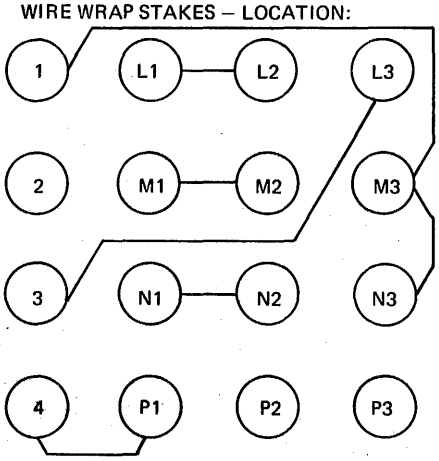


TABLE 20. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (6TH MEMORY) MODEL 8/32 (THIRD 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000					
		108-0	208-0	106-0		1	2	3	4
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3					●			
	M3							●	
	N3							●	
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

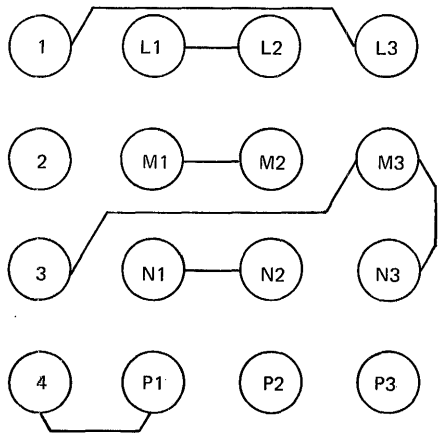


TABLE 21. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (7TH MEMORY) MODEL 8/32 (SECOND 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000					
		108-0	208-0	106-0		1	2	3	4
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3							●	
	M3							●	
	N3					●			
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:

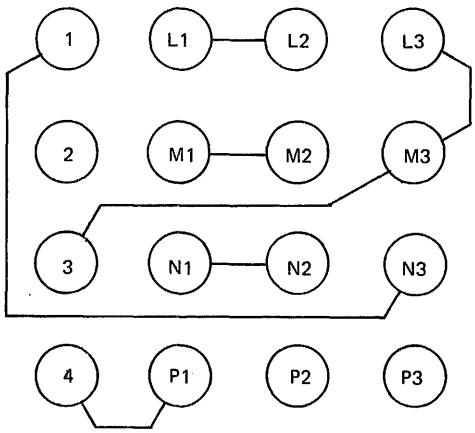
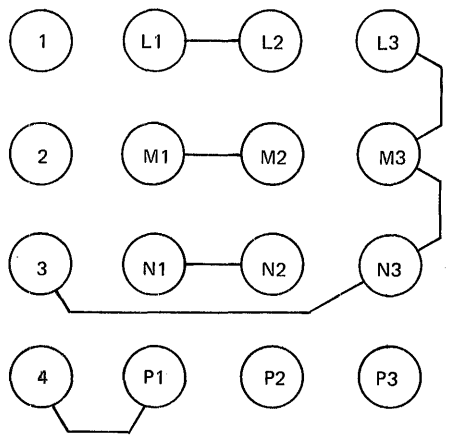


TABLE 22. 32KB MEMORY ADDRESS CODE STRAPPING: MODEL 7/32 (8TH MEMORY) MODEL 8/32 (FIRST 128KB)

		ADDRESS INPUTS			TIE POINT	PULL-DOWN POINTS		PULL-UP POINTS	
		XMA150	XMA140	MA000					
		108-0	208-0	106-0		1	2	3	4
		L1	M1	N1	P1				●
EXCLUSIVE-OR INPUTS	L2	●							
	M2		●						
	N2			●					
	P2								
	L3							●	
	M3							●	
	N3								●
	P3								

● WIRE JUMPER CONNECTION

WIRE WRAP STAKES – LOCATION:



Install the 32-206 Module only in chassis with Local Memory Interface (LMI) printed circuit boards that have 35-534R08 or higher revision.

The 32-206 modules may be configured to form three basic expansion blocks:

MEMORY BLOCK		INSTALLATION
A	128KB Memory Block only	When total memory capacity is 128KB install four (4) 32-206 modules in the upper half of the basic twin chassis.
B	128KB up to 512KB memory (Memory Blocks are in 128KB memory block increments)	Install all 32-206 modules in the first expansion chassis.
C	512KB up to 1024KB memory	Install all 32-206 modules in the first and second expansion chassis.

Part Number 02-409F02 denotes a 32-206 module without parity. The PARO signal is deactivated by connecting A97, Pin 09 (Tie Point "B"), to Gnd (Tie Point "C").

Part Number 02-409F01 denotes a 32-206 module with parity. The PARO signal is activated by connecting A97, Pin 09 (Tie Point "B"), to A97, Pin 10 (Tie Point "A").

Both strappings are implemented on the component side of the printed circuit board. Refer to the *32KB Core Memory Maintenance Manual,* Publication Number 29-493 or 29-513 for additional information.

The 32-206 module requires on-board strapping for address coding.

The address code strapping for each 32-206 module in the 128KB memory block is described in Table 22.

The address code strapping for memory blocks over 128KB is described in Tables 15 through 21.

Deactivate the DATA UNAVAILABLE (DUA0) signal by connecting A97,Pin 02 (Tie Point "F"), to Gnd (Tie Point "G").

For further details on cabling and backplane requirements, refer to the *Model 8/32 System Installation Manual,* Publication Number 29-449.

POWER CONSIDERATIONS

The Model 8/32 configured with 32-206 modules does not require power supply temperature tracking.

In such a configuration, disconnect the 17-357 thermistor assembly from TA and TB and install (solder) a fixed resistor 1K ohm ±5% (21-001F09) in its place.

Recheck the power supply, voltage setting as follows:

Mnemonics	Voltage Setting
P15	+16.5 Volts
N15	- 16.5 Volts

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