THEORY OF OPERATION
09826-66576 CRT ALPHA BOARD

1.0 SCOPE AND GENERAL DESCRIPTION:

1.1 Scope

This document describes the circuitry contained on the 09826-66576 display board. The board includes digital logic which controls monitor timing and produces the alpha display.

The following documents should be on hand when studying the theory of operaton:

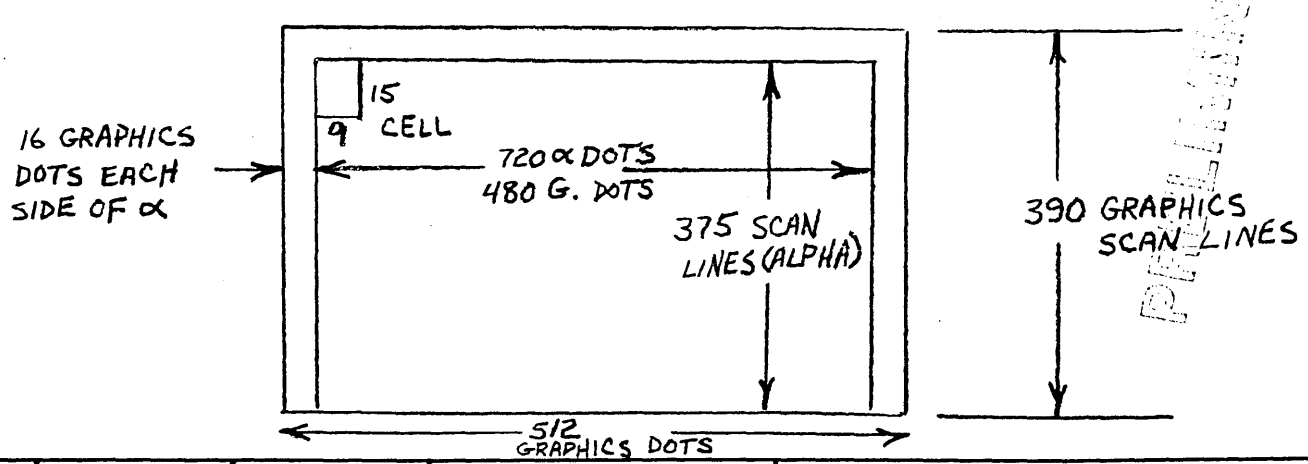
09826-66576-4	Schematic Diagram - 2 sheets
09826-66576-6	Block Diagram - 1 sheet
09826-66576-7	Timing Diagrams - 3 sheets

1.2 Display Capability:

The 9836A display is a memory mapped, raster scan CRT utilizing magnetic deflection. The screen size is 300 mm diagonal with a usable area of approximately 160 mm x 210 mm. Up to 25 lines of 80 characters can be displayed at one time, from a character set containing 256 different characters. With this character set, the 9836A can display all 128 ASCII characters, as well as the HP Roman extention and Japanese characters.

The display has character atrributes. They are: half bright, underline, inverse video, and blinking. Any combination of the above attributes can be used.

The 9836A has graphics standard, with a graphics raster 512 dots wide and 390 dots high. The graphics screen extends outside the alpha screen by 16 graphics dots on each side, and extends 15 scan lines above the alpha screen in the vertical direction. Alpha and graphics dots do not overlay. One graphics dot = 3/2 of an alpha dot. The cell for the alpha characters is 9x15, with most characters fitting in a 7x9 cell. The size of an "A" (typical character) is 1.9 mm wide by 3.7 mm high. See diagram:



LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A	STK NO
THEORY OF OPERATION	
BY Jim Brokish	DATE October 6, 1981
APPD	SHEET NO 1 OF 12
SUPERSEDES	DWG NO A-09326-66576-9

In the normal alpha display, alpha and graphics dots are exclusive OR'ed so that if graphics and alpha dots ever overlay, the dot will be turned off. The only exception to this is if alpha is in inverse video mode. In this case, the graphics will come out full bright over the half or full bright inverse video background. This was done to maintain full compatibility with the 9826A.

The alpha and graphics displays are both memory mapped. Access to the display memory is time multiplexed, or windowed. After each character cycle to the display, a time slot is available for read-write access by the mainframe to the display memory. The interface is asynchronous which means that the access time of the display memory is variable. The best case time from ACS bar true to DTACK bar true is about 250 nsec. The worst case is about 575 nsec.

The alpha and graphics displays can be turned on and off independently of each other without disturbing the memory contents of either. The alpha display is turned on and off by writing a byte to the LSI controller. The graphics display is turned on if its memory is accessed with A15 low, and turned off is A15 is high.

2.0 SOFTWARE CONSIDERATIONS

2.1 General

There are 2K bytes of read-write memory available for character storage, and 2K bytes available for attribute storage. This memory is organized as word wide on the data bus, character on the lower data bus, and attributes on the upper data bus. All CRT memory can be written to or read from by the 68000. The word located at the programmed starting address of the 6845 will be displayed at the upper left hand corner of the CRT. Sequentially increasing addresses correspond to display positions which move to the right along a line of text. When the end of a line is reached, the next character position will be at the left end of the next line down. There are 80 characters displayed in each line and 25 lines on the display. Using the attributes, the soft key label area can be implemented in half bright inverse underline mode. The hardware also supports a mechanism for blanking either the text or SFK parts of the screen, or both, without affecting the contents of display memory.

A Motorola 6845 CRT controller is used to generate most of the video signals. This is a programmable part, and must be set up by software to supply proper timing for the system. A read or write to the 6845 is supported in the 9836A. The software can therefore read the current position of the cursor. This is not supported in the 9826A. The video timing is determined primarily by the

characteristics of the CRT analog drive board. Setup parameters appear is section 2.5. Both 50 and 60 Hz refresh will be supported in the 9836A, jumper selectable on the alpha board. BA15 in the upper data byte is buffered and connected to this jumper, so that it can be read by the 68000. 1=50 Hz, 0=60 Hz. The position of the cursor can be controlled by writing a linear cursor address to the 6845. The cursor will appear as a two scan line blinking underline if the setup parameters used in 2.5 are used.

2.2 Memory Space Usage

The first physical address of the character memory is 512001. The characters are stored in the upper data byte- that is, starting at 512000. Either of the bytes can be accessed individually in byte mode, or both can be accessed at once in word mode. All three access types are allowed. The address line A15 is used for on/off control of the horizontal, high voltage board. A write to the CRT memory with A15 a one will disable the horizontal drive and CRT high voltage. In normal operation A15 should be lo when CRT RAM is accessed. The address line A14 is used to enable a 50/60 Hz latch which sets the pulse width of the vertical retrace pulse. The line A2 is used as an input to the latch. Normally, A14 should be low on a read or write to alpha memory. A read or write to 516004 (BA14=1,BA2=1) gives 50 Hz. A read or write to 516000 BA14=1,BA2=0) will select the 60 Hz pulse width. The CRT controller is also set up differently for 50/60 Hz. (See 2.5)

The 6845 register pointer register is located at address 510001. Data written to this register sets up which 6845 register will be accessed when a write to address 510003 is executed. This space is also multiply mapped because only the address lines A1 and A13-A24 are decoded.

2.3 6845 Register Definition:

The 6845 contains 16 registers, R0-R15. The first 12 registers should not be changed from their power up initialization parameters, as they affect hardware timing. The last 4 may be modified as required by the system software. The functions of these registers are listed below.

R12 - Start address (H)
R13 - Start address (L)
These two registers determine the address of the character which appears in the upper left hand corner of the CRT, as well as performing some control functions. (see Special Features)
R14 - Cursor position (H)

R15 - Cursor position (L)

For a more complete description of the internal registers of the

2.4 Special Features

The 6845 has 14 address lines which are used to access the display memory. Because the display memory requires only 11 address lines, 3 lines (synchronized with the display) are free for the implementation of special features. In the 9836A design, these three lines have been assigned as: KEYS(MA12), TEXT(MA13), and FLD(MA11). By definition, when the FLD line in high, characters are being displayed in the soft key area, and when it is low, characters are being displayed in the text area. The 9836A uses the KEYS and TEXT lines to turn on/off either or both sections of the screen.

KEYS	TEXT	Function
0	0	All characters and attributes off
0	1	Text on, SFK characters and attributes off
1	0	Text characters and attributes off, SFK on
1	1	All on

The lines KEYS and TEXT are "statically" controlled by writing to the start address registers of the 6845. The FLD line is also controlled by the contents of the start address registers, however it can be made to toggle by the display sequencing, indicating where the soft key area starts. So by changing the start address, system software can adjust the starting position of the soft key area, and have selective on/off control of the text area and the SFK area of the alpha screen. Note however that changing the starting position of the soft key area also changes the physical location of the character displayed in the upper left hand corner of the CRT.

With two lines of soft keys at the bottom of the screen, the address of the upper left hand corner of the screen is 513001H (the soft key boundary) minus 730H (80*23 lines) equals 5128D1H. The soft key character RAM starts at 512001 or 513001. (double mapped)

2.5 Initialization:

The 6845 CRT controller must be initialized at power up. Each of the 16 registers should be written with valid data, before any writes to the alpha or graphics memory. The analog drive board requires the first 10 registers to be set up as follows:

Register	60 Hertz data		50 Hertz data	
	Dec	Hex	Dec	Hex
R0	114	72	114	72
R1	80	50	80	50
R2	76	4C	76	4C
R3	6	06	6	06
R4	26	1A	32	20
R5	10	0A	3	03
R6	25	19	25	19
R7	25	19	28	1C
R8	0	00	0	00
R9	14	0E	14	0E

The remaining registers may be set up as desired. For a two-line cursor which blinks at 1/16 of the frame rate, R10=76 Dec, R11=13 Dec.

3.0 ALPHA DIGITAL THEORY OF OPERATION

3.1 General:

The alpha digital section contains the character and atrribute read/write memory, the character set ROM, an LSI CRT controller and TTL logic necessary for system interfacing and general control.

The following discussion will reference the alpha logic block diagram, schematic diagram, and timing diagrams.

3.2 Definition of signals in the Alpha Digital:

3.2.1 System interface signals:

BD0-BD7:	lower 8 bits of the system data bus
BD8-BD15:	upper 8 bits of the system data bus
BA1-BA15:	lower 15 bits of the system address bus
GCS bar	Graphics Chip Select
ACS bar	Alpha Chip Select
BR/W	Buffered Read/Write (low = write)
DTACK bar	System Data Transfer Acknowledge
BLDS bar	System Buffered Lower Data Strobe
BUDS bar	System Buffered Upper Data Strobe
VPA bar	Valid Periferal (6800) Address
VMA bar	Valid Memory (6800) Address

3.2.2 CRT Related Signals

GRES bar	Graphics reset
GRAPHICS bar	Graphics video (0=beam on)
GHRTC	Horizontal Sync for graphics
GVRTC bar	Vertical Sync for graphics

AHRTC	Analog horizontal sync pulse
AVRTC bar	Vertical Sync for the analog board
HALF bar	Half Bright Video (active low)
FULL bar	Full Bright Video (active low)

3.2.3 Signals on the timing diagram

DCLK	Dot Clock (25.77 MHz)
A,B,C,D	State counter outputs
S/L bar,L/S bar	Shift or load timing signal
DLE bar	Data latch enable (active low)
CCLK	Character Clock (1/9 dot clock frequency)
EXADDR bar	0 = External (system) Address to CRT RAM
WE bar,EXD bar	0 = write enable and external data enable
SEL	External select (1 = memory cycle request)

3.3 Alpha Logic Description:

A description of each block on the block diagram and its associated parts on the schematic diagram is given below.

3.3.1 Data Bus Buffer:
Includes U4 and U5, two bidirectional tristate buffers. They are used to reduce loading on the system data lines. This buffer is enabled with any access to the CRT controller, the alpha memory, or the graphics memory. Its direction is controlled by the system read/write line.

3.3.2 Data Bus Isolation Buffer:
Includes U9,10,14, and 15, which isolate the internal alpha data bus from the external (buffered) system bus. U9 and 10 are unidirectional tristate buffers which are enabled on a write to the alpha memory. The enable timing is controlled by U48, which enables the buffers only after the RAM output has been tristated for one cycle, and holds the data to the RAM for one cycle after WE bar to the RAM goes away.
U14 and 15 are latches used to hold data on an alpha memory read. These latches are required because the alpha memory begins another cycle immediately after the system access, and would not necessarily hold data on the bus long enough for the 68000 read cycle.

3.3.3 Character, Row, Control and Attribute Pipeline Latches:
Includes U20, 21 and 37. For U20 and 21, data is latched on the leading (inactive) edge of S/L bar. This allows ample time for the 300 nsec charcater ROM to set up the outputs to the shift register. U37 on the other hand, is clocked by the leading (inactive) edge of DLE bar. This is to allow the 6845 300 nsec from

the trailing edge of character clock to get data setup on the LS374. These occur during every character cycle. U20 holds the ASCII character read out of CRT RAM. U21 holds the four bit number which indicates which row of the character should be displayed, and the four attribute bits from the attribute RAM. U37 latches blanking, cursor, vertical retrace, and horizontal retrace signals from the LSI controller.

3.3.4 Character ROM

Includes only U28, a 4K by 8 Read Only Memory. The pin connections and speed requirements of the part are compatible with a 300 nsec, 2732A pinout EPROM. The addressing is set up so that the 8 most signifigant bits of the ROM address inputs define the character to be displayed, and the fout least signifigant bits determine the row of the character to be displayed. The character cell size is 9 dots wide by 15 dots high, but only 7 bits, D0-D6 are used for dots in the cell. The other bit, D7 is the half shift bit, and if it is a one, this line of the character is delayed by one half dot. The seven dots are inserted in the middle of the 9 wide cell, leaving two default spaces between characters in the horizontal direction. There are no default spaces in the vertical direction. Most characters fit in a 7x9 cell, some using more dots for decenders, etc.

3.3.5 Parallel to Serial

Includes U29 and U24, two paralled in serial out 4 bit shift registers. One row of a character is loaded into the shift register every character time. This occurs on the rising edge of DCLK when L/S bar is high. A dot is shifted out on every positive edge of DCLK, if the output of the shift register is a one the beam will be on, if it is a zero, the beam will be turned off.

3.3.6 Half Shift and Dot Stretcher

The half shift circuit consists of U43, 30, 35, and 36. U43, a D flip flop is used to pipeline the video from the shift register through U16 to U30, the negative edge triggered flip flop in less than one half dot period. U34, the S194 is not fast enough to get the video to U30 on time. The half shift bit from the character ROM is latched in U36, and goes to one of the select lines of U35, the S151 multiplexer. A low will select dots from U43 directly, and a high will select dots delayed 1/2 dot period by the negative edge triggered S112, U30. The underline/cursor and blink/ blank attributes are also combined at this stage. When underline/cursor is true, that character line is inverted. This is for BASIC software, which, for an insert cursor uses a full cell cursor over the character. Exclusive ORing the character with the cursor allows viewing of the character when the cursor is put in this

mode. The enable input is used for the blink/blank input, and if either is true, the output is disabled (0's sent out).

The dot stretcher circuit includes R1, R2, C25, C31, and Q1, and inverts and stretches single dots to compensate for the limited bandwidth of the video amps. Without this circuit, vertical alpha lines come out dimmer than horizontal lines. If a series of dots are on, the last dot will be stretched. This is done with the RC time constant of R2 and C31, coupled with the saturation affect of the transistor. Other methods of compensating for the limited bandwidth of the video amps, such as pulling the cathode extra low on the first dot of any series of dots exist, and should be investigated in any future design.

3.3.7 Blanking and Attribute Logic:

The attributes are stored in the attribute RAM as follows:

BD8	Inverse Video
BD9	Blinking
BD10	Underline
BD11	Half Bright

This logic includes U11,16,22,23,25,35,42 and 44. Normal half bright gives an ordinary character, only half bright. Underline will underline the character on line 15 of the cell. Inverse video inverts the character. Blinking characters will blink at 1/64 of the frame rate, as set by U46--that is, 0.94 Hz for 60 Hz, and 0.78 Hz for 50 Hz. The attributes can be mixed in any fashion. Blanking is driven by the blanking signal. See section 2.4, Special Features.

3.3.8 Attribute Logic and Video Mixer

Includes U35, 11, 12, and 17. The underline, cursor, and blanking signals are mixed as in 3.3.6. The resulting signal is run through the dot stretcher, and to the 8 to 1 multiplexers U12 and U17. The truth tables for the functions implemented look as follows:

Graphics	Dots	Inverse Video	Full	Half
0	0	0	0	0
0	0	1	1	0
0	1	0	HB bar	HB
0	1	1	0	0
1	0	0	HB bar	HB
1	0	1	1	0
1	1	0	0	0
1	1	1	1	0

U11 inverts the full and half signals, and drives the signal open collector to the analog board. The outputs are pulled up with 200 Ohm and series terminated with 50 Ohm to reduce EMI. The jumper allow future addition of a bead if required for EMI.

3.3.9 LSI CRT Controller:

Includes U19, a Motorola 6845 CRTC. This part supplies the screen refresh memory address to the CRT RAM, and contains a timing chain for the derivation of vertical and horizontal retrace signals. Other functions performed in this part include the generation of the signals: CRSR, RA0-RA3,FLD-KEYS-TEXT, and DEN. CRSR supplies timing for the cursor logic. RA0-RA3 are the row address lines used by the character ROM and determine which row of a character is to be displayed. FLD-KEYS-TEXT are "extra" memory address lines which are used for on/off control of the text and SFK areas of the screen. DEN (display enable) is used to determine when the screen should be blanked.

The CRTC contains registers which are used by system software to control the display. The two most important ones are: The cursor position register, and the start address register (controls alpha on/off and soft key area). Other registers in the 6845 control the display format and are set up with an initialization routine.

3.3.10 Address Mux:

Includes U1,2, and 3. The purpose of the address multiplixer is to select the CRT RAM address from either the CRTC or the system address lines. The timing of the selection is controlled by the signal EXADDR bar.

3.3.11 Character RAM and Attribute RAM

Includes U7 and U8, 100 nsec, 2Kx8 RAMs. 100 nsec access times are required to allow enough time for two accesses to the RAM in one character cycle. The output enable lines of the RAMs are set up to be tristated one dot cycle before a write, to prevent bus contention between the buffers and the RAM data lines.

3.3.12 Interface Logic

Includes U6,13,24,25,43,33, and 18. The three major functions performed are: system interfacing to the 6845 CRTC, system interfacing to CRT RAM, and control of the tristate buffers which drive the system data bus.

The 68000 has provisions for interfacing to 6800 peripheral chips such as the 6845. The interface is accomplished with the use of the lines VPA bar, VMA bar, and E. The sequence of events is as follows: (see the 6845 write cycle timing diagram) The 68000

begins a normal memory cycle to the address of the 6800 peripheral, which returns Valin Peripheral Address. (VPA bar) In response to this action, the 68000 synchronizes the transfer with the "E" line, and asserts VMA bar low. Unfortunately, address strobe is not held valid ling enough for the complete 6800 cycle and ACS bar may go away to soon. This is the reason for the cross coupled NOR gates of U13, the 6845 chip select timing is controlled by VMA bar, not by ACS bar.

The character and attribute RAM are written and read just like system memory. Access to the CRT RAM is asynchronous, the memory cycles are synchronized with the use of DTACK bar. The sequence of events for a CRT RAM cycle are as follows: ACS bar is asserted with A13 high (memory is addressed in CRT RAM space). The first positive edge of DCLK after BLDS bar goes low clocks a one into the first stage of a two stage synchronizer. (U43) The second stage of the synchronizer, U36, clocks in the output of the first stage on the first positive transition of DCLK after L-S bar goes high. The signal thus generated is called SEL and is used to initiate a memory cycle. The rising edge of EXADDR bar indicates the end of the memory cycle and causes DTACK bar to be given. U33 is used to latch DTACK and to protect against a slow termination of the cycle by the system, causing an unintended CRT memory cycle. The two stage synchronizer is required because of the asynchronous nature of the access. If the set up time of the F374 is not met, the output may oscillate a few times before settling to a final state. An "F" part is used to minimize oscillations on the output. The two stage synchronizer will guarantee that these expected oscillations will not cause false logic signals to propagate through the circuit.

3.3.13 Timing and Control Logic

Includes U36,41,44,47,27,43,and 48. Insight to the operation of the timing and control logic can be obtained by examination of the CRT ALPHA TIMING DIAGRAM.

The key point to notice is that system accesses of the CRT RAM are time multiplexed with the synchronous accesses required by the display (CRT priority). During every character cycle there is a time window long enough for an external memory cycle. Processor system accesses are synchronized to this window by the timing and control logic state machine. Each character cycle is divided into nine states by the state counter U41 and state latches, U43 and 48. These states are indicated on the timing diagram as S0-S8. Each positive edge of the dot clock initiates a new state, negative edges of this clock are not used in the state machine. Character and attribute data is latched into the pipeline buffers U20 and 21 at the end of S8.(inactive edge of S/L bar) If an access request has been asserted before the end of S7 in the previous cycle it

will be serviced during the time slot between the start of S1 and the end of S4. DTACK bar will be given and data latched out at the end of S4. The states S5 to S0 are always used for display memory cycles.

The state mahine has two inputs and five outputs, the inputs are select and read/write, these lines determine the output states in the time interval between the end of S0 and S4 (an external access). The output states between the end of S4 and S0 are always the same. Only two of the outputs are actually controlled by the state machine, the other three are cyclic signals which run continuously (clocks). The two controlled lines are EXADDR bar and WE bar, EXD bar. EXADDR bar is used to gate the processor system address onto the CRT RAM memory and for timing of DTACK bar and data latching. This line pulses low only during external write cycles to the CRT RAM. It is used to gate external data onto the internal CRT data bus, and to enable the CRT RAM chips to accept data. The three clock lines are used to sequence the data pipeline and provide a clock to the 6845. They are L/S bar, DLE, and CCLK. All three of these signals have the same frequency, 1/9th the dot clock, but different phases.

3.3.14 50/60 Hertz Select

Consists of U15, JA1. BD15 of the upper data bus does not go through the buffers to D7 of the attribute RAM as one would expect. Rather, it goes to the 50/60 Hz jumper. This jumper can be read just as a bit of data from the RAM would be. Data written to this bit is ignored.

3.3.15 AHRTC ON/OFF Latch and Pulse Shrinker

Consists of U33 and U45. A write to CRT memory with A15=1 disables horizontal drive and turns off the beam. The analog board is triggered on the negative edge of AHRTC, and requires the negative edge to be around the 77th character of the scan. Due to a bug in the 6845, the trailing edge of HRTC must occur off the screen, or the cursor will always fill the cell.(not desired) This is the reason the pulse shrinker, U45 is required. As long as HRTC is low, the output will be low. When HRTC goes high, the counter counts to four, and then holds itself off from counting any further. The AHRTC pulse will then be two character times. (698 nsec)

3.3.16 VRTC Pulse Stretcher and 50/60 Hz Latch

The graphics board generates its own start of frame signal from the inactive edge of the vertical retrace pulse. However, the 6845 only sends out a vertical retrace pulse with a 16 scan line length. If the 6845 VRTC were set up to give the same trailing edge position for both 50 and 60 Hz, the graphics board would force

the pulse into a position where the AC coupled vertical retrace on the analog board would put some of the text off the screen. The 50/60 Hz latch stores the present setup, 0=60, 1=50 Hz. The latch is clocked with BA14 ANDed with EXADDR, and latches in BA2. Normal accesses to CRT RAM should be made with BA14=0. Reads or writes with BA14=1 will clock the latch. The counters load 253 for 60 Hz, and 215 for 50 Hz. These numbers assure that from the trailing edge of VSYNC, there are six scan lines before the start of alpha and graphics video on the next frame in both 50 and 60 Hz mode. AVRTC bar and GVRTC bar are isolated from each other by NOT gates.

3.3.17 Crystal Oscillator and Buffers

Consists of U18, 26, and 27. The alpha dot clock is driven from a 25.7715 MHz crystal oscillator. The jumper JB2 can be pulled to allow automatic testing to use their own clock. S04 NOT gates are used to buffer the clock to give the needed drive capability. They are in the same package to keep approximately the same delay between the clocks. The maximum skew of the crystal is 45/55. This max skew is critical for some timing on the graphics board. On the alpha board, the negative edge is used only for the half shift circuit, and 40/60 skew is acceptable.