THEORY OF OPERATION

09826-66562-9 Floppy Control Board

I. INTRODUCTION

The floppy control board is designed to interface with up to two 5 1/4" double density dual sided drives to the 9826/36 bus. The drive has a 270K byte formatted capacity. The actual transfer rate is 16K bytes/sec with the default interleave and track to track stagger.

The standard diskette is formatted with 16 sectors per side, two physical sides per track, and thirty five tracks total. Each physical side of a track is called a track-side. There are therefore 70 physical track-sides.

Of the 70 track-sides actually available, 66 are used. The other four are spares, decided on at initialization. The total number of track-sides available to the user is constant at 66, and that information is recorded in the directory. In fact, up to four additional tracks will be formatted to aid in the seeking of the user available tracks. The last track formatted is always physical track 34. The numbering of logical records is cylinder mode addressing, proceding from side 0 to side 1 and then to the next track.

The board provides for all low level encoding and decoding activity to be done on the board. The seek and initialize operations require the use of the host processor's time. The board does have a single sector buffer allowing the mass storage operations to be interrupted by I/O activity or live keyboard.

II. SYSTEM BUS INTERFACE

ADDRESSING

The address space of the internal mini-floppy is defined as $440000 to $44FFFF. This space is decoded off the board to a single line select called chip select floppy (CSF'). The addresses of most of the locations on the board are multi-mapped. Only the address lines required are decoded. Two of the undecoded address lines (A14,A15) are used to

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 2 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

determine bus cycle length. Those bits are critical in the address, as shorter than the required cycles will cause errors because of improper timing.

The chip select is further subdivided on the board to address registers, on-board RAM, and the LSI Floppy Disc Controller (FDC). This job is done by decoder U42, gate U4, and gate U29. In addition gates U23 and U30 provide proper timing relationships by qualifying raw chip selects with other control signals.

U29 decodes the accesses to the FDC. This address space is further divided by address lines BA1 and BA2 to access each register. The internal registers are the command register (00), the track register (01), the sector register (10), and the data register(11).

U4 decodes the primary address of the on-board RAM. That address is further divided by address lines BA1-BA8 to address each of the 256 bytes in the RAM. U42 both decodes and divides the register selects to access the extended command registers (XCMD), the extended status register (XSTAT), and the special function clear extended status (CLRXSTAT).

It is important to remember that this board has its own internal bus. This bus transfers data to and from the floppy disc controller and the on board RAM. The bus usually is tied to the system bus by U31, a bidirectional buffer. At some times during command execution the internal bus is "broken off" of the system bus and carries transfers only between the FDC and the on- board RAM. These transfers are controlled by the state machine.

A summary of the valid addresses to the board follows:

$445000	XCMD	write	625ns
$445000	XSTS	read	625ns
$445400	CLRX	write	625ns
$44E000- $44E1FF	on board ram	read-write	1us
$44C000	command reg	write	1us (in FDC)
$44C002	track reg	read-write	1us " "
$44C004	sector reg	read-write	1us " "
$44C006	data reg	read-write	1us " "

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 3 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

EXTENDED COMMAND

The extended command register (U25) is an 8 bit register which controls board function. The bit assignments are:

1) Drive active
1) Pre-comp high
2) Headl
3) Reset FDC'
4) Read/write'
5) Local
6) Address 0 (A0)
7) Address 1 (A1)

At power up the extended command register (XCMD) is cleared. This in turn will reset the FDC. The register is write only, and therefore a copy of the register contents must be maintained in system RAM in order to set and clear individual bits. A short description of each bit's function follows.

The drive active bit will enable the floppy drive selected by bits 6&7. In single drive applications, that will always be drive 0. The immediate consequence is that the drive active LED will light on the front panel of the selected drive. The drive active bit is also an input to the motor-on circuit, and it will always start and hold the motor on.

The pre-comp high bit specifies that the higher level of pre-compensation will be used by any writes to the diskette. The bit is set for inner tracks where more pre-comp is required and it is cleared for outer tracks where little or no pre-comp is needed. The subject of write precompensation will be enlarged on later in section V.

The side select bit goes directly to the drive interface cable. It is used to specify the physical head to read and write on the selected drive. The selection is not latched by the drive.

Reset FDC' serves two purposes. First, it stretches the reset pulse at power up. The bit is cleared by system reset, and of course remains low until re-written by software. Secondly, it allows the resetting of the FDC chip independent of the other peripherals. This ability allows for the recovery from certain error conditions as part of re-try algorithms.

The READ/WRITE' bit is used to configure the on-board state machine for transfers on the internal bus. If set, the state machine will transfer data from the FDC to the on-board RAM. If cleared, the transfers will be from the RAM to the FDC. In other words, the state of the READ/WRITE' bit must agree with the type of operation occurring to the diskette.

LOCAL is perhaps the most important XCMD bit. When true the internal bus is under local control. Accessing the RAM or FDC from the system bus is not allowed. The bus buffer is also prevented from taking data from, or placing data on the system bus.

Since the length of transfers is controlled by circuitry on the proccessor board (sync mode), any attempt to access these locations will appear to be successful. That is, no bus error will result. When the local bus is separated, during read or write operations to the FDC or RAM, read data will not be valid and the transfer of write data will not occur.

Local also passes the FDC and RAM signals to state machine control. WE' and RE' for the FDC, as well as WE' and CE' for the RAM are on a tri-state bus. If LOCAL is set the state machine drives those signals with U8. If LOCAL is not set the signals are driven from system control lines by half of U43. Local also selects the FDC continuously. Local mode does not disable the reading of XSTAT or the writing of XCMD.

The address 0 and address 1 lines are used for drive select. Since this board only controls up to two drives, address 1 line is not used. The address 0 line chooses drive 0 when it is cleared; and drive one when it is set.

EXTENDED STATUS REGISTER

The extended status register (1/2 U43) is a read only register which provides additional information about the condition of the FDC and drive not contained in the FDC status register. The bit assignments are as follows:

1) Data request
2) Media change
3) Margin error
4) Interrupt

The data request bit is a copy of the data request output of the FDC. It is used during initialize operations. Together with interrupt it controls the flow of data into the FDC from the system bus during the time-critical initialize operation.

The media change is set each time the write protect switch goes from false to true. That will happen whenever the disc is fully removed from the drive. U21 and U27 monitor the write protect lines from the two drives. The bit is cleared by the CLRXSTAT special function address.

The margin error bit is set by a read data transition too close to a read clock edge. It is used while initializing the diskette to evaluate the media quality. The theory of that reduced margin check is described in section V. The bit is cleared by the CLRXSTAT special address.

The interrupt bit is a direct copy of the interrupt output to the bus from the FDC. During initialize operations the interrupts of the entire system are masked. The fast handshake mode of data transfer is used and this copy of the interrupt bit is used to signal command completion.

ON-BOARD RAM

The local RAM has a 256 byte structure. The board has provisions for the use of 2112 (256X8) or 2114 (1KX8) RAMs. This is allowed by two sets of pads in the same board area. If the 2114 RAM is used, only 1/4 of the part is addressable.

When the internal bus is in the remote mode, the state of each lower address line is loaded into U19 & U24 at the beginning of each RAM cycle. This is done through gate U30 which removes the load signal when address strobe goes high. The address is latched until it is changed by the next access to the local RAM.

When the bus is in the local mode, the state machine will increment the address of RAM after each transfer of data to the FDC. The starting address used in that process is the last address read to the outside bus. It is important to read the first address of the local RAM each time before passing control to the state machine.

The state machine is a shift register and a data

selector. Each time a data request is issued by the FDC a positive-going edge shifts through the snift register. When that edge reaches the last stage the output of U41 removes the high input to the shift register,since pins 1 and 2 are logically anded. A zero then shifts through, causing two strobes to be created. Both strobes go low at the same time. The output at U23 is low for 500ns. The output at U23 is low for lus. Those two strobes are used to generate all control signals. They are connected into the respective signals through selector U8. One half of the inputs of U15 are the write operation controls, and the other half control the read operations. The select input of U8 is the READ/WRITE' signal previously described. The last thing that the state machine does is to increment the address counters (U19&U24) through U41.

FLOPPY DISC CONTROLLER

Accesses to the floppy disc controller registers involve several parts. The timing relationships of the FDC are quite different than the usual 68000 cycle.

U14 consists of two latches for the register select inputs of the FDC. They latch data on a rising clock from U22. That occurs on the falling edge of buffered address strobe'. The latches are required to meet hold time specifications at the end of the cycle. Anotner job done by U14 is the selection of the data register for all local transfers. The set inputs bring the outputs to a 1-1 state whenever LOCAL is true.

Gate U29 decodes the FDC chip select. Those two parts serve to hold FDC chip select on whenever LOCAL is true, and to stretch the select during reads. In a read U29 sees both CSFDC and REFDC low and holds CSFDC low througn U29 until REFDC is removed.

A summary of the FDC commands available follows;

0H	Restore (h=0 head load, h=1 nead unload)
1H	Seek
2H	Step (same direction last stepped)
3H	Step and update
4H	Step in
5H	Step in and update
6H	Step out
7H	Step out and update
82	Read single sector, logical side 0
8A	Read single sector, logical side 1
A2	Write single sector, logical side 0
AA	Write single sector, logical side 1
C0	Read address
E0	Read track
FX	Force interupt (X=Interupt mask)

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9336A STK NO

THEORY OF OPERATION

BY Ron Rogers/JR DATE October 13, 1981

APPD SHEET NO 8 OF

SUPERSEDES DWG NO A-09326-66562-9

The FDC status word returned is a function of tne last command issued to the controller. A summary of status words follows:

Bit	All Type 1 Commands	Read Address	Read Sector
S7	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	0
S5	Head loaded	0	Record Type
S4	Seek Error	RNF	RNF
S3	CRC Error	CRC Error	CRC Error
S2	Track 0	Lost Data	Lost Data
S1	Index	DRQ	DRQ
S0	Busy	Busy	Busy

Bit	Read Track	Write Sector	Write Sector
S7	Not Ready	Not Ready	Not Ready
S6	0	0	Write protect
S5	0	Write Fault	Write Fault
S4	0	RNF	0
S3	0	CRC Error	0
S2	Lost Data	Lost Data	Lost Data
S1	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy

MISCELLANEOUS

Gate U23 and U30 generate BUSEN. BUSEN turns on the bus buffer whenever the local RAM or the FDC are addressed. The exception is when LOCAL is high, in which case the access is disallowed. The direction control is taken from R/W' through U41.

Whenever control is passed from the external control lines to the state machine, the signals involved are momentarily not driven by either. In order to assure that no glitches occur the lines REFDC, WEFDC, RERAM, and CERAM all have resistor pull-ups.

A 10 MHz clock is provided to the board from the mother board. The clock is buffered by U41 immediately, to cut down

capacitance and also to improve EMI. The clock is used in the write pre-compensation of data directly. The clock is divided to 2 MHz by U26 for use in the state machine. It is also divided to 1 MHz for the FDC clock.

III. FLOPPY DISC INTERFACE

GENERAL

The connection between this board and the mini-floppy drives it controls is through a 34 conductor ribbon cable. The description of the signal levels is available in the ANSI standard #X3T9/846, "AMERICAN NATIONAL STANDARD FOR THE INTERFACE BETWEEN FLEXIBLE DISC CARTRIDGE DRIVES AND THEIR HOST CONTROLLERS".

There are several special circuits on the drive interface side of the FDC. They manage motor control, wait for the drive to reach operating speed, and buffer signals to and from the drive. The highly specialized read and write circuits are described in sections V and VI.

READY

The ready circuitry detects index pulses from the drive selected. The pulses are inputs to a one shot with a time constant of 250ms. The input pulses are 200ms apart whenever the motor is at proper speed. The leading edge of the index pulse is used as the one shot trigger. As long as the motor is on, and a diskette is inserted, ready should be constant true. That is because the one shot timing period is longer than the pulse spacing. Each drive interface has its own ready circuit. This prevents a wait period after drive select is changed.

UP-TO-SPEED

An extension to the ready function is the up-to-speed output from shift register U1. After the motor is on, each index pulse clocks the shift register. The input is tied high, and after 3 clocks a "1" appears at the output. That signal is applied to head load timing (HLT) of the floppy disc controller. The result is that whenever a high level command, such as read sector or write sector is executed, the operation can not begin until three index pulses after motor on. The shift register is cleared whenever the motor is off.

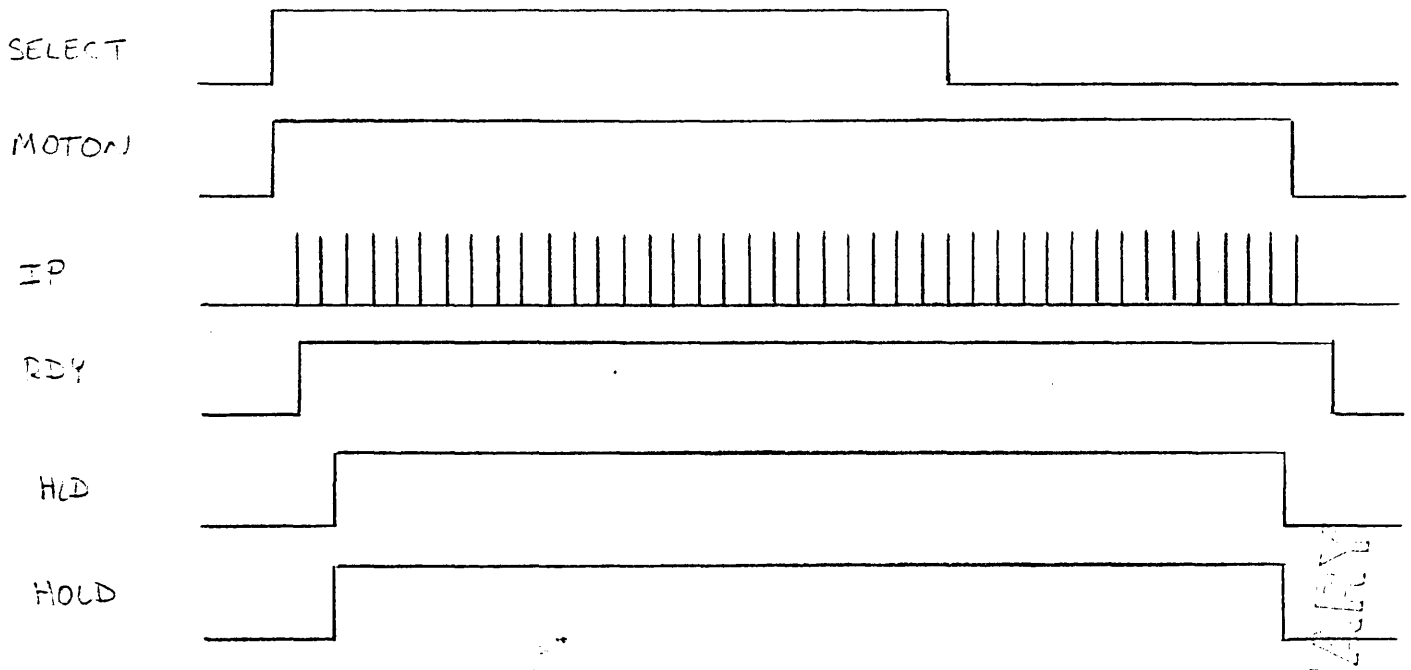


FIG 1 MOTOR TIMING

MOTOR-ON

Motor-on control is provided by U45 and U17. The function of the gates is to hold the motor on after a command for three seconds. Gate U45 ands the signals head load (HLD) from the FDC and ready. The output of gate U45 is HOLD, a signal that holds the motor on.

HLD is a signal intended to be used in drives with a head load solenoid. It is asserted by any high level command and remains on until 15 index pulses after command completion. If the diskette is removed from the drive, or the door is opened, ready will disappear and hold will change to false. If this gate was not there the motor would stay on forever, since HLD will remain for 15 index pulses, and no index pulses occur with no disc.

Gate U17 allows either the XCMD bit or the HOLD signal to keep the motor on. Normally the XCMD select bit is high during all low level software driver activity. The function of hold is to allow for control to pass back to high level

software and return to the driver without incurring the 600ms wait to come to speed.

DRIVE SELECT

Address 0 comes from the XCMD register, U34 inverts the signal A0 generating A0'. These signals control all of the multiplexers and demultiplexers. U32 generates SEL0 and SEL1 control signals for the drives. U44 and U47 are the multiplexers for all the signals coming from the drives. This also includes the ready signal and the media change bit which are generated on the controller. The signals output to the drive WG and STP are gated by U49 and qualified by A0 and A0'. The other output signals do not require gating.

MISCELLANEOUS

The only other interface logic not in the serial data streams is the write gate protection. Gate U45 ands the write gate signal from the FDC with reset so that write gate is never asserted at power on.

The remaining packages in the interface area are buffers and receivers. U9 buffers the outputs of the FDC so that they are not required to drive the standard TTL bus drivers (U33, U39 & U40). The floppy bus drivers are open collector gates that are terminated by 150 ohm pull-ups on the floppy drive electronics board. U35 and U38 are Schmitt trigger packages which receive the drive signals.

IV. PHYSICAL FORMAT

MODIFIED FREQUENCY MODULATION ENCODING

The best place to start a description of MFM is with frequency modulation (FM) encoding. As the name implies the data is distinguished to be a one or zero by the frequency of the data pulses. The system starts with a clock signal of 125 KHz. Each 8 uS a pulse occurs that defines the cell boundaries. If the data is all zeroes that is all there is.

Whenever a one occurs in the bit pattern an extra pulse is added to the "data" cell, half way between the clocks. That pulse doubles the frequency. The decoding of FM data is easy since a simple one-shot circuit can see the extra pulse as a one.

In review FM has clock cells and data cells each 4us long. Every clock cell has a transition in it. Any bit that is a one will have a transition in the data cell.

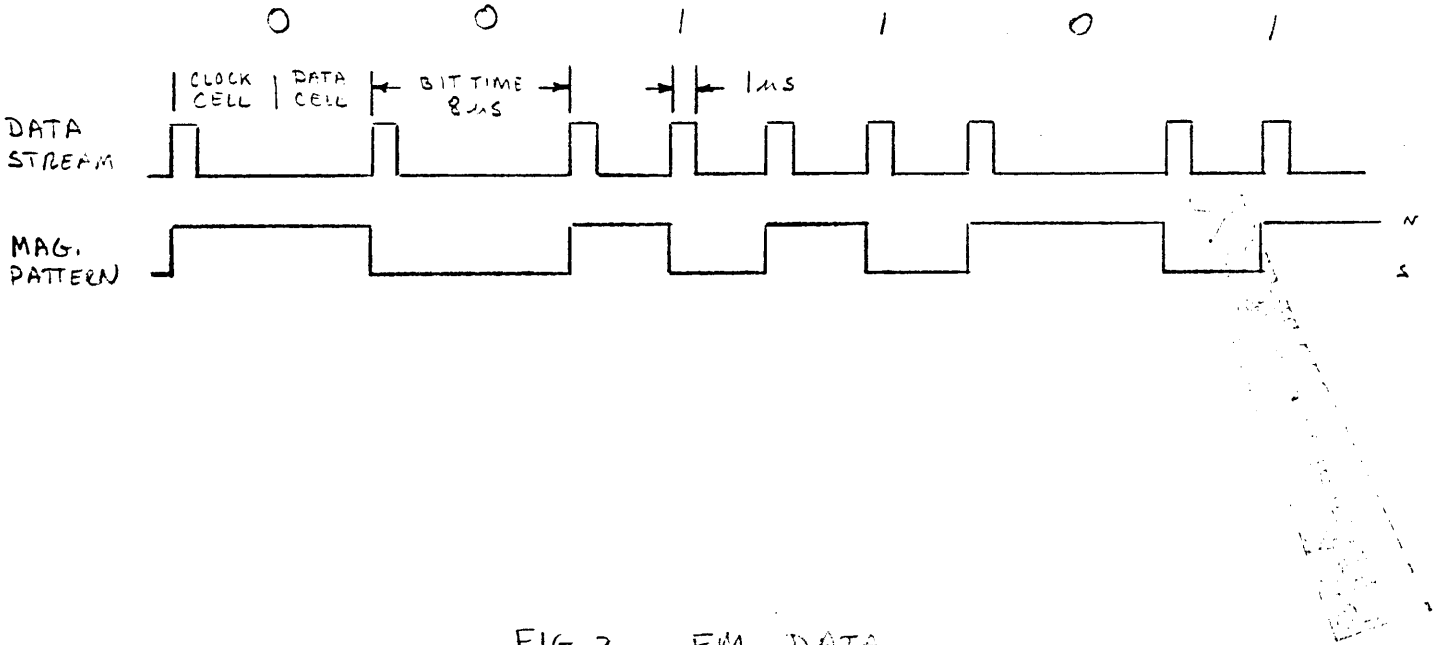


FIG. 2 FM DATA

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 13 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

MFM data is based on a series of clock pulses 4 us apart. If there are no ones, that is all there is. If a one occurs, things are a little more complex. Not only is a pulse written between the two clocks, but the clock pulse for the bit is not written. In addition the clock cell for the following bit must be empty. That will naturaly occur if the next bit is a one, but if the next bit is a zero, nothing is written in either cell.

That helps keep the transition density low, but the data is now phase modulated instead of frequency modulated. There are now identical bit streams possible with two entirely different interpretations depending on the phase they start in in. Almost any practical method of decoding MFM data is going to involve the use of a phase lock loop.

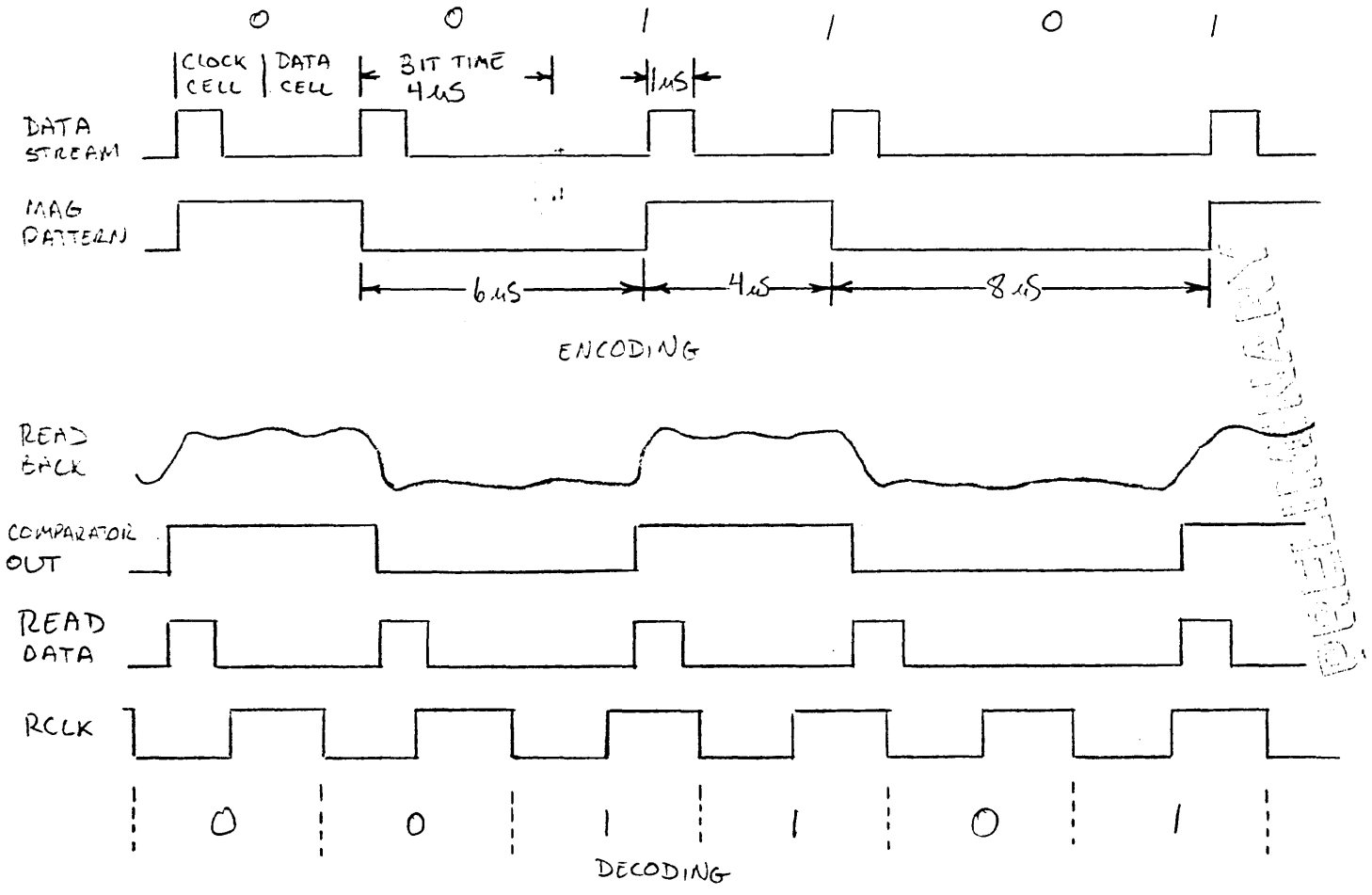


FIG. 3 MFM DATA

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 14 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

CORPORATION STANDARD PHYSICAL FORMAT

Most of the divisions using mini-floppys have all agreed to a single physical format. The purpose of the standard is to guarantee that there are no impediments to the interchange of data built into the media initialization.

The format of the disc is 33 logical cylinders (0-32), each having two sides (0-1), and each side having 16 sectors (0-15). The corporate standard defines exactly what bytes are written on each track.

Number of bytes	Hex Value	Description
85	4E	Post Index Gap
16	4E	Sector
12	00	Sync Field
3	A1 (note 1)	
1	FE	ID Address Mark
1	XX	Cylinder Number
1	XX	Side
1	XX	Sector Number
1	01	Block Length
2	XX	CRC
22	4E	ID Gap
12	00	Sync Field
3	A1 (note 1)	
1	FB	Data Address Mark
256	XX	Data
2	XX	CRC
28	4E	Sector Postamble
155 (note 2)	4E	Pre-index Gap

REPEAT 16X

notes: 1 The A1 pattern in this field is missing a clock transition between bits 4 and 5.
2 Minimum pre-index gap based on 3.6% motor speed variation, write 4E until index pulse.

The CRC mentioned above is a 16 bit cyclic redundency check. The polynomial is G(X) = X^16+X^12+X^5+1. The register is initialized to ones and includes all information starting with the address mark and up to the CRC bytes.

V. WRITE PRECOMPENSATION NETWORK

The purpose of write precompensation is to change the outgoing bit data stream in such a way as to improve the integrity of the signal that returns during reads. The reason that this is possible has to do with the way in which the transitions interact on the media. Each pulse that the FDC sends to the drive causes a flux reversal on the media. By looking at the resulting magnetization pattern of two adjacent transitions, it is obvious that they interact. In many cases the interaction of several flux reversals has no net effect. In other cases, a pattern of reversals will always shift the pulse a predictable direction.

The magnitude of this shift is a product of many variables. The biggest variable is the physical spacing between the pulses on the media. The closer together the pulses, the more interaction. This means that transitions on the outer tracks are not effected as much as those on the inner track, since the bit densities are higher on the inner tracks.

The circuit on this board is capable of multi-level pre-comp. It uses a 10MHz clock to shift the bit stream, and can therefore make 100ns changes in the bit positions. The decision about whether to shift early or late comes from an algorithm inside the FDC.

As each pulse comes out write data (pin 31 of the FDC), the information of early and late is latched by U36. Package U46 synchronizes the data with clock edges and creates a pulse of 1us duration. The pulse shifts through shift register U50. The output tap of the shift register used is selected by U47, under control of the early and late signals and also the pre-comp level select.

Suppose pre-comp level select is nigh, then for normal (neither early nor late) bits the middle tap is selected. All such normal bits are delayed 200ns (referenced to output #1). If early is true, the no-delay output is selected, and if late is true 400ns delay is selected. If the pre-comp level select is low, the data is always taken from the 100ns delay tap and there is no pre-comp.

The purpose of two pre-compensation levels is to maximize the margin with wich the data is written. Levels are not specified in the corporate standard. Each division

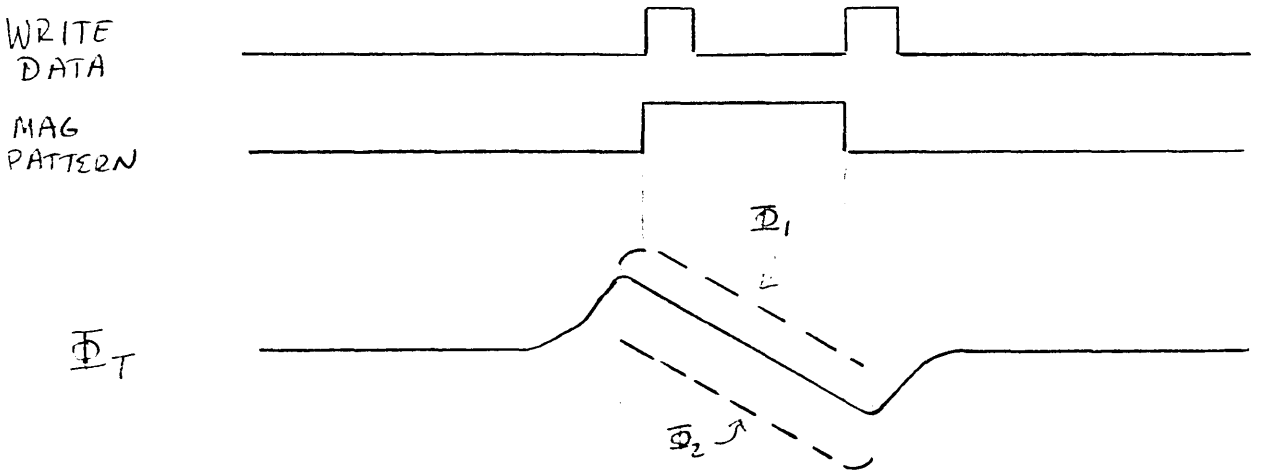


FIG. 4 PULSE SPREADING

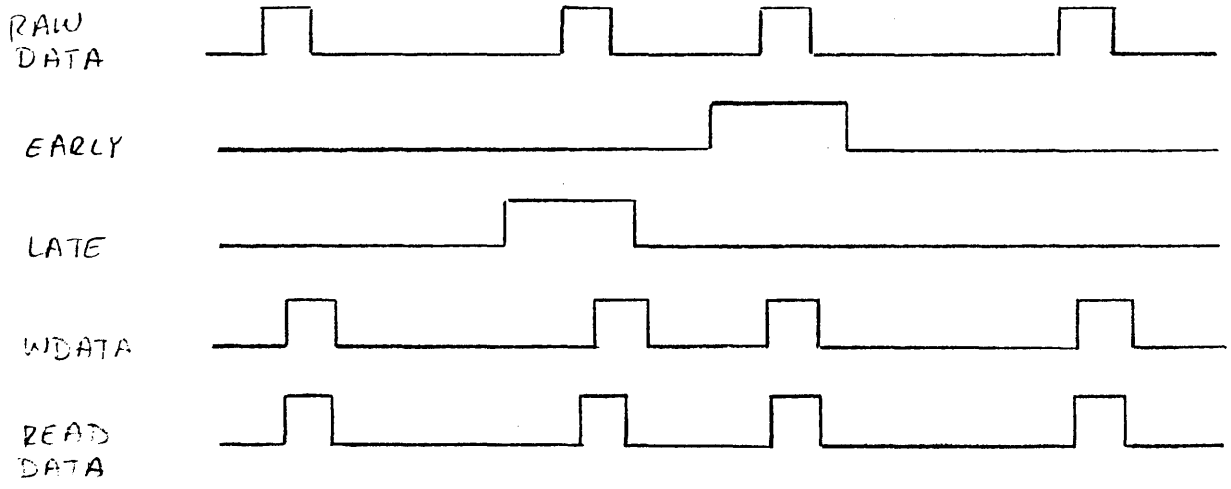


FIG. 5 PRE-COMP

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 17 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

has determined the amount and selectability of pre-comp. It should not cause interchange problems, since any pre-comp on the inner tracks should be better then none. The reading drive has no way to distinguish the amount of pre-comp used.

V. READ RECOVERY

Read recovery is the biggest challenge of any magnetic storage device. The read recovery circuit can be divided into two major blocks. The most important part is the phase lock loop. It is responsible for generating the read clock signal (RCLK) that the FDC uses to recognize cell boundaries. The second part is the loop management circuit, responsible for controlling the locking and unlocking of the phase lock loop.

PHASE LOCK LOOP

1) Block diagram

The block diagram of the phase lock loop is shown below. The voltage controlled oscillator (VCO) is U12, Q1-4, Q8, Q9, CR2, CR3, and a few resistors. The sampling section is Q5, Q6, Q10-14, and CR5. The filter is C6, C7, and R22. The frequency clamper is Q7, Q15, and CR1. The phase clamp is R42 and U13.

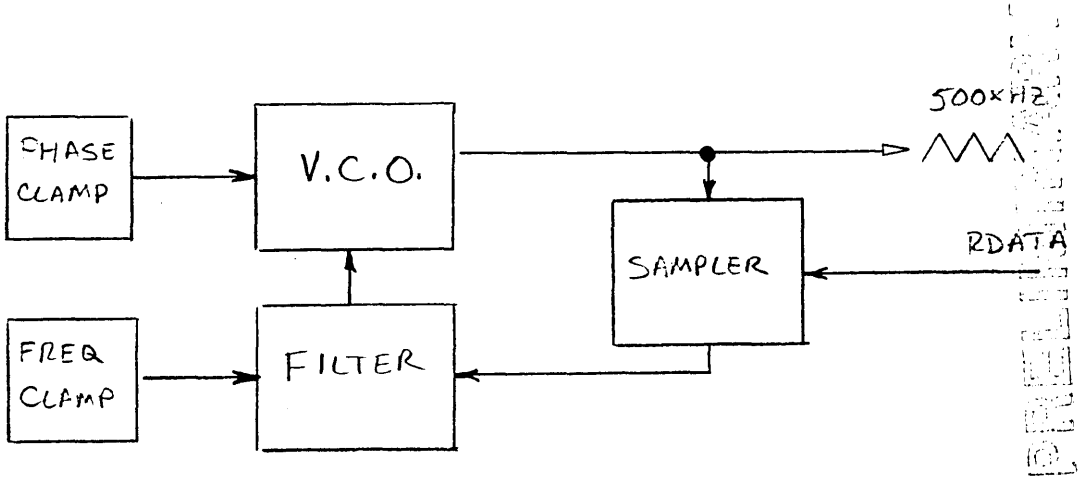


FIG. 6 PHASE LOCK LOOP

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 18 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

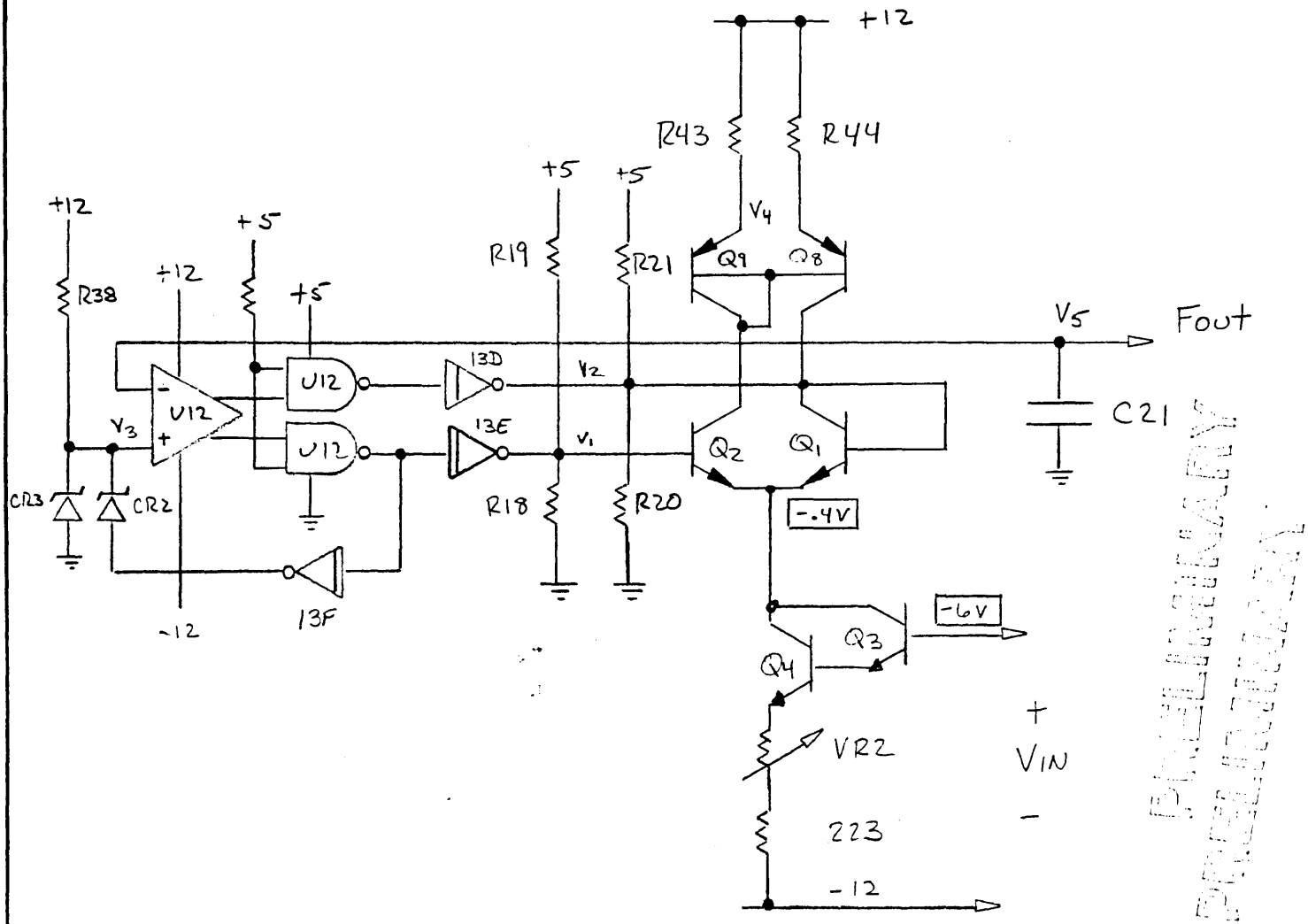
2) Voltage controlled oscillator

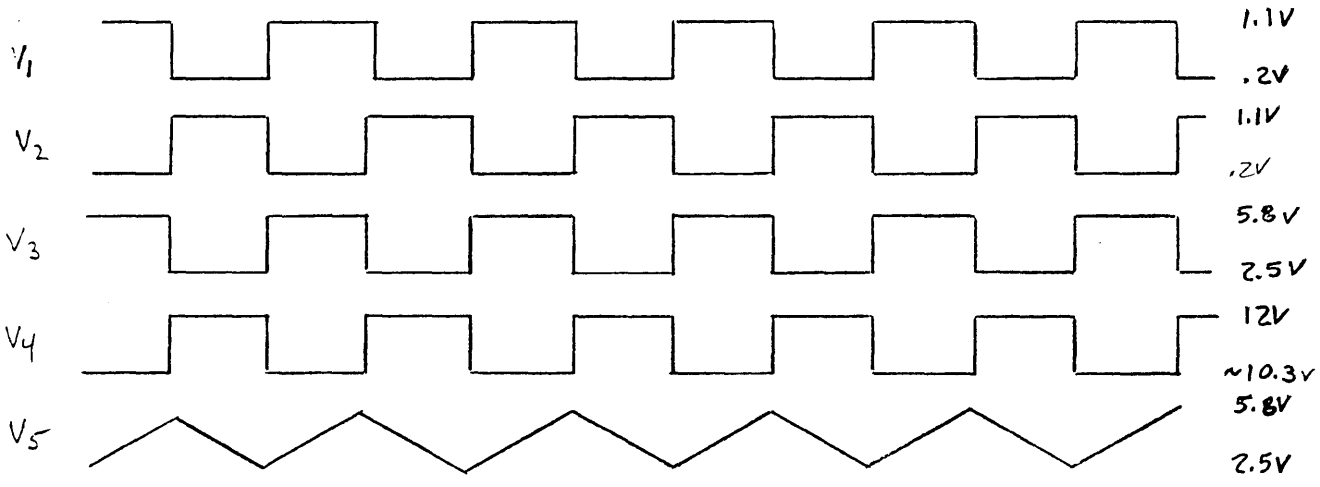
The VCO is a triangle wave generator normally at 500 KHz. The voltage on the base of Q3 is converted to a current by darlington Q3-Q4 and resistors R23 and VR2. The voltage across R23 and VR2 is two base emitter drops lower than the input voltage. The current through the resistors is directly proportional to the control voltage. That current also flows through the collector of the darlington. It is the control current supplying a current mirror made up of Q1, Q2, Q8, Q9, and resistors R43 and R44.

The comparator U12 can be in one of two states. The differential outputs can have pin 9 high and pin 11 low or vice-versa. The outputs are buffered by open collector inverters in U13. The two outputs connected to transistors are limited by the resistor bias networks (R18-21) to 1.1 volt excursions. The output of U13f is used to generate a square wave at the positive input of the comparator. The high level voltage of the square wave occurs when U13f's output is high and the voltage rises to CR3's zener voltage. When the output of U13f is low the square wave is at the low voltage of CR2's zener plus about .2 volts. In both cases the zeners are biased by R38.

If the triangle voltage is increasing, the voltage on the base of Q2 is higher then the voltage on the base of Q1. That will result in Q2 being on and Q1 being cut-off. All of the control current flows through Q9 and Q2 causing a voltage drop across R43 equal to the product of the control current and the resistance. The voltage on the base of Q9 is just one diode drop lower then the voltage across R43. That same voltage is on the base of Q8. The emitter of Q8 matches the voltage on the emitter of Q9, and therefore R44 has the same voltage across it as R43. Since R43 and R44 are the same value and share the same voltage, the control current is mirrored in Q8. With Q1 cut-off all of the current in Q8 flows into C21. That constant current causes a linear ramping of C21's voltage.

The voltage on C21 will continue until the comparator sees that it has reached the upper limit. That limit is set by the voltage of zener CR3. When the comparator changes states the base of Q1 is above the voltage on the base of Q2. In that mode Q1 is on and Q2 is cut-off. With Q2 cut-off no current flows through Q9, R43, R44 or Q8. The full control current flows through Q1. This time it is





				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 20 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

7830-006-L

supplied by C21, and the voltage there is a linearly decreasing ramp.

Once again the comparator is responsible for sensing the limit. With the comparator in this state pin 9 is high and the output of open collector U13f is low. The voltage on the comparator input is now set by zener CR2 whose voltage is lower then CR3. When the voltage reaches this lower limit the whole process begins again.

Each time the comparator changes the triangle from increasing to decreasing slope U2b is clocked. Its output is read clock (RCLK). RCLK changes states at each triangle peak. The frequency of RCLK is one half of the VCO frequency or nominally 250KHz.

If the voltage is increased on the base of Q3 the currents are higher, and the slope of the voltage on C21 is steeper. An increase in voltage at Q3's base leads to an increase in frequency. A decrease in voltage will cause a corresponding decrease in frequency.

3) Sampling section

The second part of the PLL is the sampling section. The triangle is buffered by darlington Q10 and Q11 so that the sampling activity will not disturb the VCO. CR5 and Q14 convert the triangle wave to a triangle current available at the the collector of Q14. This begins with the voltage on CR5. It is biased by R48. The voltage on the emitter of Q14 is .7 volts above that voltage. The upper end of R47 is the triangle voltage and the lower end is fixed at about three volts. A triangle wave current results.

Most of the time that current flows to ground through sampling gate U13c. Whenever sample goes high, the current flows into a second current mirror. CR4 is a biasing diode that assists in the turn off of the current at the end of the sample interval.

The current mirror made up of Q12, Q13, Q5, and Q6 uses the sampling current to either pump up or pump down the filter voltage to track the data.

If sample occurs while the triangle is ramping down the pulse is early. The frequency should be increased, so the filter voltage is increased by directing the sampling current

into the filter through Q12. The other three transistors in the mirror are cut-off.

If the pulse is late, the frequency of the VCO is high. The filter voltage is decreased by mirroring the sampling current out of the filter. The mirror has Q13, Q5, and Q6 on. R28 and R29 reflect equal current as in the other mirror. This decreases the filter voltage, and in turn the VCO frequency.

The further from the triangle trough the pulse occurs, the higher the sampled triangle current, and the more correction. The result is that the sampling pulses cause the VCO to change frequency in such a way as to center the triangle troughs on the sampling pulses. Once they are centered, small changes in the data stream frequency are tracked.

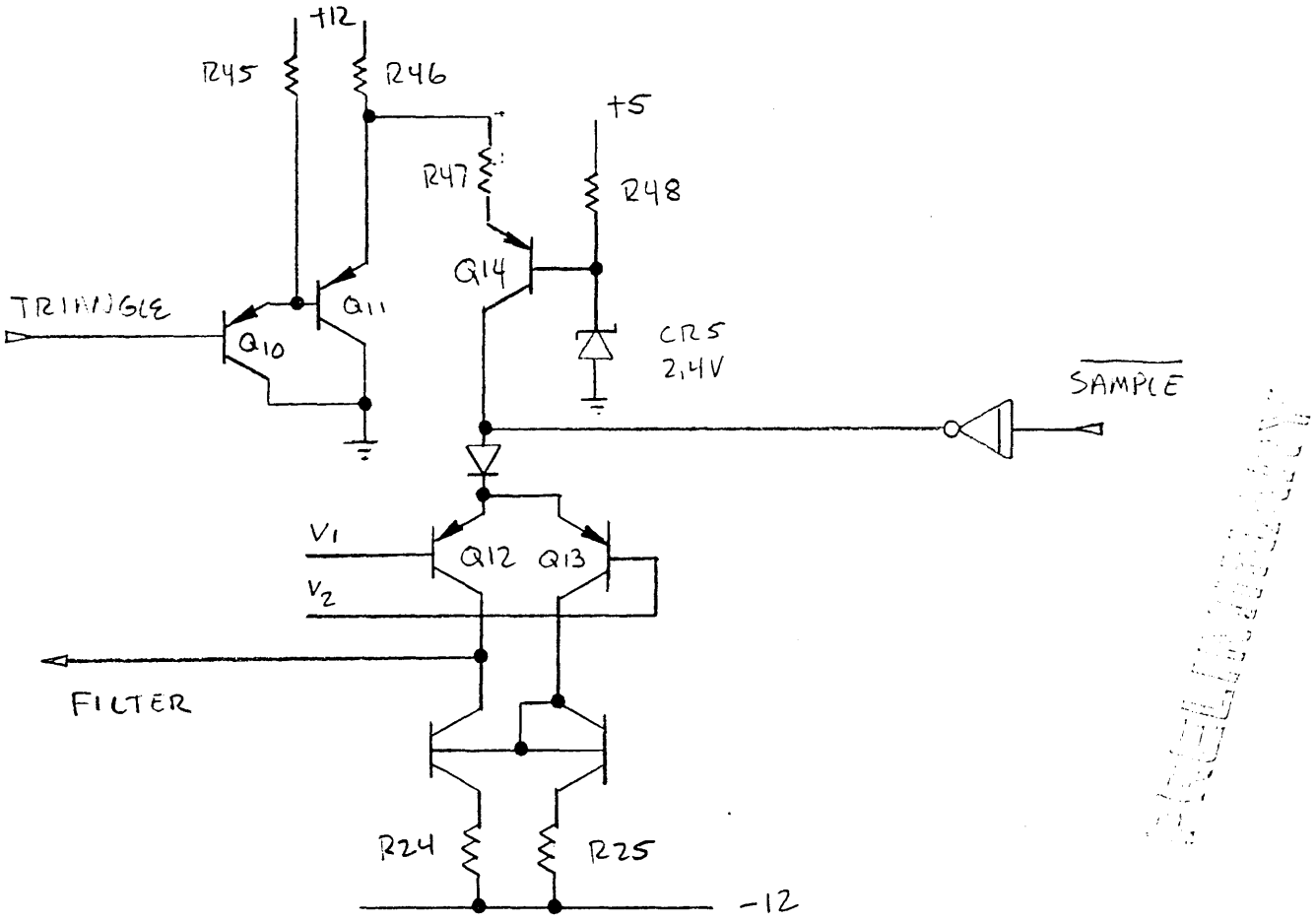


FIG. 8

				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 22 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

4) Filter

The filter is made up of C6, C7, and R22. The purpose of the filter is to slowly ajust the VCO control input in response to sampling pulses. The filter is required to average out bit shift variations and to mask some of the noise impulses. The measure of the quality of the filter is in the trade off between acquisition range and margin.

Acquisition range for the present filter design is nearly plus or minus 20% of the nominal data stream frequency. The margin performance of the PLL has been traded off slightly in favor of lock range, but it still compares favorably with all other designs tested.

5) Frequency clamp

Whenever the phase lock loop is not tracking data, it returns to a free run state. The job of bringing the frequency to the free run value is done by the frequency clamp. The circuit involves CR1, Q7, Q15, R49, R26, and R27.

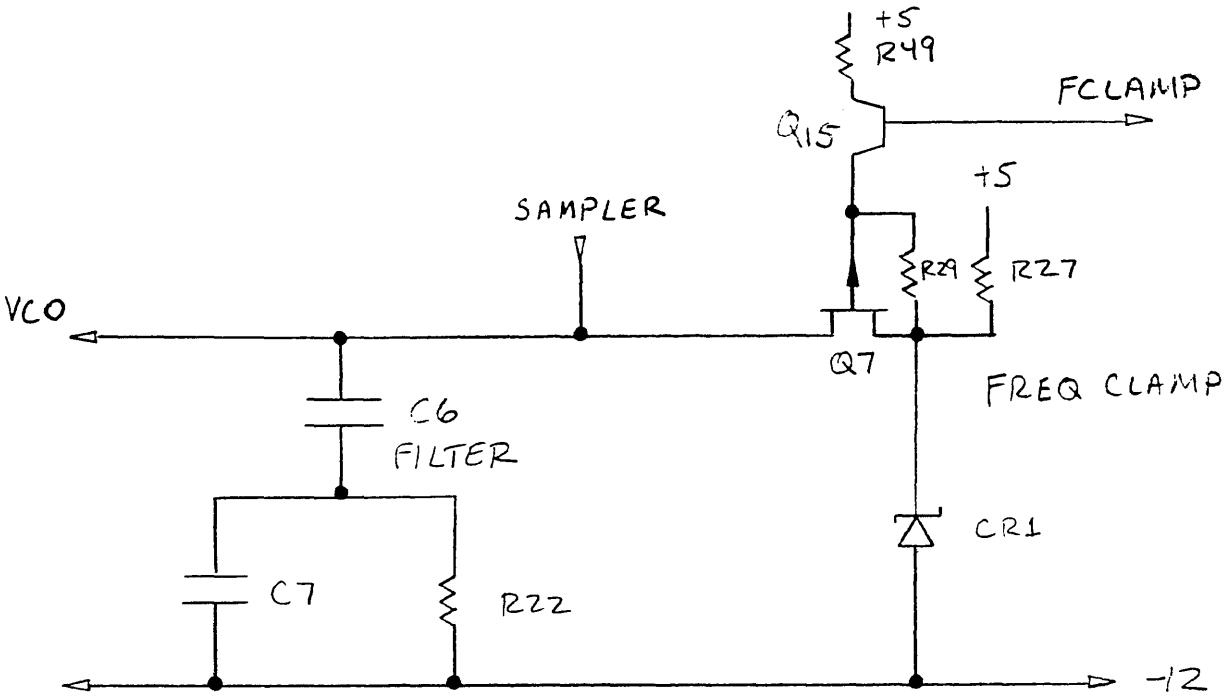
On a high level output from U13a, Q15 is cutoff. This means that no current flows through R26. The voltages of the gate and source of FET Q7 are equal. In that mode, the depletion mode FET connects the filter (C6) to the zener voltage on CR1. The voltage on CR1 is 5.6 volts above -12. That voltage appears across the filter, and in turn is the control voltage of the VCO.

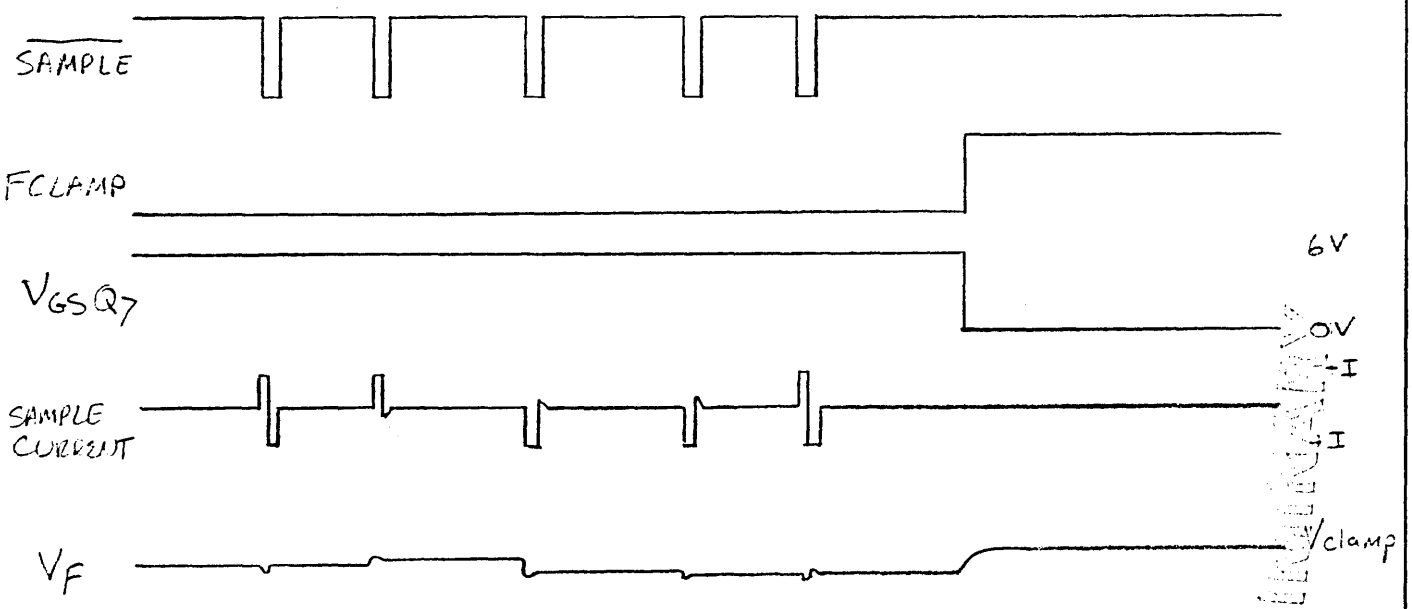
If the output of U13a is low, R49 has slighty more then 4 volts across it. The emitter current in Q15 is about 4ma. The collector voltage at Q15 will be near ground with only 2ma through R26. This means Q15 is saturated. The gate to source voltage of Q7 is then greater than 6 volts, and pinch off occurs.

The resistance of VR2 is adjusted with the circuit in the free run mode to yeild a VCO output frequency of 500 KHz. Then when the phase lock loop is ready to acquire lock, it always starts from that free run frequency.

6) Phase Clamp

Another feature of this phase lock loop is the phase clamp ability. Phase clamping is used to put the VCO output at a given point in its cycle. In this design, the triangle





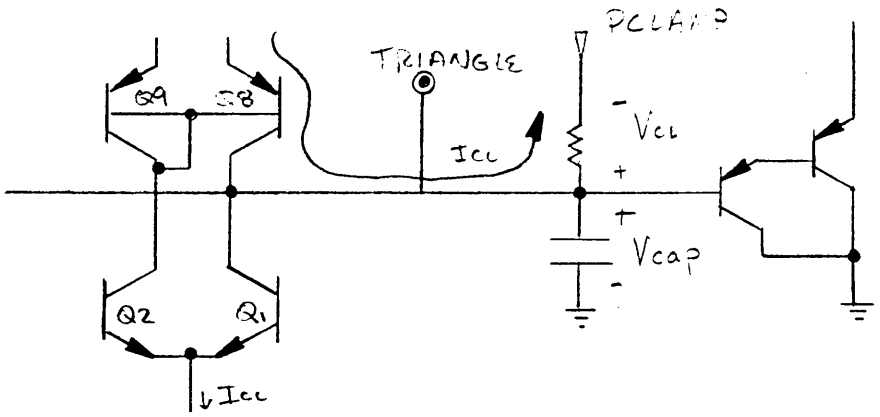
FILTER AND FREQ. CLAMP

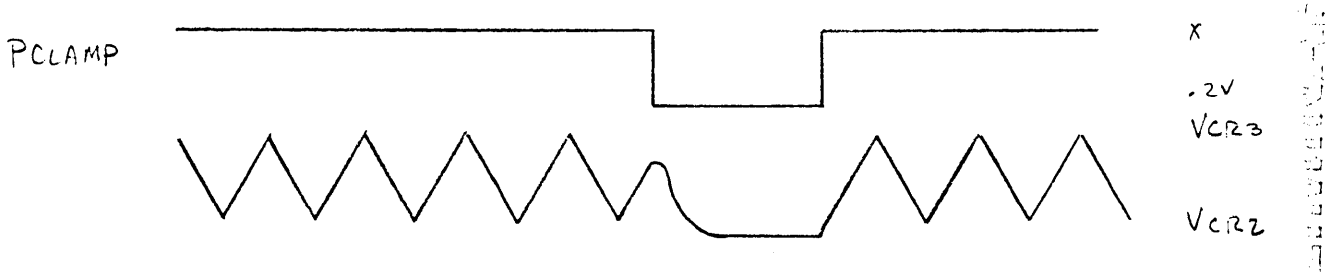
				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1931
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 24 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

wave is held at its minimum voltage until released. As discussed before that point in the cycle is where the read data pulses are to be locked to. By releasing on the first read data pulse from phase clamp, the phase lock loop has the advantage of only having to correct for frequency differences.

The benefit of phase clamp is that the probability of acquiring lock is improved. The speed at which the lockup occurs is also improved. This is because without phase clamp both phase and frequency must be brought in lock. That is diffucult enough to do that in the extreme case locking to harmonics of the actual data stream is possible.

The circuit element used to phase clamp is R42. When the output of U13b goes low, current flows out of the filter and into R42. No matter what state the comparator was in, eventually the voltage on C21 will go slightly below the lower trip point. At that time the comparator will always be mirroring current into C21. That current will flow through R42 seting up the clamp voltage. That is an equilibrium condition that will exist until phase clamp is released.





				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 25 OF
	REVISIONS			SUPERSEDES	DWG NO A=-0926-66562-9

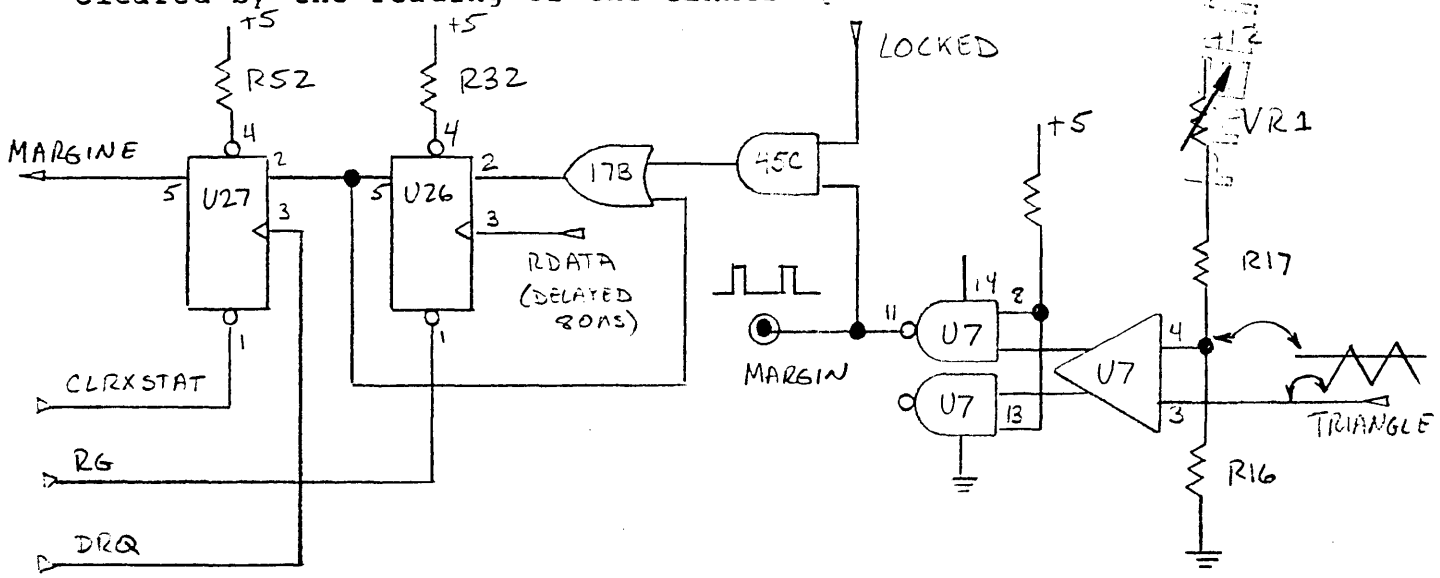
7) Margin output

Another section of hardware in the analog section creates the signal margin. The purpose of margin is to define an area of the read clock signals within which no transitions should fall. This signal is in no way related to the actual reading of the data stream by the FDC. Instead the signal is used by the host processor during initialize operations to check media quality.

The elements involved are VR1, R16, R17, and U7. The triangle wave from the VCO is fed into the positive input of U7 A voltage is set up on the negative input by adjusting VR2. The voltage is adjusted slightly below the triangle wave peak. For a small time before and after the peak, margin is true.

The margin output is anded with the "locked" signal by gate U45c. The margin pulses are then applied to the combination of U17b and U21a. Each time a read data pulse occurs after "locked" is true the margin line is sampled. If the edge of read data falls in the range too close to a RCLK edge U21a will clock high and U17b will latch it. The circuit is only cleared by RG going low at the end of the header or sector.

If the output of U21a is high during a sector that we are actually reading, then the next DRQ output of the FDC will clock margin errror latch U27b to true. The output of margin error is available through the extended command register. It can only cleared by the reading of the CLRXTS special address.



				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 26 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

LOOP MANAGEMENT

Now that the functions of the analog section have been described it should be obvious that some of the control signals needed to lock and unlock are going to be complex. The loop management section provides all of these siganls, and also creates the read data sent to the FDC. The sections involved are the delay line, the (sync field) discriminator, the lockup controller, and the phase clamper.

1) Delay line

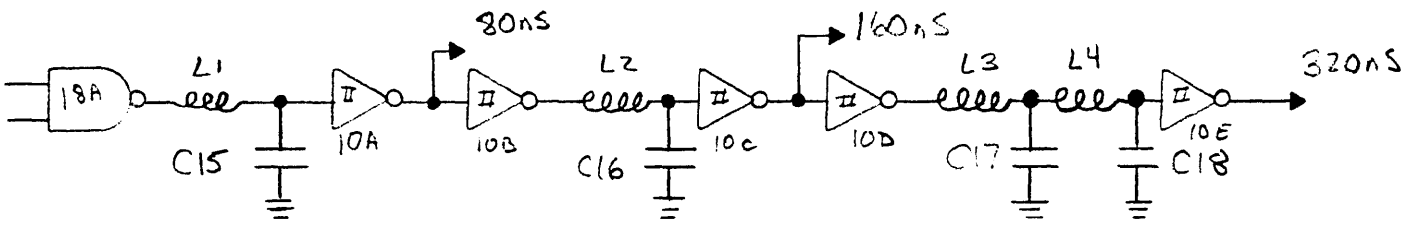
The delay line is made up of L1-4, C1-4, U10, U4a, U6d, and U18a. The read data pulses are applied to U18a directly from the drive interface. HLT is anded with the pulses so that only valid read data is fed to the delay line. The 1us wide pulses go through the three sections of the delay line.

The first section of the delay line is a delay of 80ns. The output of the first section (U10) is the start signal for processed read data. The second section is another 80ns delay. The output of the second section (U10) is used to end sample. The final section delays another 160ns. The final output (U10) stops processed read data.

Gate U4a creates the sample signal. Sample is a 160ns wide pulse starting with the raw read data edge propagates to U18a and ends when the edge appears at U10. The sample pulses are also gated with "track".

Gate U6d creates the 240ns read data pulses sent to the FDC. They are started with the output of U10, and are centered in the sampling pulses just described. When the raw data edge reaches the processed read data pulse is terminated.

Some otner signals are taken from the delay line to be used by other sections of the circuit. The line leaving U10a is a bit clock for the discriminator. A tap at U10b is delayed read data for the margin error detector. Here the delay is to make up for comparator (U7) response time.



				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 27 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

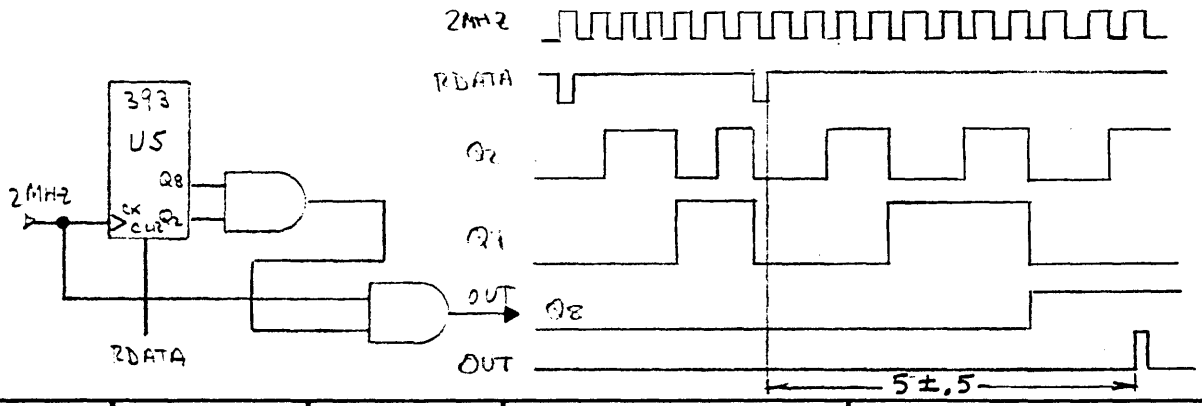
2) Discriminator

The discriminator nas the task of finding sync fields for the pnase lock loop to lock to. Every section of read data that can be independently read is preceded by a sync field. It is the part of the data stream that is intended for lock up. The discriminator is half of U5, U18b, and U18d. It will pulse when not in a sync field, and stop pulsing in a sync feild.

U5 pin 1 is connected to a 2 MHz clock. The clear for U5a (pin 2) is connected to processed read data inverted by U35f. In between read data pulses the counter will count up. If the counter reaches a count of ten, a pulse will appear at U18d's output with clock high. The clock qualifier is required since the counters are ripple counters and false outputs would occur otherwise.

If the read pulses are more than 5us apart, an output pulse is possible. Since the clock is asynchronous with respect to read data there is variability in the operation depending on the phase relationship of the signals. If the pulses are 5.5us apart an output pulse is guaranteed. This means that in areas with only 4us spaced pulses the counter is always cleared before a count of 10 is reached. The output of the discriminator is used to clear out the lock up controller whenever a non sync-field spacing occurs in the data stream.

The shift register U28 delays the discriminator output for four read data transitions before it is applied to the counters in the loop manager. This is done because the RG (read gate) output of the FDC can be delayed 16uS after the FDC finds the last byte of zeros. Without this register delay, there is a possibility of improper operation if a read address command is given to close to the end of a sync field.



				MODEL 9836A	STK NO
				THEORY OF OPERATION	
				BY Ron Rogers/JR	DATE October 13, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 28 OF
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-9

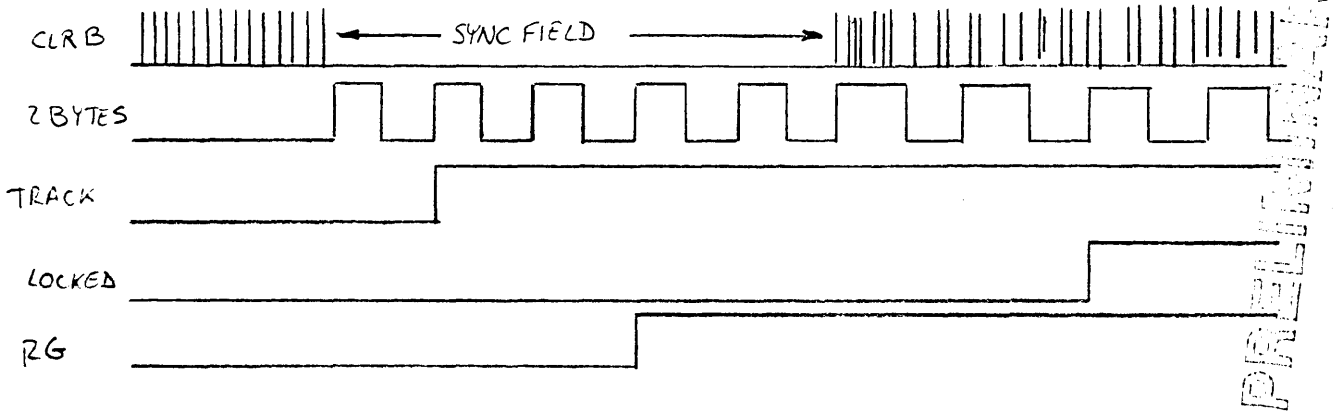
3) Lock up controller

The lock up controller is responsible for the generation of the track and locked signals. It responds to the inputs from the data stream, the discriminator and the read gate (RG) from the FDC. The track signal switches the analog section between its free run and tracking mode. The locked signal informs the margin error circuit of when the phase lock loop is locked to the data stream.

The components in the circuit are U5b, U6a-b, U10f, and U11. RG from the FDC informs the circuit that the read data stream has been recognized by the FDC to be a sync field, and that the controller is now looking at the read data. RG is inverted by U6a and gated in U6b with the discriminator pulses so that whenever RG is asserted the discriminator is ignored.

The output pulses from U6b thus qualified are used to clear out the lock up controller. The first part of the controller is U5b. It counts read data transitions and its output clocks U11 once each two bytes. A count of 16 transitions will always translate to two bytes in a sync field since there is exactly one transititon per bit.

U11 is a shift register with the inputs tied high. For each two bytes of a sync field, the register shifts one position. When four bytes of sync have been counted pin 4 (output 2) goes high. This is the signal "track", telling the phase lock loop to start tracking data. Lock is also used to gate the sample pulses through gate U4a, so its appearance also starts sampling activity. If the operation of lockup is completed and RG is asserted, pin 13 (output 8) will signal "locked" to the margin error circuit.



LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A	STK NO
THEORY OF OPERATION	
BY Ron Rogers/JR	DATE October 13, 1981
APPD	SHEET NO 29 OF
SUPERSEDES	DWG NO A-09826-66562-9

4) Phase clamp

The process of phase clamp was described in the analog section. The VCO is stopped and held until the next data transition in order to start the PLL in phase with the data. U2a and U18c are the parts involved in that activity. U2a is cleared whenever not locked. When the signal track comes true it appears on the input of U2a and at gate U18c. The output of gate U18c goes low and phase clamps the triangle wave. The next transition clocks U2a removing the Q' output from U18c. This releases the triangle wave and the phase lock loop is free to track the data.

5) Miscellaneous

There are a few parts in this area of tne schematic not yet described. They are related to read recovery and yet are not strongly related to any of the above sections.

U35c and U17c provide for the use of the VFOE' output of the FDC. That output is provided for use with certain phase lock loops. It allows for tracking of data through gaps which is useful in executing read track commands. Because of the high gain bandwidth of the pnase lock loop on this board, its exclusive use was ruled out. If VFOE is required for some service operation, the VFOE' test point can be jumpered to the LOCK test pin.

TEST POINT SUMMARY

The test points provided on this board are to assist in the checking of the operation of both the floppy control board and the drive. With the exception of LOCK, all test points are outputs. The drive capacity of all test points is one low power schottky load, do not exceed that without careful consideration.

LOCK

The LOCK test point is an input to the phase lock loop lock up controller. When low, it forces lock up (or prevents unlock) of the phase lock loop. It is used in conjunction with the VFOE test point to allow full track read operations. In that case, a jumper between the two test points enables enables this feature. With the jumper installed, normal board operation will continue. Some degradation in long term transfer rate will occur due to harmonic locking.

VFOE

The VFOE test point is an unbuffered connection to the VFOE output of the FDC chip. This pin should be used with extreme caution since a direct connection to the chip makes it susceptible to static discharge. The output may be useful in determining if the FDC is deriving data from the read data stream. In general, the RG pin on the FDC is more useful.

TRIGGER

This pin is for use in signature analysis. Addressed at $445800 this pin can be used for start/stop.

DRQ

The data request test point is a buffered output of the FDC signal. If data requests are issued, data is being transferred on the internal bus. This means that the FDC is finding valid record headers for the sector it is attempting to read. Transfer of the data on the internal bus will occur even if a CRC error is found, since the error will not be realized until the end of the sector.

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A	STK NO
THEORY OF OPERATION	
BY Ron Rogers/JR	DATE October 13, 1981
APPD	SHEET NO 31 OF
SUPERSEDES	DWG NO A-09826-66562-9

IP

The index pulse test point is useful in checking for index pulses from the drive. If the moter is on, media is installed, and the door is closed, index pulses should occur every 200 msecs. The index pulse rate can be used to check motor speed. Tnat is an adjustment on the drive servo board.

RDY

Ready is the output of the ready one-shot. It indicates that the motor is on and index pulses are coming from the drive. It should be either high or low, never pulsing. If pulsing, a problem occurs with the one-shot or the motor speed is grossly out of adjustment.

WG

This test point is a buffered copy of the write gate signal from the FDC. This signal should be high when a write occurs to the drive.

RDATA

Read data is a complex signal that can check some of tne drive function. If observed on a lus per div scale, it should have pulses spaced at 4, 6, and 8 us. Tne pulses will nave a lot of jitter, this is normal. This test point is useful for higher level testing of tne floppy controller board, and therefore is available at the test connector J3.

2MHZ

This test point is the 2 Mhz clock which drives the board. It is divided down from the 10Mhz input from the system. This test point is primarily to check if the clock exists on tne board and as a clock for signature analysis.

TRIANGLE

Triangle is an intermediate signal in the generation of the read clock. It should be a triangle wave with two equal sloped portions. If unequal or curved and distorted sections are seen, there is trouble in the voltage controlled oscillator.

FILTER

Filter is the input to the VCO. The filter voltage is actually between -12 and the filter test point. So if measured to ground, you should remember the more negative the voltage the lower the VCO frequency. The voltage should be roughly -6.4 volts when the phase lock loop is tracking data and nearly that at all other times.

MARGIN

MARGIN is the output of the margin generating circuit. It should be adjusted to 200 nsecs when the phase lock loop is in the free run mode. It is also available at the test connector J3.

RCLK

Read clock is the output of the VCO section. It should be adjusted to 250Khz when the phase lock loop is in the free run mode. It is also available at the test connector J3.

WDATA

WDATA is the write data signal to the drive after pre-comp. It will show the proper operation of the pre-comp circuitry. This should be observed on the 1us per div sweep. The pulses will be spaced at precise 4, 6, and 8us intervals with subgroups of pulses at the pre-comp level around the large groups.

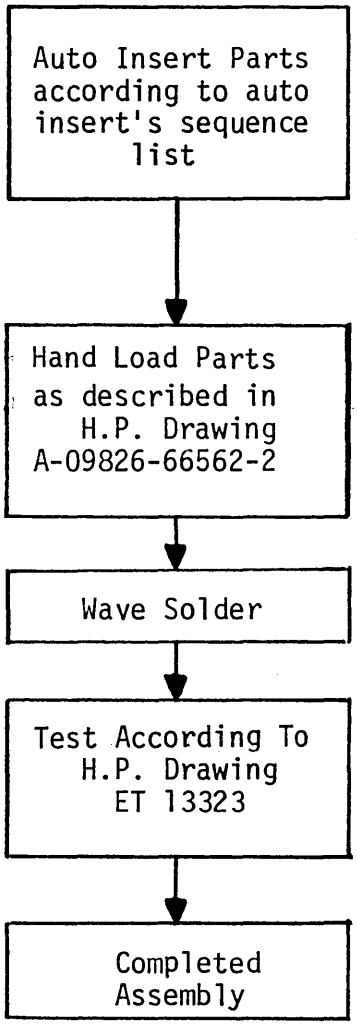
STEP

This testpoint is a buffered duplicate of the control signal STEP. When the drive is told to restore, seek, or any other command that requires the head to move in or out, pulses will be seen at this point. They should be 6 msecs apart for all operations but restore where they will be 20 msecs apart.

HEWLETT-PACKARD CO.

ASSEMBLY AND TEST FLOW CHART

09826-66562, FLOPPY CONTROL BOARD



PRELIMINARY

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A	STK NO
ASSEMBLY AND TEST FLOW CHART	
BY Jon Rubinstein	DATE October 2, 1981
APPD	SHEET NO 1 OF 1
SUPERSEDES	DWG NO A-09826-66562-1

7830-006-L

HEWLETT-PACKARD CO.

ASSEMBLY PROCEDURE

09826-66562, FLOPPY CONTROL BOARD

I. PURPOSE:

This document establishes a standard procedure for assembling the 09826-66562 P.C. assemblies.

II. AUTO INSERTION:

Auto-insert in accordance with auto-insert list.

III. HAND INSERTION:

Insert parts according to the following chart:

Part #	Quantity	Description	Location
0140-0198	4	200pf Capacitor	C15-C18
0160-2204	1	100pf Capacitor	C7
1853-0036	8	2N3906 Transistor	Q8-Q15
1854-0215	6	2N3904 Transistor	Q1-Q6
1855-0082	1	JFET	Q7
1990-0654	1	LED	LED1
2100-3351	2	Variable Resistor	VR1, VR2
1251-4510	1	6 Pin Conn	J3
1251-5615	1	34 Pin Conn	J4
09826-61661	1	Floppy Ribbon Cable	J2

NOTES:

1. Install LED1 with polarity markers toward the bottom of the board.
2. Install J3 with the connector pins toward the top of the board.

IV. FINAL ASSEMBLY:

After wave soldering, clean up the board and inspect for solder shorts, broken or improperly soldered components, or any other defects. Make any necessary repairs. Install blue PC board extractor (4040-0754) in the top left corner and red PC board extractor (4040-0750) in the top right corner.

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A	STK NO
ASSEMBLY PROCEDURE	
BY Jon Rubinstein	DATE October 2, 1981
APPD	SHEET NO 1 OF 1
SUPERSEDES	DWG NO A-09826-66562-2

7830-006-L

HEWLETT-PACKARD CO.

TEST PROCEDURE

09826-66562, FLOPPY CONTROL BOARD

I. PURPOSE:

This document establishes the method to be followed for verifying proper operation of the 09826-66562 Floppy Control Board.

II. TESTING REQUIRED:

All assemblies are to be tested in accordance with HP Drawing ET 13323.

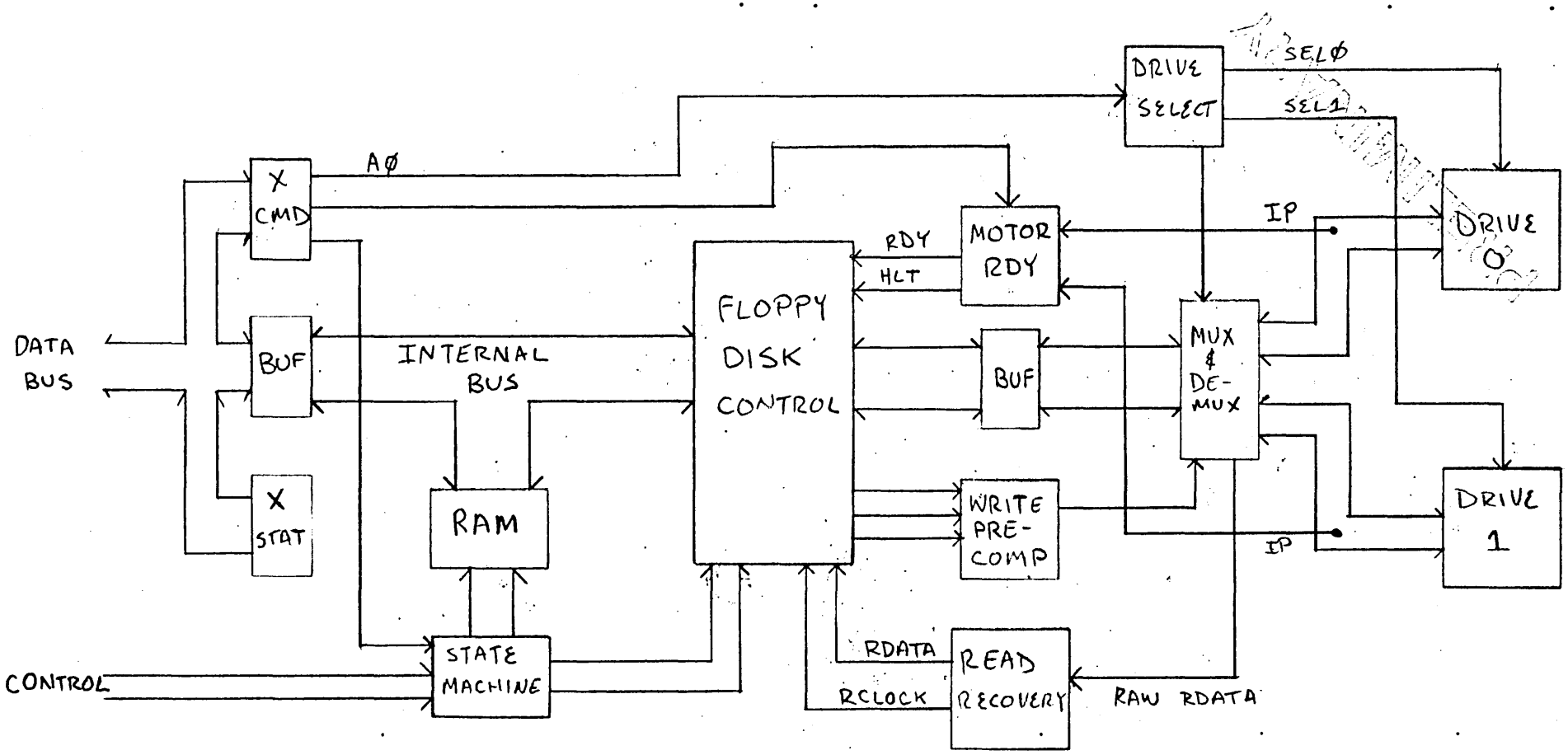
				MODEL 9836A	STK NO
				TEST PROCEDURE	
				BY Jon Rubinstein	DATE October 2, 1981
LTR	PC NO	APPROVED	DATE	APPD	SHEET NO 1 OF 1
	REVISIONS			SUPERSEDES	DWG NO A-09826-66562-3

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A-09826-66562-6

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY J.R. DATE 10/1/81

ENGINEER JON RUBINSTEIN

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE BLOCK DIAGRAM

NEXT ASSEMBLY

FINISH SCALE

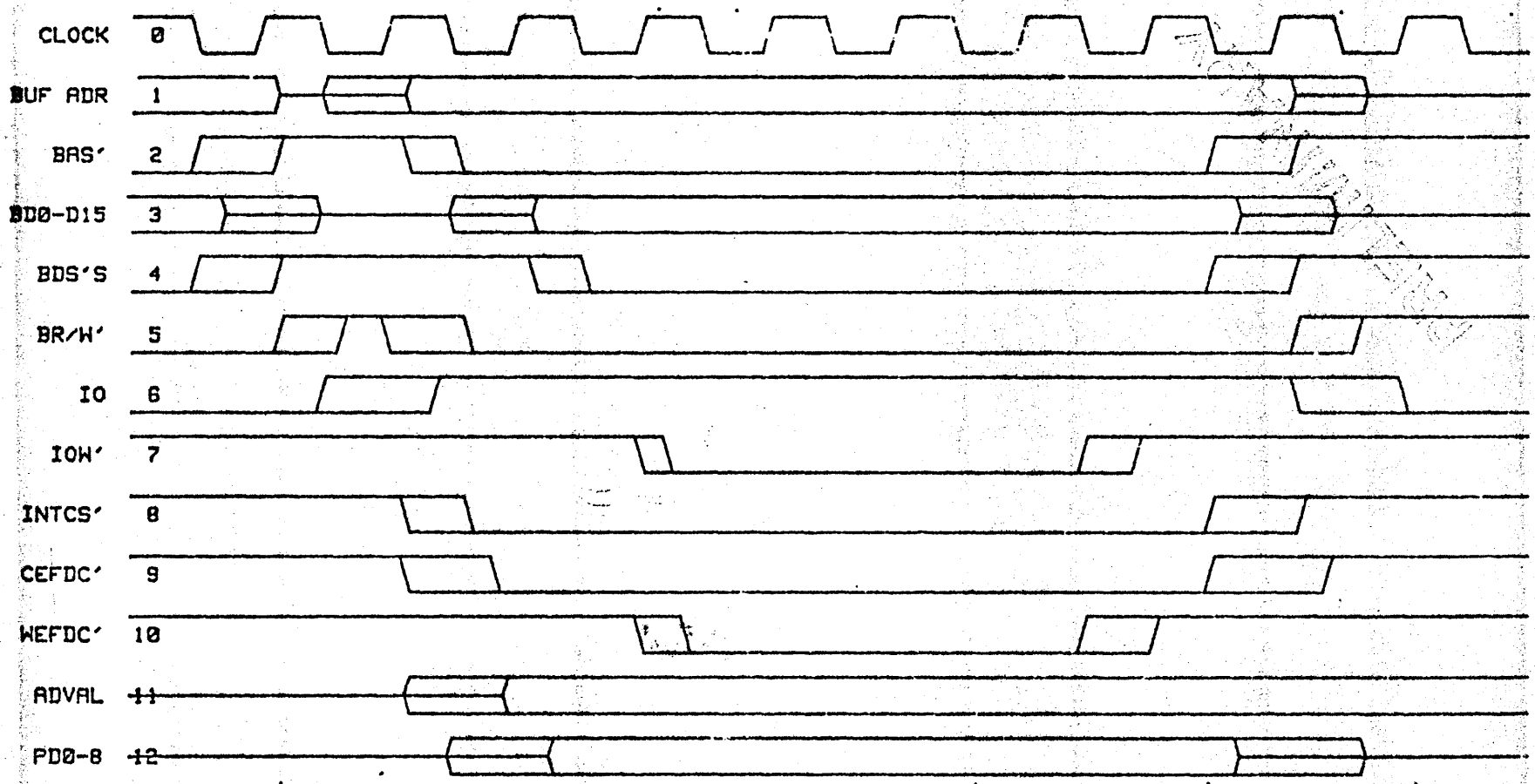
HEWLETT hp PACKARD

PART NUMBER A-09826-66562-6

ENGINEERING RESPONSIBILITY ▨ SEPIA ▨

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY 9872A | DATE

ENGINEER Ron Rogers | 6 NOV 80

RELEASE TO PROD. | 11-17-80

SUPERSEDES DWG.

TITLE: TIMING (WRITE TO F.D.C.)

NEXT ASSEMBLY

FINISH | SCALE

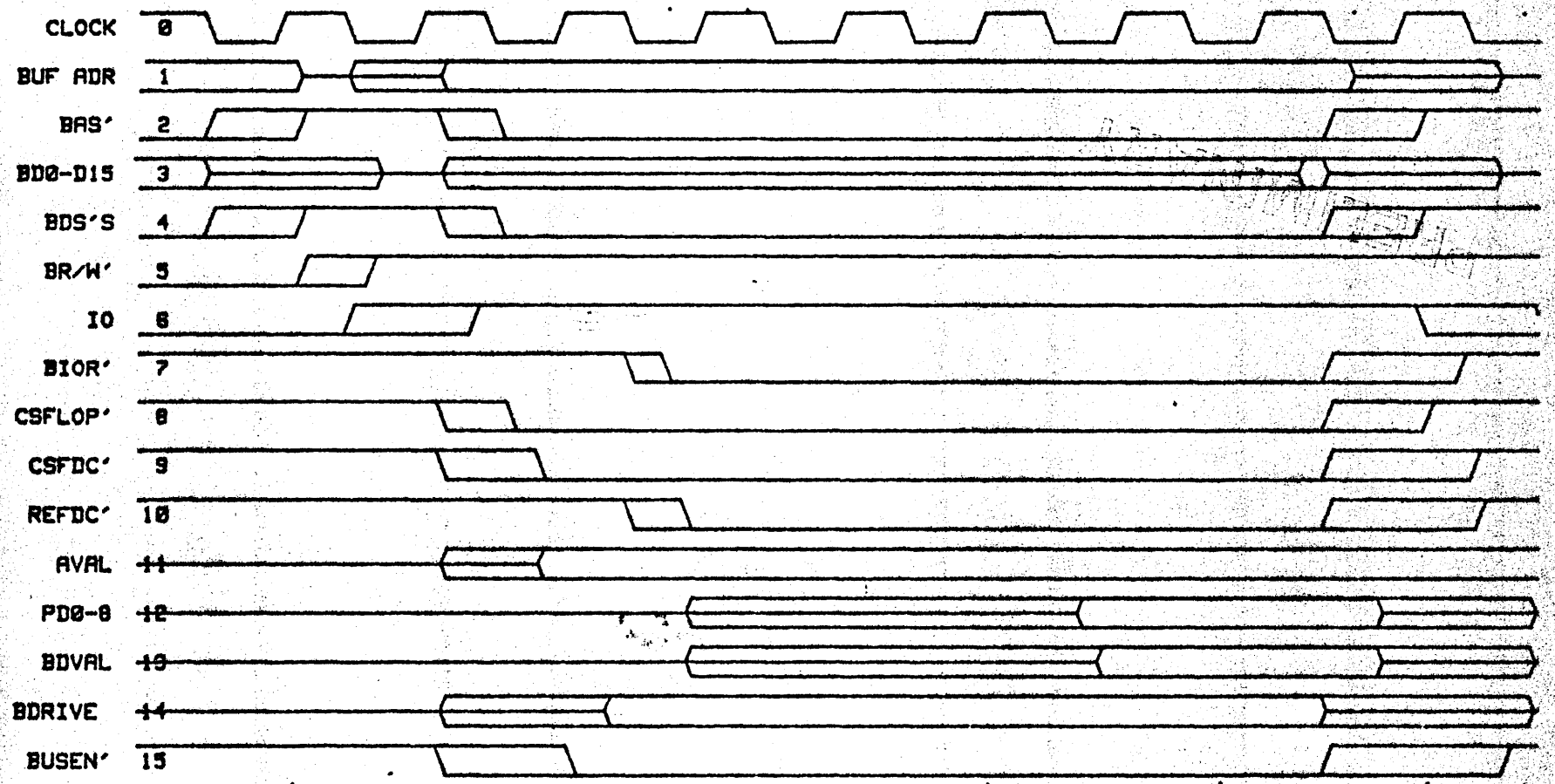
HEWLETT PACKARD

PART NUMBER A - 09826-66562-7

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
OMIT OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY 9872A | DATE

ENGINEER Ron Rogers | 6 NOV 80

RELEASE TO PROD. | 11-17-80

MANUFACTURING CODE

TITLE: TIMING (READ OF F.D.C.)

NEXT ASSEMBLY

MODEL | SCALE

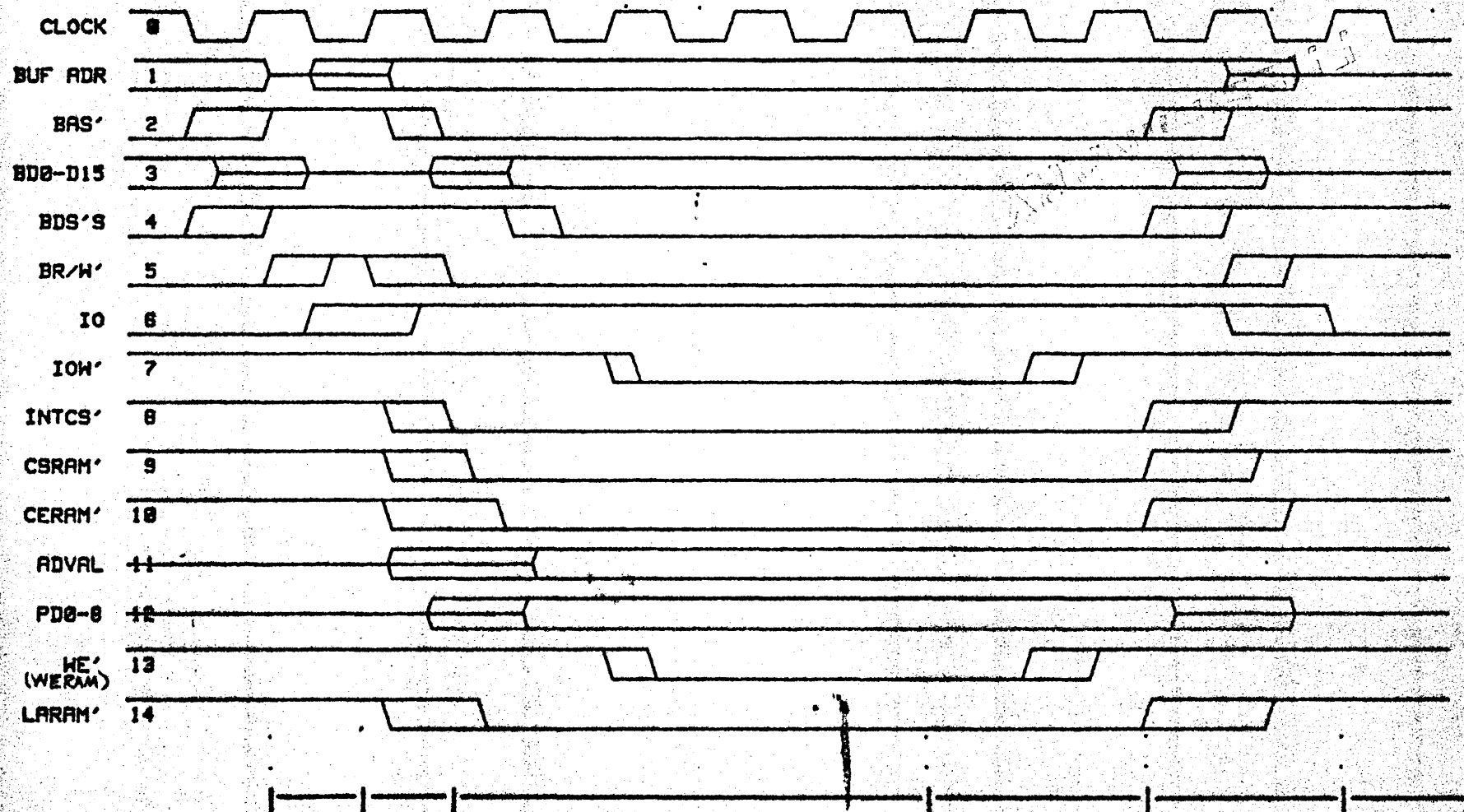
HEWLETT PACKARD

PART NUMBER 09826-66562-7

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.02 inch
XX.X ± 0.2 mm or ± 0.1 inch
BREAK OUT ONE XX AND ONE XX.X
PER COMP. STD. 000

DRAWN BY: 9872A — DATE:

ENGINEER: Ron Rogers — 6 NOV 80

APPROVED FOR RELEASE: 11-17-80

TITLE: TIMING (WRITE TO RAM)

NEXT ASSEMBLY

FINISH — MATERIAL

HEWLETT PACKARD

PART NUMBER: A - 09826-66562-7

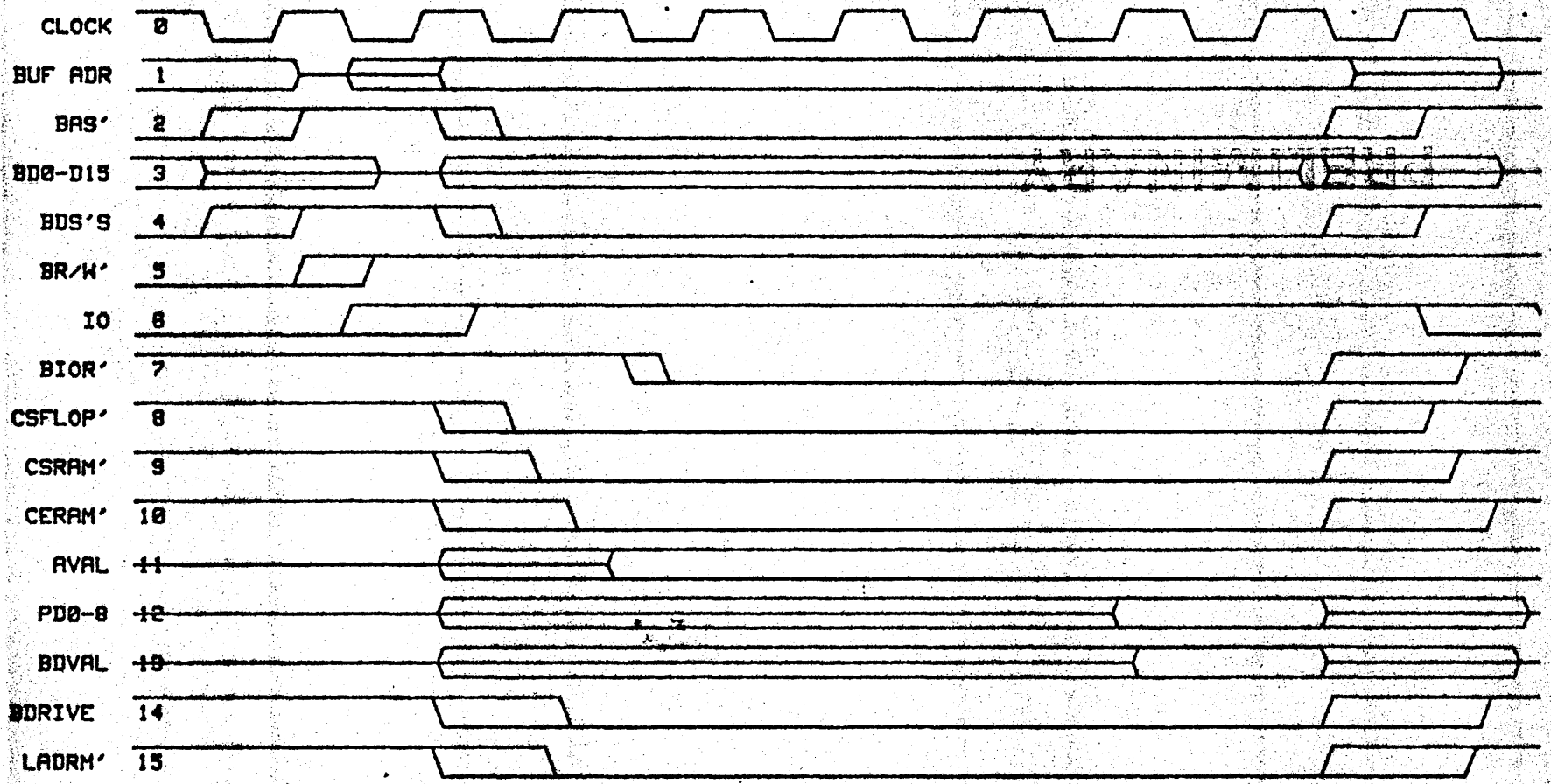
SHEET 3 OF 6

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	35	38	43
45	48	51	53									40		

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 905

DO NOT SCALE THIS DRAWING

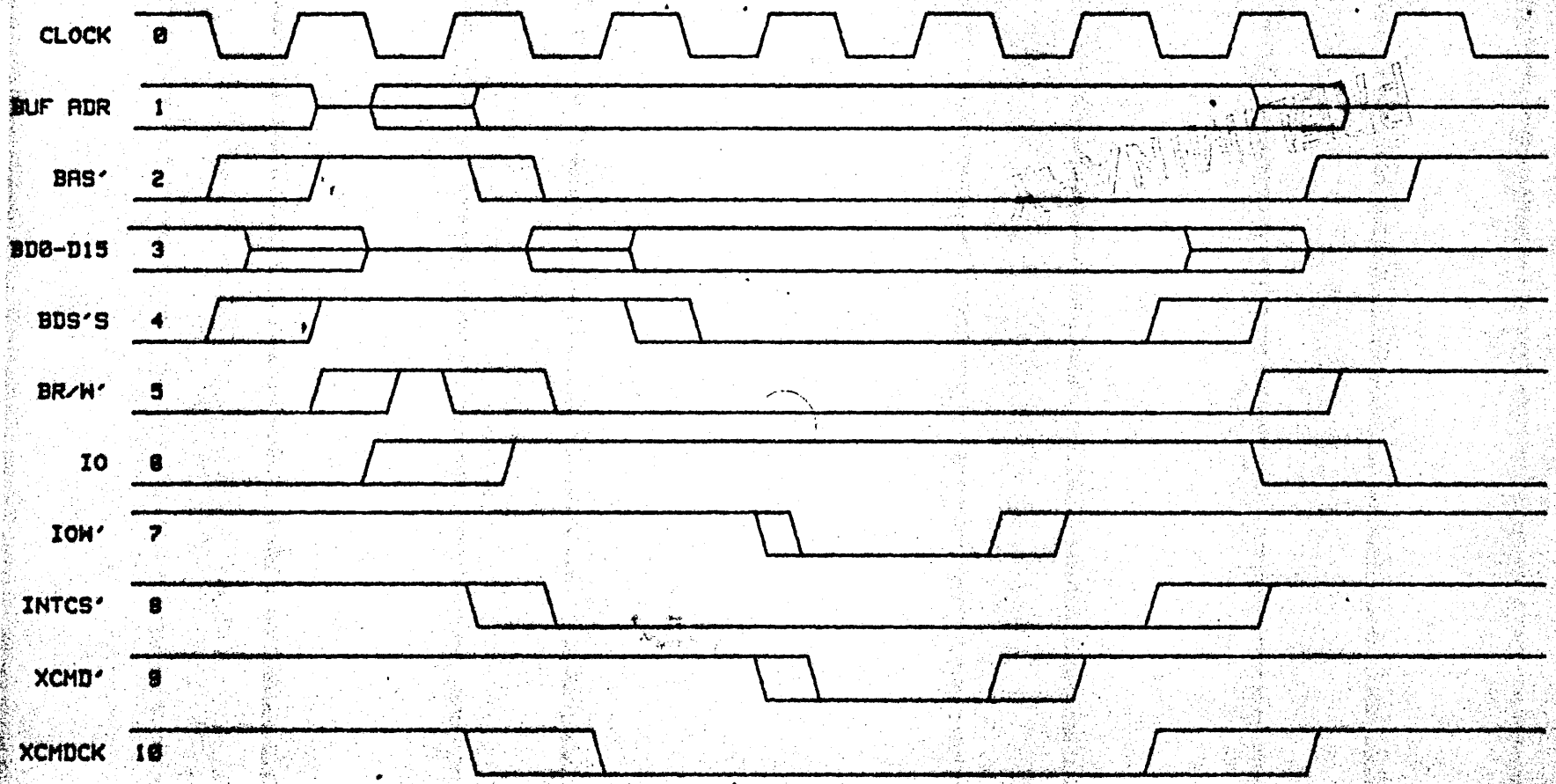
DRAWN BY: 9872A	DATE	TITLE: TIMING (READ OF RAM)	HEWLETT PACKARD
ENGINEER: Ron Rogers	6 NOV 80		
RELEASE TO PROD.	11-17-80	NEXT ASSEMBLY	PART NUMBER: A - 09826-66562-7

PRINTED ON [illegible] CLEARPRINT

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.8 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
HP CORP. STD. 008

DO NOT SCALE THIS DRAWING

DRAWN BY: 9872A	DATE
ENGINEER: Ron Rogers	6 NOV 80
RELEASE TO PROD.	11-17-80
REFERENCE DWG.	

TITLE: TIMING (WRITE XCMD)

NEXT ASSEMBLY

FINISH SCALE

HEWLETT PACKARD

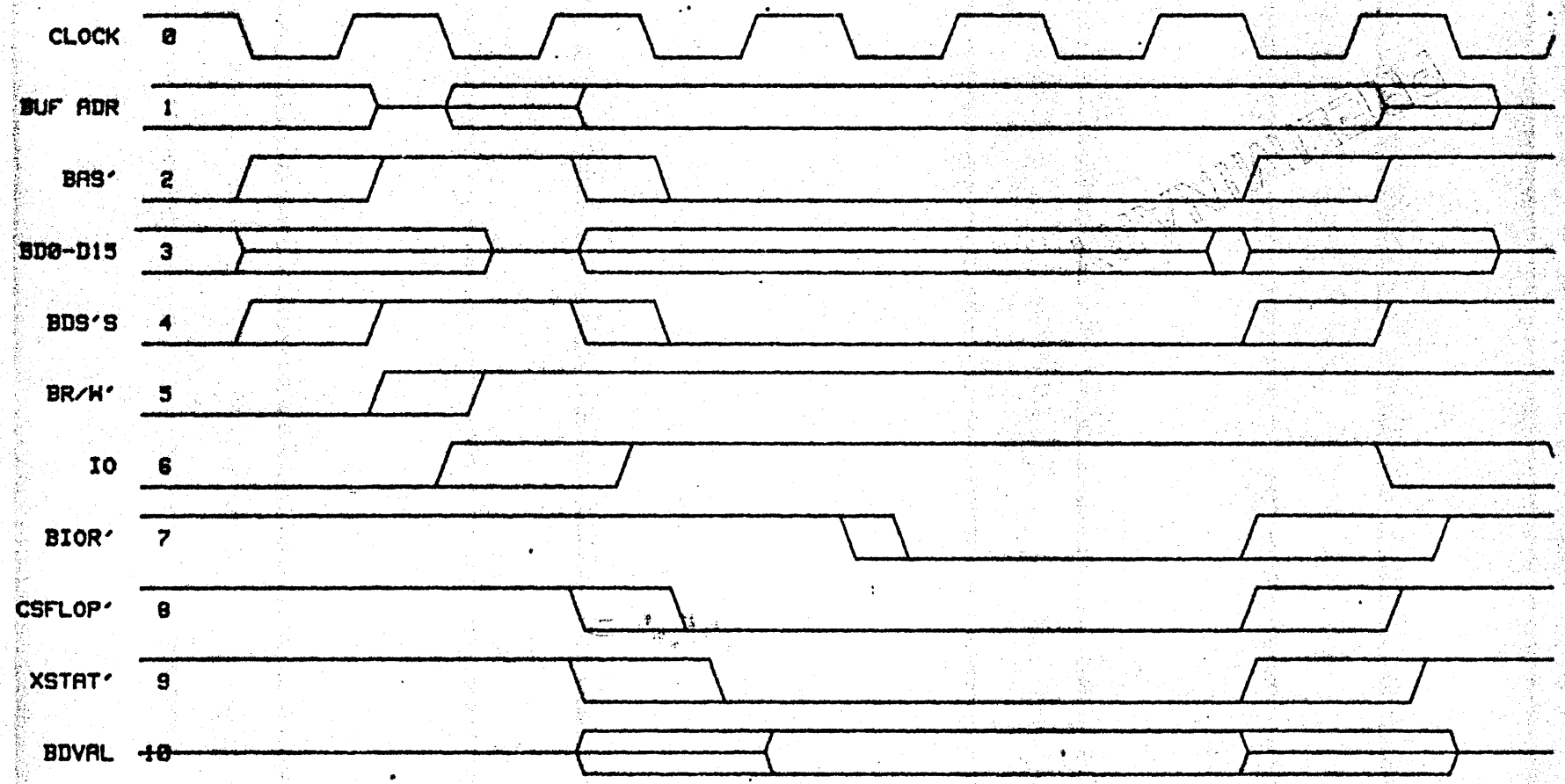
PART NUMBER A - 09826-66562-7

SHEET 5 OF 10

ENGINEERING RESPONSIBILITY ☑ SEPIA ☑

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 008

DO NOT SCALE THIS DRAWING

DRAWN BY: 9872A	DATE:
ENGINEER: Ron Rogers	DATE: 6 NOV 80
RELEASE TO PROD.	DATE: 11-17-80
PROJECT ENG.	

TITLE: TIMING (READ XSTAT)

NEXT ASSEMBLY

FINISH SCALE

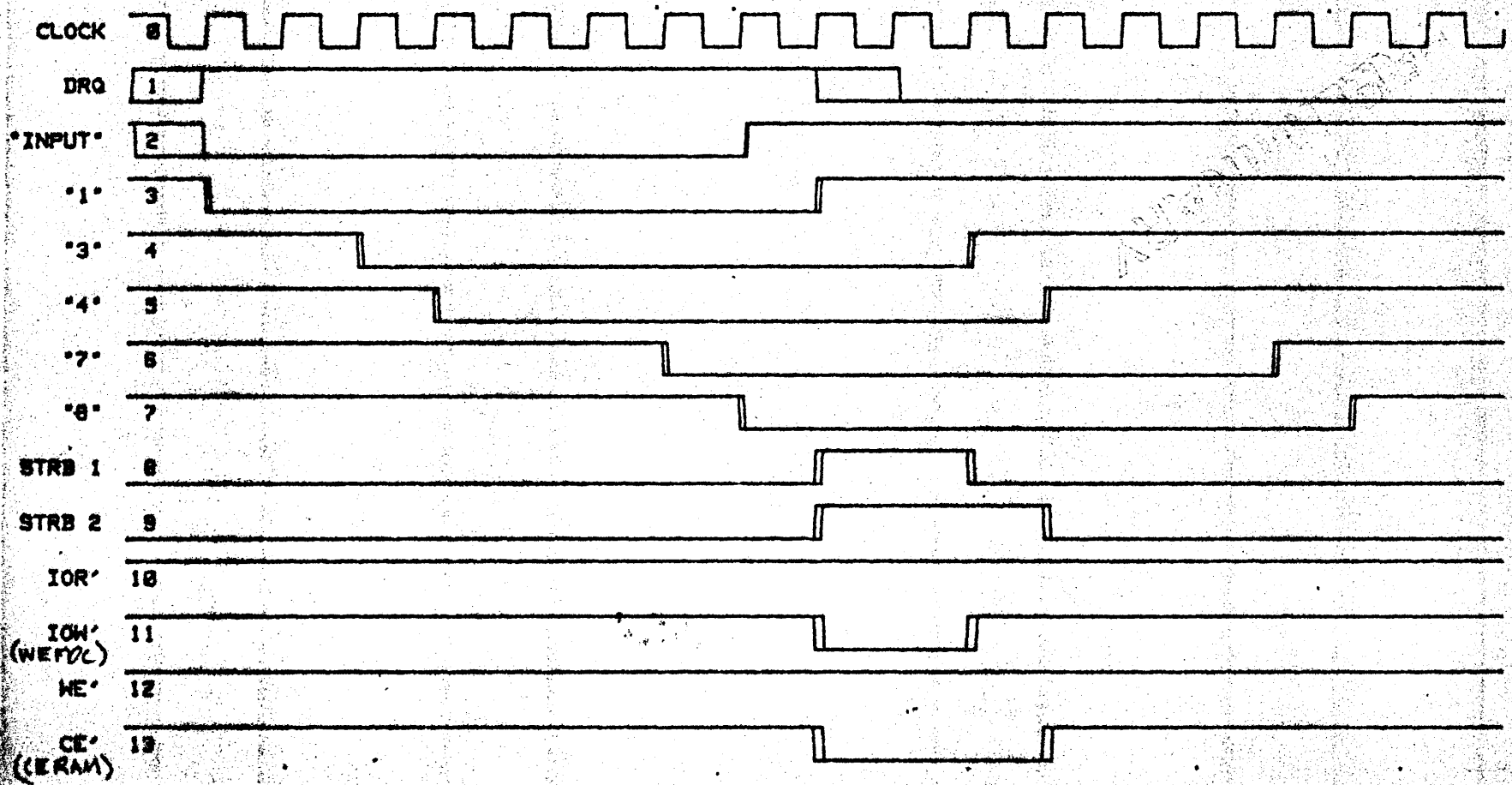
HEWLETT PACKARD

PART NUMBER: A - 09826-66562-7

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[signature]	11-17-80



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.01 inch
XX.X ± 0.2 mm or ± 0.1 deg
STRIKE OUT ONE XX AND ONE XX.X
PER CORP. STD. 008

DO NOT SCALE THIS DRAWING

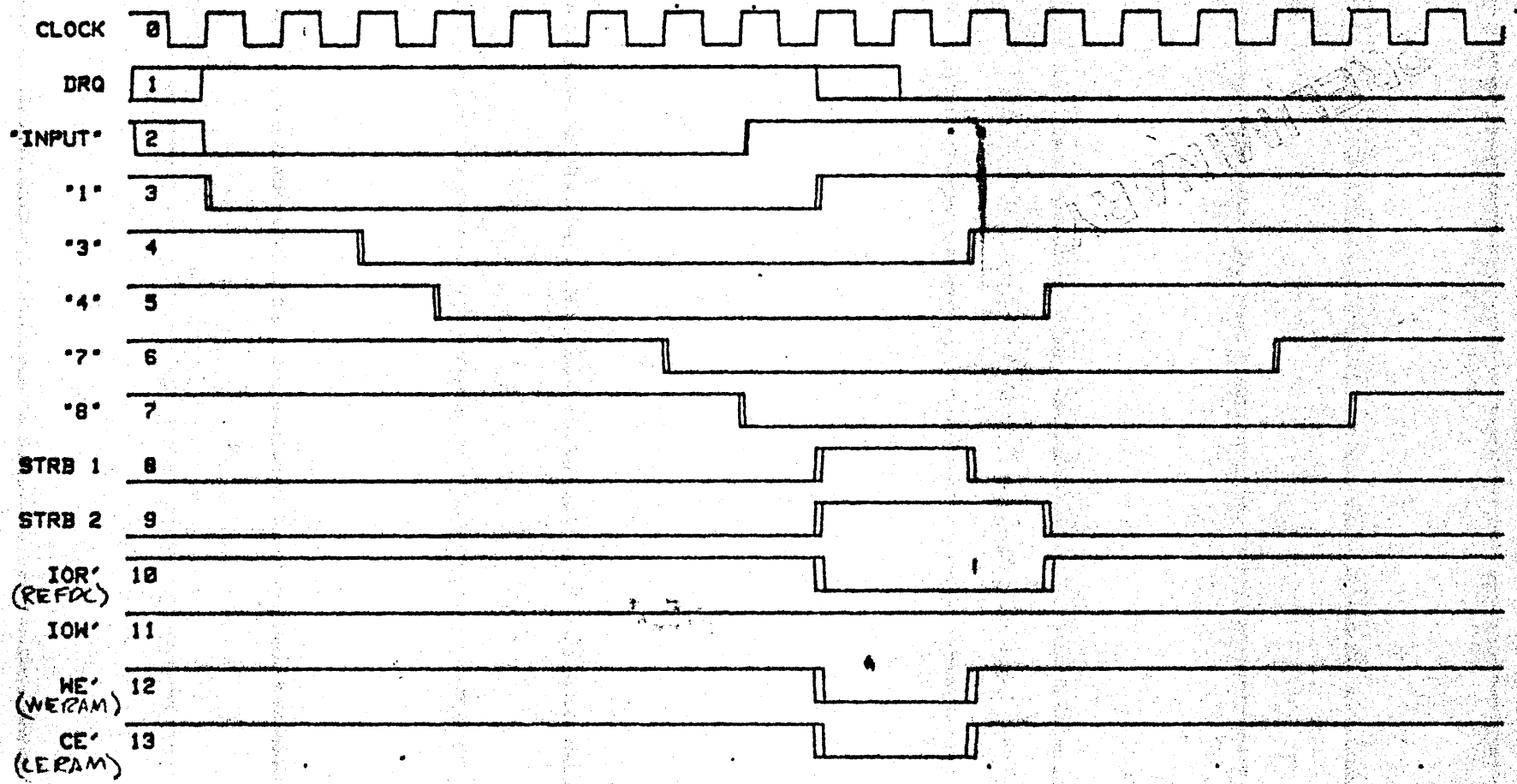
DRAWN BY: 9872A	DATE	TITLE: TIMING (INTERNAL RAM → F.D.C.)	HEWLETT PACKARD
ENGINEER: Ron Rogers	6 NOV 80		
RELEASE TO PROD. [signature]	11-17-80	NEXT ASSEMBLY	PART NUMBER: A - 09826-66562-7
		FINISH / SCALE	

SHEET 7 OF 10

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-17-80

A - 09826-66562-7



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 608

DO NOT SCALE THIS DRAWING

DRAWN BY: 9872A	DATE:
ENGINEER: Ron Rogers	DATE: 6 NOV 80
RELEASE TO PROD.	11-17-80
PURCHASING REL.	

TITLE: TIMING (INTERNAL F.D.C. TO RAM)

NEXT ASSEMBLY:

FINISH: SCALE:

HEWLETT PACKARD

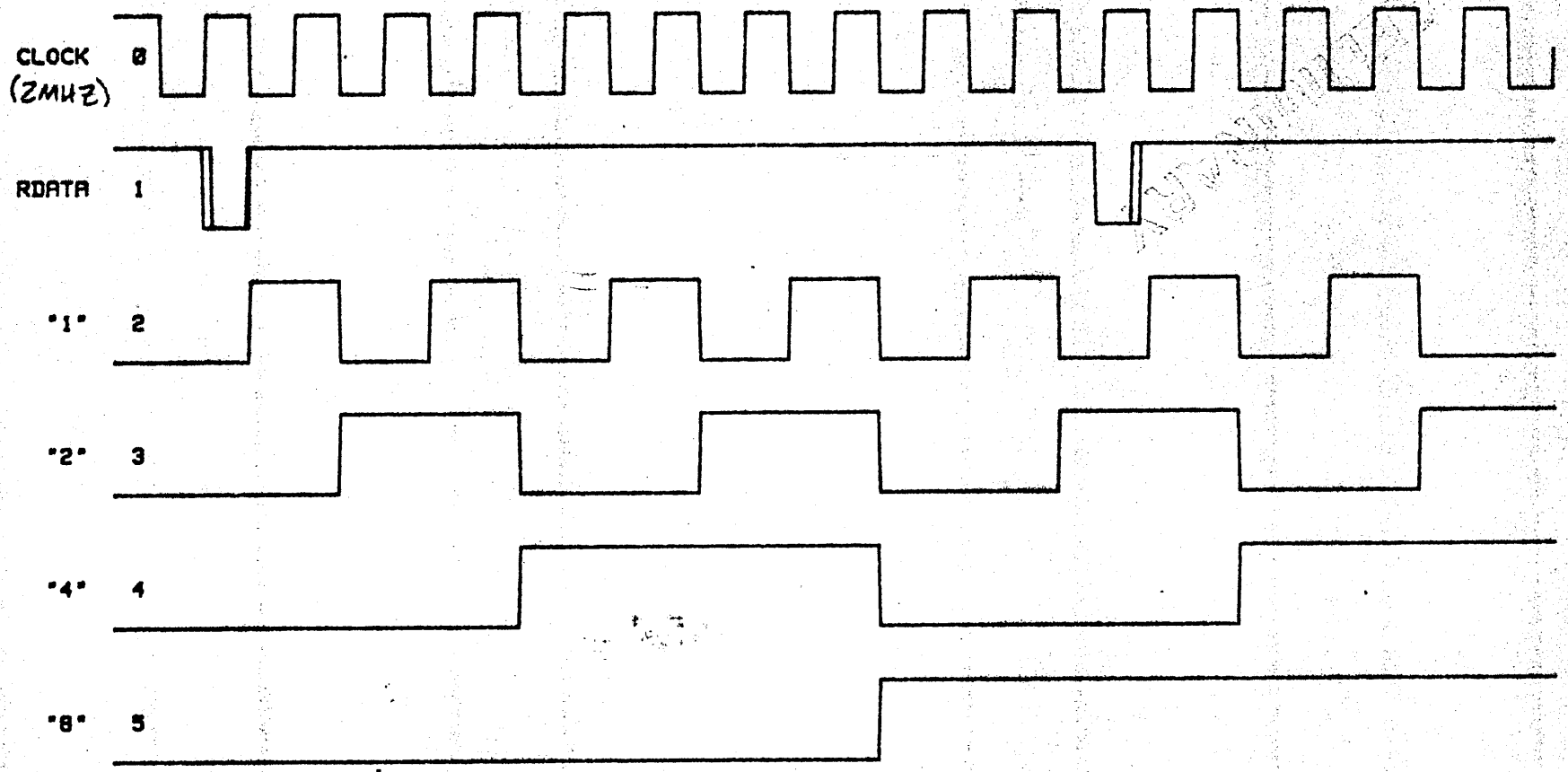
PART NUMBER: A - 09826-66562-7

ENGINEERING RESPONSIBILITY ☑ SEPIA ☑

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	35	38	43	
48	50	51	53									70			

- 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[signature]	11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.5 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 905

DO NOT SCALE THIS DRAWING

9872A

DRAWN BY: Ron Rogers — DATE: 6 NOV 80

ENGINEER

RELEASE TO PROD. — 11-17-80

TITLE: TIMING (MAX CASE DISCR, NO CLEAR)

NEXT ASSEMBLY

FINISH — SCALE

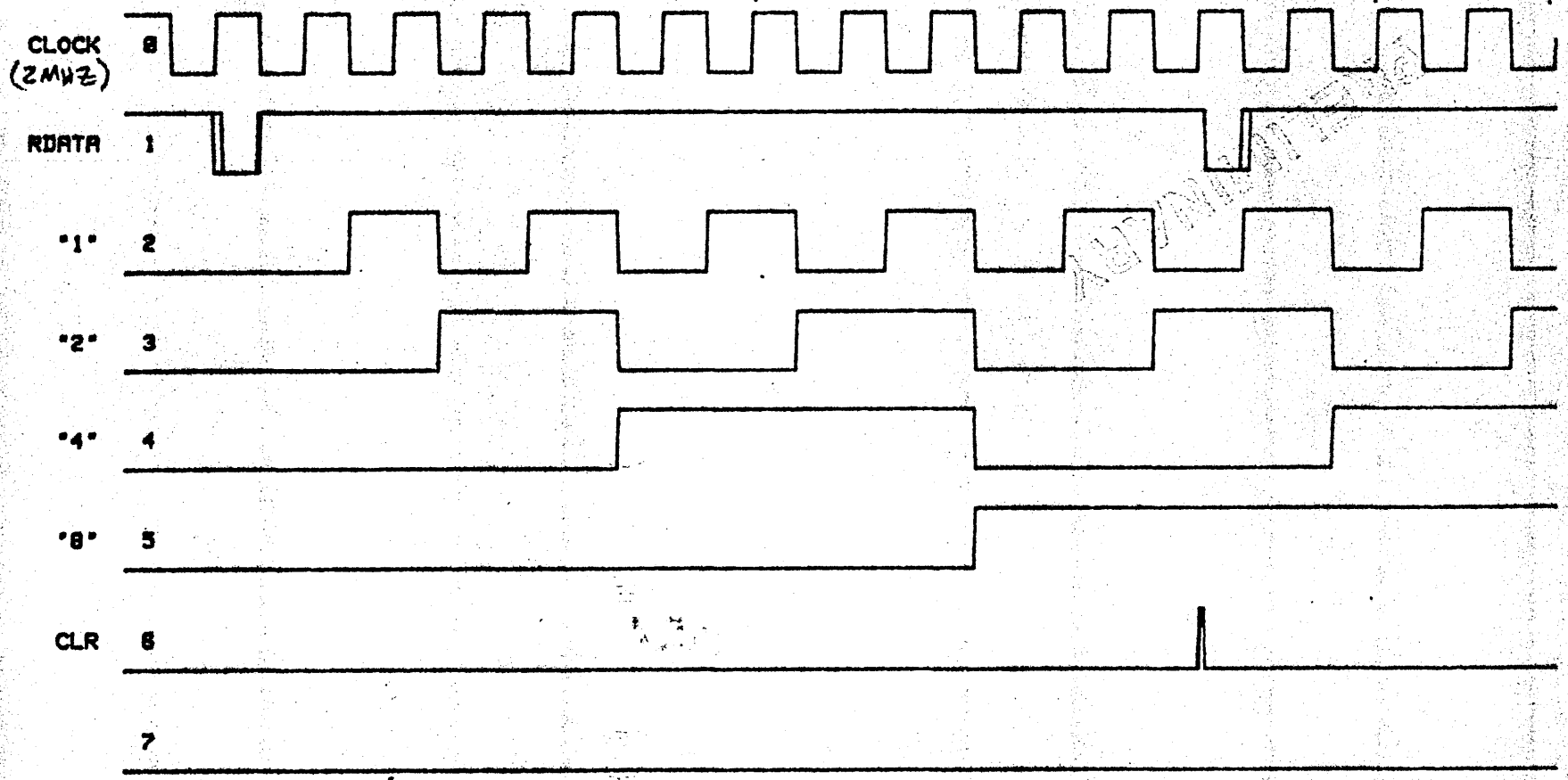
HEWLETT PACKARD

PART NUMBER: - 09826-66562-7

ENGINEERING RESPONSIBILITY ■ SEPIA ☒

A - 09826-66562-7

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[signature]	11-17-80



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES: XX ± 0.8 mm or ± 0.4 mm
XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 606

DO NOT SCALE THIS DRAWING

DRAWN BY: 9872A	DATE:
ENGINEER: Ron Poners	6 NOV 80
RELEASE TO PROD. [signature]	11-17-80
SUPERSEDES DWG.	

TITLE: TIMING (MIN CASE DISCR. CLEAR)

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

PART NUMBER: A - 09826-66562-7

SHEET 10 OF 10

BUS CHARACTERISTICS

09826-66562-8, FLOPPY CONTROL BOARD

I. DC LOADING SPECS.

Pin	Name	Parts	Ioh	Iol
2	10 MHz	74LS04	20	0.4
12	CSFLOP'	74LS04, 74LS27, 74LS138	60	1.2
39	RESET'	74LS174	20	0.4
41	IOW'	74LS08, 74LS32, 74LS244 (2)	80	1.2
42	IOR'	74LS08, 74LS244	40	0.6
45	BR/W'	74LS04, 74LS138	20	0.8
46	BAS'	74LS04, 74LS32	40	0.8
50	BA1	74LS74, 74LS193	40	0.8
51	BA2	74LS74, 74LS193	40	0.8
52	BA3	74LS193	20	0.4
53	BA4	74LS193	20	0.4
54	BA5	74LS193	20	0.4
55	BA6	74LS193	20	0.4
56	BA7	74LS193	20	0.4
57	BA8	74LS193	20	0.4
59	BA10	74LS138	20	0.4
60	BA11	74LS138	20	0.4
63	BA12	74LS27, 74LS138	40	0.8
64	BA13	74LS27, 74LS10, 74LS138	60	1.2
87	BD8	74LS640, 74LS273	40	0.6
88	BD9	74LS640, 74LS273	40	0.6
89	BD10	74LS640, 74LS273	40	0.6
90	BD11	74LS640, 74LS273	40	0.6
91	BD12	74LS640, 74LS273	40	0.6
92	BD13	74LS640, 74LS273	40	0.6
93	BD14	74LS640, 74LS273	40	0.6
94	BD15	74LS640, 74LS273	40	0.6
			uA	mA

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A | STK NO

BUS CHARACTERISTICS

BY Jon Rubinstein | DATE October 2, 1981

APPD | SHEET NO 1 OF 5

SUPERSEDES | DWG NO A-09826-66562-8

II. BUS DRIVING SPECS.

Pin	Name	Parts	Ioh	Iol
11	INT2'	74LS04	400	8.0
87	BD8	74LS640	3000	24.0
		74LS244	3000	24.0
88	BD9	74LS640	3000	24.0
		74LS244	3000	24.0
89	BD10	74LS640	3000	24.0
		74LS244	3000	24.0
90	BD11	74LS640	3000	24.0
		74LS244	3000	24.0
91	BD12	74LS640	3000	24.0
92	BD13	74LS640	3000	24.0
93	BD14	74LS640	3000	24.0
94	BD15	74LS640	3000	24.0
			uA	mA

III. SIGNALS NOT IN USE

Pin	Name	Comments
5	DMAR0'	Provision for future use of DMA
6	DMAR1'	"
7	DMACK0'	"
8	DMACK1'	"
15	DMARDY'	"
16	INT3'	Provision for multi-drive controller
17	INT6'	"
18	INT5'	"
21	BG1	Provision for a bus controller
22	BG2	"
23	BG2	"
24	BR'	"
25	DONE'	"
26	BGACK'	"
27	SPARE1	System spares
28	SPARE2	"
29	SPARE3	"
30	ENDT'	Enable data transfer acknowledge
31	FC0	Provision for auto-vector
32	FC1	"
33	FC2	"
32	DTACK'	Data transfer acknowledge
38	BERR'	Bus error
43	BLDS'	Buffered lower data strobe
44	BUDS'	Buffered upper data strobe
49	HALT'	
58	BA9	Buffered address #9
65	BA14	" #14
66	BA15	" #15
67	BA16	" #16
68	BA17	" #17
69	BA18	" #18
70	BA19	" #19
71	BA20	" #20
72	BA21	" #21
73	BA22	" #22
74	BA23	" #23
77	BD0	Buffered data #0
78	BD1	" #1
79	BD2	" #2
80	BD3	" #3
81	BD4	" #4
82	BD5	" #5
83	BD6	" #6
84	BD7	" #7

LTR	PC NO	APPROVED	DATE	REVISIONS

MODEL 9836A | STK NO

BUS CHARACTERISTICS

BY Jon Rubinstein | DATE October 2, 1981

APPD | SHEET NO 3 OF 5

SUPERSEDES | DWG NO A-09826-66562-8

IV. CAPACITIVE LOADING

Pin	Name	Parts	Capacitance
2	10MHZ	74LS04	12.2
5	DMAR0'		2.7
6	DMAR1'		2.3
7	DMACK0'		2.7
8	DMACK1'		2.3
11	INT2'	74LS04*	30.0
12	CSFLOP'	74LS04, 74LS27, 74LS138	19.9
15	DMARDY'		2.6
16	INT3'		2.7
17	INT6'		2.5
18	INT5'		2.7
21	BG1		2.4
22	BG3		2.7
23	BG2		2.3
24	BR'		2.7
25	DONE'		2.6
26	BGACK'		2.7
27	SPARE1		2.5
28	SPARE2		2.7
29	SPARE3		2.7
30	ENDT'		2.7
31	FC0		2.6
32	FC1		2.7
33	FC2		2.6
34	DTACK'		2.7
37	RESET'	74LS04	26.0
38	BERR'		2.6
41	IOW'		40.3
42	IOR'	74LS244, 74LS08	32.5
43	BLDS'		2.3
44	BUDS'		2.3
45	BR/W'	74LS04, 74LS138	28.0
46	BAS	74LS32, 74LS04	29.1
49	HALT'		2.5
50	BA1	74LS193, 74LS74	36.3

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A | STK NO

BUS CHARACTERIZATIONS

BY Jon Rubinstein | DATE October 2, 1981

APPD | SHEET NO 4 OF 5

SUPERSEDES | DWG NO A-09826-66562-8

Pin	Name	Parts	Capacitance
51	BA2	74LS193, 74LS74	35.7
52	BA3	74LS193	24.2
53	BA4	74LS193	19.1
54	BA5	74LS193	28.4
55	BA6	74LS193	23.8
56	BA7	74LS193	28.0
57	BA8	74LS193	21.4
58	BA9		2.3
59	BA10	74LS138	26.3
60	BA11	74LS138	23.9
63	BA12	74LS27, 74LS138	33.7
64	BA13	74LS27, 74LS138, 74LS10	79.7
65	BA14		2.4
66	BA15		2.4
67	BA16		2.4
68	BA17		2.4
69	BA18		2.4
70	BA19		2.4
71	BA20		2.4
72	BA21		2.4
73	BA22		2.4
74	BA23		2.4
77	BD0		2.4
78	BD1		2.4
79	BD2		2.4
80	BD3		2.4
81	BD4		2.4
82	BD5		2.4
83	BD6		2.4
84	BD7		2.4
87	BD8	74LS640, 74LS273, 74LS244*	56.4
88	BD9	74LS640, 74LS273, 74LS244*	46.1
89	BD10	74LS640, 74LS273, 74LS244*	58.4
90	BD11	74LS640, 74LS273, 74LS244*	59.7
91	BD12	74LS640, 74LS273	46.8
92	BD13	74LS640, 74LS273	44.8
93	BD14	74LS640, 74LS273	44.8
94	BD15	74LS640, 74LS273	42.3

*Output connected to bus.

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL 9836A STK NO

BUS CHARACTERIZATIONS

BY Jon Rubinstein DATE October 2, 1981

APPD SHEET NO 5 OF 5

SUPERSEDES DWG NO A-09826-66562-8