

This page provides a running history of changes for a multi-page NOTE: drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-

and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other

	attention-getting outline).				
Ltr	REVISIONS			DATE	INITIALS
Α					
		· · · · · · · · · · · · · · · · · · ·			
			· · · · · · · · · · · · · · · · · · ·		
		· · · · · · · · · · · · · · · · · · ·			
				<u> </u>	<u> </u>
				<u></u>	
		· · · · · · · · · · · · · · · · · · ·	 	<u> </u>	
				<u> </u>	
					6 855
				3.73	
			· · · · · · · · · · · · · · · · · · ·		
		·			
		······································			
del No.	9836	Stock No.		L	<u> </u>
le		1 Stock No.	•		
scription	Theory of Operation		Date	07 Octobe	r 1981
	Jim McLucas	·····		t No.	of 12
ersedes				A 00	826-66553-9



TABLE OF CONTENTS 09826-66553 POWER SUPPLY BOARD

							PAG	SE.	
1.	INTRODUCTI	<u>on</u>					1	+	
2.	MINUS 12 V	OLT REGULATOR				• • • • • • •	1	!	
	2.2. Pul 2.3. Fre 2.4. Sof 2.5. Pow 2.6. Ene 2.7. Cur 2.8. Fil 2.9. Out 2.10. Dam 2.11. Vol	se Width Modu quency Comper t Start Circu er Switch and rgy Storage I rent Limit Ci ter Capacitor put LC Filter ping Network. tage Sense	lator (PWM). sation itry d Diode rcuitry					† † † † † † † † † † † † † † † † † † †	
3.	+12 VOLT R	EGULATOR		• • • • • • • • •				7	
4.	3.2. Adj 3.3. Pul 3.4. Fre 3.5. Sof 3.6. Pow 3.7. Tra 3.8. Fil 3.9. Cur 3.10. Out 3.11. Vol 3.12. Ove 3.13. Shu 3.14. Inh	ustable Volta se Width Modu quency Comper t Start Circu er Switch and nsformer ter Capacitor rent Limit Ci put LC Filter tage Sense rvoltage Prof tdown	age Divider ulator usation d Diode crcuitry tection					9	
			age Divider lator						.′
	4.5. Sof	t Start Circ	itry		• • • • •	् ्		0	
			MODEL 9836		STK NO				
			Theory	of Operat	ion				
			BY Jim McL	ucas		DATE 07	Octobe	r 1981	
Pq.1	APPROVED	DATE	APPD			SHEET NO	2	0F	12

DWG NO A-09826-66553-9

PC NO

SUPERSEDES

REVISIONS



TABLE OF CONTENTS 09826-66553 POWER SUPPLY BOARD

	<u>P</u>	AGE
4.	+5 VOLT REGUALTOR (Continuted)	
	4.6. Power Switch and Diode	10 10 11
5.	INHIBIT CIRCUITRY	11
6.	POWER UP RESET	12
7.	PFAIL SIGNAL	12
8.	POWER UP SEQUENCE	12
9.	POWER DOWN SEQUENCE	12

4				MODEL	9836	STK NO				
					Theory of	Operation				
				ВУ	Jim McLuc	as	DATE 07	0ctober	1981	
Α	See Pa.1									10
LTR	PC NO	APPROVED	DATE	APPD			SHEET NO		0F	12
		REVISIONS			DES		DWG NO A-	-09826-6	6553-9)



THEORY OF OPERATION 09826-66553 POWER SUPPLY BOARD

1. INTRODUCTION:

This document describes the operation of the 09826-66553 Power Supply Board.

The following documents should be on hand when studying this Theory of Operation:

POWER SUPPLY IRS

POWER SUPPLY BLOCK DIAGRAM C-09826-66553-6

POWER SUPPLY SCHEMATIC C-09826-66553-4

PULSE WIDTH MODULATOR SG3524 DATA SHEET

2. MINUS 12 VOLT REGULATOR:

The -12V output is generated by a switching regulator which converts the positive raw DC into a regulated -12 volts. This approach allows the 9826 power supply to operate from a single NICAD battery for power fail protection.

2.1. Input LC Filter:

The -12V regulator shares an LC input filter (L6, C5, C6, and C10) with the +12V regulator. The raw DC is passed through L6 to the Pulse Width Modulator (PWM) and to the Power Switch and Diode network. The LC filter keeps 40kHz interference out of the Raw DC supply and therefore prevents the switching frequency interference from being conducted or radiated out of the AC power line connection.

2.2. Pulse Width Modulator (PWM):

The PWM is an SG3524 integrated circuit which contains a +5V reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shut-down circuitry. The current limiting circuitry is not used in the -12V regulator.

R51 and C26 set the oscillator frequency to 40kHz nominal. U6; the PWM used in the -12V regulator, generates the 40kHz ramp and the 40kHz oscillator pulses which are used by the PWM's

				MODEL	9836	STK NO				
					Theory of Operation					
				ВУ	Jim McLuc	as	DATE	07 October	1981	
Α	See Pg.1			APPD			SHEET NO	4	0F	12
LTR	PC NO APPROVED DATE REVISIONS		SUPERSE	DES		1	A-09826-6	<u> </u>		



in the +12V and +5V regulators (U5 and U3), i.e., the +12V and +5V regulator PWM's are slaved to the -12V regulator PWM. Therefore, if the oscillator in U6 is not working, then the +12V and +5V regulators will not operate.

The +5V reference from pin 16 of U6 is divided down to 2.5V by R50 and R52 and is applied to the inverting input of the PWM error amplifier. The -12 output voltage is sensed by R4, R7, and R8, and is fed back to the non-inverting input of the PWM.

2.3. Frequency Compensation:

C25 and R49 are connected between pins 9 and 1 of the PWM to provide frequency compensation and prevent oscillation in the feedback loop.

2.4. Soft Start Circuitry:

R6, R24, CR5, C8 provide soft starting for the -12V supply. As long as pin 9 of the PWM is held low, the base drive to U2 is inhibited. When power is turned on, C8 is discharged and pin 9 of U6 is held low through CR5. C8 will begin to charge toward V raw and will cause the voltage on pin 9 of U6 to ramp up. The base drive to U2 will be 40kHz pulses which will increase in width until the voltage on C8 causes the voltage on pin 9 of U6 to rise to its steady-state level.

The voltage on C8 will continue to rise and will cause CR5 to be reverse biased. This causes the soft start circuitry to have no further effect upon the PWM.

2.5. Power Switch and Diode:

U2 is a hybrid circuit enclosed in a T0-3 package. It contains a power Darlington and a fast recovery, high current diode. The diode is connected in series with L9 to the -12V output. The Darlington is connected in series with L4 and R27 to ground.

2.6. Energy Storage Inductor:

When the Darlington is turned ON by the base drive applied to R28, current flows through L4 and R27 to ground. This causes energy to be stored in L4. When the Darlington is turned OFF, the diode in U2 allows current to continue flowing in L4. This charges filter capacitor C17 and delivers current to the load. R27 provides a voltage which is proportioned to the current through L4. This voltage is used to drive the current limit circuitry.

				MODEL	9836	STK NO_				
_					Theory of Opera	ation				
				ВУ	Jim McLucas		DATE 07	0ctober	- 1981	
A TR	See Pq.1	APPROVED	DATE	APPD			SHEET NO	5	OF	12
		REVISIONS			ES		DWG NO A	-09826-6	66553-9	9



2.7. Current Limit Circuitry:

The voltage developed across R27 is applied through R30 to the base of Q3. Q3 is normally OFF. If the voltage across R27 exceeds 0.6V, Q3 will be turned ON and will discharge C8. This pulls pin 9 of U6 LOW, and causes base drive pulses out of pin 12 and 13 of U6 to be inhibited. This causes the Darlington in U2 to be turned OFF.

With the Darlington turned OFF, the current through R27 goes to zero, Q3 turns OFF, and C8 starts to charge up again. This will cause pin 9 of U6 to go HIGH, which causes base driver pulses to be applied to the Darlington. If the -12V supply is still shorted, Q3 will again pull pin 9 of U6 LOW causing the Darlington to be turned OFF. This process will continue until the short across the -12V supply is removed.

2.8. Filter Capacitor:

The filter capacitor, C17, smoothes out the 40kHz ripple. However, due mainly to its equivalent series resistance (ESR) and inductance, additional filtering is required.

2.9. Output LC Filter:

The output LC filter consisting of L9, C24, and C30 further reduces the 40kHz ripple on the output of the -12V supply.

2.10. Damping Network:

A damping network, C7 and R29, is connected across the filter capacitor to privide gain and phase margin in the feedback loop. This works by AC coupling a low value resistor of 0.47 ohms across the LC circuit formed by L4 and C17.

2.11. Voltage Sense:

The -12V across filter capacitor C17 is sensed by the voltage divider consisting of R4, R7, and R8. Part of the output voltage is fed back to pin 2 of U6. This is the non-inverting input of the error amplifier.

2.12. Shutdown:

A TTL signal can be applied to pin 10 of U6. This line is also connected to pin 10 of U5 in the +12V regulator. The SHUTDOWN line is not used unless the unit contains a Battery Option.

				MODEL	9836	STK NO					
				Theory of Operation							
				ВУ	Jim McLuca	ıs	DATE	07	0ctobe	r 1981	
A LTR	See Pg. 1	APPROVED	DATE	APPD			SHEET N	0	6	OF	12
	REVISIONS		SUPERSEC	DES		DWG NO	A-0	9826-6	6553-9)	



With the Battery Option, a logic HIGH is applied to the SHUTDOWN line to turn the Power Supply Board OFF before the relay in series with the battery is de-energized. This prevents arcing of relay contacts.

When a HIGH is applied to the SHUTDOWN line the +5V regulator will be turned OFF by the INHIBIT circuitry when the -12V supply voltage drops to -10V.

3. +12 VOLT REGULATOR:

The +12V Regulator is very similar to the -12V regulator. The main difference is the way the POWER SWITCH AND DIODE circuit is connected to provide a positive output instead of a negative output.

Because of the similarity to the -12V Regulator, the description in this section will be brief.

3.1. Input LC Filter:

L6, C5, C6, and C10 function as the input filter to the +12V Regulator. This filter keeps RFI out of the AC input, and prevents AC line transients from being applied to the +12 Volt Regulator.

3.2. Adjustable Voltage Divider:

R3, R9, and R26 divide the +5 Volt reference of U5 down to 2.5 volts. This voltage is applied to the non-inverting inputs of the error amplifier in U3 and U5, the PWM's for the +5 Volt Regulator and the +12V Regulator.

3.3. Pulse Width Modulator:

The PWM is an SG3524, and is the same as the PWM in the -12 volt supply. The $40\,\text{kHz}$ ramp and the $40\,\text{kHz}$ oscillator pulses are generated by U6, the PWM in the $-12\,\text{V}$ regulator.

3.4. Frequency Compensation:

C14 and R22 are connected between pins 9 and 1 of the PWM to provide frequency compensation of the feedback loop.

				MODEL	9836	STK NO				
					Theory of Operation					
				ву	Jim McLucas DATE 07 October 1981					
A LTR	See pg.l	APPROVED	DATE	APPD			SHEET NO	7	0F	12
				SUPERSE	DES		DWG NO	A-09826	-66553-9	



3.5. Soft Start Circuitry:

R47, C4, and CR7 provide soft starting for the +12 volt supply. CR10 provides fast discharge of C4 when power is turned OFF so that soft starting will function if the AC line switch is turned off and on quickly. CR2 prevents possible start-up problems by not allowing pin 9 of U5 to go negative.

3.6. Power Switch and Diode:

Ul is a power hybrid which is the same as U2 in the -12 volt regulator. However, in the +12 volt supply, the diode is connected to ground and the output of the switch (pin 1) is connected to L3, which acts as an energy storage inductor for the +12 volt regulator. This arrangement provides a positive output voltage.

3.7. Inductor:

The inductor, L3, serves as the energy storage inductor for the +12 volt supply.

3.8. Filter Capacitor:

C16 filters the 40kHz ripple out of the +12 volt supply. However, additional filtering is required and is provided by the output LC filter.

3.9. Current Limit Circuitry:

The voltage across R38 is proportional to the +12 volt output current. This voltage is applied to one of the comparators in U4. When the voltage exceeds 200mV, the comparator switches and its output goes LOW (pin 2 of U4). This discharges C12 and then CR6 pulls pin 9 of the PWM LOW, which causes U1, the Power Switch and Diode, to be turned OFF. If the overload on the output remains, then R37 will cause C4 to discharge, and when the overload is removed, the +12 volt regulator will soft start. This prevents the current limit circuitry from locking up when an overload occurs and then is removed.

C15, which is across the comparator input (U4 pins 4 and 5), prevents the comparator from switching on 40kHz noise spikes. R20 provides 10mV of bias to the non-inverting input of the comparator to keep it from latching with its output L0W due to its internal offset voltage.

				MODEL	9836	STK NO		
					Theory of Operation			
				ву	Jim McLucas	DATE 07 October 1981		
Α	See Pg.]		APPD		SHEET NO 8 OF 12		
LTR	PC NO	APPROVED	DATE	AFFO		A 00000 ((FF2 0		
	REVISIONS		SUPERSEDES		DWG NO A-U9020-00553-9			



3.10. Output LC Filter:

The output filter consisting of L8, C23, and C29 reduces the 40kHz ripple on the output of the +12 volt supply.

3.11. Voltage Sense:

The +12 volts at the input to the output LC filter is divided down to +2.5 volts by R46 and R48, and then fed back to pin ! of the PWM, U5. The feedback loop will keep the voltage at U5, pin 1, equal to the reference voltage at U5, pin 2.

3.12. Overvoltage Protection:

The overvoltage protection circuitry consists of CR8, CR9, R43, R44, and C21. Execpt for CR8, all of this circuitry is also used to provide overvoltage protection for the +5 volt regulator.

If the +12V output rises to 13.3 volts, the zener diode, CR8 begins to conduct. When the output of the +12 volt supply rises to about 14 volts, the SCR (CR14) turns ON. This causes a large current to flow through the 15 amp fuse in series with the unregulated DC supply, and the fuse blows. With the DC input voltage removed, the regulator turns OFF.

Noise immunity is provided for the SCR gate circuit by R43, R44, and C21.

3.13. Shutdown:

See Section 2.12.

3.14. Inhibit Circuitry:

See Section 5.

4. +5 VOLT REGULATOR:

The +5 volt regulator is basically the same as the +12 volt regulator, except that the SHUTDOWN line is not connected to the +5 volt regulator.

4.1. Input LC Filter:

The input filter consists of L5, C1, and C20. This filter keeps 40kHz interference out of the unregulated DC supply and out of the AC input and keeps AC line transients out of the +5 volt regulator.

				MODEL 9836 STK NO	
				Theory of Operation	
Â				By Jim McLucas DATE 07 October 1981	
A LTR	See pg.1		DATE	APPD SHEET NO 9 OF 12	
Lin	PC NO APPROVED DATE REVISIONS			SUPERSEDES DWG NO A-09826-66553-9	



4.2. Adjustable Voltage Divider:

See Section 3.2.

4.3. Pulse Width Modulator:

The PWM is an SG3524 and is the same as the PWM's in the \pm 12 volt regulator and the \pm 12 volt regulator. The 40kHz oscillator pulses and the 40kHz ramp are generated by U6, the PWM in the \pm 12 volt regulator.

4.4. Frequency Compensation:

C18 and R39 are connected between pins 9 and 1 of the PWM (U3) to provide frequency compensation of the feedback loop.

4.5. Soft Start Circuitry:

R53, C2, and CRII provide soft starting for the +5 volt regulator. CRI3 provides fast discharge of C2 when power is turned OFF so that soft starting will function if the AC line switch is turned OFF and ON quickly.

4.6. Power Switch and Diode:

Q1, Q2, and CR3 make up the Power Switch and Diode. The diode is connected to ground, and the output of the power switch (pin 1) is connected to L2, which functions as an energy storage inductor. This arrangement provides a positive output voltage.

Q4 provides drive current to Q2. The drive current is independent of the magnitude of Vraw to allow operation to about 8 volts.

4.7. LC Filter:

The LC FILTER which consists of L2 and C3 reduces the 40kHz ripple in the +5 volt output. The 40kHz ripple is further reduced by the output LC filter.

4.8. Current Limit Circuitry:

The voltage across R45 is proportional to the current flowing out of the +5 volt regulator. This voltage is applied to one of the comparators in U4. When the voltage exceeds 100mV the comparator switches, and its output goes L0W (pin 13 of U4). This discharges C19 and then CR12 pulls pin 9 of the PWM L0W, which causes the Power Switch and Diode to be turned OFF. If the overload on the output remains, then R54 causes C2 to discharge, and when the

				MODEL	9836	STK NO			
					Theory of Operation				
				ву	Jim McLuca	as	DATE 07 October 1981		
Α	See pg. 1						SHEET NO. 10 OF 12		
LTR	PC NO	APPROVED	DATE	APPD			SHEET NO 10 OF 12		
	REVISIONS			SUPERSEC	DES		DWG NO A-09826-66553-9		



overload is removed, the +5 volt regulator will soft start. This prevents the current limit circuitry from locking up when an overload occurs and then is removed.

R21 provides 10mV of bias to the inverting input of the comparator to keep it from latching with its output L0W due to its internal offset voltage.

4.9. Output LC Filter:

The output LC filter consists of L7, C22, and C28. This filter reduces the 40kHz ripple on the output of the +5 volt supply.

4.10. Voltage Sense:

The +5 volts at the junction of R45 and L2 is divided down to +2.5 volts by R40 and R42 and then fed back to pin 1 of the PWM, U3. The feedback loop keeps the voltage at U3, pin 1, equal to the reference voltage at U3, pin 2.

4.11. Overvoltage Protection:

Overvoltage protection is provided by CR8, CR9, R43, R44, and C21. Except for CR8, this is the same circuitry which is used for overvoltage protection of the +12 volt regulator.

If the +5 volt output rises to 5.9 volts, the zener diode, CR9, begins to conduct. When the voltage rises to about 6.6 volts, the SCR (CR14) turns ON. This causes the 15 amp fuse in the unregulated DC supply to blow, removing the DC input voltage to the regulator.

R43, R44, and C21 provide noise rejection for the gate of the SCR.

5. INHIBIT CIRCUITRY:

The +5 volt regulator and the +12 volt regulators are both inhibited from turning ON until the output of the -12 volt supply is at least 10 volts negative. The INHIBIT function is provided by CR15, CR16, R55, and the current limit circuitry internal to the +5 volt and +12 volt PWM's (U3 and U5).

When the output of the -12 volt supply is less than 10 volts negative, zener diode CR16 is not conducting. When the -12 volt output is 10 volts negative, zener diode CR16 conducts. This effectively grounds pin 4 on U3 and pin 4 of U5. This allows the PWM's to being operating.

				MODEL	9836	STK NO		
					Theory of Operation			
				ву	Jim McLucas	DATE 07 Octo	ber 1981	
	See pq.l			APPD		SHEET NO 11	0F	12
LTR	PC NO APPROVED DATE REVISIONS			SUPERSED	ES .		826-66553-	.9



6. POWER UP RESET:

Two comparators in U4 are used as Schmitt triggers in the POWER UP RESET circuitry. The input to the first comparator (pin 9 of U4) is the output from the 5 volt regulator. When this output reaches 4.5 volts, the first comparator switches. The output of the first Schmitt trigger (pin 14 of U4) connects to C11 which together with R14 provides about 120ms delay before the second Schmitt trigger switches. After the 120ms delay, the output of the second Schmitt trigger (pin 1 of U4) goes HIGH, providing a POWER UP RESET pulse for the 68000 microprocessor.

C13, across pins 6 and 7 of U4, prevents false triggering of the comparator due to $40 \, \text{kHz}$ noise.

7. PFAIL SIGNAL:

A fullwave rectifier on the Rectifier Board rectifies the AC voltage in the secondary of the power transformer. This unfiltered signal is connected to the Power Supply Board which then connects it to the Mother Board. The Mother Board carries the PFAIL signal to the Battery Option Board.

8. POWER UP SEQUENCE:

- A. The -12 volt supply must be at least 10 volts negative before the +5 volt and the +12 volt supplies can operate.
- B. +5 volts ramps up in about 60ms.
- C. +12 volts ramps up in about 120ms.

9. POWER DOWN SEQUENCE:

- A. +12 volts starts down first.
- B. +5 volts goes down.
- C. -12 volts goes down last.

The actual times involved depend upon the loading on each supply.

9836 MODEL STK NO Theory of Operation Jim McLucas 07 October 1981 DATE RY See Pa. 12 12 SHEET NO APPROVED DATE DWG NO A-09826-66553-9 REVISIONS SUPERSEDES