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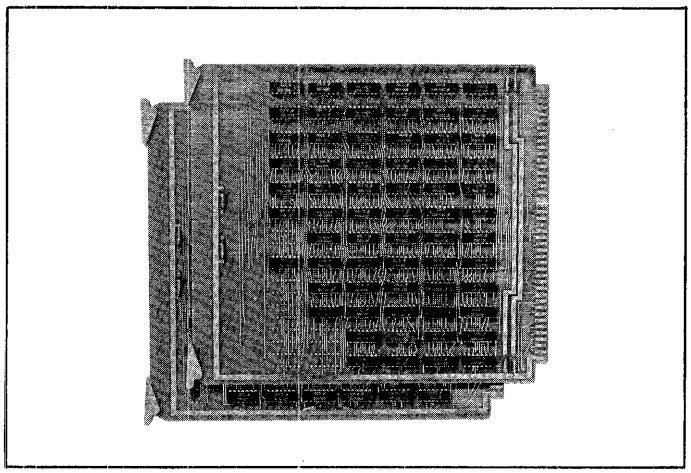
digital computers

EXTENDED ARITHMETIC UNIT 12579A



The Extended Arithmetic Unit (EAU) option for Hewlett-Packard 2116/2115 Computers permits *Integer Multiply, Integer Divide, Double Load, Double Store, Long Shifts,* and *Long Rotations* to be performed by hardware instead of program subroutines. The EAU option is a complete, ready-to-use package. The hardware consists of two cards that plug into the computer main frame. Also included are punched tapes containing software subroutines modified for 2116/2115 Computers equipped with EAU. This highly effective combination of hardware and software speeds processing without imposing any special programming requirement on the user. (See programming on the next page.)

TABLE 1. SHIFT/ROTATE EXECUTION TIMES

Number of Shifts or Rotations	Execution Time 2116	2115
1 to 4	3.2 μs	4.0 μs
5 to 8	4.8 μs	6.0 μs
9 to 12	6.4 μs	8.0 μs
12 to 16	8.0 μs	10.0 μs

ARITHMETIC OPERATIONS AFFECTED BY THE EXTENDED ARITHMETIC UNIT

INTEGER OPERATIONS	MAXIMUM EXECUTION TIMES BASIC 2116	2116 w/EAU	BASIC 2115	2115 w/EAU
Multiply	150 μs	19 μs	187 μs	24 μs
Divide	310 μs	21 μs	387 μs	26 μs
Double Load/Store	60 μs	6 μs	75 μs	8 μs
FLOATING POINT OPERATIONS				
Multiply	750 μs	344 μs	936 μs	430 μs
Divide	1500 μs	448 μs	1873 μs	560 μs
Square Root	6450 μs	3940 μs	8550 μs	4925 μs

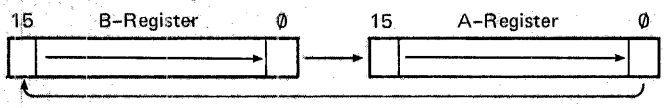
● REGISTER REFERENCE INSTRUCTIONS ADDED BY THE EXTENDED ARITHMETIC UNIT

(Execution times depend on number of rotations or shifts; see Table 1)

• RRR:

To rotate the B- and A-registers right 1 to 16 places.

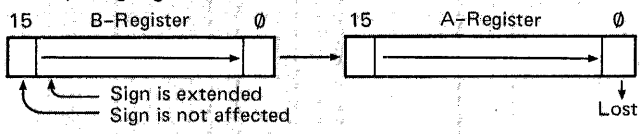
Assembly language: RRR N



• ASR:

To arithmetically shift the B- and A-registers right 1 to 16 places.

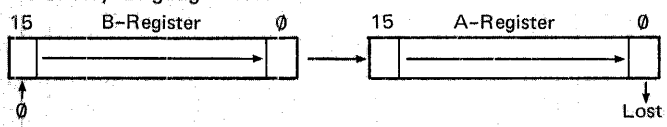
Assembly language: ASR N



• LSR:

To logically shift the B- and A-registers right 1 to 16 places.

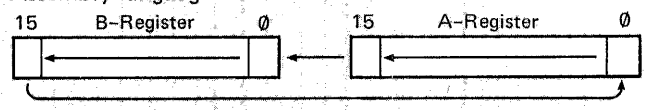
Assembly language: LSR N



• RRL:

To rotate the B- and A-registers left 1 to 16 places.

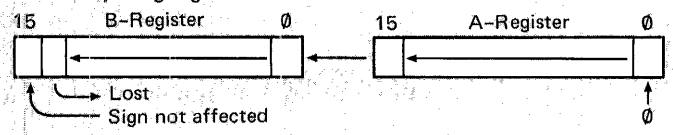
Assembly language: RRL N



• ASL:

To arithmetically shift the B- and A-registers left 1 to 16 places.

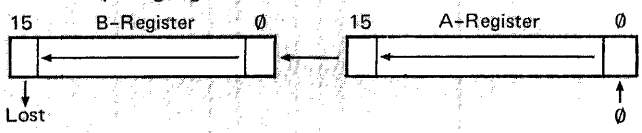
Assembly language: ASL N



• LSL:

To logically shift the B- and A-registers left 1 to 16 places.

Assembly language: LSL N



PROGRAMMING

No special programming is required to use the Extended Arithmetic Unit. The operations that use the EAU option can be called using Assembly language, FORTRAN, or ALGOL.

ASSEMBLY LANGUAGE PROGRAMMING

EXAMPLE: Multiply the integer quantities I and J.

Operation	Operand
LDA	I
MPY	J

(The result is in the B- and A-registers.)

EXAMPLE: Divide the two-word integer quantity I by the integer quantity J.

LDB	I
LDA	I+1
DIV	J

(The quotient is in the A-register; the remainder is in the B-register.)

EXAMPLE: Load X, a two-word quantity, into the A- and B-registers.

DLD	X

(X = address of the first word of the two-word quantity.)

EXAMPLE: Store a two-word quantity from the A- and B-registers into two consecutive locations in memory.

DST	X

(X = address of the first of the consecutive locations in memory.)

FORTRAN PROGRAMMING

Programming with HP 2116/2115 Extended ASA Basic FORTRAN is the same as with standard FORTRAN:

Multiplication = *
Division = /

EXAMPLE: Multiply quantities I and J and store the result in the M Register.

```
M = I *J
```

ALGOL PROGRAMMING

Programming with HP 2116/2115 ALGOL is the same as with standard ALGOL.

Multiplication = *
Division = / (real result); \(integer result)

EXAMPLE: Divide I by J and store the result in Z.

```
Z = I/J     (Z is a real quantity.)
```

SPECIFICATIONS

EAU CURRENT SUPPLIED BY COMPUTER

4.68A (+4.5V Supply)
3.3A (-2V Supply)

CARD DIMENSIONS

Height: 7-3/4 inches (196,8 mm)
Width: 8-11/16 inches (220,7 mm)

WEIGHT

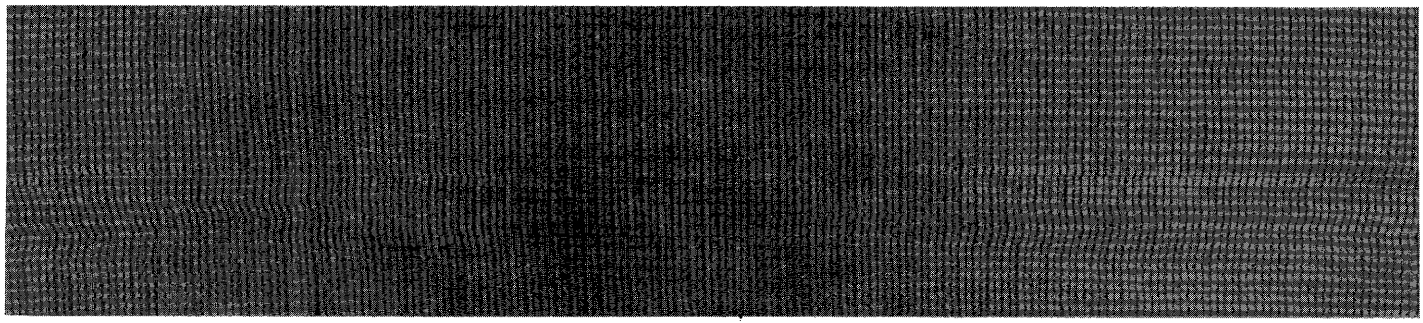
Net	Shipping
3 lb (1,36 kg)	5 lb (2,27 kg)

EQUIPMENT SUPPLIED

1. EAU Logic Card, Part no. 02116-6202.
2. EAU Timing Card, Part no. 02116-6196.
3. Punched tapes containing software systems modified for 2116/2115 Computers with EAU option.

NOTE: EAU option may be field installed, using field installation kit 12579A. However, for installation in HP 2116A Computers with a serial number prefix up to and including 747-, assistance by an HP computer field engineer *is required.*

Ordering information for the Extended Arithmetic Unit is contained in the HP 2116 and 2115 Computer Data Sheets.



For more information, call your local HP Sales Office or East (201) 265-5000 • Midwest (312) 677-0400 • South (404) 436-6181
West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94303. In Europe, 1217 Meyrin-Geneva, Switzerland

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HEWLETT PACKARD DYMEC DIVISION

EXTENDED ARITHMETIC UNIT

Computer Option M9

model 12579A

MANUAL SUPPLEMENT 15 MAY 68

SUPPLEMENT DESCRIPTION

This supplement provides installation and operation information for the HP 12579A Extended Arithmetic Unit. When purchased and documented as part of a complete computer system, the Unit is identified as Option M9.

1. GENERAL DESCRIPTION

2. The Extended Arithmetic Unit (EAU) option for Hewlett-Packard 2116A/2115A Computers permits Integer Multiply, Integer Divide, Double Load, Double Store, Long Shifts, and Long Rotations to be performed by hardware instead of by programmed subroutines. The HP Model 12579A Extended Arithmetic Unit is a complete, ready-to-use package. The hardware consists of two printed circuit cards that plug into the computer main frame. Also included are punched tapes containing software subroutines modified for 2116A/2115A Computers with the EAU option. This combination of hardware and software speeds processing without imposing any special programming requirements on the user. Execution times required for processing in computers fitted with the EAU option are given in Tables 1 and 2.

3. INSTALLATION

4. Extended Arithmetic Unit HP 12579A may be field installed in either the HP 2115A or the HP 2116A Computer. However, for HP 2116A Computers bearing serial prefix number 747- or less, a qualified HP computer field service engineer will be required to perform the EAU installation. To install the HP 12579A Extended Arithmetic Unit, proceed as follows:

a. Make certain that the computer POWER switch is set to the OFF position.

b. Insert the EAU Timing (02116-6196) and EAU Logic (02116-6202) plug-in printed circuit cards into the appropriate receptacle slots of the computer main frame as shown in Table 3.

c. Return the computer POWER switch to the ON position to resume normal computer operation.

Table 1. Arithmetic Operations Affected by the Extended Arithmetic Unit

INTEGER OPERATIONS	MAXIMUM EXECUTION TIMES			
	BASIC 2116A	2116A w/EAU	BASIC 2115A	2115A w/EAU
Multiply	150 μs	19 μs	187 μs	24 μs
Divide	310 μs	21 μs	387 μs	26 μs
Double Load Store	60 μs	6 μs	75 μs	8 μs
FLOATING POINT OPERATIONS				
Multiply	750 μs	344 μs	936 μs	430 μs
Divide	1500 μs	448 μs	1873 μs	560 μs
Square Root	6450 μs	3940 μs	8550 μs	4925 μs

Table 2. Shift/Rotate Execution Times

Number of Shifts or Rotations	Execution Time
1 to 4	3.2 μs
5 to 8	4.8 μs
9 to 12	6.4 μs
13 to 16	8.0 μs

Table 3. EAU Printed Circuit Card Slot Locations

EAU Printed Circuit Card	Computer Model	Slot Location
EAU Timing Card 02116-6196	HP 2115A	16
	HP 2116A/B	109
EAU Logic Card 02116-6202	HP 2115A	17
	HP 2116A/B	110

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5. OPERATION

6. The Extended Arithmetic Unit requires no special programming. All EAU operations can be called through the use of standard Assembler language, FORTRAN, or ALGOL. An EAU version of the Assembler is furnished with this option. The mnemonics and corresponding machine instruction codes which identify the basic EAU operations are listed in Table 4. Four of these instructions (MPY, DIV, DLD, and DST) cause two computer words to be generated. The first word is the instruction code, and the second is a 15-bit operand address. The manner in which the basic Extended Arithmetic Unit operations may be called and examples of obtainable results are described in subsequent paragraphs of this section.

7. MULTIPLICATION

8. Calling the multiply (MPY) instruction causes the computer to multiply the contents of the A-register by the contents of a memory location, and to store the product into registers B and A, respectively.

9. The following are examples of programming the multiply instruction in FORTRAN, ALGOL, and Assembler language:

a. FORTRAN: Multiply quantities I and J and store the result in M.

M=I*J

b. ALGOL: Multiply I by J and store the result in Z.

Z=I*J (Z is a real quantity)

c. Assembler Language:

Label	OP Code	Operand
	MPY	{ m[,I] / lit }

m	absolute or relative address expression
I	Indirect addressing indicator
lit	literal value

The result is stored right-justified in the combined B- and A-registers as illustrated in Figure 1.

Example (1): MPY VALUE

Before Execution	After Execution
(B) = any value	(B) = $*147761_8$ (1/2 product)
(A) = 000173_8 (multiplicand)	(A) = 006564_8 (1/2 product)
(VALUE) = 000034_8	(VALUE) = 000034_8 (multiplier)

Example (2): MPY DANTE

Before Execution	After Execution
(B) = any value	(B) = $*147761_8$ (1/2 product)
(A) = 101325_8 (multiplicand)	(A) = $*154275_8$ (1/2 product)
(DANTE) = 061111_8	(DANTE) = 061111_8 (multiplier)

*In Example (2), note that the split negative result is shown as it appears when each of the two registers is viewed individually. In practice, the B- and A-registers jointly contain a single, right-justified product consisting of eleven octal digits. The true product in this example (expressed in octal eight's complement form) is 31774354275. Refer to Figures 1 and 2 for further clarification.

Example (3): MPY = D20

Before Execution	After Execution
(B) = any value	(B) = 000000_8 (1/2 product)
(A) = 000075_8 (multiplicand)	(A) = 002304_8 (1/2 product)
(D20) = 000024_8 (multiplier)	(D20) = 000024_8 (multiplier)

10. DIVISION

11. Calling the divide (DIV) instruction causes the computer to divide the contents of registers B and A (a two-word integer quantity) by the contents of a memory location; the quotient is stored in the A-register and the remainder is stored in the B-register.

12. Examples of programming the DIV instruction in terms of FORTRAN, ALGOL, and Assembler language are as follows:

a. FORTRAN: Divide the two-word integer quantity I by the integer quantity J and store the result in M.

M=I/J

b. ALGOL: Divide I by J and store the result in Z.

Z=I/J (Z is a real quantity)

c. Assembler Language:

Label	OP Code	Operand
	DIV	{ m[,I] / lit }

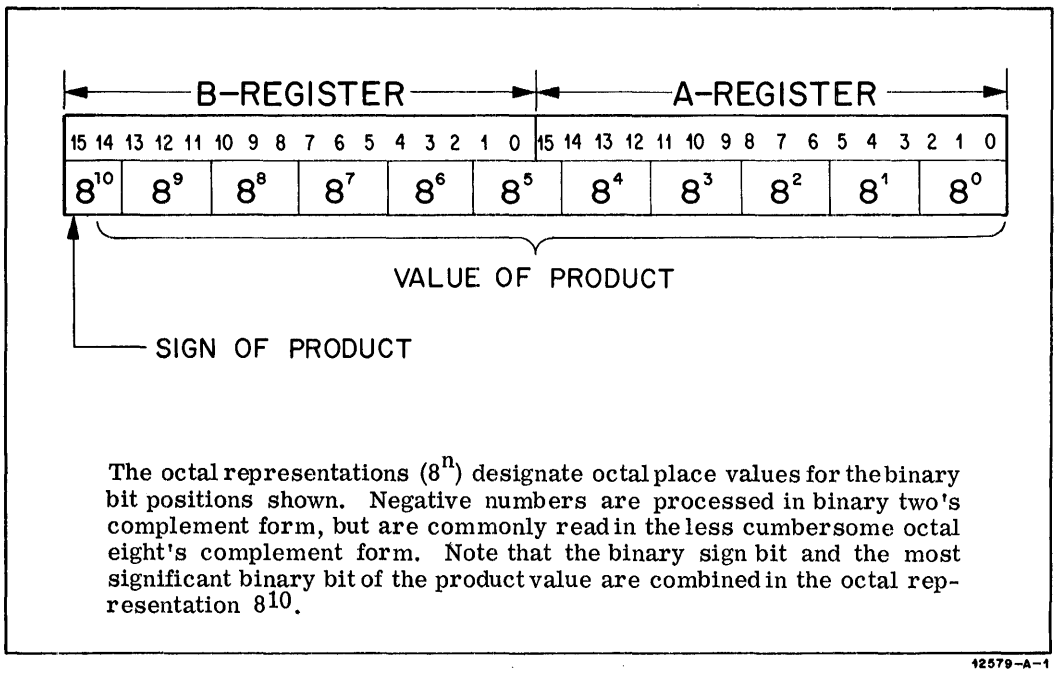
m	absolute or relative address
I	indirect addressing indicator
lit	literal value

Table 4. Extended Arithmetic Unit Machine Coding

INSTRUCTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPY	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
DIV	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
DLD	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
DST	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
ASR	1	0	0	0	0	0	1	0	0	0	0	1	*n			
ASL	1	0	0	0	0	0	0	0	0	0	0	1	*n			
LSR	1	0	0	0	0	0	1	0	0	0	1	0	*n			
LSL	1	0	0	0	0	0	0	0	0	0	1	0	*n			
RRR	1	0	0	0	0	0	1	0	0	1	0	0	*n			
RRL	1	0	0	0	0	0	0	0	0	1	0	0	*n			

*n = number of shifts or rotates:

1 = 1 shift or rotate
2 = 2 shifts or rotates
3 = 3 shifts or rotates
4 = 4 shifts or rotates
5 = 5 shifts or rotates
6 = 6 shifts or rotates
7 = 7 shifts or rotates
8 = 8 shifts or rotates
9 = 9 shifts or rotates
10 = 10 shifts or rotates
11 = 11 shifts or rotates
12 = 12 shifts or rotates
13 = 13 shifts or rotates
14 = 14 shifts or rotates
15 = 15 shifts or rotates
0 = 16 shifts or rotates



The octal representations (8^n) designate octal place values for the binary bit positions shown. Negative numbers are processed in binary two's complement form, but are commonly read in the less cumbersome octal eight's complement form. Note that the binary sign bit and the most significant binary bit of the product value are combined in the octal representation 8^{10}.

12579-A-1

Figure 1. Dual-Register Product Value

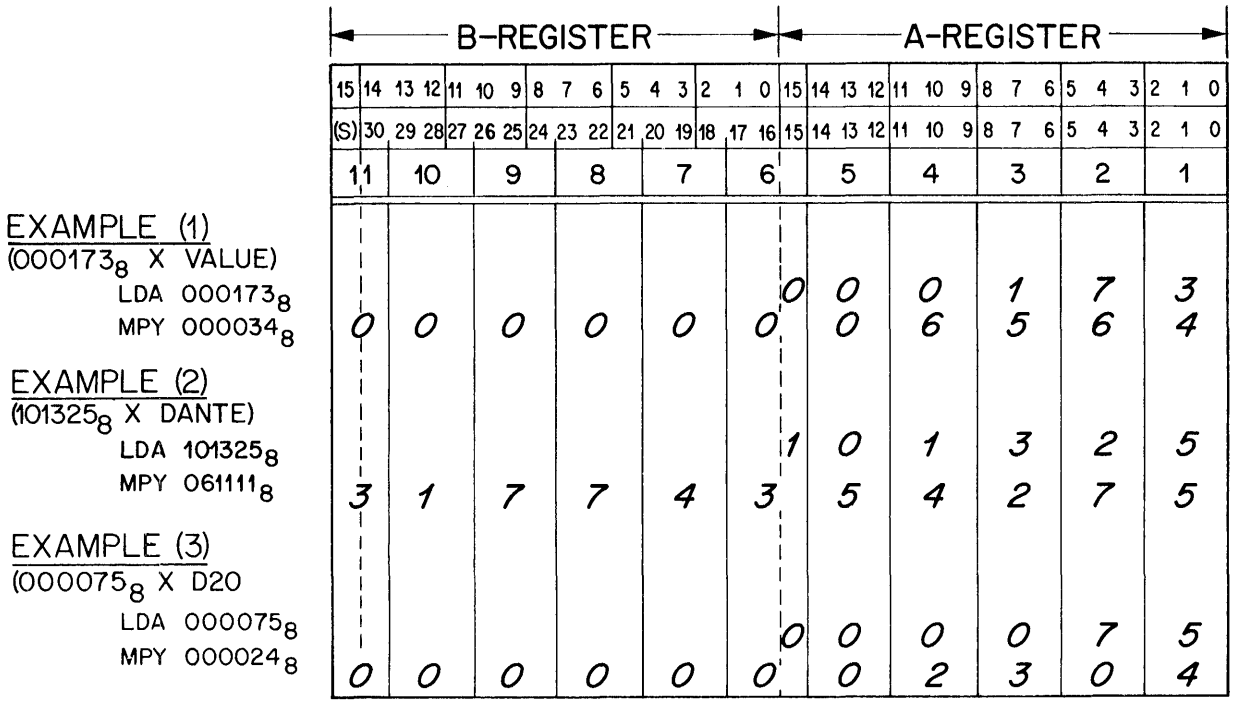


Figure 2. Format of EAU Dual-Register Product

Initially, the two-word dividend is stored in the B- and A-registers in the combined, right-justified form shown in Figure 3. At the completion of the division process, the A-register contains the quotient and the B-register contains the remainder. If an attempt is made to divide by zero, or if a divide operation results in a quotient too large for the A-register, the OVERFLOW bit will be set to signify that the results are invalid.

Example (1): DIV ALAN

Before Execution	After Execution
(B) = 000000_8 (1/2 dividend)	(B) = 000000_8 (remainder)
(A) = 054147_8 (1/2 dividend)	(A) = 000563_8 (quotient)
(ALAN) = 000075_8 (divisor)	(ALAN) = 000075_8 (divisor)

Example (2): DIV OCT73 (See Figure 4 for illustration)

Before Execution	After Execution
(B) = 000000_8 (1/2 dividend)	(B) = 000002_8 (remainder)
(A) = 000075_8 (1/2 dividend)	(A) = 000001_8 (quotient)
(OCT73) = 000073_8 (divisor)	(OCT73) = 000073_8 (divisor)

13. DOUBLE LOADING

14. Calling the double load (DLD) instruction causes the computer to load the A- and B-registers (respectively) with the contents of two consecutive locations (m and m+1) in memory.

15. Examples of programming the DLD instruction in terms of Assembler language are as follows:

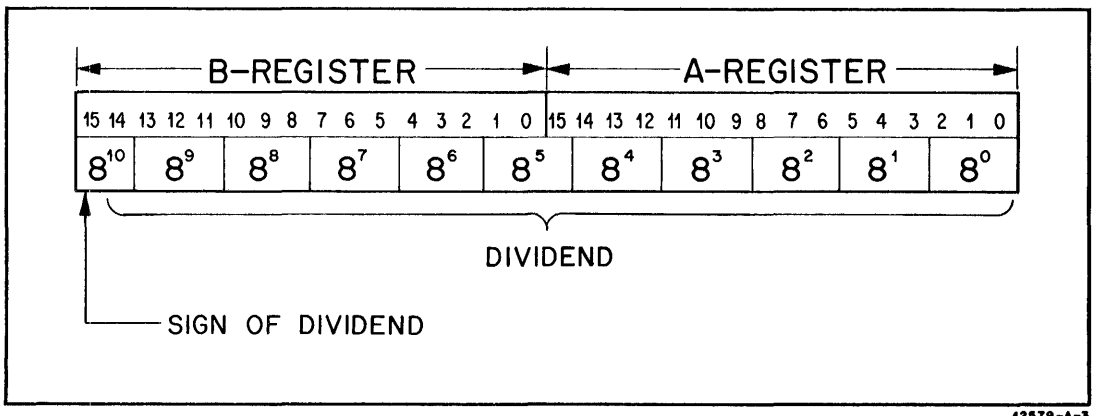


Figure 3. Format of Two-Word Dividend

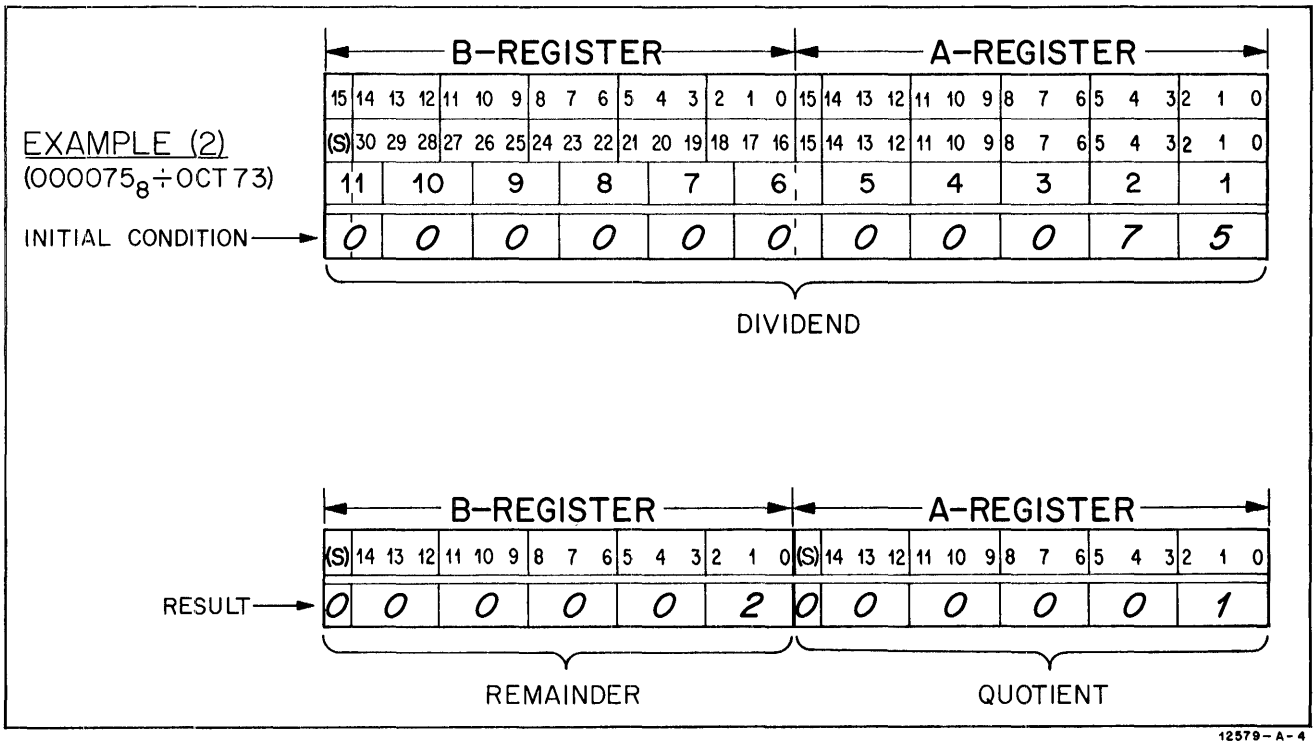


Figure 4. Division Example (2) Illustrated

a. Assembler Language DLD sequence:

Label	OP Code	Operand
	DLD	{m[,I] / lit}

m — Location of first word; contents of this location are loaded into the A-register. Contents of location m+1 are loaded into the B-register.

I — Indirect addressing indicator

lit — literal value (F only)

b. DLD Examples

Example (1): DLD FLPT

Before Execution	After Execution
(A) = any quantity	(A) = 017777_8
(B) = any quantity	(B) = 177400_8
(FLPT) = 017777_8	(FLPT) = 017777_8
(FLPT+1) = 177400_8	(FLPT+1) = 177400_8

Example (2): DLD IND,I

Before Execution	After Execution
(A) = any quantity	(A) = 035647_8 (1st word)
(B) = any quantity	(B) = 054100_8 (2nd word)
(IND) = 002177_8 (address of m)	(IND) = 002177_8 (address of m)
(m:2177_8) = 035647_8	(2177_8) = 035647_8 (1st word)
(m+1:2200_8) = 054100	(2200_8) = 054100_8 (2nd word)

16. DOUBLE STORING

17. Calling the double store (DST) instruction causes the computer to store the contents of the A- and B-registers into two consecutive memory locations (m and m+1, respectively).

18. Examples of programming the DST instruction in terms of Assembler language are as follows:

a. Assembler Language DST sequence:

Label	OP Code	Operand
	DST	m[,I]

m — Location of first word; the contents of the A-register are stored in this location. Contents of the B-register are stored in location m+1.

I — Indirect addressing indicator.

b. DST Examples:

Example (1): DST TROUT

Before Execution	After Execution
(A) = 000042_8 (1st word)	(A) = 000042_8 (1st word)
(B) = 177401_8 (2nd word)	(B) = 177401_8 (2nd word)
(TROUT) = any value	(TROUT) = 000042_8 (1st word)
(TROUT+1) = any value	(TROUT+1) = 177401_8 (2nd word)

Example (2): DST IVAN, I

Before Execution	After Execution
(A) = 000000_8 (1st word)	(A) = 000000_8 (1st word)
(B) = 017000_8 (2nd word)	(B) = 017000_8 (2nd word)
(IVAN) = 102027_8 (ind. address)	(IVAN) = 102027_8 (ind. address)
(I:2027_8) = 002777_8 (m address)	(2027_8) = 002777_8 (m address)
(m:2777_8) = any value	(2777_8) = 000000_8 (1st word)
(m+1:3000_8) = any value	(3000_8) = 017000_8 (2nd word)

19. SHIFT/ROTATE INSTRUCTIONS

20. In EAU-equipped computers, the combined word-content of the B- and A-registers (in that order) can be shifted or rotated, left or right, in bytes of from 1 to 16 bits per instruction (see Table 4). Although the execution time is very short (see Table 2) for performing shifts and rotates in variable length bytes, each bit is counted and processed individually by the computer. Shifts may be performed arithmetically or logically. EAU shift rotate instructions include ASL, ASR, LSL, LSR, RRL, and RRR. Examples of these instructions in terms of Assembler language programming are given below.

21. ASL n. When executed, the ASL n instruction causes the computer to arithmetically shift the combined contents of the B- and A-registers left n bits (see Figure 5). The value of n may equal any number from 1 to 16 inclusively, selected as specified in Table 4. Of particular importance in the ASL operation are the following:

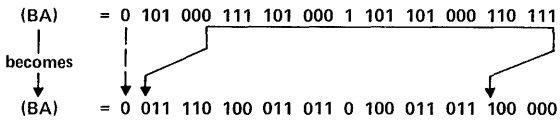
a. The sign (B15) of the two-word quantity remains stationary and unchanged in value.

b. The most significant bits shifted out of the B-register are discarded.

c. When vacated due to a left shift, the least significant bit position in the A-register is immediately refilled with a binary zero.

d. If the value of B14 remains the same as that of B15 (sign) throughout the shifting process, ASL terminates with OVERFLOW cleared. If, however, the values of B14 and B15 do not remain the same throughout the operation, ASL terminates with OVERFLOW set.

e. Example: ASL 5.



*Note that the value of the original B14 is not the same as that of the sign, and that B14 therefore causes OVERFLOW to become set. Note further that the original B12 in this example eventually shifts through the B14 position, at which time it, too, becomes capable of setting OVERFLOW -- if OVERFLOW is not already set.

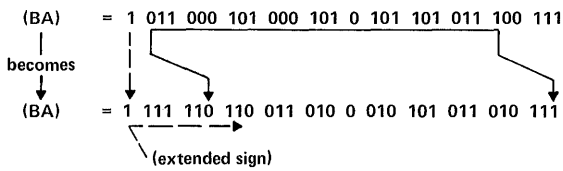
22. ASR n. When executed, the ASR n instruction causes the computer to arithmetically shift the combined contents of the B- and A-registers right n bits (see Figure 5). The value of n may equal any number from 1 to 16 inclusively, selected as specified in Table 4. Of particular impostance in the ASR operation are the following:

a. The sign (B15) of the two-word quantity remains unchanged in value.

b. The least significant bits shifted out of the A-register are discarded.

c. When vacated due to a right shift, the most significant bit position in the B-register is immediately filled with a bit value equal to that of the sign. In effect, the sign is extended to the right as a result of the ASR operation.

d. Example: ASR 5.



23. LSL n. Executing the LSL n instruction causes the computer to logically shift the combined contents of the B- and A-registers left n bits (see Figure 6). The value of n may equal any number from 1 to 16 inclusively, selected as specified in Table 4. The most important features of the LSL operation are as follows:

a. The most significant bits shifted out of position B15 of the B-register are discarded.

b. When vacated due to a left shift, the least significant bit position in the A-register is immediately filled with a binary zero.

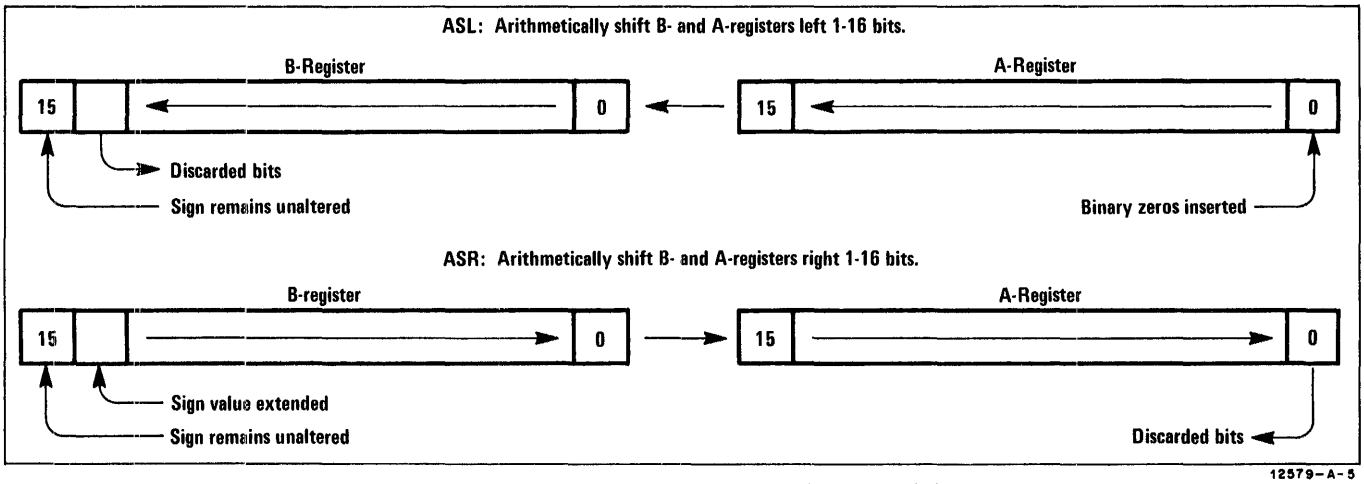
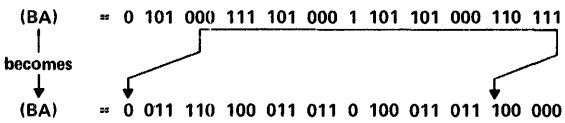


Figure 5. EAU Arithmetic Shifts ASL and ASR

c. Example: LSL 5.

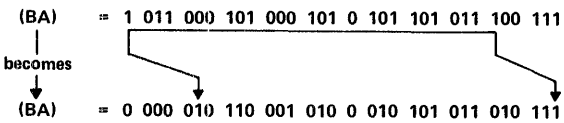


24. LSR n. Executing the LSR n instruction causes the computer to logically shift the combined contents of the B- and A-registers right n bits (see Figure 6). The value of n may equal any number from 1 to 6 inclusively, selected as specified in Table 4. The most important features of the LSR operation are as follows:

a. The least significant bits shifted out of position A0 of the A-register are discarded.

b. When vacated due to a logical right shift, B15 is immeidately filled with a binary zero.

c. Example: LSR 5.

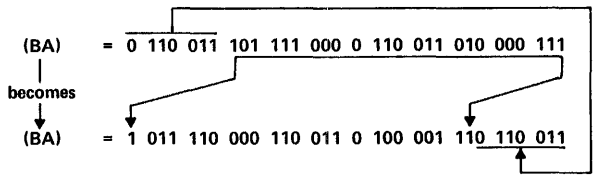


25. RRL n. Calling the RRL n instruction causes the computer to rotate the combined contents of the B- and A-registers to the left n bits (see Figure 7). The value of n may equal any number from 1 to 16 inclusively, selected as specified in Table 4. The most important features of the RRL operation are as follows:

a. No information is discarded.

b. The most significant bit (B15) rotated out of the B-register reappears as the least significant bit (A0) in the A-register.

c. Example: RRL 7.



26. RRR n. Calling the RRR n instruction causes the computer to rotate the combined contents of the B- and A-registers to the right n bits (see Figure 7). The value of n may equal any number from 1 to 16 inclusively, selected as specified in Table 4. The most important features of the RRR operation are as follows:

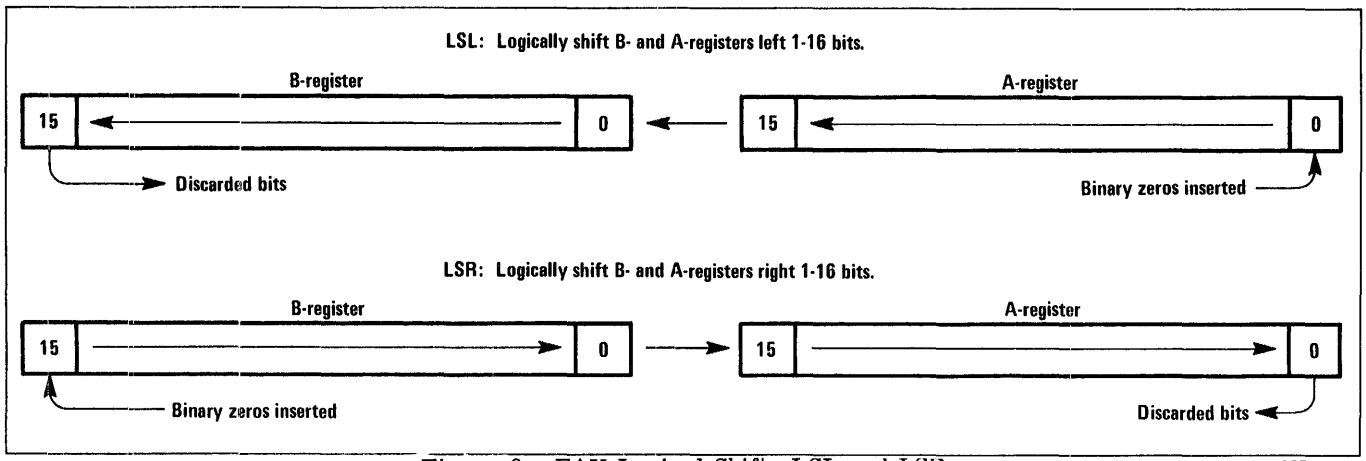


Figure 6. EAU Logical Shifts LSL and LSR

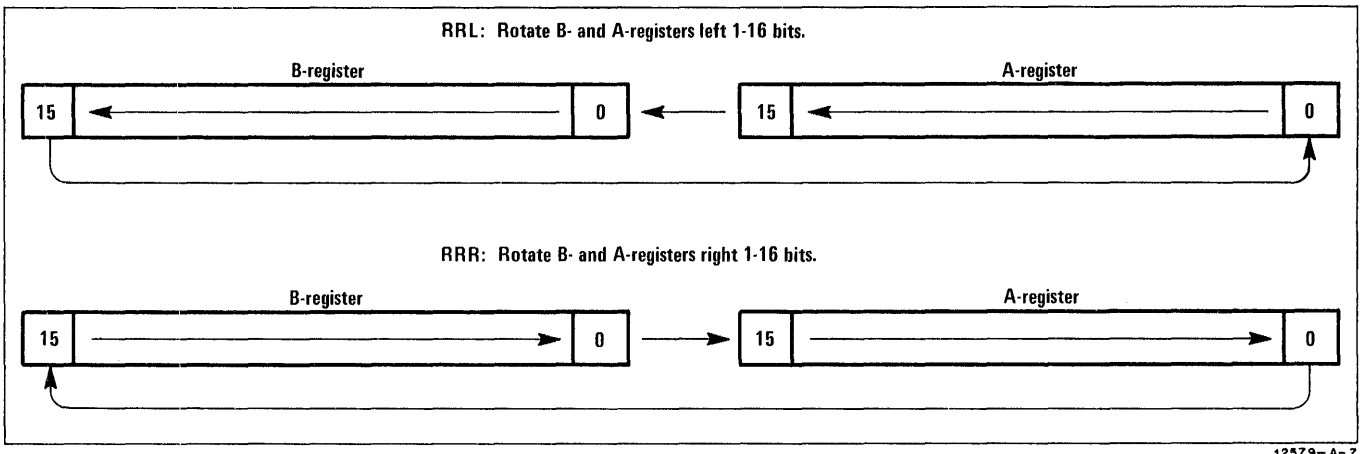
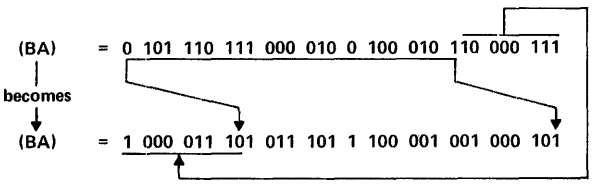


Figure 7. EAU Rotate Instructions RRL and RRR

a. No information is discarded.

b. The least significant bit (A0) rotated out of the A-register reappears as the most significant bit (B15) of the B-register.

c. Example: RRR 8.



27. HARDWARE LOGIC

28. Figures 8 and 9 are the logic diagrams for the two printed circuit boards that comprise the Extended Arithmetic option. Basically, the Extended Arithmetic Timing board (Figure 8, HP Part Number 02116-6196) provides timing signals to the Extended Arithmetic Logic board (Figure 9, HP Part Number 02116-6202). Major functional blocks are identified by shaded areas on the logic diagram for ease of location of functions.

29. TIMING BOARD. The option is enabled by a true signal (MAC) to pin 62 of the Timing board. This signal is true when bits 15 through 12 of the instruction word are 1-0-0-0, and bit 10 is 0. The remaining bits (TR0 through TR9 and TR11) code the specific EAU instruction as indicated in Table 4. The Inhibit Processor logic disables the Instruction Register and phase circuits in the processor, permitting the Memory and Phase Control logic to generate the necessary P123 phase signal. The Operation Decoder determines the type of operation to be performed (Arithmetic Shift, Logical Shift, Rotate, Multiply, Divide, Right Shift or Rotate, Double Load, Double Store), and the Operation Cycle Counter, Operation Cycle Decoder, and MP2 Gating logic determine how many memory cycles (or operations) will be used in executing the instruction. The Shift logic provides shift function signals to the Logic board, and the Overflow logic drives the Overflow indicator circuits in the processor. The Operation Exit logic ends the entire operation by advancing the P-Register to the next instruction (via the Logic board), and resetting appropriate EAU circuits.

30. LOGIC BOARD. The 23 functional blocks indicated by shading in Figure 9 identify each of the functions involved in executing the EAU instructions. The EAU timing signals from the Timing board are shown as inputs at the left of the figure. Basic computer timing signals are shown as inputs at the lower right. Four of the functional blocks are outputs to the R-S-T buses of the computer (SB0, TB15, TB0, RB0). Five blocks provide special EAU bit manipulations (Link, Carry, Sign, Overflow, Shift Overflow). Four blocks provide function signals similar to corresponding function signals in the basic processor (Complement Function, Add Function, Exclusive "Or" Function, Multiplication Add Function). Read and Store signals from the remaining ten blocks enable data transfers to and from the Registers in the same manner as corresponding signals generated on the Instruction Decoder board in the basic processor.

31. EAU HARDWARE MNEMONICS

32. Table 5 lists definitions of mnemonics relating to the Extended Arithmetic option. These include signal names defined for the basic processor, as well as names unique to the EAU option. An X ("Extended Arithmetic") or a B ("Buffered") is used in some cases to identify a signal generated by the option, but is otherwise similar or identical to a signal generated elsewhere in the processor.

33. DIAGNOSTIC PERFORMANCE CHECK

34. Table 6 provides operating procedures and a list of possible error messages which may be encountered in running the Extended Arithmetic Diagnostic program (HP Accessory Number 20422A/B). Use this program after installation and periodically thereafter to test hardware operation.

35. REPLACEABLE PARTS

36. Table 7 lists replaceable parts in alphanumerical order of their reference designations, with a description and HP part number for each part. Table 8 summarizes the total quantity of parts in order of HP Part Number. Figures 10 and 11 show the location of all parts on EAU Timing Card 02116-6196 and EAU Logic Card 02116-6202, respectively. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office.

Table 5. Extended Arithmetic Option Mnemonics

NEW	DEFINITION
ADF	Add Function
AS	Arithmetic Shift
C16	Carry bit 16
CARX	Carry flip-flop (EAU)
CLF	Clear Flag signal
CMFB	Complement Function, Buffered
CRS	Control Reset signal to I/O
CTO0	Counter at Operational Zero
D1-6	Divide operation cycles 1-6
D5L8	D5, Loop 8
DIV	Divide
DL1-4	Double Load operation cycles 1-4
DLD	Double Load
DS1-4	Double Store operation cycles 1-4
DST	Double Store
EOFB	Exclusive Or Function, Buffered
EPH	Enable Phase Signal
EPHX	Enable Phase flip-flop (EAU)
EXIT	Exit MAC operation sequence
GATE	Gate flip-flop
IIR	Inhibit Instruction Register
IIRX	IIR flip-flop (EAU)
IOSB	I/O Switch address, Buffered
ISG	Inhibit Strobe Generator
LINK	Link flip-flop
LS	Left Shift
MAC	Macro group, decoded
MAF	Multiplication Add Function
MD1-5	Multiply/Divide operation cycles 1-5
MD2G	MD2, Gated
MP1-5	Multiply operation cycles 1-5
MPY	Multiply
OASL	Overflow due to Arithmetic Shift Left
OC0-3	OCC flip-flops 0-3
OCC	Operation Cycle Counter
OVD	Overflow due to Divide operations
OVF	Overflow flip-flop
OVR	Overflow Register

NEW	DEFINITION
P1RB	Plus 1 onto R Bus
P1SB	Plus 1 onto S Bus
P123	PH1-PH2-or-PH3 signal
PH1	Phase 1, fetch
PH5	Phase 5, optional
RARB	Read A onto R Bus
RB0-15	R Bus bits 0-15
RBRB	Read B onto R Bus
RF2	Run flip-flop 2
RMSB	Read M onto S Bus
RO	Rotate
ROT5	Rotate at T5
RPRB	Read P onto R Bus
RSDS	Reset, Double Store Operation
RSET	Reset CARX flip-flop (EAU)
RT	Right shift or rotate
RTSB	Read T onto S Bus
SB0-15	S Bus bits 0-15
SDD	Sign of the Dividend
SDV	Sign of the Divisor
SIGN	Sign of the Operand
SLMB	Shift Left Magnitude, Buffered
SL14B	Shift Left bit 14, Buffered
SMD	Sign of the Multiplicand
SMR	Sign of the Multiplier
SQT	Sign of the Quotient
SRCS	Shift/Rotate Count Started
SRMB	Shift Right Magnitude, Buffered
STF	Set Flag, decoded
SWSA	Switch Store into A
SWSB	Switch Store into B
SWSM	Switch Store into M
SWSP	Switch Store into P
SWST	Switch Store into T
T0-7	Time Periods 0-7
TB0-15	T Bus bits 0-15
TEV	Time bits, Even numbered (T0, T2, T4, T6)
TOD	Time bits, Odd numbered (T1, T3, T5, T7)
TS	Time Strobe

Table 6. Diagnostic Procedures

```
          EXTENDED ARITH. UNIT DIAGNOSTIC


                ASMB,A,B,L,T
 THIS DIAGNOSTIC ALLOWS THE TESTING OF ALL THE EAU FUNCTIONS
WITH THE OPERATOR BEING ABLE TO SELECT ANY COMBINATIONS OF EAU
FUNCTIONS BEING OMITTED BY SETTING THE SW. REG.


THE CONTROL OPTIONS ARE:

     BIT   0 = MONTIOR THE NO. OF TEST CYCLES COMPLETED
     BIT   1 = MONTIOR THE RANDOM NO. GEN.
     BIT   2 = SKIP THE INDIRECT TESTS
     BIT   3 = SUPPRESS THE RANDOM NO. GEN. AND DIVISOR
     BIT   4 = LOAD THE RANDOM NO. FROM THE SW. REG.
     BIT   5 = LOAD THE DIVISOR FROM THE SW. REG.
     BIT   6 = PRINT OUT NUMBERS IN OCTAL
     BIT   7 = SKIP THE ROTATE TEST
     BIT   8 = SKIP THE LOGICAL SHIFT TEST
     BIT   9 = SKIP THE ARITH. SHIFT TEST
     BIT  10 = SKIP THE DOUBLE LOAD TEST
     BIT  11 = SKIP THE DOUBLE STORE TEST
     BIT  12 = SKIP THE MULTIPLY/DIVIDE TEST
     BIT  13 = BYPASS TELETYPE PRINT OUT
     BIT  14 = OUTPUT IS ON SERIAL TELETYPE
     BIT  15 = EXIT-HALT TEST


PROGRAM CONTROLED HALTS ARE:

     HALT 1 = XX1B     SET SW. REG. FOR CONTROL OPTIONS
     HALT 2 = XX2B     EXIT-PUSH RUN TO RESTARE
     HALT 3 = XX3B     PUT MSB INTO SW. REG.
     HALT 4 = XX4B     PUT LSB INTO SW. REG.
     HALT 5 = XX5B     PUT DIVISOR INTO SW. REG.
     HALT 6 = XX6B     CHECK FOR CAUSE OF ERROR-PUSH RUN TO RESTAR

TO START TEST:
   1 SET SW. REG. TO 2000
   2 PUSH LOAD ADDRESS
   3 SET SW. REG. FOR TTY I/O , SER. OR PARRALLEL TTY,TTY PRINT
   4 PUSH PRESET
   5 PUSH RUN

 AFTER TURNING COMPUTER OFF:
   1 SET SW. REG. TO 2017
   2 PUSH LOAD ADDRESS
   3 SET SW. REG. FOR CONTROL OPTIONS
   4 PUSH PRESET
   5 PUSH RUN
02000              ORG 2000B
                   SUP
```

Table 6. Diagnostic Procedures (Cont'd)

```
            EXTENDED ARITH. UNIT DIAGNOSTIC


**********************************************
*
*     ERROR SUB ROUTINES
*
**********************************************
  03603 003604  ERRDS DEF *+1
  03604 042111        ASC 6,DIVIDE ERROR
  03612 106612        OCT 106612
  03613 042111        ASC 4,DIVISOR
  03617 003616  ERRDE DEF *-1
*
  03620 003621  ERRMS DEF *+1
  03621 046525        ASC 7,MULTIPLY ERROR
  03630 106612        OCT 106612
  03631 003630  ERRME DEF *-1
*
  03632 003633  MPYCS DEF *+1
  03633 046525        ASC 8,MULTIPLICAND(A)=
  03643 003642  MPYCE DEF *-1
*
  03644 003645  MPYRS DEF *+1
  03645 046525        ASC 9,MULTIPLIER(DATA)=
  03656 003655  MPYRE DEF *-1
*
  03657 003660  MOVS  DEF *+1
  03660 046520        ASC 13,MPY EXIT WITH OVERFLOW SET
  03675 106612        OCT 106612
  03676 003675  MOVE  DEF *-1
*
  03677 003700  LSZES DEF *+1
  03700 055105        ASC 17,ZEROS NOT SHIFTED IN DURING LOGSR
  03721 106612        OCT 106612
  03722 003721  LSZEE DEF *-1
*
  03723 003724  ASZES DEF *+1
  03724 055105        ASC 16,ZEROS NOT SHIFTED IN DURING ARSR
  03744 106612        OCT 106612
  03745 003744  ASZEE DEF *-1
*
  03746 003747  ASOES DEF *+1
  03747 047516        ASC 16,ONES NOT SHIFTED IN DURING ARSR
  03767 106612        OCT 106612
  03770 003767  ASOEE DEF *-1
*
*
  04000               ORG 4000B
*
*
*
*
  04000 004001  MTMS  DEF *+1
  04001 047117        ASC 12,NO. OF TESTS COMPLETED=
  04015 004014  MTME  DEF *-1
*
  04016 004017  ERRS  DEF *+1
  04017 020124        ASC 7, TOTAL ERRORS=
  04026 004025  ERRE  DEF *-1

  04027 004030  MINDS DEF *+1
  04030 046105        ASC 9,LEVEL OF INDIRECT=
  04041 004040  MINDE DEF *-1
*
  04042 004043  MEROS DEF *+1
  04043 051117        ASC 6,ROTATE ERROR
  04051 106612        OCT 106612
  04052 004051  MEROE DEF *-1
```

Table 6. Diagnostic Procedures (Cont'd)

```
04053 004054  MELSS DEF *+1
04054 020114        ASC 10, LOGICAL SHIFT ERROR
04066 106512        OCT 106612
04067 004066  MELSE DEF *-1
*
04070 004071  MEASS DEF *+1
04071 020131        ASC 10, ARITH. SHIFT ERROR
04103 106512        OCT 106612
04104 004103  MEASE DEF *-1
*
04105 004106  DATAS DEF *+1
04106 042101        ASC 6,DATA+1,DATA=
04114 004113  DATAE DEF *-1
*
04115 004116  TRANS DEF *+1
04116 052122        ASC 7,TRANSFER: B,A=
04125 004124  TRANE DEF *-1
04126 004127  MDLDS DEF *+1
04127 025104        ASC 9,,DOUBLE LOAD ERROR
04140 106512        OCT 106612
04141 004140  MDLDE DEF *-1
*
04142 004143  MDSTS DEF *+1
04143 025104        ASC 10,,DOUBLE STORE ERROR
04155 106512        OCT 106612
04156 004155  MDSTE DEF *-1
*
04157 004160  MHORS DEF *+1
04160 044111        ASC 8,HIGH ORDER NO.=
04170 004167  MHORE DEF *-1
*
04171 004172  MLORS DEF *+1
04172 020114        ASC 8, LOW ORDER NO.=
04202 004201  MLORE DEF *-1
*
04203 004204  MCNTS DEF *+1
04204 045117        ASC 7,LOOP COUNTER=
04213 004212  MCNTE DEF *-1
*
04214 004215  EDIVS DEF *+1
04215 042111        ASC 7,DIVIDEND(B,A)=
04224 004223  EDIVE DEF *-1
*
04225 004226  EQUTS DEF *+1
04226 052525        ASC 6,QUOTIENT(A)=
04234 004233  EQUTE DEF *-1
*
04235 004236  EQXMS DEF *+1
04236 052530        ASC 5,QXM(B,A)=
04243 004242  EQXME DEF *-1
*
04244 004245  QXMRS DEF *+1
04245 052530        ASC 3,QXM+R=
04250 004247  QXMRE DEF *-1
*
04251 004252  REMAS DEF *+1
04252 051105        ASC 7,REMAINDER(B)=
04261 004260  REMAE DEF *-1
*
04262 004263  MOCS DEF *+1
04263 021110        ASC 12,"HDWR OVF=0,SOFTW OVF=1"
04277 106512        OCT 106612
04300 004277  MOCE DEF *-1
*
04301 004302  MOSS DEF *+1
04302 021110        ASC 12,"HDWR OVF=1,SOFTW OVF=0"
04316 106512        OCT 106612
04317 004316  MOSE DEF *-1
```

Table 6. Diagnostic Procedures (Cont'd)

```
*
  04320 004321  MEHIS DEF *+1
  04321 044111        ASC 4,HI ORDER
  04325 004324  MEHIE DEF *-1
*
  04326 004327  MELOS DEF *+1
  04327 046117        ASC 4,LO ORDER
  04333 004332  MELOE DEF *-1
*
  04334 004335  MERRS DEF *+1
  04335 041510        ASC 12,CHECH FOR CAUSE OF ERROR
  04351 106512        OCT 106612
  04352 050125        ASC 10,PUSH RUN TO RESTART
  04364 106512        OCT 106612
  04365 004364  MERRE DEF *-1
*
  04366 004367  MMSBS DEF *+1
  04367 106512        OCT 106612
  04370 050125        ASC 10,PUT MSB INTO SW.REG.
  04402 106512        OCT 106612
  04403 050125        ASC 4,PUSH RUN
  04407 106512        OCT 106612
  04410 004407  MMSBE DEF *-1
*
  04411 004412  MLSBS DEF *+1
  04412 050125        ASC 10,PUT LSB INTO SW.REG.
  04424 106512        OCT 106612
  04425 050125        ASC 4,PUSH RUN
  04431 106512        OCT 106612
  04432 004431  MLSBE DEF *-1
*
  04433 004434  MDVSS DEF *+1
  04434 050125        ASC 13,PUT DIVISOR INTO SW. REG.
  04451 106512        OCT 106612
  04452 050125        ASC 4,PUSH RUN
  04456 106512        OCT 106612
  04457 004456  MDVSE DEF *-1
*
  04460 004461  MOPTS DEF *+1
  04461 106512        OCT 106612   CARRIAGE RETURN,LINE FEED
  04462 051505        ASC 21,SET SW. REG. FOR CONTROL OPTIONS-PUSH R
  04507 106512        OCT 106612
  04510 004507  MOPTE DEF *-1
*
  04511 004512  EXITS DEF *+1
  04512 042530        ASC 12,EXIT-PUSH RUN TO RESTART
  04526 106512        OCT 106612    CARRIAGE RETURN,LINE FEED
  04527 004526  EXITE DEF *-1
*
  04530 004531  OCTAS DEF *+1
  04531 020050        ASC 4, (OCTAL)
  04535 004534  OCTAE DEF *-1
```

Table 7. Replaceable Parts

Reference Designation	hp Part No.	Description #	Note
	02116-6196	EXTENDED ARITHMETIC TIMING	
	02116-8196	BOARD:BLANK PC	
C1-C6	0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	
MC12	1820-0956	INTEGRATED CIRCUIT	
MC13	1820-0954	INTEGRATED CIRCUIT	
MC14	1820-0967	INTEGRATED CIRCUIT	
MC15	1820-0954	INTEGRATED CIRCUIT	
MC16	1820-0965	INTEGRATED CIRCUIT	
MC17	1820-0956	INTEGRATED CIRCUIT	
MC22	1820-0952	INTEGRATED CIRCUIT	
MC23	1820-0971	INTEGRATED CIRCUIT	
MC24	1820-0967	INTEGRATED CIRCUIT	
MC25	1820-0954	INTEGRATED CIRCUIT	
MC27	1820-0956	INTEGRATED CIRCUIT	
MC26	1820-0965	" "	
MC32	1820-0952	INTEGRATED CIRCUIT	
MC33	1820-0971	INTEGRATED CIRCUIT	
MC34	1820-0967	INTEGRATED CIRCUIT	
MC35	1820-0954	INTEGRATED CIRCUIT	
MC36	1820-0956	INTEGRATED CIRCUIT	
MC37	1820-0956	INTEGRATED CIRCUIT	
MC42	1820-0956	INTEGRATED CIRCUIT	
MC43	1820-0956	INTEGRATED CIRCUIT	
MC44	1820-0967	INTEGRATED CIRCUIT	
MC45	1820-0953	INTEGRATED CIRCUIT	
MC46	1820-0956	INTEGRATED CIRCUIT	
MC47	1820-0956	INTEGRATED CIRCUIT	
MC52	1820-0965	INTEGRATED CIRCUIT	
MC53	1820-0966	INTEGRATED CIRCUIT	
MC54	1820-0953	INTEGRATED CIRCUIT	
MC55	1820-0971	INTEGRATED CIRCUIT	
MC56	1820-0965	INTEGRATED CIRCUIT	
MC57	1820-0956	INTEGRATED CIRCUIT	
MC62	1820-0953	INTEGRATED CIRCUIT	
MC63	1820-0967	INTEGRATED CIRCUIT	
MC65	1820-0966	" "	
MC64	1820-0953	INTEGRATED CIRCUIT	
MC66	1820-0965	INTEGRATED CIRCUIT	
MC67	1820-0966	INTEGRATED CIRCUIT	
MC73	1820-0967	INTEGRATED CIRCUIT	
MC74	1820-0953	INTEGRATED CIRCUIT	
MC75	1820-0964	INTEGRATED CIRCUIT	
MC76	1820-0965	INTEGRATED CIRCUIT	
MC77	1820-0954	INTEGRATED CIRCUIT	
MC82	1820-0965	INTEGRATED CIRCUIT	

 # See introduction to this section for ordering information

Table 7. Replaceable Parts (Cont'd)

Reference Designation	Part No.	Description #	Note
MC83	1820-0966	INTEGRATED CIRCUIT	
MC84	1820-0968	INTEGRATED CIRCUIT	
MC85	1820-0971	INTEGRATED CIRCUIT	
MC86	1820-0965	INTEGRATED CIRCUIT	
MC87	1820-0952	INTEGRATED CIRCUIT	
MC93	1820-0965	INTEGRATED CIRCUIT	
MC94	1820-0971	INTEGRATED CIRCUIT	
MC95	1820-0971	INTEGRATED CIRCUIT	
MC96	1820-0968	INTEGRATED CIRCUIT	
MC97	1820-0964	INTEGRATED CIRCUIT	
MC105	1820-0965	" "	
MC103	1820-0965	INTEGRATED CIRCUIT	
MC104	1820-0965	INTEGRATED CIRCUIT	
MC106	1820-0968	INTEGRATED CIRCUIT	
MC107	1820-0964	INTEGRATED CIRCUIT	
MC114	1820-0952	INTEGRATED CIRCUIT	
MC115	1820-0964	INTEGRATED CIRCUIT	
MC116	1820-0968	INTEGRATED CIRCUIT	
MC117	1820-0964	INTEGRATED CIRCUIT	
MC124	1820-0964	INTEGRATED CIRCUIT	
MC125	1820-0965	INTEGRATED CIRCUIT	
MC126	1820-0968	INTEGRATED CIRCUIT	
MC127	1820-0964	INTEGRATED CIRCUIT	
	02116-6202	EXTENDED ARITHMETIC LOGIC	
	02116-8202	BOARD:BLANK PC	
C1-C6	0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	
MC14	1820-0966	INTEGRATED CIRCUIT	
MC15	1820-0966	INTEGRATED CIRCUIT	
MC16	1820-0966	INTEGRATED CIRCUIT	
MC17	1820-0956	INTEGRATED CIRCUIT	
MC22	1820-0965	INTEGRATED CIRCUIT	
MC23	1820-0964	INTEGRATED CIRCUIT	
MC24	1820-0971	INTEGRATED CIRCUIT	
MC25	1820-0971	INTEGRATED CIRCUIT	
MC26	1820-0971	INTEGRATED CIRCUIT	
MC27	1820-0956	INTEGRATED CIRCUIT	
MC33	1820-0966	INTEGRATED CIRCUIT	
MC34	1820-0965	INTEGRATED CIRCUIT	
MC35	1820-0971	INTEGRATED CIRCUIT	
MC36	1820-0971	INTEGRATED CIRCUIT	
MC37	1820-0956	INTEGRATED CIRCUIT	
MC42	1820-0952	INTEGRATED CIRCUIT	
MC43	1820-0968	INTEGRATED CIRCUIT	
MC44	1820-0953	INTEGRATED CIRCUIT	

 # See introduction to this section for ordering information

Table 7. Replaceable Parts (Cont'd)

Reference Designation	Part No.	Description #	Note
MC45	1820-0953	INTEGRATED CIRCUIT	
MC46	1820-0971	INTEGRATED CIRCUIT	
MC47	1820-0952	INTEGRATED CIRCUIT	
MC51	1820-0954	INTEGRATED CIRCUIT	
MC52	1820-0971	INTEGRATED CIRCUIT	
MC53	1820-0966	INTEGRATED CIRCUIT	
MC54	1820-0971	INTEGRATED CIRCUIT	
MC55	1820-0971	INTEGRATED CIRCUIT	
MC56	1820-0971	INTEGRATED CIRCUIT	
MC57	1820-0956	INTEGRATED CIRCUIT	
MC61	1820-0964	INTEGRATED CIRCUIT	
MC62	1820-0952	INTEGRATED CIRCUIT	
MC63	1820-0952	INTEGRATED CIRCUIT	
MC64	1820-0966	INTEGRATED CIRCUIT	
MC65	1820-0953	INTEGRATED CIRCUIT	
MC66	1820-0953	INTEGRATED CIRCUIT	
MC67	1820-0956	INTEGRATED CIRCUIT	
MC72	1820-0952	INTEGRATED CIRCUIT	
MC73	1820-0968	INTEGRATED CIRCUIT	
MC75	1820-0966	INTEGRATED CIRCUIT	
MC76	1820-0964	INTEGRATED CIRCUIT	
MC77	1820-0971	INTEGRATED CIRCUIT	
MC82	1820-0966	INTEGRATED CIRCUIT	
MC83	1820-0966	INTEGRATED CIRCUIT	
MC84	1820-0971	INTEGRATED CIRCUIT	
MC85	1820-0971	INTEGRATED CIRCUIT	
MC86	1820-0956	INTEGRATED CIRCUIT	
MC87	1820-0971	INTEGRATED CIRCUIT	
MC91	1820-0965	INTEGRATED CIRCUIT	
MC92	1820-0964	INTEGRATED CIRCUIT	
MC93	1820-0954	INTEGRATED CIRCUIT	
MC94	1820-0964	INTEGRATED CIRCUIT	
MC95	1820-0966	INTEGRATED CIRCUIT	
MC96	1820-0971	INTEGRATED CIRCUIT	
MC97	1820-0956	INTEGRATED CIRCUIT	
MC101	1820-0965	INTEGRATED CIRCUIT	
MC102	1820-0965	INTEGRATED CIRCUIT	
MC103	1820-0966	INTEGRATED CIRCUIT	
MC104	1820-0966	INTEGRATED CIRCUIT	
MC105	1820-0966	INTEGRATED CIRCUIT	
MC106	1820-0971	INTEGRATED CIRCUIT	
MC107	1820-0966	INTEGRATED CIRCUIT	
MC112	1820-0968	INTEGRATED CIRCUIT	
MC113	1820-0966	INTEGRATED CIRCUIT	
MC114	1820-0953	INTEGRATED CIRCUIT	
MC115	1820-0966	INTEGRATED CIRCUIT	
MC116	1820-0964	INTEGRATED CIRCUIT	
MC117	1820-0956	INTEGRATED CIRCUIT	
MC122	1820-0964	INTEGRATED CIRCUIT	
MC123	1820-0971	INTEGRATED CIRCUIT	
MC124	1820-0966	INTEGRATED CIRCUIT	
MC125	1820-0953	INTEGRATED CIRCUIT	
MC126	1820-0964	INTEGRATED CIRCUIT	
MC127	1820-0954	INTEGRATED CIRCUIT	

 # See introduction to this section for ordering information

Table 8. Part Number Index

℗ Part No.	Description #	Mfr.	Mfr. Part No.	TQ	RS
0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2	12	
1820-0952	INTEGRATED CIRCUIT	28480	1820-0952	9	
1820-0953	INTEGRATED CIRCUIT	28480	1820-0953	11	
1820-0954	INTEGRATED CIRCUIT	28480	1820-0954	8	
1820-0956	INTEGRATED CIRCUIT	28480	1820-0956	18	
1820-0964	INTEGRATED CIRCUIT	28480	1820-0964	15	
1820-0965	INTEGRATED CIRCUIT	28480	1820-0965 19	16	
1820-0966	INTEGRATED CIRCUIT	28480	1820-0966 22	20	
1820-0967	INTEGRATED CIRCUIT	28480	1820-0967	6	
1820-0968	INTEGRATED CIRCUIT	28480	1820-0968	8	
1820-0971	INTEGRATED CIRCUIT	28480	1820-0971 22	23	
02116-6196	EXTENDED ARITHMETIC TIMING	04404	02116-6196	1	
02116-6202	EXTENDED ARITHMETIC LOGIC	04404	02116-6202	1	
02116-8196	BOARD:BLANK PC	04404	02116-8196	1	
02116-8202	BOARD:BLANK PC	04404	02116-8202	1	

 # See introduction to this section for ordering information

EAU TIMING (02116-6196)

OPERATION CYCLE COUNTER

OPERATION CYCLE DECODER

DOUBLE STORE TIMING

DOUBLE LOAD TIMING

OPERATION EXIT

INHIB

OPERATION DECODER

DIVIDE TIMING

MULTIPLY TIMING

MD2 GATING

MEMORY AND PHASE CONTROL

RSET PH5 RF2 RT RT RO ROT5 PI23 ISG DI D2 D3 D4 D5 D6 D5L8 MP1 MP2 MP3 MP4 MP5 TBI5

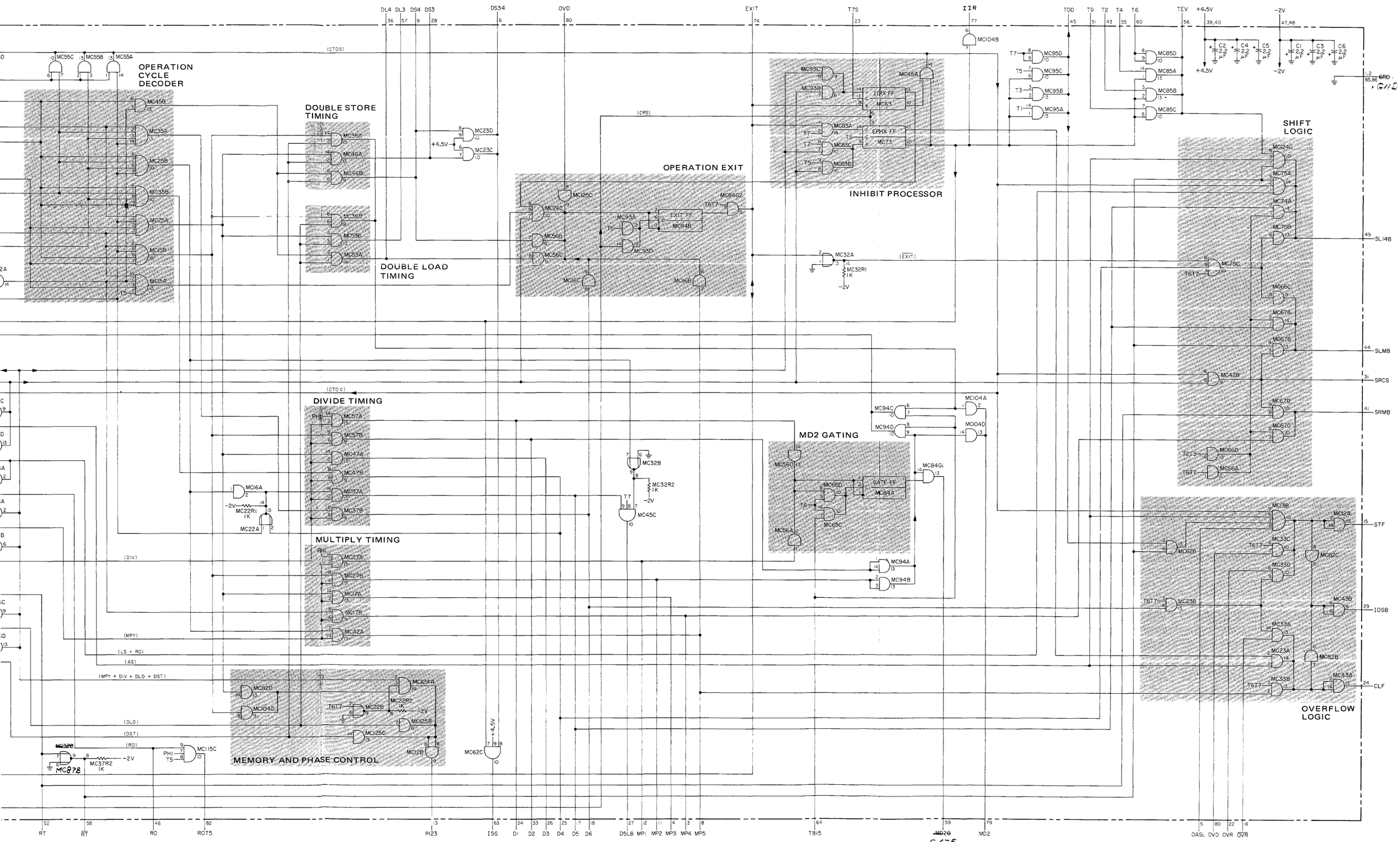


Figure 8. Extended Arithmetic Timing Board

EAU LOGIC (02116-6202) ECN 757

EAU TIMING SIGNALS FROM TIMING BOARD (02116-6196)

MP1 59 → MP1
MP2 5 → MP2
MP3 69 → MP3
MP4 46 → MP4
MP5 9 → MP5
DI 62 → DI
D2 60 → D2
D3 27 → D3
D4 6 → D4
D5 73 → D5
D6 8 → D6
DS3 67 → DS3
DS4 52 → DS4
DS34 14 → DS34
DL3 70 → DL3
DL4 18 → DL4
AS 84 → AS
RO 75 → RO
$\overline{RT}$ 78 → $\overline{RT}$
RT 57 → RT
ROT5 68 → ROT5
TEV 81 → TEV
TOD 82 → TOD
SRCS 83 → SRCS
D5L8 71 → D5L8
GATE 76 → GATE
EXIT 17 → EXIT
MD2 16 → MD2
TS 39 → TS

FROM COMPUTER

RBI5 77 → RBI5
CI6 50 → CI6
TO 15 → TO
TOTI 36 → TOTI
TI 13 → TI
MCI01D: 14, 13 → TI+T5
MCI01A: 1, 2
T5 54 → T5
T3 32 → T3
MC22C: 8, 9 → T3+T7
MC22B: 7, 6
T7 28 → T7
TIT2 51 → TIT2
T3T4 74 → T3T4
T4T5 23 → T4T5
T6 30 → T6
T6T7 11 → T6T7
T2 22 → T2
T4 24 → T4
MC47B: 7, 13,6
MC47A: 1, 9, 2, 8
MC47R2 1K → −2V
T2T3 21 → T2T3
MC47R1 1K → −2V
+4.5V 39, 40 → +4.5V
C1 2.2μF, C2 2.2μF, C3 2.2μF
−2V 47, 48 → −2V
C4 2.2μF, C5 2.2μF, C6 2.2μF
GND 1,2, 65,86

SB0 44
TBI5 80
TB0 79
SWSA 66

OUTPUT TO SB0

MP5 1, MC65A 14
TIT2 2
T6T7 2, MC33A 14
EXIT 1
MC23B 6, T4T5 3, MC65B 13
D6 6
MP5 9, MC33D 10
D3 5, MC33C 10
MC67A 2, 14, 13
D6 9, TIT2 8, MC65C 10
GATE 9, T3T4 8, MC5IB 10, MD2 6

OUTPUT TO TB15

MP4 6, T3+T7 7, MCI26C 10
RT 1, SRCS 2, TOD 9, MCI27B 10, MCII7A 2, 14, 13
RO 14, SRCS 3, MCI27A 13
MD2 3, AS 2, MCI26A 15

(LINK)

OUTPUT TO TB0

$\overline{RT}$ 6, SRCS 3, MCII4B 13
TEV 1, 4, MCII4A 14
TOD 2, MCII5A 14
MCII5D 8, 9, 10
D5L8 4, MCII5B 13, MCII7B 6, 5, 9
D5 8, T3 9, 7, MCII6C 10
T7 3, 2, MCII6A 14
MCII5C 6, 7, 10

MULTIPLICATION ADD FUNCTION

MP4 3, T3+T7 4, MC33B 13
GATE 1, T4 2, MP2 3, MC23A 14
MAF FF, MC73A 2, 1, C, 15
MP5 1, MC22A 2
D6 1, MC34A 2

(MP5+D6)
(MAF)

STORE IN A

D2 1, T4 3, 14, MC93A 13
GATE 2, MC94A 3, 14
T0+T2 2, 6, MC94B 13, MC97A 2, 14, 13
T5 9, DI 7, MC94C 8, 10
T2 8, MP3 9, MCI07D 10
DL3 6, T4 7, MCI07C 10

(SMD)
(SIGN)
(CARRY)
(SMD/SDD)
(SIGN)
($\overline{OVD}$)

LINK

MCI23D 8, 9, 10
MP4 6
SRCS 5, MCI23C 7, 10
RBI5 1, D4 14, MCI23A 13
RBI5 2, D5 3, MCI23B 12
TEV 14, TS 2, MCI24A
MCU26Z +4.5V 8, 9
LINK FF, MCI12B C, 7, 6

MCI25A 14, RT 2, TEV 1
MCI25B 3, 6, 13
SRCS 7
MCI25C $\overline{RT}$ 8, TOD 9, 10

$\overline{RT}$ 2, RBI5 14, MCI03A 1
RT 3, MCI03B 4, 13

MCI05D 9, 10, T6 8
MCI05C 7, 10, D5 6
MCI05B 4, 13, T2 3
MCI05A 1, 2, 14
T3+T7 3, MCI07B MP4 4, 13
$\overline{RT}$ 9, TEV 8, MCI25C 7, 10
SRCS 1, MCI22A RT 3, TOD 2, 14

CARRY (EAU)

MCI03C 1, 9, 10
ROT5 8, MCI24D $\overline{RT}$ 9, 10
MCI24C $\overline{RT}$ 7, 10, MCI24B 12, RO 4, 13
ROT5 6, MCI22B 13
RO 7, TOD 5, MCII3C 10
D2 1, MCI02A 2
D2 7, GATE 8, T4 9, MCI22C 10
MP5 14, MCI02D 13
MP5 4, MCII3B 13
D5 7, MCI02B 6
D5 8, TI+T5 9, MCII3D 10
MCI03D 6, 10, CI6 7
CARX FF, MCI12A 1, 2, C, 13
TS 1, MCI13A 14, 2

(SMR-MP3)
(SMR/SDV)
(SMR/SDV)

OUTPUT TO RB0

MC67B 6, 9, 8
MC64A 14, 1, MP3 2, T6T7
MC66B 13, 6, DL3 5, T6T7
MC66A 14, DS3 2, T6T7
MC66C 15, 9, D4 7, T2T3

SIGN (MULTIPLICAND/DIVIDEND) (MULTIPLIER/DIVISOR)

MC52A DI 14, 13
MC52B T4 12, MPI 5, 13
MC52C D3 6, 10, T7 7
MC52D MP3 8, 10, T3 9
MC53B 4, 3, 13
MC53A 7, 2, 14
SMD/SDD FF, MC43A 2, C, 1, 13
SMR/SDV FF, MC43B 6, C, 7, 9
MC53C 10, MC53D 9, 10
MC42B 9, MC42R2 1K → −2V, MC42A 13, MC42RI 1K → −2V
MC107A 2, 14, MP3 1

OVERFLOW

MC62A 1, 2, 13, 14
MC62RI 1K → −2V
SIGN 7, MC62B 6, 9
MC62R2 1K → −2V
CI6 2, MC63A 13
MC63RI 1K → −2V
T3 3, MC83B 4, 13 → −2V
D4 5, MC83C 7, 10
T5 9, D6 8, MC83D 10
T2

($\overline{SMR}$)

RBO 93
RSET 63

SWSA 66
SWSB 10
SWSM 33
SWSP 3
SWST 20
RARB 65

STORE IN A
STORE IN B
STORE IN M
STORE IN P
STORE IN T
READ A
READ B
READ M
READ P
READ T
MULTIPLICATION ADD FUNCTION
CARRY (EAU)
OVERFLOW
SHIFT OVERFLOW
COMPLEMENT FUNCTION
ADD FUNCTION
"EXCLUSIVE OR" FUNCTION

(MP5+D6)
(MAF)
(SMD/SDD)
(SIGN)
(ŌVD)
(T7(ŌVD)+D5L8)
(SMR-MP3)
(SMR/SDV)
(SMR/SDV)
(MP4+D5)

OVR 35
OVD 56
ŌVR 64
RBI4 25
OASL 31
CMFB 72
ADF 12
EOFB 26
RRRB 58
RMSB 34
RTSB 19
RPRB 4

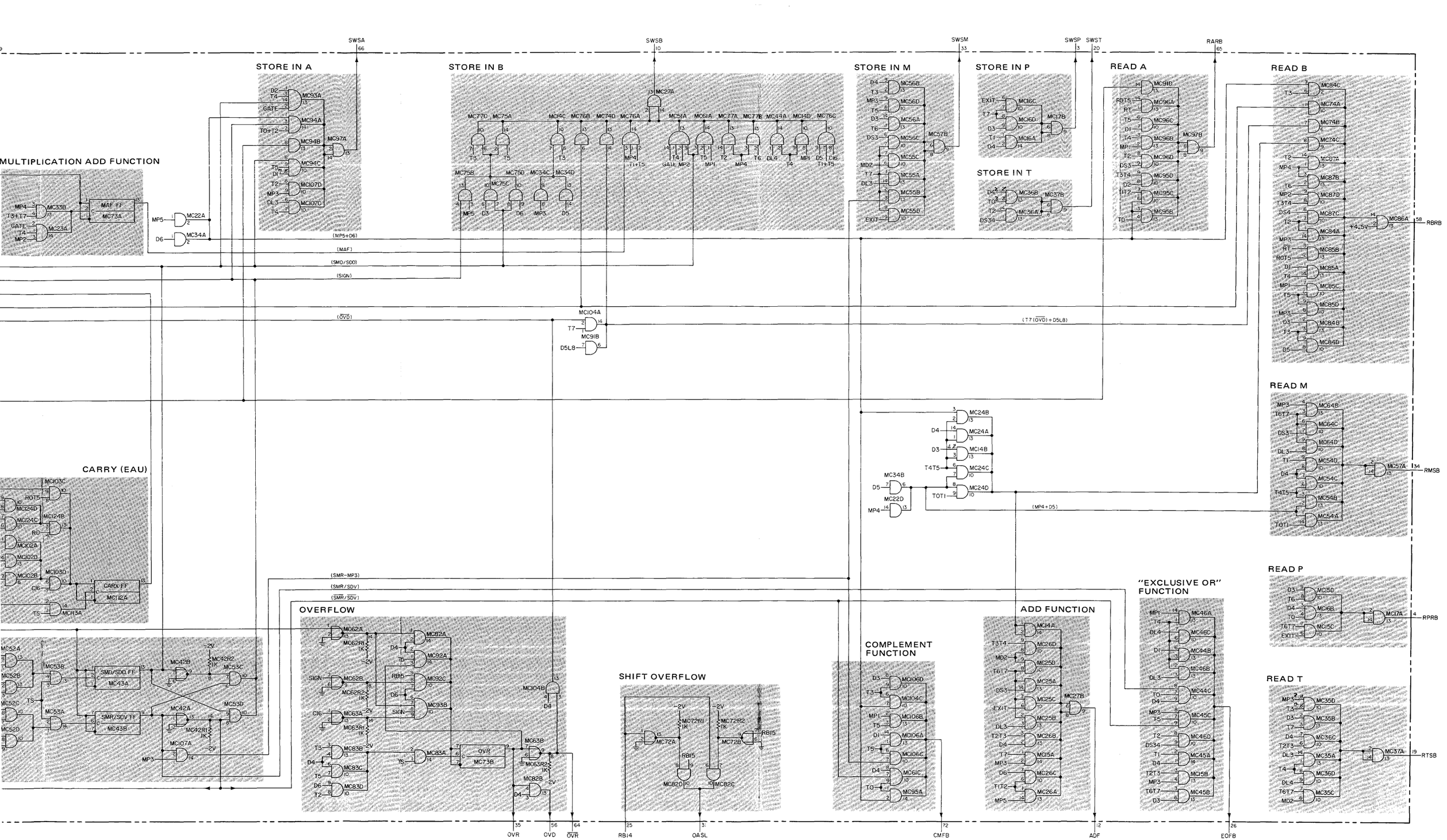


Figure 9. Extended Arithmetic Logic Board

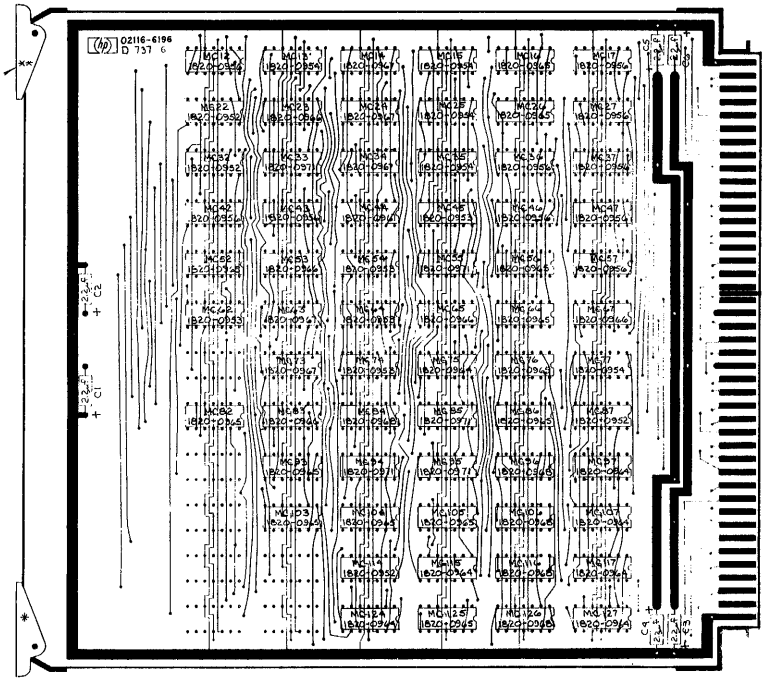


Figure 10. Components on EAU Timing Card

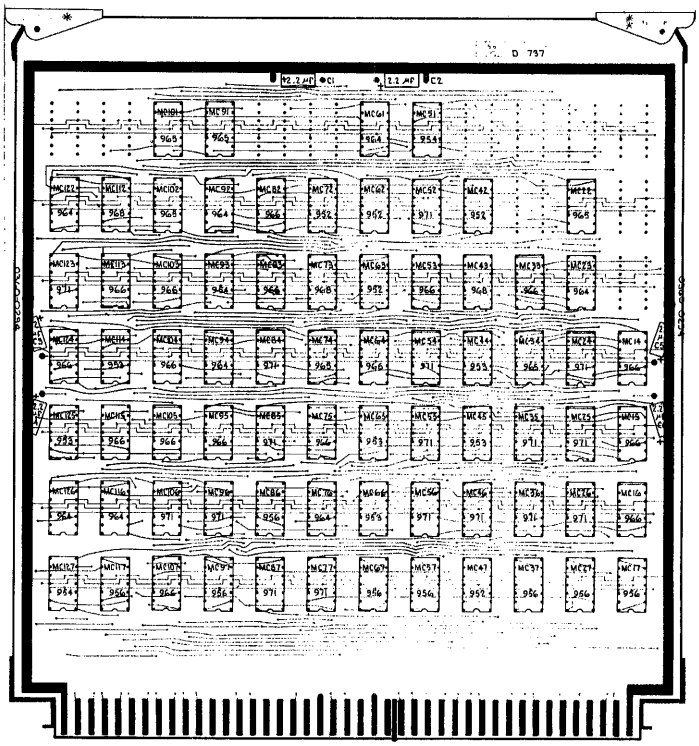


Figure 11. Components on EAU Logic Card

HEWLETT hp PACKARD

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

All Hewlett-Packard products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

For any assistance contact your nearest Hewlett-Packard Sales and Service Office.

HEWLETT hp PACKARD

12579A

EXTENDED ARITHMETIC UNIT

(FOR 2115A AND 2116A/B/C COMPUTERS)

UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

25 AUGUST 1971

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

Manual Printed: 15 May 1968

Manual Part Number: 12579-9001

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes
– – –	Extended Arithmetic Timing Board	02116-6196	E-839-6	1

Errata A and B and Change 1 dated 16 October 1968.
Errata C dated 13 June 1969.
Errata D through P dated 18 March 1970.
Errata Q through S dated 8 June 1970.
Errata T through Z dated 25 November 1970.
Errata AA and AB dated 15 December 1970.
Errata AC through AG dated 1 March 1971.
Errata AH dated 25 August 1971.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221

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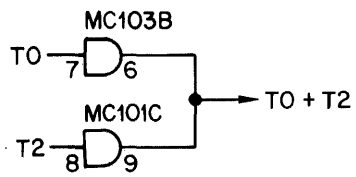
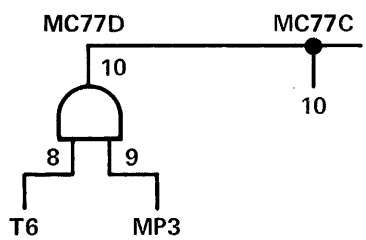
Printed in U.S.A.

ERRATA	DESCRIPTION
A	Make the following changes to Figure 8, Extended Arithmetic Timing Board: a. Below the Operation Decoder area (lower-left) of the diagram, change the microcircuit designations as follows: change MC64B to MC97B change MC64A to MC115A change MC37B to MC87B b. At pin 59 of the diagram (lower-right), change the signal mnemonic from "MD2G" to "GATE".
B	Make the following changes to Figure 9, Extended Arithmetic Logic Board: a. At the left edge of the diagram just below signal MD2 at pin 16, add input signal TS at pin 29. b. At the lower-left corner of the diagram, change the output pin for signal RBO from pin 93 to pin 43. c. In the "Output to TB15" area (upper-left) of the diagram, at pin 3 of "and" gate MC126A, change the signal from "MD2" to "RB15". d. In the "Output to TBO" area (upper-left) of the diagram, at the input to "and" gate MC114A, reverse the numbering of the input pins. e. Below the "Output to TBO" area (middle-left) of the diagram, change the designation of "and" gate MC125C to MC114C. f. In the "Store in A" area (upper-center) of the diagram, at the input to "and" gate MC94C, change the input pin 5 to pin 7. g. In the "Store in T" area (upper-right) of the diagram, at the input to "and" gate MC36B, reverse the numbering of the input pins. h. Below the "Store in T" area (middle-right) of the diagram, at the input to "and" gate MC14B, change the input pin 2 to pin 4. i. In the "Read T" area (lower-right) of the diagram, at the input to "and" gate MC35D, reverse the numbering of the input pins. j. At the lower-left of the diagram between the "Output to RBO", "Carry", and "Sign" areas, add the following circuit diagram. 
C and D	Replaced by ERRATA changes AE and AF.
E	Replaced by ERRATA change U.
F	Page 9, table 5. Delete signal mnemonic MD2G.

ERRATA	DESCRIPTION
G	Page 14, table 7. Change the part number for integrated circuit MC23 from 1820-0971 to "1820-0966".
H	Page 14, table 7. Add "MC26, 1820-0965, Integrated Circuit" in the appropriate columns.
I	Page 14, table 7. Add "MC65, 1820-0966, Integrated Circuit" in the appropriate columns.
J	Page 15, table 7. Add "MC105, 1820-0965, Integrated Circuit" in the appropriate columns.
K	Page 17/18, table 8. Change the amount figures in the "TQ" column as follows: 1820-0965 from 16 to 19. 1820-0966 from 20 to 22 1820-0971 from 23 to 22
L	Page 19/20, Figure 8. In the "Operation Cycle Decoder" area (upper-left) of the diagram, at "and" gate MC35B input pin 9, show input pin 9 connected to the line common to input pins 3 and 2 of "and" gates MC45B and MC15A respectively. Remove the connection to output pin 10 of MC44.
M	Page 19/20, Figure 8. In the upper-right of the diagram, change the ground signal from "GRD" to GND.
N	Page 21/22, Figure 9. In the lower-left of the diagram, change the ground signal from "GRD" to GND.
O	Page 21/22, Figure 9. In the upper-left of the diagram, immediately following the words "EAU LOGIC (02116-6202)", add "REV. 737".
P	Page 19/20, Figure 8. In the upper-left of the diagram, immediately following the words "EAU TIMING (02116-6196)", add "REV. 737".
Q, R, and S	Replaced by ERRATA changes AE and AF.
T	Page 1, paragraphs 2 and 4. Change all references to "2116A/2115A Computers" to read "2115A or 2116A/B/C Computers."
U	Page 1, table 3. Change "HP 2116A/B" to "HP 2116A/B/C."
V	Page 1. Enter the part no. of the manual in the lower left corner of the page, as follows: 12579-9001.
W and X	Replaced by ERRATA changes AE and AF.
Y	Page 21/22, figure 9, Extended Arithmetic Logic Board. Add an "and" gate (MC77D) to the left side of the "Store in B" circuit as follows:



ERRATA	DESCRIPTION

Z

Page 3, table 4. Under the heading "*n=number of shifts or rotates" change to read as follows:

1 = 1 shift or rotate
2 = 2 shifts or rotates
3 = 3 shifts or rotates
4 = 4 shifts or rotates
5 = 5 shifts or rotates
6 = 6 shifts or rotates
7 = 7 shifts or rotates
10 = 8 shifts or rotates
11 = 9 shifts or rotates
12 = 10 shifts or rotates
13 = 11 shifts or rotates
14 = 12 shifts or rotates
15 = 13 shifts or rotates
16 = 14 shifts or rotates
17 = 15 shifts or rotates
0 = 16 shifts or rotates

AA

Page 9, table 5. Add a signal mnemonic definition to the table as follows:

NEW	DEFINITION
TRO-15	T-register bits 0-15

AB

Page 19/20, Figure 8. In the lower right of the diagram, connect a line from pin 1 of gate MC23A to the border line of the diagram. Label the line with pin number "50" and mnemonic "AS," at the border line.

AC

Page 1, following paragraph 2. Add paragraphs 2A and 2B as follows:

2A. CURRENT REQUIRED FROM COMPUTER.

2B. To operate its logic circuits, the EAU option requires 4.68 amperes from the +4.5-volt computer power supply and 3.3 amperes from the -2-volt computer power supply.

AD

Page 1, table 2. Change table to read as follows:

Table 2. Shift-Rotate Execution Times

NUMBER OF SHIFTS OF ROTATIONS	EXECUTION TIMES	
	2115	2116A/B/C
1 to 4	4.0 μs	3.2 μs
5 to 8	6.0 μs	4.8 μs
9 to 12	8.0 μs	6.4 μs
13 to 16	10.0 μs	8.0 μs

Note

ERRATA changes AE and AF replace all previous diagnostic program data with references to the new diagnostic program procedures contained in the Manual of Diagnostics.

ERRATA	DESCRIPTION
AE	Page 8, paragraph 34. Replace paragraph 34 with the following paragraph: 34. The EAU may be checked using the Diagnostic Program Procedures, part no. 12579-90013, contained in the Manual of Diagnostics. These diagnostic procedures confirm proper operation of the EAU by running non-EAU subroutines and EAU instructions with the same arguments and then comparing the actual results with the expected results.
AF	Pages 10 through 13, table 6. Delete table 6 entirely.
AG	Page 19/20, Figure 8. At the top-center of the diagram, change pin 6 designation from DS34 to DS3,4.
AH	Page 19/20, Figure 8. At the upper-left of the diagram, in the "OPERATION CYCLE COUNTER" area, change the signal designation at pin 1 of MC77A from "T3" to "TOD".

CHANGE	DESCRIPTION
1	Note Determine whether the following change information is applicable to the assembly installed in the computer before changing the manual. Make the following change to Extended-Arithmetic Timing Board (part no. 02116-6196, Rev. 839). a. Page 19/20, Figure 8. In the Operation Cycle Counter area (upper-left) of the diagram, at "and" gates MC54C and MC64C, change the timing signal at input pins 9 from T3 to "T4". b. Page 19/20, Figure 8. In the upper-left of the diagram, immediately following the words "EAU TIMING (02116-6196)", add "REV. 839".

HEWLETT hp PACKARD

EXTENDED ARITHMETIC UNIT (EAU)

model 12579A

UPDATING SUPPLEMENT 8 JUNE 1970

MANUAL IDENTIFICATION

Manual Serial Prefixed: --

Manual Printed: 15 May 1968

Manual Part Number: 12579-9001

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Prefix-Serial	Changes

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes
--	Extended Arithmetic Timing Board	02116-6196	E-839-6	1

NOTE:

Errata A through B dated 16 OCT 68.

Errata C dated 13 JUNE 69.

Errata D through P dated 18 MAR 70.

Errata Q through S dated 8 JUN 70.

Change 1 dated 16 OCT 68.

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ERRATA

A. Make the following changes to Figure 8, Extended Arithmetic Timing Board:

a. Below the Operation Decoder area (lower-left) of the diagram, change the microcircuit designations as follows.

change MC64B to MC97B
change MC64A to MC115A
change MC37B to MC87B

b. At pin 59 of the diagram (lower-right), change the signal mnemonic from "MD2G" to "GATE".

B. Make the following changes to Figure 9, Extended Arithmetic Logic Board:

a. At the left edge of the diagram just below signal MD2 at pin 16, add input signal TS at pin 29.

b. At the lower-left corner of the diagram, change the output pin for signal RBO from pin 93 to pin 43.

c. In the "Output to TB15" area (upper-left) of the diagram, at pin 3 of "and" gate MC126A, change the signal from "MD2" to "RB15".

d. In the "Output to TBO" area (upper-left) of the diagram, at the input to "and" gate MC114A, reverse the numbering of the input pins.

e. Below the "Output to TBO" area (middle-left) of the diagram, change the designation of "and" gate MC125C to MC114C.

f. In the "Store in A" area (upper-center) of the diagram, at the input to "and" gate MC94C, change the input pin 5 to pin 7.

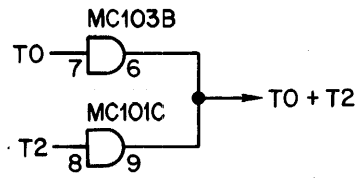
B. (Cont)

g. In the "Store in T" area (upper-right) of the diagram, at the input to "and" gate MC36B, reverse the numbering of the input pins.

h. Below the "Store in T" area (middle-right) of the diagram, at the input to "and" gate MC14B, change the input pin 2 to pin 4.

i. In the "Read T" area (lower-right) of the diagram, at the input to "and" gate MC35D, reverse the numbering of the input pins.

j. At the lower-left of the diagram between the "Output to RBO", "Carry", and "Sign" areas, add the following circuit diagram.



C. Page 10, table 6, Diagnostic Procedures. Delete the paragraphs at the bottom of the page entitled "TO START TEST" and "AFTER TURNING COMPUTER OFF".

D. Page 10, table 6, Diagnostic Procedures. Add the following steps immediately after the "PROGRAM CONTROLLED HALTS" paragraph.

1. Load the extended arithmetic diagnostic test tape (no. 20422A).

2. Set the switch register to 002000 and press the LOAD ADDRESS switch.

D. (Cont)

3. Set the switch register to the select code of the teleprinter. (For serial teleprinters, set switch register bit 14 to "1".)

4. Press the PRESET switch, then the RUN switch. The teleprinter will print out "set switch register for control options".

5. Press the PRESET switch, then the RUN switch. Set the switch register bit zero momentarily to "1" and then to "0".

6. The teleprinter will print out the number of tests completed if the diagnostic is being executed correctly. The teleprinter will also print out all errors.

7. After running the diagnostic for approximately 12 minutes, if the switch register bit 6 is a "1", the teleprinter will print out "no. of tests completed = (octal) 000002, 000000". If the switch register bit 6 is a "0", the teleprinter will print out "no. of tests completed = 131072".

8. To exit from the diagnostic, set switch register bit 5 to "1".

E. Page 1, table 3. In the "Computer Model" column, change HP2116A to read "HP2116A/B".

F. Page 9, table 5. Delete signal mnemonic MD2G.

G. Page 14, table 7. Change the part number for integrated circuit MC23 from 1820-0971 to "1820-0966".

H. Page 14, table 7. Add "MC26, 1820-0965, Integrated Circuit" in the appropriate columns.

I. Page 14, table 7. Add "MC65, 1820-0966, Integrated Circuit" in the appropriate columns.

ERRATA

J. Page 15, table 7. Add "MC105, 1820-0965, Integrated Circuit" in the appropriate columns.

K. Page 17/18, table 8. Change the amount figures in the "TQ" column as follows:

1820-0965 from 16 to 19
1820-0966 from 20 to 22
1820-0971 from 23 to 22

L. Page 19/20, Figure 8. In the "Operation Cycle Decoder" area (upper-left) of the diagram, at "and" gate MC35B input pin 9, show input pin 9 connected to the line common to input pins 3 and 2 of "and" gates MC45B and MC15A respectively. Remove the connection to output pin 10 of MC44.

M. Page 19/20, Figure 8. In the upper-right of the diagram, change the ground signal from "GRD" to GND.

N. Page 21/22, Figure 9. In the lower-left of the diagram, change the ground signal from "GRD" to GND.

O. Page 21/22, Figure 9. In the upper-left of the diagram, immediately following the words "EAU LOGIC (02116-6202)", add "REV. 737".

P. Page 19/20, Figure 8. In the upper-left of the diagram, immediately following the words "EAU TIMING (02116-6196)", add "REV. 737".

ERRATA

Q. Page 8, paragraph 34. In fourth line, change revision suffix of HP Accessory Number from "A" to "B".

R. Page 10, table 6, Diagnostic Procedures. In step 1 of the operating procedure, change revision suffix of diagnostic test tape number from "A" to "B". (The operating procedure was added to table 6 by incorporating Errata D of this supplement.)

S. Pages 11, 12, and 13, table 6, Diagnostic Procedures. If using diagnostic test tape number 20422B or a later revision, delete all information contained on these pages.

CHANGE	DESCRIPTION

1.

Note

Determine whether the following change information is applicable to the assembly installed in the computer before changing the manual.

Make the following change to Extended Arithmetic Timing Board (part no. 02116-6196, Rev. 839).

a. Page 19/20, Figure 8. In the Operation Cycle Counter area (upper-left) of the diagram, at "and" gates MC54C and MC64C, change the timing signal at input pins 9 from T3 to "T4".

b. Page 19/20, Figure 8. In the upper-left of the diagram, immediately following the words "EAU TIMING (02116-6196)", add "REV. 839".

UPDATING SUPPLEMENT 16 OCT 68

MANUAL IDENTIFICATION

Manual Serial Prefixed:

Manual Printed: 15 May 1968

Manual Part Number: 12579-9001

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Prefix-Serial	Changes

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes
-	EAU Timing Board	02116-6196	839	1

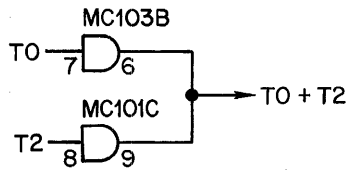
ERRATA

a. Make the following corrections on Figure 8, Extended Arithmetic Timing Board, below the "operation Decoder" block:

Change designation MC64B to "MC97B".
Change designation MC64A to "MC115A".
Change designation MC37B to "MC87B".
Change signal name MD2G to "GATE".

b. Make the following corrections on Figure 9, Extended Arithmetic Logic Board:

Add an input to the board, labeled, TS, pin 29.
Change the pin number of RB0 output from 93 to "43".
In the "Output to TB15" block, change MD2 to "RB15".
In the "Output to TB0" block, reverse the input pin numbers of MC114A.
Below the "Output to TB0" block, change designation MC125C to MC114C.
In the "Store in A" block, change the D1 input pin number from 5 to "7".
In the "Store in T" block, reverse the input pin numbers of MC36B.
Below the "Store in T" block, change the D3 input pin number from 2 to "4".
In the "Read T" block, reverse the input pin numbers of MC35D.
Add 2 gates as follows (any convenient area on the diagram):



CHANGES

1. EAU Timing Boards bearing Revision number 839 have a change in the timing of the Operation Cycle Counter. In Figure 8, change the "T3" designation at the pin 9 inputs of gates MC64C and MC54C to "T4". No other changes to the manual are necessary.

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