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HP 12966A BUFFERED ASYNCHRONOUS COMMUNICATIONS INTERFACE DIAGNOSTIC

reference manual

For HP 2100 Series Computers

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic program confirms proper operation of the HP 12966A Buffered Asynchronous Communications Interface. The basic I/O portion of the interface which includes the Flag and Control ciricits will be tested. The status, control, receive and transmit features will also be tested. The interface will be used with skip on flag, interrupt and Dual-Channel Port Controller (DCPC)*. This test uses a test hood along with special status bits provided for self testing.

1-2. REQUIRED HARDWARE

The following hardware is required:

An HP 2100 Series Computer with a minimum 8K memory.

An HP 12966A Buffered Asynchronous Communications Interface Kit with hooded self-test connector, Part No. 12966-60003 (the self-test connector wiring is shown in figure 1-1).

A teleprinter console device for message reporting (recommended but not required).

A loading device for loading the diagnostic program.

1-3. SOFTWARE REQUIREMENTS

The following software is required:

Diagnostic Configurator (part numbers below) is used for equipment configuration and as a console device driver.

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

HP 12966A Buffered Async Communications Interface Diagnostic:

Binary object tape	Part No. 12966-16001.

The diagnostic serial number (DSN) is contained in memory location 126 (octal) of the program. The DSN for this program is 103017 (octal).

*Or Direct Memory Access (DMA).

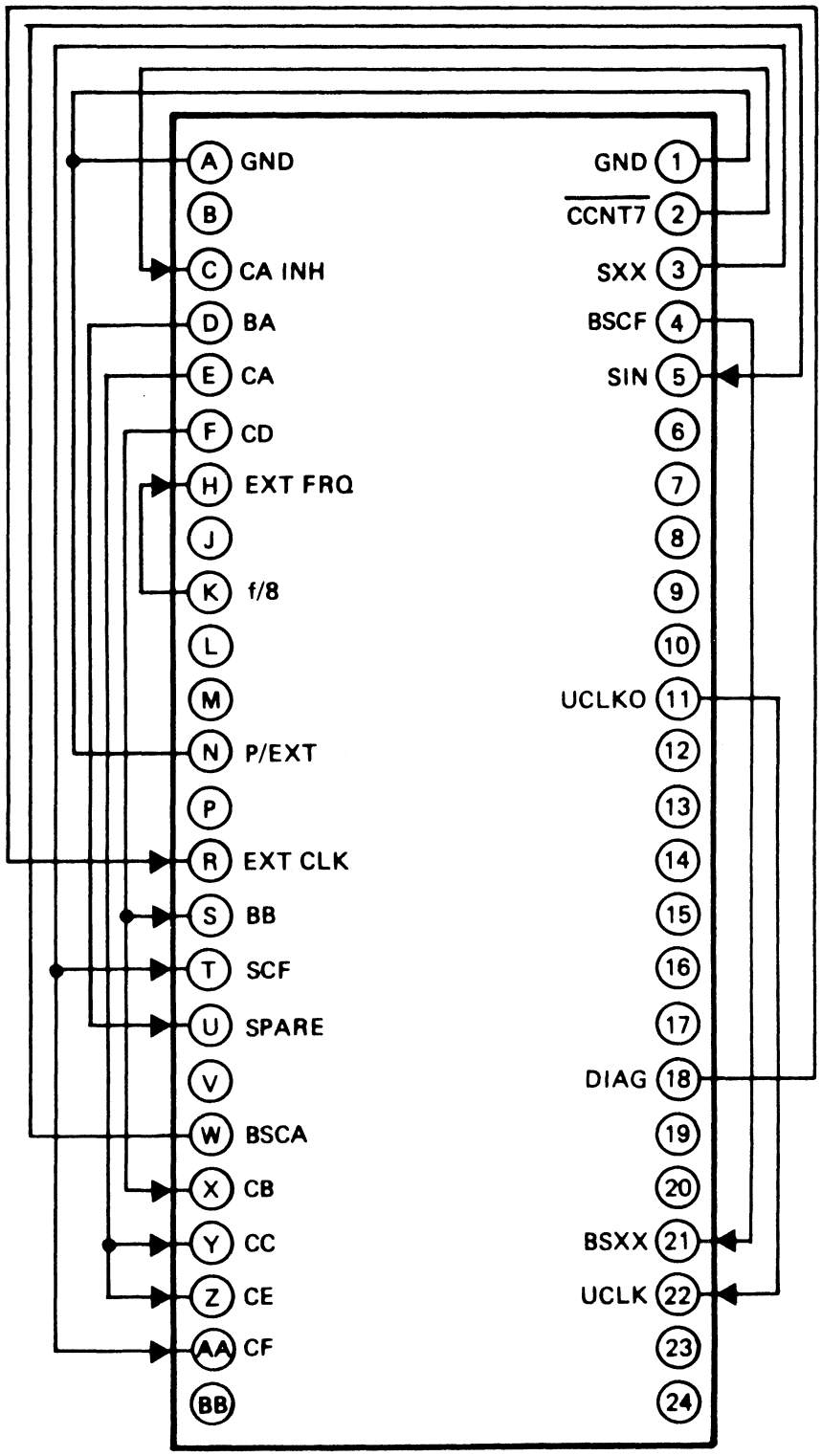

Figure 1-1. Test Connector (12966-60003)

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program consists of 11 tests plus a Control and Initialization section. The Initialization and Control sections accept the select code and options required by the tests. The tests are called into execution by the Control section as sequential or selectable subroutines. The following circuits are placed under test by this diagnostic:

Flag and Control (Basic I/O) - (TSTØØ)
Master Reset Command - (TSTØ1)
Modem related signals - (TSTØ2)
Reference and Enable Commands - (TSTØ3)
First In First Out (FIFO) buffer - (TSTØ4)
Character Counter - (TSTØ5)
Special Character RAM - (TSTØ6)
Transmit operation - (TSTØ7)
Receive operation - (TST1Ø)
Baud rate selection - (TST11)
Parity Error and Overrun - (TST12)
DCPC related circuits and data transfer - (TST13)

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device if present, for operator information then executes the tests according to the options selected on the Switch Register. The control section primarily checks Switch Register bits 15, 13 and 12.

The Control section keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 1Ø is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. Refer to paragraph 2-3.

2-3. SELECTION OF TEST BY OPERATOR

The operator has the capability to select his own tests or sequence of tests with the help of bit 9 in the Switch Register. Paragraph 3-4 outlines the test selection.

2-4. MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used to inform the operator of a failure of the interface to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operation related to the unit's function. In this case an associated halt will occur to allow the operator time to perform the function, the operator must then press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example -- Error with halt

Message: E016 CLC CH ERROR (Console Device)
Halt Code: 102016 (T- or Memory Data Register)

Example - Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024

Example - Information only

Message: H025 BI-O COMP
Halt Code: None

Error messages can be suppressed by selection of Switch Register bit 11 and error halts can be suppressed by Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e. BI-O). When Switch Register bit 12 is set the tests that are selected will be repeated, all operator intervention will be suppressed.

2-5. PROGRAM LIMITATIONS

2-6. PRIORITY STRING

The interface's capability of receiving, passing and denying priority is not completely checked by this diagnostic. If the interface does not receive priority, (PRH from the next lower select code) an error E014 NO INT will occur. To check this remove an interface of a lower select code and run the Basic I/O test and the above mentioned error should occur. Checking the interface's ability to pass or deny priority is beyond the scope of this diagnostic.

2-7. LOGIC ELEMENT

The SBB/BSBB Line Receiver (1820-0990) located at U71 pins 8, 9 and 10 is not placed under test by this diagnostic.

Section III

OPERATING PROCEDURES

3-1. OPERATING PROCEDURES

A flowchart of the operating procedures is provided on the following page, (see figure 3-1). See start points noted below.

If an unconfigured Diagnostic Configurator is to be used start at entry point A.

If a configured Diagnostic Configurator is available start at entry point B.

If a combined configured Diagnostic Configurator and an unconfigured Diagnostic is available start at entry point C.

If a combined configured Diagnostic Configurator and a configurated Diagnostic is available start at entry point D.

Note: Before the Buffered Async Comm Intfc Diagnostic is executed, the test hood must be installed.

3-2. RUNNING THE DIAGNOSTIC

The program will execute the diagnostic according to options selected in the Switch Register. At the completion of each pass of the diagnostic, the pass count is printed on the console device for operator information. If Switch Register Bit 12 was not selected, the computer will halt with 102077 (octal) in the Memory Data Register. At this point, the A-register contains the pass count. To run another pass, the operator need only press RUN.

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000 (octal). Select Switch Register options shown in table 3-2 and press RUN.

If a trap cell halt occurs (106077 octal), the user must determine the cause of the interrupt or transfer of control to the location shown in the M-register. The program may need to be reloaded to continue.

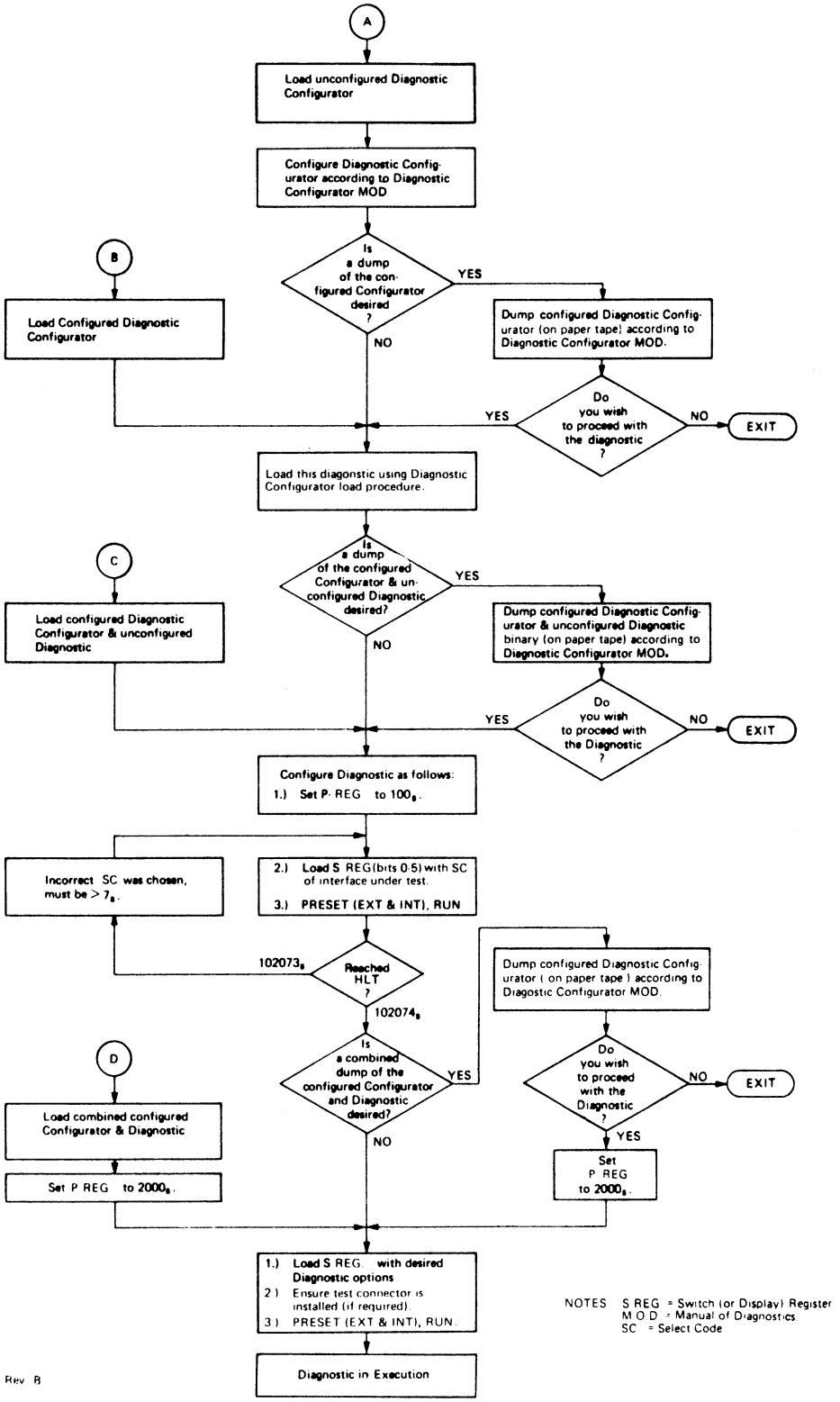

Figure 3-1. Operating Procedure Flowchart

Table 3-1. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
Ø	Test ØØ
1	Test Ø1
2	Test Ø2
3	Test Ø3
4	Test Ø4
5	Test Ø5
6	Test Ø6
7	Test Ø7
8	Test 1Ø
9	Test 11
1Ø	Test 12
11	Test 13
12-15	Reserved
B-Register	Reserved

3-4. TEST SELECTION BY OPERATOR

The Control section of the diagnostic provides the operator with a method to select his own test or sequence of tests, to be run. The operator sets Switch Register bit 9 to indicate the desire to make a selection. The computer will come to a halt 102075 (octal) to indicate it's ready for selection. If the program is running, the current test will be completed, then the program will halt. The operator then loads the A-register with the tests desired. The A-register bit Ø represents Test ØØ, bit 1 represents Test Ø1, and so on through bit 11 which represents Test 13. The operator must then clear Switch Register bit 9 and press RUN. The operators selection will then be run. If the operator clears all bits the standard sequence will be run.

Table 3-2. Switch Register Options

BIT	MEANING IF SET
Ø	Reserved
1	Reserved
2	Report all errors if set. If clear, suppress excessive error reports.
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (1Ø2Ø75); user may specify a new group of tests in the A-register, clear bit 9 and then press RUN.
1Ø	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 1Ø is set or teleprinter is not present. Also those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (1Ø2Ø76) at the end of each test; the A-register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Figure 4-1 illustrates the command formats and the interface status word. Refer to table 4-2 for additional details on the content of each test.

4-2. BASIC I/O TEST ØØ E000 - E026

Subtest 1 - Checks the ability to clear, set and test the interrupt system. The following instruction combinations are tested:

CLF Ø _ SFC Ø
CLF Ø _ SFS Ø
STF Ø - SFC Ø
STF Ø - SFS Ø

Errors in the above sequences produce error messages E000-E003 as shown in table 4-2.

Subtest 2 - Checks the ability to clear, set and test the interface Flag. The following instruction combinations are tested:

CLF SC - SFC SC
CLF SC - SFS SC
STF SC - SFC SC
STF SC - SFS SC

Errors in the above sequence produces error messages E005-E010 as shown in table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the flag and control set on the interface and the interrupt system off. The sequence of instructions is shown below:

STF Ø
STF SC
STC SC
CLF Ø

The CLF Ø instruction should inhibit an interrupt from occurring. Error message E004 occurs if CLF Ø fails.

Subtest 4 - Checks that the flag of the interface under test is not set when all other select code flags are set. Error message E011 occurs if a flag is set incorrectly.

Subtest 5 - Checks the ability of the interface to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt from the Select Code. If not, error message E014 occurs.

Check that the interrupt occurred where expected. Th interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and/or E015 will occur if the hold off fails. This test also checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur. Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the SC Control and Flag set, there is no interrupt following a CLC SC instruction. The following sequence of instructions are used:

```
STC SC
STF SC
STF 0
CLC SC
```

If the CLC SC fails to inhibit an interrupt, error message E016 will occur.

Subtest 7 - Checks that the CLC 0 instruction inhibits interrupts when the SC Control and Flag are set. The following sequence of instructions are used:

```
CLF SC
STC SC
STF SC
STF 0
CLC 0
```

If the CLC Ø fails to inhibit an interrupt, error message EØ17 will occur.

Subtest 8 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the operator panel perform the following actions:

Sets the interface Flag (EXTERNAL).

Clears the interface Control (EXTERNAL).

Turns off the interrupt system (INTERNAL).

Clears the I/O data lines (EXTERNAL).

4-3. MASTER RESET TEST Ø1 EØ3Ø - EØ34

This test provides additional testing of the I/O portion of the interface. The operation on the CLC Ø instruction and the Master Reset Command is verified.

4-4. MODEM STATUS TEST Ø2 EØ35 - EØ42

The test verifies the operation of the three modem control signals (CA, CD and SBA) and the five modem status lines (SBB, CB, CC, CE and CF).

4-5. REFERENCE AND ENABLE COMMANDS TEST Ø3 EØ43 - EØ6Ø

This test verifies the operation of both the Reference and Enable Commands. Also included in this test is the Device Interrupt status bit.

4-6. FIRST IN FIRST OUT BUFFER TEST Ø4 EØ61 - EØ64

This test confirms proper FIFO operation by the use of three test patterns. The first pattern is sequential data, the second all zeros and the third consists of all ones. The Master Reset Command is used to clear the FIFO. Also the interface is operated in Character Mode. The Valid Data bit in the input data word is expected. The interface Flag should become set by the Valid Data condition.

4-7. CHARACTER COUNTER TEST Ø5 EØ65 - E11Ø

This test verifies the increment and decrement abilities of the Character Counter. Included in this test is testing of the Buffer Half Full, Buffer Full and Buffer Empty Flags.

4-8. SPECIAL CHARACTER RAM TEST Ø6 E111 - E112

This test provides testing of the Special Character RAM and Special Character Mark status bit. The RAM is filled with ones using WORD 6 Commands. Characters are then supplied and the Special Character Mark is expected. Then the RAM is reset to contain all zeros using WORD 6 Commands. Characters are again supplied and the Special Characer Mark bit in the status word is examined.

4-9. UART TRANSMIT TEST Ø7 E113 - E116

This test provides testing of the UART. The idle state of the BA line is examined. The start bit is expected. All combination of data characters, character size, parity and number of stop bits are tested. When error E115 occurs the actual and expected data displayed contain the start bit, the data bits, the parity bit if used and the stop bit(s).

4-10. UART RECEIVE TEST 10 E117 - E134

The ability of the UART to receive data in all combinations of data format is checked. The Special Character Flag and BREAK Flag are tested. The ECHO mode of operation is included in this test. When error E120 occurs the actual and expected data are the ASCII characters and no parity, start or stop bits are displayed.

4-11. BAUD RATE SELECT TEST 11 E135 - E136

This test makes a check on the ability to select by program control a given baud rate. A coarse check is made of the clock rate.

4-12. OVER-RUN AND PARITY ERROR TEST 12 E137 - E143

Over-run and parity errors are generated by the program and the OVPEFLG is expected. The OVPEFLG is reset using a WORD 5 Command.

4-13. DCPC TEST 13 E144 - E154

Basic DCPC control circuits including SRQ are checked. If the system does not have a DCPC no data transfer will take place. Witn DCPC installed and configured into the Diagnostic Configurator the program will perform testing of transmit and receive operations.

4-14. ERROR INFORMATION MESSAGES/HALT CODES

Table 4-1 summarizes the halt codes. Table 4-2 provides a complete description of the individual halts.

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS Ø to 13	
102000-102067	Error (E) & information (H) messages ØØ-67
106000-106054	Error (E) & information (H) messages 1ØØ-154
CONTROL	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test (A-register = test number).
102077	End of diagnostic run.
106077	Trap cell halts in location 2-77.
NOTE: See table 4-2 for a complete explanation of individual halts.	

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test Control	BUFFERED ASYNC COMM INTFC DIAG	Header message. Output at initial start of diagnostic.
None	Test Control	Test XX	Information message before error messages (XX = test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	Test Ø	EØØØ CLF Ø- SFC Ø ERROR	CLF/SFC Ø combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102001	Test Ø	EØØ1 CLF Ø- SFS Ø ERROR	CLF/SFS Ø combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102002	Test Ø	EØØ2 STF Ø- SFC Ø ERROR	STF/SFC Ø combination failed. STF did not set Flag or SFC caused skip with Flag set.
102003	Test Ø	EØØ3 STF Ø- SFS Ø ERROR	STF/SFS Ø combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102004	Test Ø	EØØ4 CLF Ø DID NOT INHIBIT INT	With interface Flag and Control set, CLF Ø did not turn off interrupt system.
102005	Test Ø	EØØ5 CLF SC- SFC SC ERROR	CLF/SFC SC combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102006	Test Ø	EØØ6 CLF SC- SFS SC ERROR	CLF/SFS SC combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102007	Test 0	E007 STF SC-SFC SC ERROR	STF/SFC SC combination failed. STF did not set Flag or SFC caused skip with Flag set.
102010	Test 0	E010 STF SC-SFS SC ERROR	STF/SFS SC combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX, where XX = select code that caused that interface Flag to set.
102012	Test 0	E012 INT DUR-ING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURED	Card interrupted a second time after initial interrupt was processed and interrupt system was turned back on.
102014	Test 0	E014 NO INT	No interrupt occurred with interface Flag and Control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not store the correct return address in memory.
102016	Test 0	E016 CLC SC ERROR	CLC SC did not clear interface Control with the interupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear interface Control.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the interface Flag.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear Control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines. Data lines should be zero.
102024	Test 0	H024 PRESS PRESET (EXT& INT), RUN	Press PRESET (EXTERNAL, INTERNAL) then RUN.
None	Test 0	H025 BI-O COMP	Basic I/O tests completed.
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly and one or several instructions was processed incorrectly during the interrupt.
102030	Test 1	E030 FLAG NOT SET BY CLC 0	The Flag is reset by the program and then the instruction CLC 0 is executed. The interface Flag should be set.
102031	Test 1	E031 CONTROL NOT RESET BY CLC 0	The Control is set by the program and then the instruction CLC 0 is executed. The interface Control should be reset.
102032	Test 1	E032 FLAG NOT SET BY MR COMMAND	The Flag is reset by the program and a Master Reset Command is given. The Flag should be set.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102033	Test 1	E033 FLAG SET - STATUS RESET FAILED	A WORD 5 Command with a Master Reset Command is given to the interface. This command resets the status word and initializes the interface. No condition should be present that would set the Flag FF.
102034	Test 1	E034 CONTROL NOT RESET BY MR COMMAND	The Control is set by the program and the Master Reset Command is sent to the interface. The Control is reset by this command.
102035	Test 2	E035 STATUS IS XXXXXX EXP YYYYYY (SBA-SCA, SBB-SCF, CF)	Using a WORD 4 Command to activate then deactivate the SBA/SCA signal, the program verifies the SBA/SCA and SBB/SCF circuits. The SBB/SCF is observed in the status word.
102036	Test 2	E036 STATUS IS XXXXXX EXP YYYYYY (CA, CC, CE)	The CA signal is activated and deactivated using a WORD 4 Command. The program observes the CC and CE bits in the status word.
102037	Test 2	E037 STATUS IS XXXXXX EXP YYYYYY (CD, CB)	The CD signal is activated and deactivated using a WORD 4 Command. The program observes the CB bit in the status word.
102040	Test 2	E040 STATUS NOT RECEIVED ON INPUT AFTER CLC SC	A known status response is expected on input after a CLC SC instruction has cleared the Control FF.
102041	Test 2	E041 STATUS RECEIVED ON INPUT AFTER STC SC	The program is not expecting to receive status on input after the STC SC instruction.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102042	Test 2	E042 STATUS IS XXXXXX EXP YYYYYY (MR)	The status is obtained following a Master Reset Command and verified.
102043	Test 3	E043 STATUS IS XXXXXX EXP YYYYYY (EN SBB-SCF)	The modem status line SBB/SCF is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102044	Test 3	E044 STATUS IS XXXXXX EXP YYYYYY (EN CF)	The modem status line CF is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102045	Test 3	E045 STATUS IS XXXXXX EXP YYYYYY (EN CE)	The modem status line CE is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102046	Test 3	E046 STATUS IS XXXXXX EXP YYYYYY (EN CC)	The modem status line CC is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102047	Test 3	E047 STATUS IS XXXXXX EXP YYYYYY (EN CB)	The modem status line CB is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102050	Test 3	E050 STATUS IS XXXXXX EXP YYYYYY (REF SBB-SCF)	The modem status bit SBB/SCF is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit SBB/SCF is deactivated and the WORD 2 Command testing repeated.
102051	Test 3	E051 STATUS IS XXXXXX EXP YYYYYY (REF CF)	The modem status bit CF is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CF is deactivated and the WORD 2 Command testing repeated.
102052	Test 3	E052 STATUS IS XXXXXX EXP YYYYYY (REF CE)	The modem status bit CE is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CE is deactivated and the WORD 2 Command testing repeated.
102053	Test 3	E053 STATUS IS XXXXXX EXP YYYYYY (REF CC)	The modem satus bit CC is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CC is deactivated and the WORD 2 Command testing repeated.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102054	Test 3	E054 STATUS IS XXXXXX EXP YYYYYY (REF CB)	The modem status bit CB is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CB is deactivated and the WORD 2 Command testing repeated.
102055	Test 3	E055 STATUS IS XXXXXX EXP YYYYYY (EN MR)	The ENABLE is initialized to enable all modem status interrupts. The resetting of ENABLE by a Master Reset Command prevents the Device Interrupt from occurring.
102056	Test 3	E056 STATUS IS XXXXXX EXP YYYYYY (REF MR)	The REFERENCE is initialized to contain ones. The resetting of REFERENCE by a Master Reset Command prevents the Device Interrupt from occurring.
102057	Test 3	E057 FLAG SET - LOCK INOPERATIVE	Master Reset Command sets the LOCK. A Device Interrupt is then generated, which is prevented from setting the Flag by the LOCK.
102060	Test 3	E060 FLAG NOT SET - DEVINT	A Device Interrupt is permitted to set the Flag because the LOCK is reset.
102061	Test 4	E061 DATA IS XXXXXX EXP YYYYYY (FIFO)	Test data is stored in the First In First Out (FIFO) buffer. This data is then verified for accuracy. Three test patterns are used. They are: all zeros, all ones and ascending data patterns.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102062	Test 4	E062 DATA IS XXXXXX EXP YYYYYY (FIFO MR)	The FIFO is filled with test data and a Master Reset Command given. The FIFO contents are checked for zeros.
102063	Test 4	E063 VALID DATA BIT NOT SET	The FIFO is filled with test data. The interface is placed in receive mode and the data from the FIFO is input. Each input should be accompanied by the Valid Data bit.
102064	Test 4	E064 FLAG DID NOT SET, CHAR MODE ENABLED	With Character Mode enabled characters are inputted. The Flag should be set for each character input.
102065	Test 5	E065 INC CHAR CTR CNT=XXXXXX EXP YYYYYY	The interface is placed in transmit mode and test data is supplied a character at a time. After the output of a character the contents of the Character Counter is inputted and verified. This testing checks the increment capability of the Character Counter.
102066	Test 5	E066 STATUS IS XXXXXX EXP YYYYYY (BHFLG NOT SET)	The interface is operated in transmit mode and the FIFO is half filled by outputting 64 characters. The Buffer Half Full Flag should set.
102067	Test 5	E067 FLAG NOT SET BY BHFLG	The Buffer Half Full Flag is set and the interface Flag is expected to set.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102073	Config-uration	None	I/O select code entered at configuration is invalid. Must be greater than 7. Reenter a valid select code and press RUN.
102074	Config-uration	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter the desired group of tests to be executed into the A-register and press RUN. (See table 3-1.)
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register equals the test number). To continue press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Switch Register options may be changed (A-register has the pass count). To continue press RUN.
106000	Test 5	E100 STATUS IS XXXXXX EXP YYYYYY (WORD5&CBH)	The Buffer Half Full Flag is reset using a WORD 5 Command.
106001	Test 5	E101 STATUS IS XXXXXX EXP YYYYYY (BFFLG NOT SET)	The interface is operated in transmit mode and the FIFO is filled by outputting 128 characters. The Buffer Full Flag should set.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106002	Test 5	E102 FLAG NOT SET BY BFFLG	A Buffer Full Flag is present and the interface should set its Flag.
106003	Test 5	E103 STATUS IS XXXXXX EXP YYYYYY (WORD5&CBF)	A WORD 5 Command is given to reset the Buffer Full Flag.
106004	Test 5	E104 STATUS IS XXXXXX EXP YYYYYY (BEFLG NOT SET)	The interface is placed in receive mode and characters are inputted, emptying the FIFO buffer. On the 128th character the Buffer Empty Flag should set.
106005	Test 5	E105 FLAG NOT SET BY BEFLG	The interface Flag should be set by the Buffer Empty Flag.
106006	Test 5	E106 STATUS IS XXXXXX EXP YYYYYY (WORD5&CBE)	A WORD 5 Command is given to reset the Buffer Empty Flag.
106007	Test 5	E107 FIFO MR DID NOT RESET CHAR CTR	The Character Counter is initialized to all ones. A Master Reset Command is then given to reset the counter.
106010	Test 5	E110 STATUS IS XXXXXX EXP YYYYYY (CA INH)	The FIFO is filled causing the Character Counter to overflow (CCNT7 NOT). This overflow inhibits signal CA from producing CC and CE.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106011	Test 6	E111 DATA IS XXXXXX EXP YYYYYY (SPCH)	The Special Character RAM is initialized. Sample data is presented and the program examines the Special Character Mark bit in the received data word. Two test patterns are used. An all ones and all zeros test patterns.
106012	Test 6	E112 DATA IS XXXXXX EXP YYYYYY (SPCH)	The Special Character RAM is initialized. The Special Character Mask bit in the input data word is checked. An ascending data pattern is used to provide for addressing testing.
106013	Test 7	E113 BA = 0 AFTER MR	A Master Reset Command is given. The UART should place a logical one on line BA.
106014	Test 7	E114 DATA IS XXXXXX EXP YYYYYY (UART CHAR CTR DOWN)	Data is placed in the FIFO. The program supplies clocks and the UART accepts data from the FIFO. The program checks the contents of the character counter.
106015	Test 7	E115 BA = 1 (NO START BIT)	During a transmit operation the expected start bit was not present.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106016	Test 7	E116 DATA IS XXXXXX EXP YYYYYY (UART XMIT # STOP, ZZZ PARITY, # BITS PER CHAR	A transmit operation is performed. All combinations of data, parity, character length and number of stop bits are used. When no teleprinter is available
103016	Test 7	None	the A register contains the actual data and the B holds the expected data. The operator depresses RUN and a second halt occurs (103015 octal) with A-register holding the WORD 3 command used to select the frame parameters.
106017	Test 10	E117 STATUS IS XXXXXX EXP YYYYYY (TEST, BB)	Receive data BB is checked by observing RIN which is available to the program as the Test bit in the status word.
106020	Test 10	E120 DATA IS XXXXXX EXP YYYYYY (UART RCVE #STOP, ZZZ PARITY, # BITS PER CHAR	The interface is in receive mode. Test serial data is presented to the UART. This data contains all combinations of data, parity, character length and number of stop bits.
103020	Test 10	None	When no teleprinter is available the A-register contains the actual data and the B-register holds the expected data. The operator depresses RUN and a second halt occurrs (103020 octal) with the A-register holding the WORD 3 Command used to select the frame parameters.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106022	Test 10	E122 PARITY ERROR	During a receive operation a parity error has occurred.
106026	Test 10	E126 STATUS IS XXXXXX EXP YYYYYY (SPCHFLG)	The Special Character RAM is initialized and a receive operation is performed. Test data that contains characters that have been flagged as special characters are used. The Special Character Flag in the status word is expected.
106027	Test 10	E127 FLAG NOT BY SPCHFLG	The interface Flag is expected to be set by the presence of the Special Character Flag.
106030	Test 10	E130 STATUS IS XXXXXX EXP YYYYYY (SPCHFLG RESET)	A WORD 5 Command with the Clear Special Character Flag bit set is given. The Special Character Flag should be reset.
106031	Test 10	E131 STATUS IS XXXXXX EXP YYYYYY (BREAK FLAG)	A receive operation is started and the serial data in line is placed in the mark state and held there for sufficient time for the BREAK Flag to set. This flag is expected in the status word.
106032	Test 10	E132 FLAG NOT SET BY BREAK	The interface should set its Flag FF because the BREAK Flag is set.
106033	Test 10	E133 STATUS IS XXXXXX EXP YYYYYY (BREAK RESET)	A WORD 5 Command is given with the Clear BREAK Flag bit set. The status word is then examined for the reset.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106034	Test 10	E134 STATUS IS XXXXXX EXP YYYYYY (ECHO)	The operation of the ECHO is tested. A receive operation is set up with ECHO enabled. Serial data is presented and the results monitered.
106035	Test 11	E135 BAUD RATE SLOW (XXXXXX)	A transmit operation is performed and timed. The duration of the transmitted buffer is in excess of 4% of the allowable time. The A register contains the WORD 4 Command used to select the baud rate.
106036	Test 11	E136 BAUD RATE FAST (XXXXXX)	Same as E135 except rate is fast. The duration was insufficient. The A-register contains the WORD 4 Command used to select the baud rate.
106037	Test 12	E137 STATUS IS XXXXXX EXP YYYYYY (OVER-RUN)	A receive operation is set up and data is supplied to the interface. The FIFO is allowed to fill. With excess data presented to the interface, the OVPEFLG is set. The OVPEFLG is expected to be present in the status word.
106040	Test 12	E140 FLAG NOT SET BY OVPEFLG	The interface Flag FF should become set because the OVPEFLG is set.
106041	Test 12	E141 STATUS IS XXXXXX EXP YYYYYY (OVPEFLG RESET)	A WORD 5 Command is used to reset the OVPEFLG. The status word should indicate the reset condition.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106042	Test 12	E142 NO PARITY ERROR (XXXXXX)	A receive operation is set up and data with incorrect parity is supplied to the interface. The OVPEFLG should become set. The status word is examined for this condition.
106043	Test 12	E143 OVPELFG NOT RESET (WORD5&CLPE)	A WORD 5 Command is used to reset the OVPEFLG A check of the interface status word is then made.
106044	Test 13	E144 FLAG SET BUFFER FLAGS (DCPC=1)	Buffer flags are prevented from setting the interface Flag because DCPC is enabled.
106045	Test 13	E145 FLAG SET BY DEVINT WITH SRQ	A data request is generated. The DCPC is enabled and the Service Request (SRQ) becomes set. Conditions are then created to produce a Device Interrupt. This DEVINT is now prevented from setting the interface Flag FF by the set state of the SRQ FF.
106046	Test 13	E146 FLAG NOT SET AFTER CLF CH (SRQ)	The pending Device Interrupt is now permitted to set the interface Flag FF because the SRQ FF is reset by the CLF instruction.
106047	Test 13	E147 SRQ SET WHILE LOCK = 1	A Master Reset Command is used to set the LOCK FF. A data request is then generated which is now prevented from setting the SRQ FF by the LOCK.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test 13	H150 DCPC DATA TRANSFER OMITTED-NO DCPC	The configuration of the system does not include a DCPC. There can be no data transfer using DCPC.
106051	Test 13	E151 DATA IS XXXXXX EXP YYYYYY (DCPC TRANSMIT)	A typical data transmit operation is performed using the DCPC to handle the data from memory.
106052	Test 13	E152 STATUS IS XXXXXX EXP YYYYYY (STATUS ERROR IN DCPC TEST)	After completing a data transfer using the DCPC the status of the interface is examined and an abnormal response was encountered.
106053	Test 13	E153 DATA IS XXXXXX EXP YYYYYY (DCPC RECEIVE)	A typical data receive operation is performed using the DCPC to transfer data into the memory.
106054	Test 13	E154 DCPC ABNORMAL COMPLETION	After the completion of a DCPC transfer the residual character count in the DCPC should be zero.
106077	Test Control	None	Halt stored in locations 2-77 to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot number which interrupted. Diagnostic may be partially destroyed and have to be reloaded if it was caused by a CPU failure; the problem should be corrected before proceeding.

4-14. DEFINITION OF TERMS

BA - Transmit Data
BB - Receive Data
BEFLG - Buffer Empty Flag
BFFLG - Buffer Full Flag
BHFLG - Buffer Half Full Flag

CA - Request To Send (RQS)
CB - Clear To Send (CLS)
CBE - Clear Buffer Empty Status Flag (WORD 5+CBE)
CBF - Clear Buffer Full Status Flag (WORD 5+CBF)
CBH - Clear Buffer Half Full Status Flag (WORD 5+CBH)
CC - Data Set Ready (DSR)
CD - Data Terminal Ready (DTR)
CE - Ring Indicator (RNG)
CF - Receive Line Signal (RLS)
CHAR CTR - Character Counter

DEVINT - Device Interrupt

EN - Enable (WORD 1 Command)

FIFO - First In First Out Buffer

INC - Increment (INC CHAR CTR)

MR - Master Reset (BIT 15 of WORD X Command)

OVPEFLG - Over-run / Parity Error Flag

RAM - Random Access Memory (Special Character Memory)
RCVE - Receive Mode (WORD 4+NOT XMIT)
REF - Reference (Reference WORD 2 Command)

SBA - Secondary Transmit Data
SBB - Secondary Receive Data
SCA - Secondary Request To Send (SRQS)
SCF - Secondary Receive Line Signal (SRLS)
SPCH - Special Character
SPCHFLG - Special Character Flag
SRQ - Service Request (DCPC)

UART - Universal Asynchronous Receiver/Transmitter

WORD 0 - Transmit Data Word
WORD 1 - Enable Device Status Interrupt Word
WORD 2 - Device Status Reference Word
WORD 3 - Character Frame Control Word
WORD 4 - Interface Control Word
WORD 5 - Interrupt Status Reset Word
WORD 6 - Special Character Word
WORD 7 - Reserved

XMIT - Transmit Mode (WORD 4+XMIT)

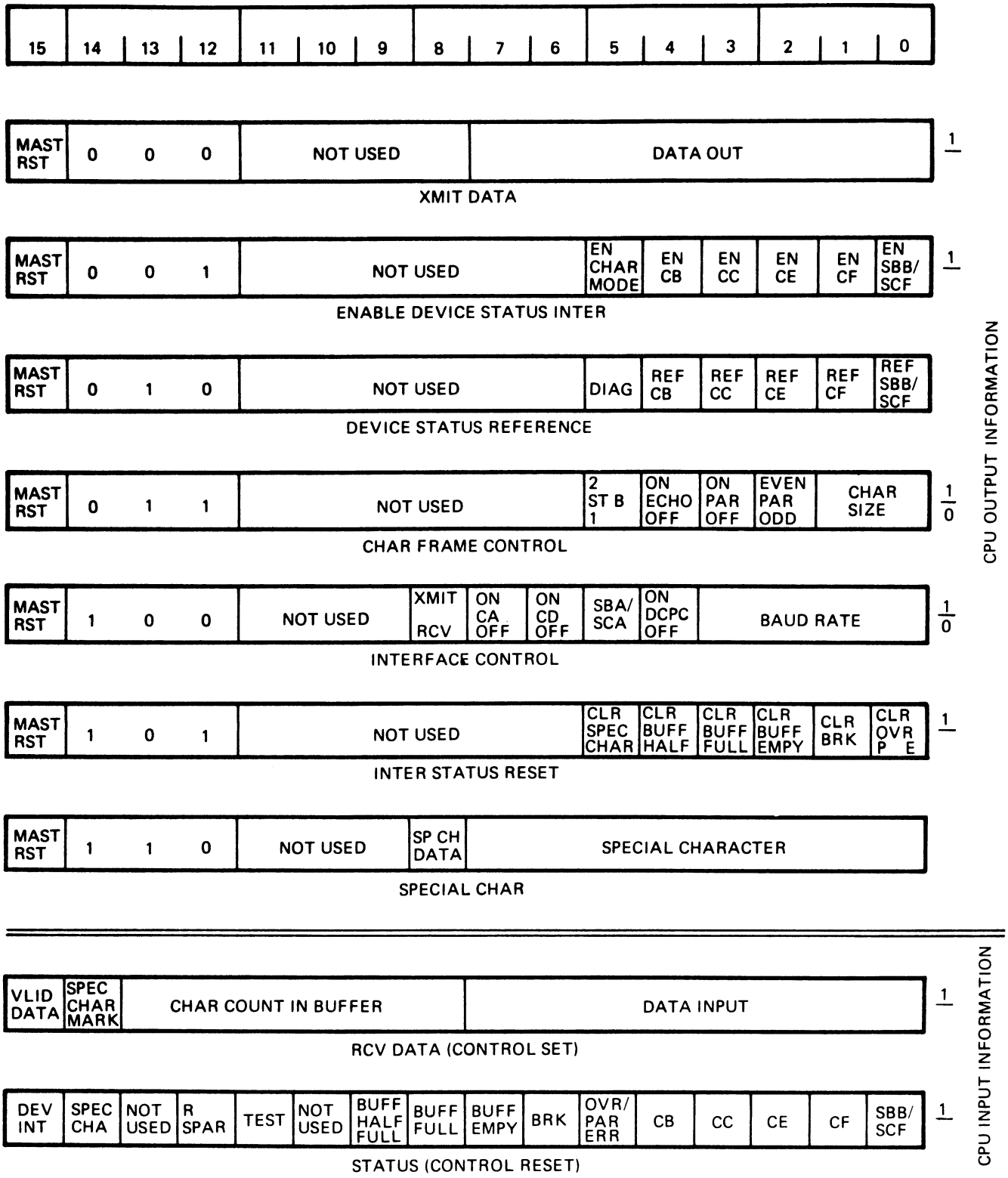

Figure 4-1. Command, Status and Data Formats