GRC TBC-11 SPECIFICATIONS
October, 1978

SYSTEM FUNCTIONS

TERMINATOR

The last card in a Q-bus backplane must be a terminator. The TBC provides a 220 ohm impedance termination for the bus.

POWER SEQUENCING

The power signal generation circuit provides proper powering up and powering down of an LSI-11 system. In addition, systems with non-volatile memory (i.e. core) can provide handling of power interruptions. For such systems, a power-fail software routine can save the contents of the stack pointer register, the processor status word register, the general purpose register, and other device registers which the user desires saved. A power-up software routine, which is part of the power-fail software, will restore the saved registers when the system is initialized.

PROM BOOTSTRAP

Space is provided for two 8-bit PROMS to be used for a bootstrap. Their addressing is set to respond to 173000(8) with a window of 256(10) words. The window size may be changed to 512, 1024, or 2048 words and the address may be placed at any multiple of the window size starting at zero by modifying a set of jumpers on the board. Proms of the 2704/2708/2716 family or equivalent may be used.

CONSOLE PANEL

The TBC contains logic to interface an external SPDT switch to provide the Halt/Run Enable function. The TBC will also drive an incandescent or (optional) LED lamp to indicate when the processor is "Running" (i.e. fetching instructions). Optional console panel functions are a manual line time clock On/Off switch and a LED type "DC On" indicator.

PROGRAMMABLE LINE TIME CLOCK

Sometimes called Real Time Clock, the line time clock, when activated, generates an interrupt on the Event line, synchronized to the AC line frequency. The clock is automatically turned on by software during the bootstrap in version 3 of RT-ll operating system. Options available are external clock input, external clock turn-on, and interrupt line rather than Event line stimulation.

RT-11 V03 turns on the clock automatically. Version 2 does not. To turn it on:

- 1. Boot the system
- 2. Halt the system
- 3. Access location 177546
- 4. Insert the value 100
- 5. Type "P" to continue

The LTC requires 28VAC-center tapped with the center tap connected to ground. Power should be connected to pins BCl and BEl on one side of the quad backplane, and correspondingly to pins DCl and DEl on the other side. It can also be connected at PC foil pads at the front of the board, labeled Jl-l and Jl-2. The current requirement is about 15 ma.

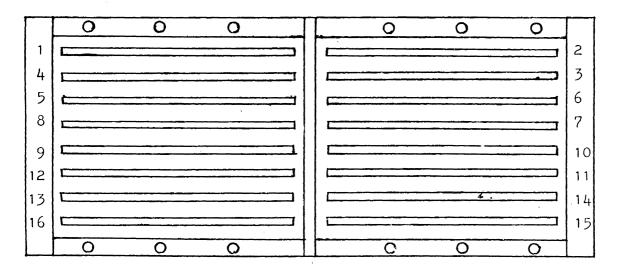
The LTC control register is at octal address 177546 with contents as shown below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	l	()
0	0	0	0	0	0	0	0	MON	ΙE	S	0	0	0	0	0

BITS DESCRIPTION

15-8 Zero - Not used

- 7 MON Monitor is set when a line time clock (LTC) pulse has occurred (every 16.67 ms for 60 Hz and 20 ms for 50 Hz). Reset by being read and BINIT. Read only.
- 6 IE Interrupt Enable, when set, enables interrupts from LTC. Interrupt is generated on either the BEVNT L line or the BIRQL line, depending on the state of bit 5. Reset by writing a "0" or by BINITL. Read/write.
- 5 S Select, when set along with bit 6 and an interrupt occurs, activates the BIRQL line. A vector of 100(8) is generated when the processor responds. When reset, under the same conditions as above, the BEVNTL line is activated. Set by writing a "l" into it. Reset by writing a "0" or by BINITL. Read/write.
- 4-0 Zero Not used.



BACKPLANE

TBC Placement

Boards should be placed in the backplane in such a manner that backplane continuity is preserved. This requires that the slots be filled in order starting from the upper left and proceeding downward in a zig-zag pattern with the TBC as the last board. See figure.

Jumper Options

To disable the addressing for the PROM sockets, jumper G39-G40 must be cut. (This jumper normally sets the address range.)

The following tables indicate which jumpers (Gxx) should be in place for PROMs and other options. Use Tables 2 and 4 to set the PROM starting address and address range, Table 3 to set the window size, and Table 1 to set the power. Use Table 5 to convert the Line Time Clock from automatic to manual turn-on, or from internal line frequency to externally generated clock. An external line clock can be connected through J2 pin 4 or backplane pin BK1.

Table 1

Power Options	· G28,	G29,	G25,	G26,
For Proms	<u>G29</u>	<u>G30</u>	G26	G27
į		ν,		
2704	In	Out	In	Out
2708	In	Out	In	Out
82S2 7 08	Out	Out	DC	Out
2716	Out	In	Out	In

Dc=Don't care

Table 2

Prom	G1,	G2,	G4,	G5,	G7,	G8,	G10,	G11,	Notes
Starting	G 2	G 3	G5	G 6	G8	G9 -	G11	G12	
Address	-	No.			******		-		
0 0 X X X X	Out	In	Out	In	Out	In	Out	In	
$0.1 \times \times \times \times$	Out	In	Out	In	Out	In	In	Out	1,2
0 2 X X X X	Ou t	In	Out	In	In	Out	Out	In	2
0 3 X X XX	Out	In	Out	In	Ιn	Out	In	Out	1,2
0 4 X X X X	Out	Ιn	In	Out	Out	In	Out	Ιn	
05XXXX	Out	In	In	Out	Out	In	In	Out	1,2
06xxxx	Out	In	In	Out	In	Out	Out	In	2
07 X X X X	Out	In	Ιn	Out	In	Out	In	Out	1,2
1 0 XXXX	In	Out	Out	Ιn	Out	In	Out	In	1,2
11XXXX	In	Out	Out	In	Out	In	In	Out	1,2
12XXXX	In	Out	Out	In	Ιn	Out	Out	In	2
1 3 X X X X	In	Out	Out	Ιn	Ιn	Out	In	Out	1,2
1. 4 X X X X	In	Out	In	Out	Out	In	Out	In	
15 X X X X	In	Out	In	Out	Out	In	In	Out	1.,2
16 X X X X	In	Out	In	Out	In	Out	Out	In	2
17xxxx	In	Out	In	Out	In	Out	In	Out	1,2

XXXX=See table 4.

- * Normal factory setting
- Notes: 1. Starting address not available for 2708, 2716, etc, with window size of 1024. See Table 2. (Both G10-G11 and G11-G12 out)
 - 2. Starting address not available for 2716, etc., with window size of 2048. See Table 2. (G10-G11, G11-G12, G7-G8 and G8-G9 out)

Table 3

Prom Wind															
256		-													
512	Out	In .	Out	In	Out	Out	In	Out	In	Out	Out	Ιn	Out	Ιn	2704
1024 2048															

Boot = Normal factory setting

Table 4

Prom	G37,	G38,	G39,	G39,	When
Address Range	<u>G39</u>	<u>G39</u>	<u>G40</u>	<u>G41</u>	Used
XX1000XX1776	In	Out	Out	Out	
xx3000xx3776	Out	In	Out	Out	Boot
xx5000xx5776	Out	Out	In	Out	
XX7000XX7776	Out	Out	Out	In	
xx0000xx1776	In	Out	Out	Out	2704
xx2000xx3776	Out	In	Out	Out	2704
xx4000xx5776	Out	Out	In	Out	2704
xx6000xx7776	Out	Out	Out	Ln	2704
X00000X03776	In	Out	Out	Out	2708
x04000x07776	Out	In	Out	Out	2700
x10000x13776	Out	Out	In	Out	270b
x14006x17776	Out	Out	Out	1.12	1 300
X00000X07.776	In	Out	Cut	Cast	1 / 20
x10000x17776	Out	In	Out	Out	2716
x20000x27776	Out	Out	In	Out	2716
x30000x37776	Out	Out	Out	In	2716

^{*} Normal factory setting

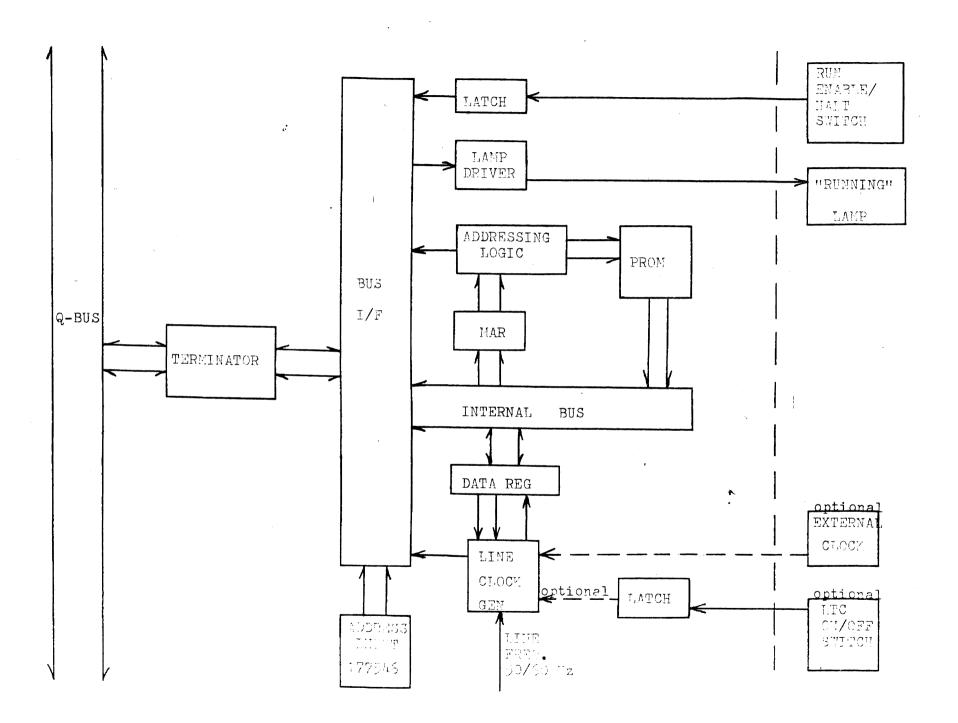
Table 5

Misc.	Jum	pers
Otions	<u>In</u>	<u>Out</u>
Auto Ltc.	G52,	G53,
	G53	G54
Manual Ltc.	G53,	G52,
	G54	G53
Int. Ltc.Clk.	G49,	G50,
	G50	G51
Ext. Ltc.Clk.	G50,	G49,
	G51	G50
For "RUN"	Cut	run
light being	betw	een
LED	pads	R16
	and a	add
	47 ol	hm 1/4W
	resi	stor.

* Normal factory setting

Cable Pinouts:

- J2 pin #:
- 1. LTC manual switch "on" position
- Run-Enable/Halt switch "Run" position
 Run-Enable/Halt switch "Halt" position
- 4. External clock
- 5. 5 volts6. no connection
- 7. DC-on light wired for LED
- 8. LTC manual switch "off" position
- 9. Running light, incandescent or LED (LED requires change as per Table 5)
- 10. Ground



LOG HAGRAT