

SC01 SERIES  
LARGE CAPACITY DISK CONTROLLER  
TECHNICAL MANUAL



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## TABLE OF CONTENTS

	<u>Title</u>	<u>Page</u>
SECTION 1 INTRODUCTION		
1.1	SCOPE	1-1
1.2	GENERAL INFORMATION	1-1
1.3	FEATURES	1-1
1.3.1	Microprocessor Architecture	1-1
1.3.2	Packaging	1-2
1.3.3	Buffering	1-2
1.3.4	Error Correction	1-2
1.3.5	Self-Test	1-2
1.3.6	Optional and Configuration Switches	1-3
1.3.7	Device Addressing	1-3
1.4	FUNCTIONAL CHARACTERISTICS	1-3
1.4.1	Model SC01/A	1-4
1.4.2	Model SC01/B	1-4
1.4.3	Model SC01/C	1-4
1.5	ORGANIZATION AND USE OF MANUALS	1-6
1.5.1	Technical Manuals	1-6
1.5.2	User's Manuals	1-6
1.5.3	Applications Notes	1-7
1.5.4	References	1-7
SECTION 2 DESIGN INFORMATION		
2.1	PHYSICAL DESCRIPTION	2-1
2.1.1	SC Microprocessor Board (A Board)	2-1
2.1.1.1	Switches and Connectors	2-1
2.1.1.2	PROM Locations	2-5
2.1.2	SC B Board	2-5
2.1.3	Product Identification and Marking	2-6
2.2	CONTROLLER ORGANIZATION	2-9
SECTION 3 INSTALLATION		
3.1	INSPECTION	3-1
3.2	SETUP	3-1
3.2.1	Device Address Selection	3-1
3.2.2	Interrupt Vector Address	3-2
3.2.3	Interrupt Selection	3-2
3.2.4	Index and Sector Pulse Selection	3-2
3.2.5	Option and Configuration Switch	3-4

## TABLE OF CONTENTS

	<u>Title</u>	<u>Page</u>
3.3	PHYSICAL INSTALLATION	3-4
3.4	DISK DRIVE SETUP	3-5
	3.4.1 Sectoring	3-5
	3.4.2 ID Plug	3-5
3.5	CABLING	3-5
	3.5.1 A Cable	3-7
	3.5.2 B Cable	3-7
	3.5.3 Grounding	3-7
3.6	TESTING	3-7
	3.6.1 Self-Test	3-8
	3.6.2 Register Examination	3-8
	3.6.3 Diagnostics	3-8
	3.6.3.1 Diagnostic Patches	3-8
	3.6.3.2 Loading Diagnostics	3-8
	3.6.3.3 Running Diagnostics	3-9
 SECTION 4 INTERFACES		
4.1	GENERAL	4-1
	4.1.1 Connectors and Cables	4-1
	4.1.2 Input Circuits	4-2
	4.1.3 Output Circuits	4-2
	4.1.4 A Cable Signals	4-2
	4.1.4.1 Signals to Disk Drive	4-3
	4.1.4.2 Signals From Disk Drive	4-6
	4.1.5 B Cable Signal	4-7
	4.1.5.1 Signals to Disk Drive	4-7
	4.1.5.2 Signals From Disk Drive	4-7
4.2	LSI-11 Q-BUS INTERFACE	4-9
	4.2.1 Device Priority	4-10
	4.2.2 Bus Signals	4-10
	4.2.3 Initialization and Power Sequencing	4-11
	4.2.4 Electrical Specifications	4-11

## LIST OF TABLES

<u>Table No.</u>	<u>Title</u>	<u>Page</u>
Table 1-1	Characteristics of DEC Disk Subsystems	1-5
Table 1-2	SC01 Series - General Specifications	1-8
Table 2-1	PROM Size/Memory Capacity	2-2
Table 3-1	Bus Address/Register - Range Configurations	3-2
Table 4-1	Tag Bus Decode, SMD/MMD/CMD	4-5
Table 4-2	LSI-11 Interface Signals (SU0110401)	4-13
Table D-1	Drives Supported (SC01/B3)	D-2
Table D-2	Drive Configurations (SC01/B3)	D-2
Table D-3	Alternate Address Selection (SC01/B3)	D-4
Table D-4	Alternate Vector Selection (SC01/B3)	D-4
Table D-5	Configuration Switch Settings (SC01/B3)	D-5
Table D-6	Option Switch Settings	D-5

## LIST OF FIGURES

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
Figure 2-1	SC01 Series Controller	2-3
Figure 2-2	SC Microprocessor Board	2-4
Figure 2-3	SC B Board	2-7
Figure 2-4	SC01 Block Diagram	2-10
Figure 3-1	Unit Cabling	3-6
Figure 4-1	A Cable Signals	4-4
Figure 4-2	B Cable Signals	4-8

## APPENDIXES

<u>Appendix</u>	<u>Title</u>	<u>Page</u>
Appendix A	Reference Documents	A-1
Appendix B	Option Switches	A-2
Appendix C	LED Indicators	A-6
Appendix D	SC01/B3 Configuration and Address Selection	D-1

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# SECTION 1

## INTRODUCTION

### 1.1 SCOPE

This manual provides information related to the capabilities, design and installation of the SC01 disk controller. This controller can be used in LSI-11 based systems to interface to any large disks having a Storage Module Drive (SMD) interface. This controller is capable of emulating a number of disk subsystems built for the PDP-11 by Digital Equipment Corporation. Details of the functional characteristics of the controller in a particular emulation can be found in the appropriate User's Manual.

### 1.2 GENERAL INFORMATION

The SC01 Disk Controller is an embedded two board controller for use with the DEC LSI-11. Other companion products with similar design include the SC11 for the PDP-11/04-60, and the SC70 for the PDP-11/70. The basic controller is based on an advanced design concept which permits it to be readily adapted to a wide range of controller applications. On the host computer side, the SC01 interfaces to the LSI-11 Q-Bus, and executes all programmed I/O and DMA operations executed by its DEC disk controller counterpart. On the drive side, the SC01 interfaces to the industry standard Storage Module Drive (SMD) interface, originally defined by CDC, but currently available on almost all large disk drives. Most versions of the SC01 controller emulate a DEC large disk controller. In many cases, these controllers are capable of operating with disks having different characteristics than those used in the DEC disk subsystems.

The SC01 controller provides the capability of operating with disks having storage of 40 to 600 megabytes. The SC01 series of controllers provide emulation of DEC PDP-11 controllers not currently available for the LSI-11, including the RM02 and RP06 Massbus drives.

### 1.3 FEATURES

#### 1.3.1 Microprocessor Architecture

The SC01 design incorporates a unique (patent pending) 16-bit bipolar microprocessor to perform all control operations. The microprocessor application provides for reduced component count, high reliability, easy maintainability, and, most importantly, the ability to change the functional capability of the controller by

means of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate by providing enhancement features such as built-in self-test during power-up and built-in disk formatting.

### 1.3.2 Packaging

The SC01 is constructed on two PC boards which plug directly into an LSI-11 backplane. No cabling is required between the computer and the disk controller. The controller obtains its power from the LSI-11 backplane. The two boards of the controller are connected together with AMP pins along each side of the board, thus eliminating cables between the two boards or special backplane wiring. Cables to the disk drives are connected on the top edge of the board.

### 1.3.3 Buffering

The controller contains a 1K x 16 high speed RAM buffer used to store the device registers of the controller being emulated and for data buffering. Most emulations set aside 768 words for data buffering providing for three sectors (768 words) of buffering. With this amount of buffering, and the strategies used to employ it, data late situations on the computer bus are not possible.

### 1.3.4 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) generator and checker capable of correcting single burst errors of up to 11-bits in length and detecting a burst of longer length. In some emulations the data correction is performed in the controller and is therefore transparent to the user, while in others, the error position and pattern are presented via registers to the computer for software correction. The latter technique is employed for emulations of DEC controllers which include this error correcting technique.

### 1.3.5 Self-Test

The controller incorporates internal self-test routines which are executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk interface circuitry. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is completely operational. If the controller fails the self-test, it leaves at least one LED error lamps turned on, and the controller cannot be addressed from the computer.



### 1.3.6 Option and Configuration Switch

A single eight pole DIP switch (SW1) located on the A board is used to configure the firmware for disk sizes and to invoke certain options. The meaning of these switches is dependent on model and are listed in Appendix B for the current SC01 models.

A second four pole DIP switch (SW2) located at the top of the A board is used to enable extended functions of the various controller versions; it is accessible to the user while the controller is installed in the system. The meanings of these switches is dependent on the model and are also listed in Appendix B.

### 1.3.7 Device Addressing

The controller has means of selecting different bus device starting addresses and the number of device registers which can be accessed by the computer. In the SC01, selection is accomplished by means of a PROM which can detect four starting addresses and select the required number of registers. Selection of one of the four is performed by jumpers on the B board. The interrupt vector address is determined by the microcode and is appropriate for the particular firmware version incorporated. A standard and 1-3 alternate vector is usually provided.

## 1.4 FUNCTIONAL CHARACTERISTICS

The functional characteristics of the controller are provided by the firmware of its microprocessor. Firmware is available to emulate a number of DEC's large disk subsystems. These are:

- Model SC01/A - emulates the DEC RP11 controller with RP02 or RP03 drives.
- Model SC01/B - emulates the DEC RJM02/03 and RJP06 disk subsystems.
- Model SC01/C - emulates the DEC RK611 controller with RK06 or RK07 drives.

Some models of the SC01 provide for a one-to-one mapping between the logical drive being emulated and the physical drive attached to the controller. Others provide for mapping two or more logical drives onto a single physical drive. In such cases, there is some reduction in performance because of the elimination of overlapped seeks.

A further description of the three emulation models is given below. Detailed functional characteristics of these models can be found in the applicable User's Manuals.

#### 1.4.1 Model SC01/A

The Model SC01/A emulates the operation of the DEC RP11E controller which was designed to interface with RP02 or RP03 disk drives. This basic controller architecture is used in numerous Model A versions to handle a wide variety of disk drives whose specifications do not match those of any comparable DEC drive and are not suited for other emulations. All versions of the Model A controller entail the mapping of a standard, expanded, or contracted size logical RP02 or RP03 onto a specific make or class of disk drives. The characteristics of the RP02 and RP03 drives are given in Table 1-1.

#### 1.4.2 Model SC01/B

The Model SC01/B emulates the functions of the RJM02/03 or RJP06 disk subsystems. In these DEC disk subsystems, the majority of the controller logic is located redundantly in each of the disk drives which interface to the Unibus via the Massbus and the RH11 Massbus Controller. The SC01/B controllers emulate the entire functions contained in the disk drives and the RH11 Massbus Controller. These subsystems are not available from DEC for the LSI-11. These drives are supported by all operating systems except RT-11. The SC01/B is primarily applicable to disk drives of 40, 80, 160, 200, 300 and 600 megabytes.

Versions of the SC01/B entail mapping of either: standard or expanded size RM02 logical units onto 40, 80, 160, 300 or 600 megabyte disk drives; or a standard or expanded size RP06 logical unit onto 200, 300, or 600 megabyte disk drives. A definition of the DEC RM02/03 and RP06 disk drives is given in Table 1-1.

#### 1.4.3 Model SC01/C

The Model SC01/C emulates the operation of the DEC RK611 controller which interfaces to RP06 and RP07 disk drives. These drives are supported by all DEC operating systems. The SC01/C model is used with the Cartridge Module Drive (CMD) or Hunter Drive. Refer to Table 1-1.

TABLE 1-1  
CHARACTERISTICS OF DEC DISK SUBSYSTEMS

CHARACTERISTICS	RP02	RP03	RP06	RM02	RK06
Platters/Drive	11	11	11	3	2
Tracks/Cylinder	20	20	19	5	3
Cylinders/Drive	203	406	815	823	411
Sectors/Track	10	10	22	32	22
Bytes/Sector	512	512	512	512	512
MBytes/Drive	20.8	41.6	174.4	67.4	13.9
Speed	2400	2400	3600	2400	2400
Bit Density (BPI)	2020	2020	4040	6060	2400
Data Rate (K Words/Sec)	102.4	102.4	400	403	270

## 1.5 ORGANIZATION AND USE OF MANUALS

Emulex disk controller documentation is organized into three basic categories: Technical Manuals, User's Manuals, and Applications Notes. There are also other references applicable to application of the controllers.

### 1.5.1 Technical Manuals

A Technical Manual is provided for each basic disk controller model; SC01, SC11, and SC70. This manual provides information which is common to all microcode versions of the applicable controller, including: general information and features; functional characteristics and specifications; general design description; physical description; configuration and installation procedures; and interface specifications. This manual does not contain any information related to a specific emulation version, programming procedures, and other such data required to functionally apply the controller; such information is contained in other manuals as specified below.

Technical Manuals available for the current Emulex controller series are:

- SC0151001 - SC01 Series Controllers
- SC1151001 - SC11 Series Controllers
- SC7051001 - SC70 Series Controllers

Similar manuals will be made available for future controller product series.

### 1.5.2 User's Manuals

Controllers are classified into basic models according to the class of DEC disk subsystem being emulated. A model designation has common functional characteristics for all hardware controller series (i.e., SC01, SC11, SC70). The basic models available are:

- A - RP11/RP02/RP03
- B - RJM02/RWM03, RJP06/RWP06
- C - RK611/RK06/RK07

Within each model, there may be several versions of microcode (e.g., A1, A2, etc.) designed to support a particular set of disk drive characteristics.

Since application is dependent upon the model and, in some cases, version, there are separate User's Manuals provided for each model/versions as applicable. These are designated as:

SCXX51001 - SC11/A Models  
SCXX51002 - SC11/B1 Models  
etc.

The appropriate User's Manual contains such information as: functional specifications; disk drive characteristics (typical); applicable diagnostics; disk pack formatting; CSR definitions and function codes; and controller option switch settings. In addition, applicable Applications Notes related to diagnostic patches and operations plus other detailed information are included.

### 1.5.3 Applications Notes

Emulex Applications Notes are published as supplemental information to the Technical and User's Manuals, and contain specific and detailed technical information. Certain of these, particularly those related to diagnostic and operating system patches, are included in the User's Manuals. A complete list of currently available Applications Notes is available upon request.

### 1.5.4 References

Other applicable reference documents are listed in Appendix A. In general, Emulex manuals assume the user is completely familiar with all pertinent aspects of DEC computers, packages, peripherals and controllers, etc. and no type of tutorial material on these elements is included. Also, information on applicable disk drives is very limited in Emulex documents, and the manufacturer's documentation should be consulted for details.

TABLE 1-2  
 SC01 Series  
GENERAL SPECIFICATIONS

The following specifications apply to all SC01 series large disk controllers.

CHARACTERISTIC	SPECIFICATION
FUNCTIONAL	
Design	High-speed bipolar microprocessor-based controller for integration of industry-standard SMD and Winchester type mass storage devices to host LSI-11 computer; incorporates unique (Patent Pending) design to achieve extreme high-speed operations with minimum hardware.
Computer Interface	Standard Q-Bus via quad interface on B board (power and ground only to A board).
Disk Interface	Storage Module Drive (SMD) interface standard; serial data rate up to 10 MHz.
Bus Address Range	0 - 128K Words.
Bus Register Base Address	Four selectable start locations.
Vector Address	2 or 4 firmware selectable vectors.
Priority Level	Jumper selectable, BR4 or 5.
Error Control	On-board 32-bit ECC and 16-bit CRC hardware for error detection/correction under microprogram control.
Status Display	Four edge-mounted LED's for mode/error/status display under microprogram control.
Option Switches	Twelve on-board slide switches for selection of program-controlled operating/configuration options.

Table 1-1 (Cont'd)

CHARACTERISTIC	SPECIFICATION
Buffer Memory	2048 byte high-speed RAM buffer, accessible to the microprogram, for data buffering and internal storage operations. Typically 1536 bytes used for data buffering.
PHYSICAL	
Packaging	Two printed circuit boards interconnected by AMP Mod 1 pins; standard Q-Bus quad interface. Extractor handles provided for easy insertion/removal.
Mounting	Any two adjacent quad slots in standard backplane or system unit.
Disk Cable and Connectors	One common 60-pin control (A) flat cable connector on SC Micro-processor Board; two 26-pin radial data (B) flat cable connectors on SC B board.
Physical Drives	1 or 2 per controller.
ELECTRICAL	
Unibus Interface	Approved line drives/receivers used exclusively; one unit load per bus signal line.
Disk Interface	Differential line drivers and receivers used on all signal lines. Daisy-chain (A) and radial (B) cable lengths up to 100 and 50 feet respectively.
Power	+5V +5%, 9 AMPS max, standard backplane/system unit pins used.
ENVIRONMENTAL	Exceeds all environmental ranges and conditions specified for commercial LSI-11 computers and applicable disk drives.

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## 2.1 PHYSICAL DESCRIPTION

All Emulex SC01 series controllers incorporate the same physical hardware. The controller consists of two quad size printed circuit boards which are designed to plug directly into an LSI-11 card cage and backplane. The printed circuit boards are coupled electrically and physically by two rows of AMP mod 1 pins. Proper separation of the two boards is maintained by four spacers which are held in place by screws. Figure 2-1 shows the complete SC01 two board assembly.

### 2.1.1 SC Microprocessor Board (A Board)

The top board of the controller assembly is Part Number SU1110401 and is known as the SC Microprocessor or A board. This board contains the high speed bipolar microprocessor elements of the controller, and is common to both the Emulex SC01 and SC11 series of controllers.

The A board is shown in Figure 2-2. The board is a four layer PCB with power and ground planes on the inner layers and interconnects on the outer layers. The board dimensions are 8.7 inches wide by 10.4 inches high corresponding to the DEC quad board size.

The board plugs into the four backplane connectors of an LSI-11 backplane. The 18 pins of each connector row are designated A through F - excluding the letters G, I, O, and Q - from right to left. The component side pins are designated 1 and the bottom side pins are designated 2. Except for PDP-11 and LSI-11 daisy-chains signals, this board interfaces only the standard plus 5 volt and ground pins. Although the A board does not interface to the Q Bus, it does occupy a full quad slot, and therefore, provision is made to jumper through the two daisy-chain signals (BIAK and BDMG) on the A and C connectors to ensure continuity to the B board and succeeding devices. These jumpers are P, R, W, and X. The jumpers labeled S, T, U, V and Y should be left open as these are the Unibus bus grant signals used in the SC11 controller series.

#### 2.1.1.1 Switches and Connector

The A board has a 60-pin flat cable connector labeled J1 at the top edge. This connector is for the A cable which daisy-chains control and status information to all the drives.

Table 2-1

PROM SIZE/MEMORY CAPACITY

PROM LOCATIONS	PROM SIZE	ADDRESS	TOTAL CAPACITY
0-11	4x1024	0-1023	48x1024
12-23	-	-	
0-11	4x1024	0-1023	48x2048
12-23	4x1024	1024-2047	
0-11	4x2048	0-2047	48x2048
12-23	-	-	
0-11	4x2048	0-2047	48x3072
12-23	4x1048	2048-3071	
0-11	4x2048	0-2047	48x4096
12-23	4x2048	2048-4095	

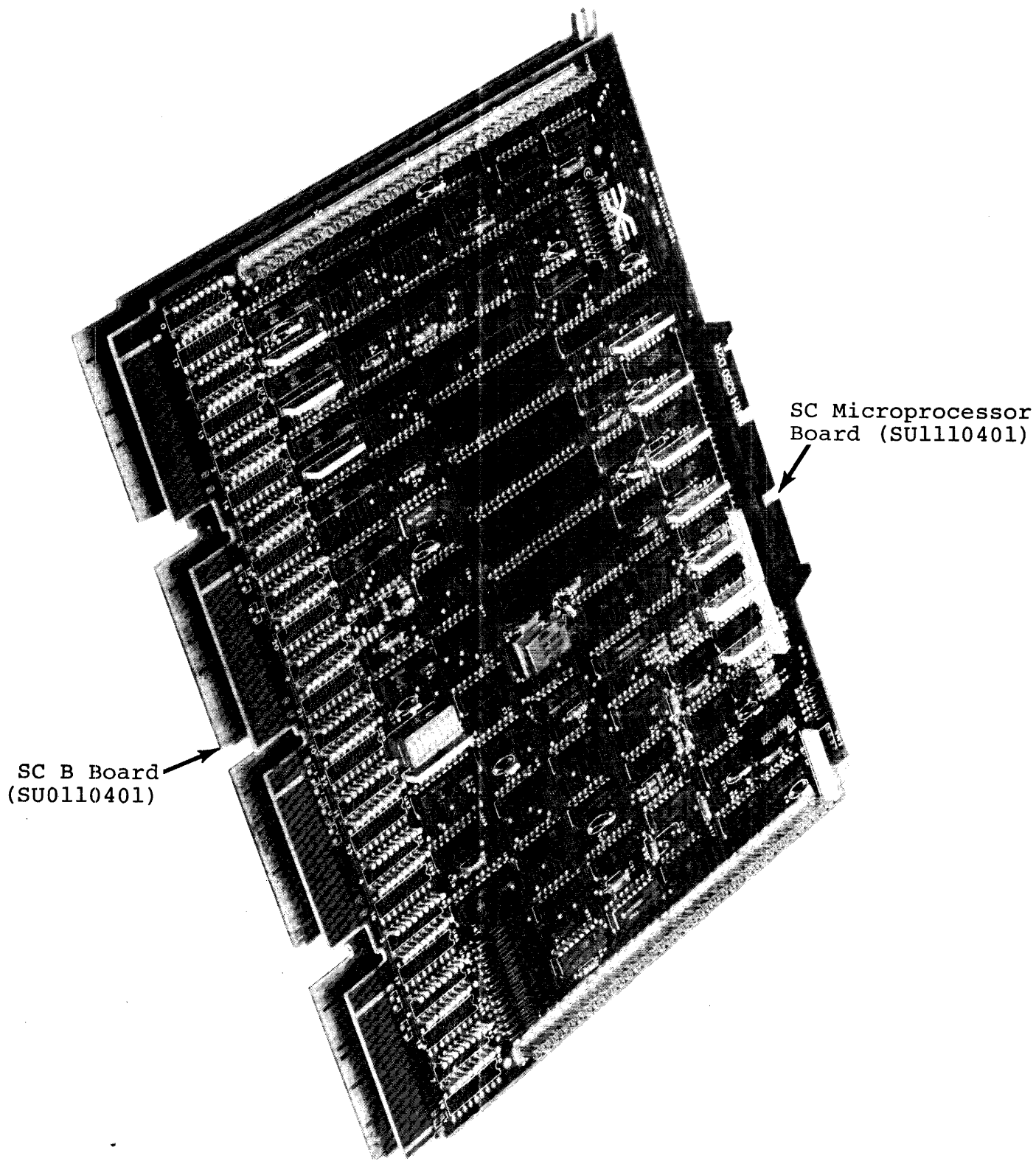


Figure 2-1  
SC01 Series Controller

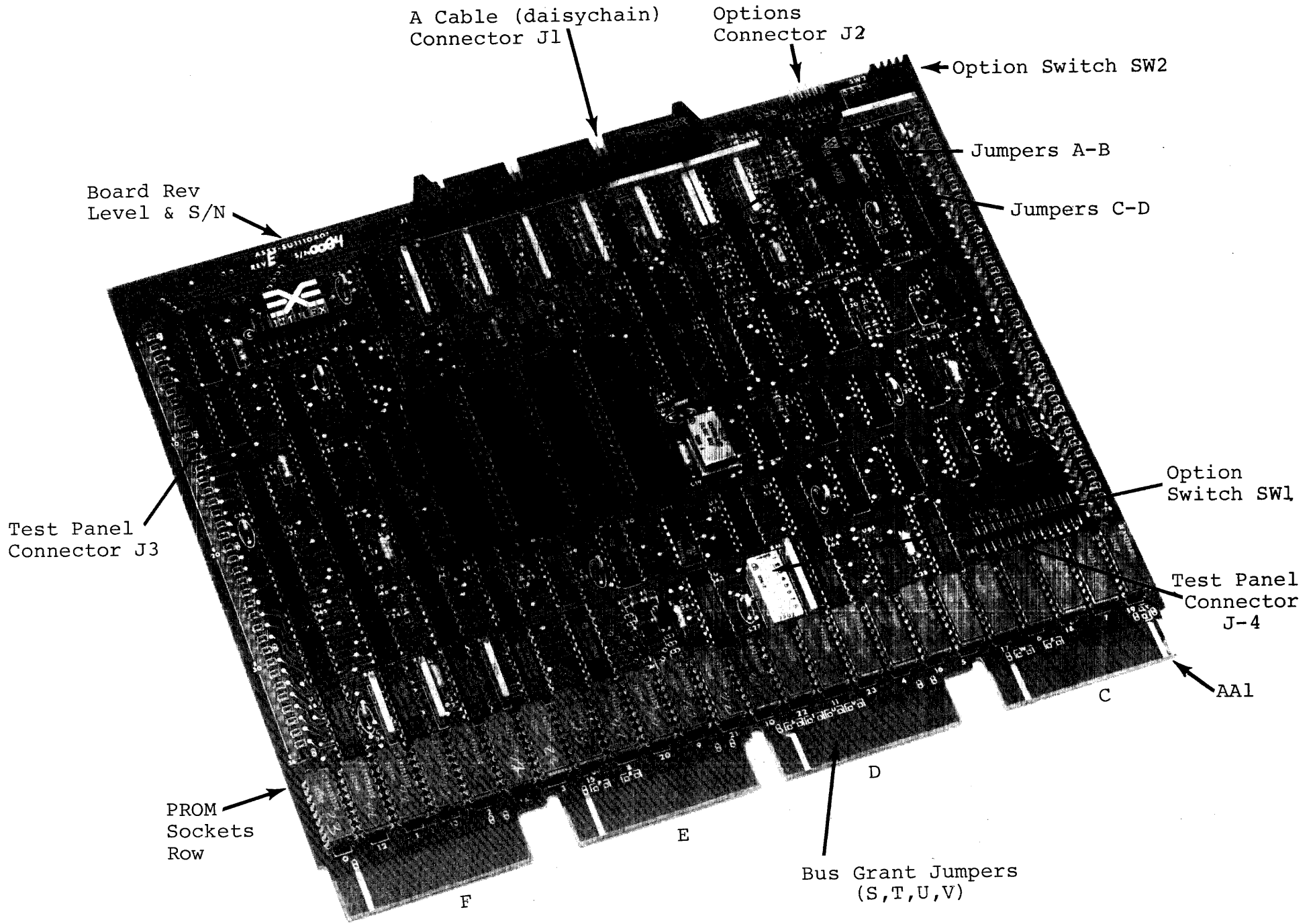


Figure 2-2  
SC Microprocessor Board

Connector J2 (if present) parallels switch SW2 and can be used to remote the switch.

Connectors J3 and J4 are used with the Emulex test panel during manufacture test and factory repair. They have no use in normal operation.

The DIP switch labeled SW1 is the option switch used to configure the firmware for drive and functional options to the basic controller. The use of these switches differs from one model to another. A summary of its use is found in Appendix B.

The switch labeled SW2 on the top right edge of the board is used to enable extended functions and formatting.\* Refer to Appendix B.

#### 2.1.1.2 PROM Locations

The microprocessor board contains a total of 24 locations for the PROM control memory. These IC locations are on the bottom row as indicated in Figure 2-2. Each location may have either a 4 x 1024 or a 4 x 2048 bit PROM installed to achieve different control memory capacities. PROM locations 0-11 (marked below the IC) contain the lower portion of control memory, and PROM locations 12-23 contain the upper portion. Table 2-1 gives the total control memory size for the different PROM sizes which can be installed.

Most of the SCXX/A emulations require only 1K of program space and therefore 12 4 x 1024 PROMS are used. The SCXX/B emulations require 2K of program space and either 12 4 x 2048 or 24 4 x 1024 PROMS are used.

#### 2.1.2 SC B Board

The bottom board of the controller assembly is designated Part Number SU0110402 and is known as the B board. This board contains the interface circuitry to the LSI-11 Q-Bus, the RAM buffer, the disk data circuitry including the ECC, and the interface to two drive B cables. The B board is shown in Figure 2-3. The board is a four layer PCB with power and ground planes on the inner layers and interconnects on the outer layers. The board dimensions and backplane connector arrangements are the same as the A board. The board contains card extractor handles which interface mechanically with the card cage of the LSI-11 or expansion cabinets. These handles are used for convenience in inserting and extracting the two board controller assembly and also act as a card retention mechanism when the controller is installed.

\*Note: Switch SW2 is not incorporated on Rev. A levels of the A board.

Although the B board is a quad size board, it makes use of the Q Bus connections only on the A and B connectors, so that the controller may be used with the DEC backplanes which use the C and D connectors for other functions.

NOTE

If such backplanes are used, it will be necessary to cut the etch between CM2 and CN2 and also between CR2 and CS2.

The power source in the lower left corner of the board generates -5 volts from the +5 volts for the disk cable drivers.

The B board can interface to two disk drives via the 26-pin connectors designated J1 and J2 at the top edge of the board. These connectors are for the radial B cables which transfer data between the drive and the controller. The two connectors are identical and interchangeable.

A set of four LED display lights are mounted along the top edge of the board as shown in Figure 2-3. These lights display operating and diagnostic status of the controller, and the interpretation depends upon the version of the controller.

### 2.1.3 Product Identification and Marking

The SC01 controller consists of the two boards defined in Paragraph 2.1.1 and 2.1.2. Each board has a unique part number and carries its own current revision level and board serial number. Locations of these identifications is shown in Figures 2-2 and 2-3 respectively. An individual disk controller board has the letter prefix "SU" to designate it as a board subassembly.

The two board set is combined into a controller assembly; for the LSI-11 compatible controller, the complete 4-digit prefix is "SC01", where the "SC" defines it as a complete two board assembly. This assembly is defined by a configuration code and revision level as follows:

SC01WW - XXX-YY-Z REV. W

1. The designation "WW" is a sequence number which differentiates between any different hardware versions which may exist in the SC01 series. The standard version is "01".

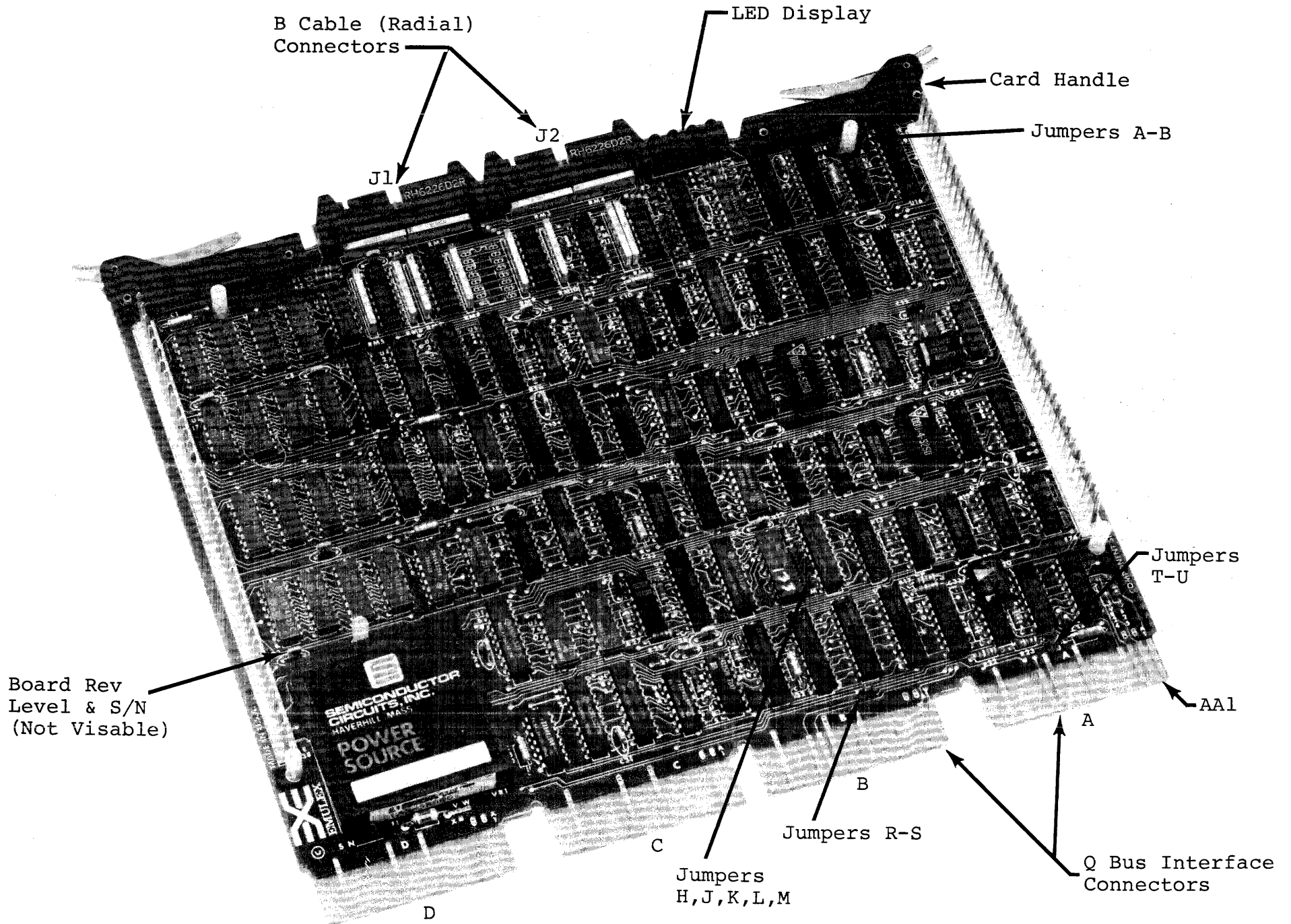


Figure 2-3  
SC B Board

2. The designation "XXX" identifies the microcode PROM set which implements the model (e.g., A, B, C), version (e.g., 1, 2, etc.), and revision level. For example, the B revision level of the A1 version will carry the code "A1B".
3. The "YY" designates any special hardware configuration. Currently, the only such configuration involves jumper strapping of the location of the Sector and Index pulses (A or B cable) and the bus address/range decode. Current codes are:

X0 - S&I on B Cable  
X1 - S&I on A Cable  
1X - SC01/A  
2X - SC01/B  
3X - SC01/C

4. The designation "Z" specifies the bus interrupt level: 4 = BR4; 5 = RB5.

The configuration is given on a label located on the SC Microprocessor Board. This label is installed at the time of shipment, and also contains the serial number of the completed assembly (which differs from the individual board serial numbers). The revision level is also for the completed assembly. This serial number is maintained for the complete assembly as long as the original boards stay together. Should one board be replaced by Emulex, a new serial number will be issued.

The individual boards are also marked with the Emulex name and have a "Made in USA" designation.

NOTICE

A patent application is pending on certain elements of the controller design, and this is so marked on the boards.



## 2.2 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC01 controller is shown in Figure 2-4. The controller is organized around a 16-bit high speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and a control store is implemented with 1K x 4K or 2K x 4K PROMS. Control store size is normally 1K or 2K depending on the emulation.

The controller incorporates a 1K x 16 high speed RAM buffer which is used to store the device registers of the controller being emulated and provide three sectors (768 words) of data buffering.

The A Cable Register (ACR) provides the storage for all the A cable signals going to the drives. The inputs from the selected drive can be tested by the microprocessor.

Serial data from the drive is converted to 16-bit parallel data and transferred to the buffer by the microprocessor. Likewise, data accessed from the buffer by the microprocessor is a serialized and sent to the drive under control of the servo clock received from the drive.

A 32-bit ECC shift register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC generation and checking is done independent of the microprocessor, but the correction process which involves the determination of the error position and pattern is done under the control of the microprocessor.

The DAL interface to the Q-Bus is a 16-bit bidirectional path using DEC approved transmitters and receivers. This path is used for programmed I/O DMA and transferring the interrupt vector. All transfers to or from the DAL interface are performed by the microprocessor. Address detection of the device address on the Q-Bus is performed by a PROM being used as a decoder. The Q-Bus multiplexes both data and addresses over the same set of DAL lines. All DMA timing is done by hardware, but the address and data transfers are done by the microprocessor.

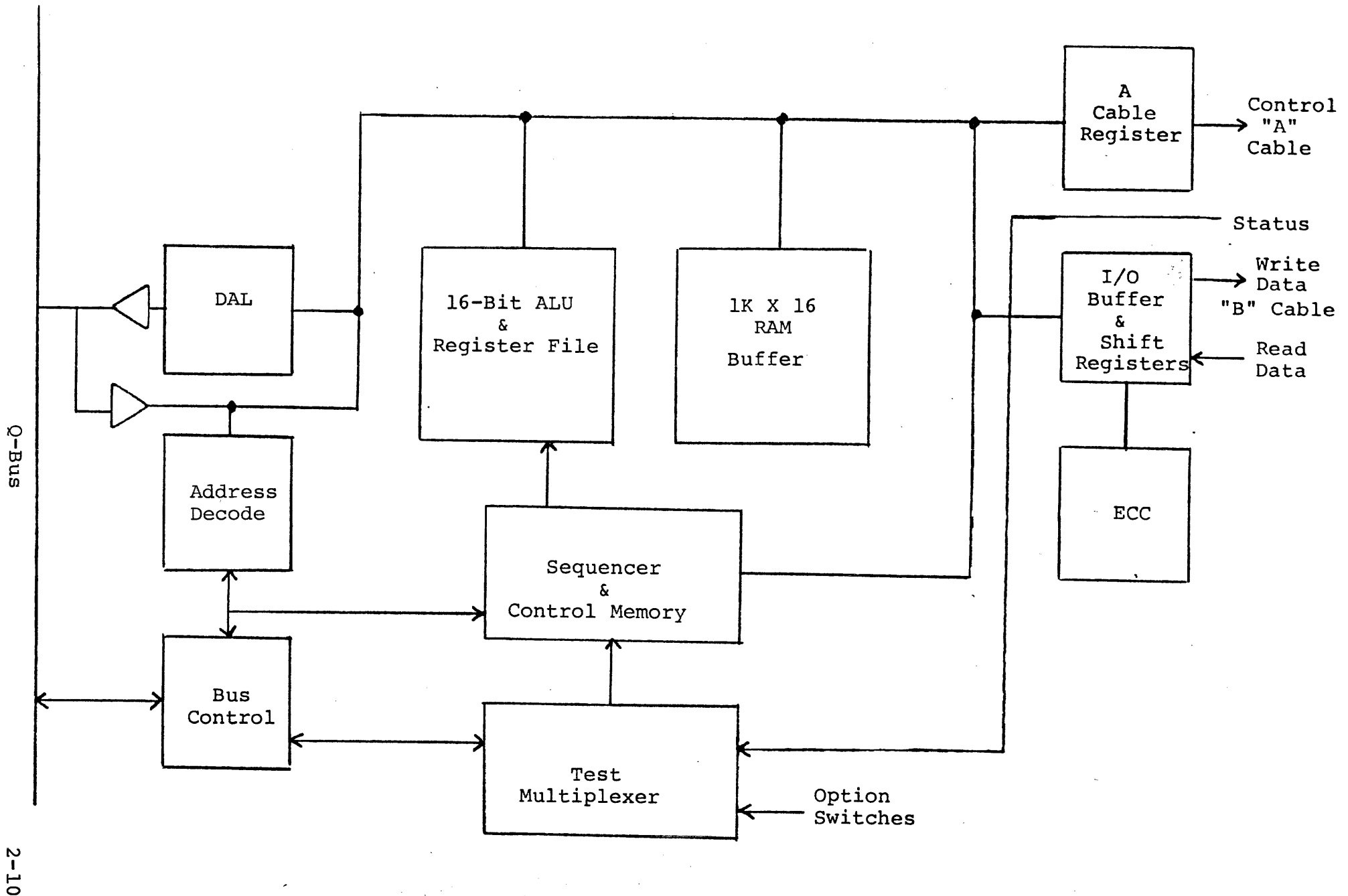


Figure 2-4  
SC01 Block Diagram

## SECTION 3 INSTALLATION

This section describes the step by step procedure for installation of the SC01 disk controller in an LSI-11 system.

### 3.1 INSPECTION

A visual inspection of the unit is recommended after unpacking. Specific checks should be made for such items as bent or broken pins or component leads, damaged components, or any other visual evidence of physical damage. The PROMS should be examined carefully to insure that they are firmly and completely seated into the sockets.

### 3.2 SETUP

Several configuration setups must be made on the controller before mounting it into the computer. In general, the unit will be configured to the customer requirements at the factory, but the setup information is listed here in case it becomes necessary to alter the setup after leaving the factory or if the proper setup was not performed at the factory.

To perform configurations on the B board, it will be necessary to separate the two boards. This is done by removing the four screws holding the Microprocessor A board to the B board and gently pulling the two boards apart until the AMP pins of the B board are clear of their receptacles. When the configuring is complete, the two boards should be reconnected again by carefully inserting the AMP pins into their correct and respective receptacles and replacing the four screws on the top of the A board. Inspect the AMP pins to insure that pins on the B board have not been misaligned into wrong sockets on the A board.

#### 3.2.1 Device Address Selection

The SC01 has an option of four device address locations and number of registers. The selection is made by jumpers between wire-wrap posts on the B board as indicated in Table 3-1. Refer to Figure 2-3 for physical location of these jumpers.

Table 3-1  
 BUS ADDRESS/REGISTER  
 RANGE CONFIGURATIONS

Emulex Model	DEC Models	Jumper Connections	Starting Address	Number of Registers
SC01/A	RP02, RP03	J to H	776700	16
SC01/B	RM02, RP06	K to H	776700	20
SC01/C	RK06, RK07	L to H	777440	16

### 3.2.2 Interrupt Vector Address

In the SC01 the interrupt vector address is supplied by the firmware. The vector address corresponds to the standard vector address assigned to the DEC controller being emulated. At least one alternate vector is also supplied. Alternate vectors are firmware dependent, and are selected via jumpers E-F and C-D on the B board.

### 3.2.3 Interrupt Selection

The SC01 controller interrupts on one of two interrupt lines depending on the type of LSI-11 computer. The selection is made by jumpers on the B board. For an LSI-11/23, the interrupt should be on the BIRQ5 signal and jumper R-S should be made and jumper T-U deleted. For the LSI-11 and LSI-11/2 computers, the interrupt should be on the BIRQ4 signal with jumper T-U being made and C-S being deleted. Refer to Figure 2-3 for physical location.

### 3.2.4 Index and Sector Pulse Selection

The SC01 series controllers are designed to have the Index and Sector pulse signals of the B cable from each physical drive. These signals are necessary to drive the sector counter associated with each B port. All the DEC emulations require an updated sector counter which can be read by the computer. Failure to have a valid sector counter can cause incorrect operation of rotational position sensing software. In some cases, this may not be important.

Depending on the disk drive, the Index and Sector signals may not be standardly available in the B cable. The Century drives have these signals available on both the A and B cables. The CDC drives standardly provide Index and Sector only on the A cable, but can be moved to the B cable by minor rewiring of the drive backplane or can be ordered from the factory with this wiring.

NOTE

It is recommended that all disk drives always be ordered to specify that Sector and Index be on the B cable.

It is possible to operate with the Index and Sector signals from the A cable if there is only a single physical drive or if proper operation of the sector counter in the device registers is of no concern. To operate with the Index and Sector pulses from the A cable, they must be ungated in the drive so that they are not a function of the drive being selected and will constantly be available even while the controller's microprocessor is polling nonexistent drives.

CAUTION

Failure to ungate the Sector and Index pulses may result in improper controller/drive operation. Refer to the Drive Manual.

A controller must be configured for receiving the Index and Sector pulses from the B cable or the A cable. This is done on both the A board and the B board as described below. (Refer to Figure 2-2 and 2-3 for location of the jumpers):

For Index and Sector pulses on the B cable:

- a. Install jumper A-B on the B board.
- b. Leave out jumpers A-B and C-D on the A board.

For Index and Sector pulses on the A cable:

- a. Leave out jumper A-B on the B board.
- b. Install jumpers A-B and C-D on the A board.

NOTE

If not specified in the purchase order, Emulex will standardly wire the A and B boards for Sector and Index pulses on the B cable.

### 3.2.5 Option and Configuration Switch

The DIP switches labeled SW1 at the bottom center of the A board is used to configure the firmware for certain disk drive characteristics and functional options. The use of these switches varies from one SC01 model to another. In addition, there is a four pole switch labeled SW2 on the top right of the A board which is used to invoke disk formatting and extended functions. Definition of the use of each switch can be found in Appendix B of this manual for currently available emulations. A more detailed description can be found in the User's Manual for the particular emulation model.

### 3.3 PHYSICAL INSTALLATION

In determining which slots to plug the controller into, it must be remembered that there must be boards in all slots ahead of the disk controller so that the two daisy-chained signals on the bsckplane have continuity up to the controller. The SC01 can be placed far down the DMA priority chain since it has an adequate amount of buffering to prevent data late errors, permitting assignment of higher DMA priority to other modules plugged into the LSI-11.

The controller boards should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. An attempt to force the boards into a slot with the components facing in the wrong direction may damage the backplane connectors. Always insert and remove the boards with the computer power off to avoid possible electrical damage to the boards. If the LSI-11 card cage can accommodate the extractors on the B board, they should be engaged and will be very useful for engaging and extracting the dual board controller. Be sure that both boards are properly in the throat of the connectors before attempting to seat the boards into the backplane.

### 3.4 DISK DRIVE SETUP

The disk drive must be configured for the proper number of sectors and have an ID plug.

#### 3.4.1 Sectoring

The disk drive must be configured for 32-sectors on all controller models except the SCXX/C which is configured for 33-sectors. 32-sectors per track is equivalent to a sector size of 420 dibits. The exact method of entering this 420 count into the logic of the drive will differ from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

For CDC drives, a value of 419 should be entered into the sector length switches. This is done by closing sector switches 0, 1, 5, 7, and 8.

#### 3.4.2 ID Plug

An ID plug in the range of 0-3 should be placed in the drive. Be careful that no two drives have the same number. Some drives have their address selected via switches on one of the logic cards, and do not use an ID plug.

### 3.5 CABLING

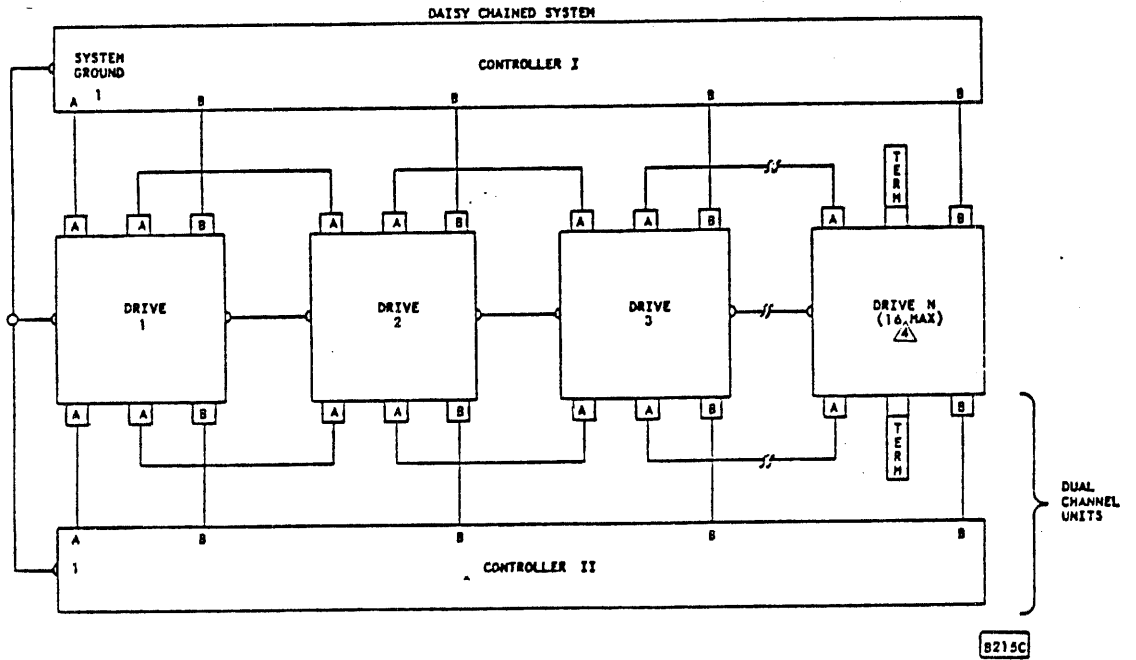
The subsystem cabling of the drives and controller is shown in Figure 3-1.

#### 3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is supplied by the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

#### CAUTION

The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate properly.



Notes:

1. Termination of "A" cable lines are required at controller and the last unit of the daisy chain.
2. Termination of "B" cable receiver lines are made at the controller and are on the unit's receiver cards.
3. Maximum cumulative A cable length per controller = 100 feet.  
Maximum individual B cable length = 50 feet.
4. The SC01 controller is limited to two physical drives.

Figure 3-1  
Unit Cabling



### 3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports on the B board of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

#### CAUTION

Observe the same caution on connector reversal given in paragraph 3.4.1.

### 3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put online with the controller. It can be connected for performing local offline maintenance on the drive.

#### CAUTION

Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

## 3.6 TESTING

### 3.6.1 Self-Test

When power is applied to the computer, the controller will execute a built-in self-test. The LED indicators on the top edge of the B board will flash momentarily. If all LED's turn off, the controller has completed its self-test. If an LED is on after the power-up, there is a problem in the controller and it is unusable. The controller is not addressable from the computer bus when the LED is on. See Appendix C for meaning of LED indicators. Most emulations will blink one of the LED's if self-test passes and no drive is seen on-line.

### 3.6.2 Register Examination

A quick check of the ability to read the controller's registers from the computer console can be made. All of the registers can be examined. A good register to examine at this point is the Drive Status Register. If the Drive  $\emptyset$  is online and ready, the contents of the register should be as follows:

<u>Model</u>	<u>Address</u>	<u>Contents</u>
SCXX/A	776710	140000 or 160000
SCXX/B	776712	010600 or 011600
SCXX/C	777452	100301

### 3.6.3 Diagnostics

The Emulex SCXX controllers execute the DEC diagnostics for the controller being emulated.

#### 3.6.3.1 Diagnostic Patches

The diagnostics may require some patches if they have not already been patched. The patches fall into three categories:

- a. Patches required to correct coding problems in the diagnostics. In some cases, they are supplied by DEC.
- b. Patches required to handle non-standard disk size, e.g., 19 track RM02 in the SCXX/B1 emulation.
- c. Patches to delete DEC controller maintenance-oriented functions not implemented in the controller. These patches are generally associated with the maintenance mode or where testing is done in the lower level logic test diagnostics. The performance exercises and formatters do not have any patches of this type.

The required patches for all three types of patches are available in the form of Application Notes from Emulex.

#### 3.6.3.2 Loading Diagnostics

The diagnostic program required should be loaded from paper tape, disk or magnetic tape. A convenient way of handling diagnostics is by the XXDP Diagnostic Monitor program. XXDP will allow the patches to be placed into the program so that they do not have to be entered

every time the program is loaded. It also will allow for convenient loading for disk or mag tape.

### 3.6.3.3 Running Diagnostics

Although the diagnostics may be started and run without the listings, the listing will provide a complete set of operational instructions and explain all the function capabilities of the program. In general, it is not necessary to have a complete listing of the diagnostic program for normal evaluation or maintenance of the disk subsystems.

When errors do occur, be sure to carefully evaluate the complete printout and try to correlate between error printouts. It should be remembered that with the SCXX/A emulations, the cylinder and track numbers of the printout do not correspond to the cylinder and track of the physical drive.

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## SECTION 4 INTERFACES

### 4.1 GENERAL

The controller interface conforms to the Flat Cable Interface Specification for SMD, MMD, FMD, and CMD disk drive families of Control Data Corporation (refer to Table A for reference document numbers). It should be noted that because of certain differences in drive characteristics, the interpretation and/or timing of various interface signals may differ between CDC drive types and also between a given CDC type drive and the equivalent drive type of another manufacturer.

Generally, each version of the controller is set up to interface a given type of drive so that these differences are handled by firmware, in which case no adapter is required. Subtle differences between makes and/or models of drives may require timing and/or functional modifications to an existing firmware package and/or addition of a hardware adapter to the disk drive.

For disk drives which do not incorporate the standard flat cable interface, a hardware adapter will generally be required at the disk drive to physically interface the standard flat cable connector to the type of connector on the drive. This adapter may in some cases include circuitry to handle functional/timing conversion of various signals to match an existing firmware set. In some cases, a special firmware implementation may be necessary.

The following defines the general physical electrical and functional characteristics of the controller disk interface.

#### 4.1.1 Connectors and Cables

The disk controller interfaces with the disk drive by two cables. The 60 conductor A cable daisy-chains to all the drives and plugs into the connector on the A board of the controller. The 26 conductor B cable is a cable between the drive and the controller and plugs into one of the connectors on the B board of the controller. The I/O cable characteristics are as follows:

### A cable

Type	30 twisted pair, flat cable
Twist Per Inch	2
Impedance	100 $\pm$ 10 ohms
Wire Size	#28 AWG, 7 strands
Propagation Time	1.6 to 1.8 ns./ft.
Maximum Cable Length	100 ft. cumulative
Connector Type	2 x 30 pins, 0.025" Sq, on 0.1" grid

### B cable (with ground plane)

Type	26 conductor, flat cable with ground plane and drain wire
Impedance	130 $\pm$ 15 ohms
Wire Size	#28 AWG, 7 strands
Propagation Velocity	1.65 ns./ft.
Maximum Cable Length	50 ft.
Connector Type	2 x 13 pins, 0.025" Sq, on 0.1" grid

#### 4.1.2 Input Circuits

The input receivers for the A and B cables are MC3450 quad differential receivers equivalent to 75108 receivers. The lines of the B cable are terminated with 82 ohms to ground. The lines of the A cable are terminated with 56 ohms to ground.

#### 4.1.3 Output Circuits

All output circuits to the drive are MC3452 quad transmitters equivalent to 75110A transmitters. The A cable is terminated with 56 ohms to ground from each line.

#### 4.1.4 A Cable Signals

There are 21 signals defined to the drive from the controller, and there are nine signals defined to the controller from the drive via the A cable. Refer to Figure 4-1.

Of the 20 controller-to-drive signals, 10 lines form a Tag Bus on which either Cylinder Address, Track Address, or Control functions are transmitted according to the state of three Tag designator lines. These operations are defined in Table 4-1 for SMD, MMD, and CMD class drives.

One signal, Busy, is used for dual channel drive operation only. The Address Mark Found signal is not used by SCXX series controllers.

There are special considerations associated with the Index and Sector pulses which are always on the A cable (refer to Section 3).

#### 4.1.4.1 Signals to Disk Drive

##### 1. Unit Select Tag

When this signal is asserted, the drive selected by the binary code on the Unit Select lines becomes selected and remains selected as long as the Unit Select Tag is asserted. In dual channel drives, this signal is also used to reserve the selected drive.

##### 2. Unit Select

These four lines are a binary code to select a logical number of the drive. The two high order bits are always zero since the controller can only select four drives (0-3).

##### 3. Tag 1

A pulse of approximately 1.2 microseconds which strobes the cylinder address, specified on the Bit lines, into the drive.

##### 4. Tag 2

A pulse of approximately 1.2 microseconds which strobes the head address, specified on the Bit lines, into the drive.

##### 5. Tag 3

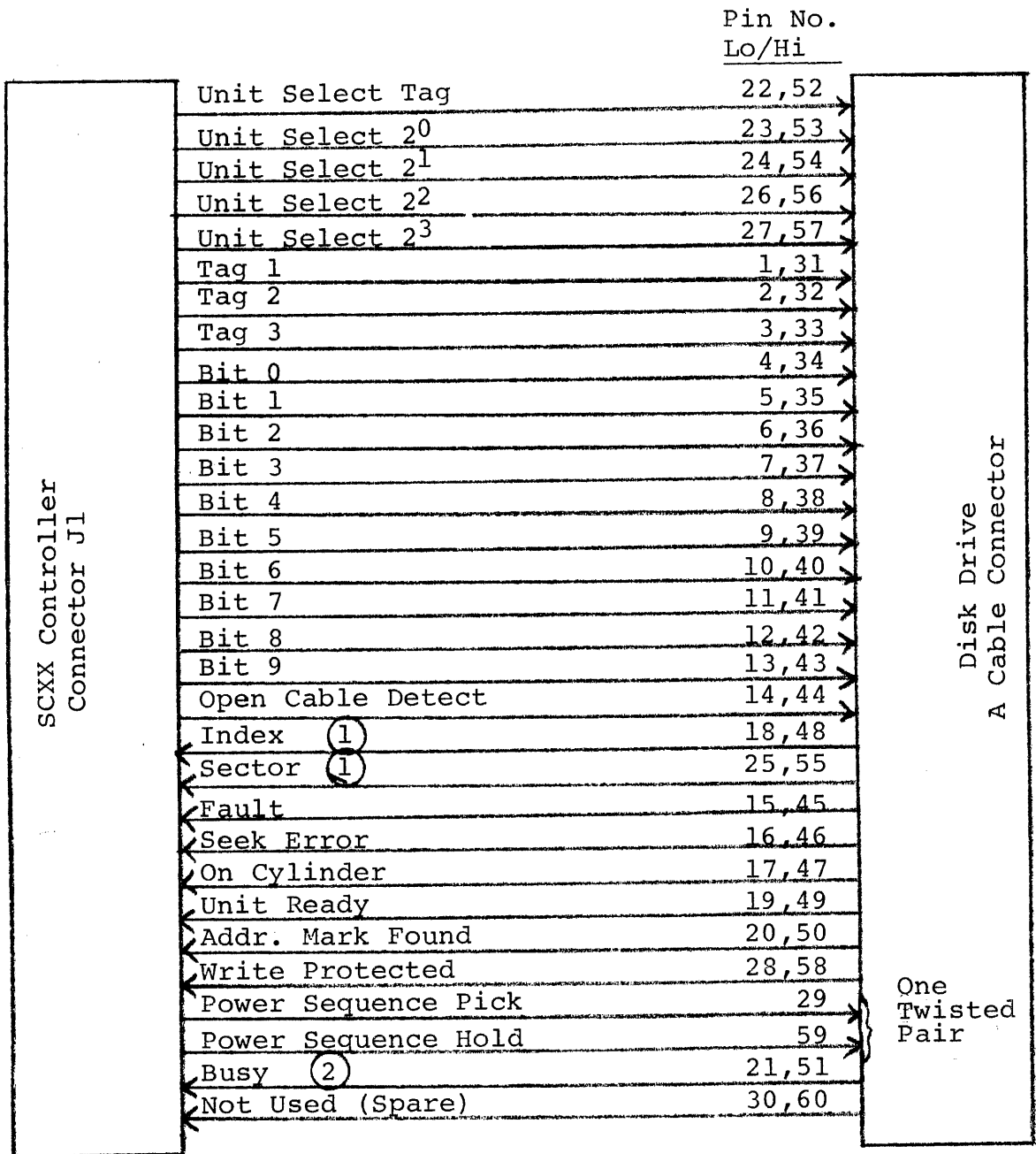
The Tag 3 is asserted for initiation of control functions specified on the Bit lines.

##### 6. Bit Lines (Tag Bus)

These ten lines carry the cylinder address (Tag 1), the head address (Tag 2), or a control function (Tag 3).

##### 7. Open Cable Detector

This signal is asserted all times to the drives when the cable is connected and the controller powered-up.



Notes

1. If Index and Sector pulses on A Cable are used, SCXX must be properly configured, system is limited to single drive operation, and drive must be selected as Unit 0.
2. Dual Channel Units only

Figure 4-1  
A Cable Signals



Table 4-1

TAG BUS DECODE, SMD/MMD/CMD

BUS	TAG 1 IN	TAG 2 IN	TAG 3 IN
	CYLINDER ADDRESS	HEAD SELECT	CONTROL SELECT
Bit 0	$2^0$	$2^0$	Write Gate
1	$2^1$	$2^1$	Read Gate
2	$2^2$	$2^2$	Servo Offset Plus
3	$2^3$	$2^3$	Servo Offset Minus
4	$2^4$	$2^4$ $\triangle_2$	Fault Clear
5	$2^5$		AM Enable
6	$2^6$		RTZ
7	$2^7$		Data Strobe Early
8	$2^8$		Data Strobe Late
9	$2^9$		Release $\triangle_1$



Dual channel units only.



This bit is also a fixed-volume select on a CMD drive. The stored volume address and "Tag 1" result in a volume select if the cylinder address is valid. A zero denotes the cartridge and a one denotes the fixed disks.

## 8. Power Sequence Pick and Hold .

These two signals are used to control the power-up sequencing of the drives so that only one drive powers-up at a time. These two signals will be at a ground potential when the controller is powered-up.

### 4.1.4.2 Signals From Disk Drive

#### 1. Fault

When this signal is asserted, a fault condition exists in the drive.

#### 2. Seek Error

When this signal is asserted, a Seek Error has occurred. The error is cleared by performing a return to zero. The signal indicates that the drive was unable to complete a seek within 500 milliseconds.

#### 3. On Cylinder

This signal indicates that the drive has positioned the heads over the desired cylinder.

#### 4. Unit Ready

This signal indicates that the drive is selected and up to speed, that the heads are positioned over the recording tracks, and that no fault condition exists within the drive.

#### 5. Write Protected

This signal is asserted when the drive is Write Protected. Any attempt to write while protected will cause a fault to be issued.

#### 6. Busy (Dual Channel Only)

This signal is asserted when the drive is reserved and/or selected by the other channel.

#### 7. Index

See paragraphs 3.2.4 and 4.1.6

#### 8. Sector

See paragraphs 3.2.4 and 4.1.6

#### 4.1.5 B Cable Signal

There are two signals defined to the drive from the controller, and there are seven signals defined to the controller from the drive via the B cable (refer to Figure 4-2).

Two of the signals from the drive - Index and Sector - are not always present in all drives, although these signals can be wired into the B cable. There are special considerations associated with these signals when they are not on the B cable (refer to Section 3).

##### 4.1.5.1 Signals to Disk Drive

1. Write Data

This signal carries the data which is to be recorded on the disk pack.

2. Write Clock

This signal is the clock used to transmit the Write Data to the drive. It has a positive edge in the center of the bit cell. The Write Clock is derived from the Servo Clock received from the selected drive.

##### 4.1.5.2 Signals From Disk Drive

1. Read Data

This signal transmits the recovered data in NRZ form.

2. Read Clock

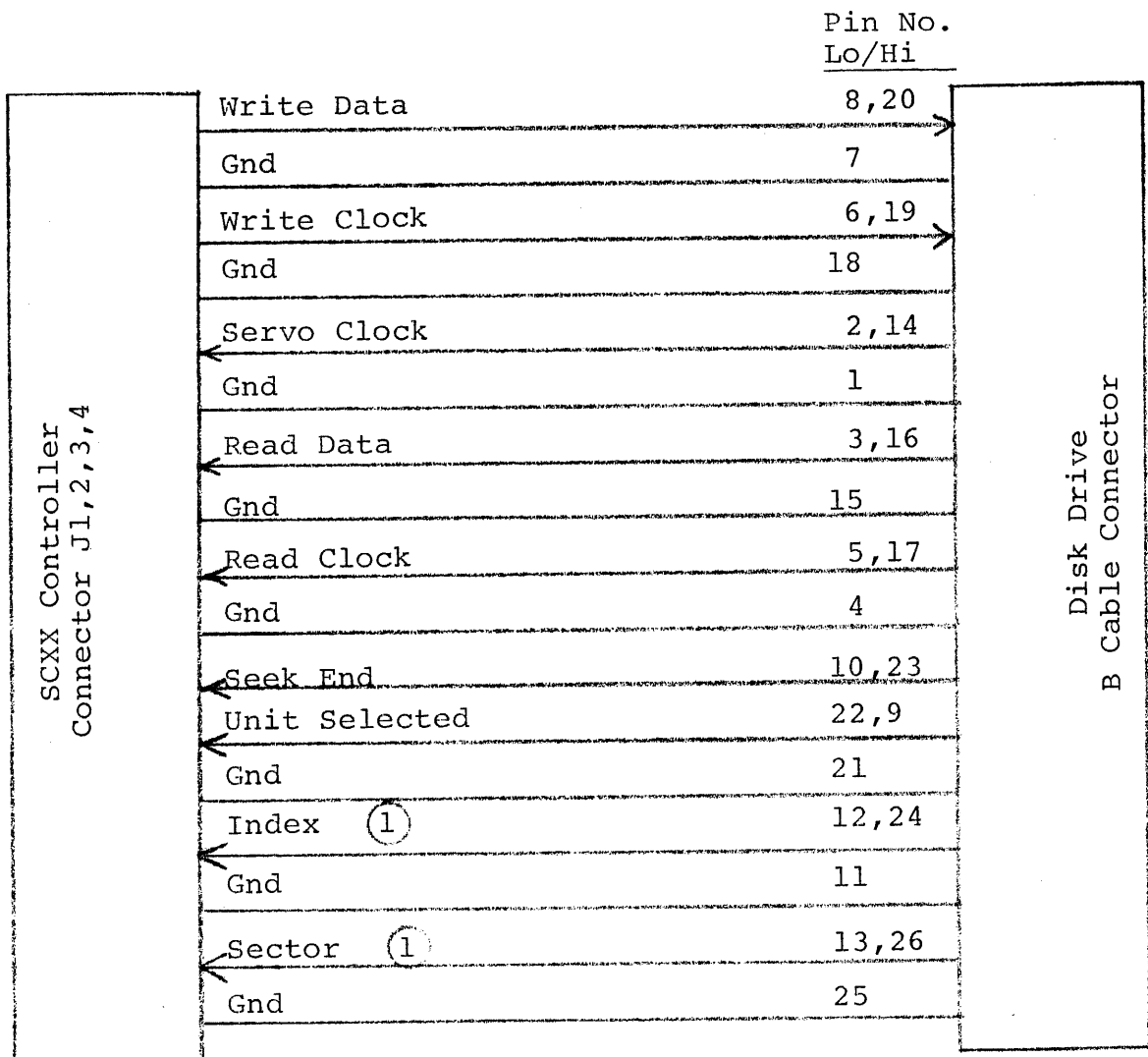
The Read Clock positive edge clocks the Read Data into the controller. This signal must be in phase lock with the data on the pack within ten microseconds after turning on Read Gate.

3. Servo Clock

This signal is a phase locked 9.677 MHz clock synchronized with the servo track of the drive. This signal is used to generate the Write Clock during write operation.

4. Seek End

Seek End is the logical combination of On Cylinder and Seek Error to indicate that a seek operation has terminated.



Note

1. Index and Sector pulses must be on the B Cable for multiple drive operation. Not all drives have these signals available on both the A and B Cables.

Figure 4-2  
B Cable Signals

#### 5. Unit Selected

This signal is asserted when the unit is selected. It is used by the controller to verify that a single unit has been selected in response to the assertion of the Unit Select Tag.

#### 6. Index

This signal is a pulse of approximately 2.5 microseconds occurring once per revolution. The leading edge of this pulse is considered to be the leading edge of sector zero.

#### 7. Sector Mark

This signal is a pulse of approximately 1.25 microseconds defining the beginning of all sectors except sector zero. The timing of the Sector Mark must be established in the drive by switches or jumpers as specified by the manufacturer. In some cases, there may be a Sector Mark defining a short unused sector immediately preceding the Index Pulse.

### 4.2 LSI-11 Q-BUS INTERFACE

The SC01 interfaces directly to the internal I/O bus of the LSI-11 (refer to Paragraph 2.1.3 for a description of the physical bus interface and definition of the module contact finger identification). The following types of I/O transfers occur between the controller and the processor and/or memory modules via the bus:

#### 1. Programmed I/O Transfers

These operations are executed by either single or double operand instructions; transfers to the controller may be either an 8-bit byte or a full 16 bit word. Programmed transfers are always for the purpose of exchanging control and status between the controller and the processor. The controller executes the following specific types of programmed bus cycles: DATI, DATO, DATOB, DATIO, DATIOB.

#### 2. DMA Transfers

All data read or write transfers, including read check and write check operations, are performed as full word DMA transfers between the controller and a memory device on the bus. The SC01 acts as the bus master controlling the transfer in all cases, using control information previously supplied by programmed instructions from the processor.

### 3. Interrupts

The controller generates several types of interrupts to the processor to flag the occurrence of various events (end of block, error condition, etc.). The controller generates a program interrupt vector for all interrupt conditions.

#### 4.2.1 Device Priority

Controller priority for DMA and interrupt requests is established by its physical position on the bus. The selection of device priorities is a system consideration. Since a disk memory involved relatively high peak transfer rates, and because delays in servicing data transfer requests may result in loss of information, the disk controller will normally be located in a relatively high priority position. However, because the buffering scheme of the SC01 will prevent data overrun conditions, it may be desirable to place the unit in lower bus priority positions to avoid data late conditions in devices with limited buffering. The board can physically mount in any pair of quad height card slots after the processor.

#### 4.2.2 Bus Signals

The LSI-11 Bus Signals to and from the SC01 via the A, B, C, D connectors on the SC B board (SU0110401) are tabulated in Table 4-2. The following should be noted:

1. All data and control signals used by the controller are interfaced via the A and B connectors, even though the unit plugs into all four connectors.
2. Power and ground connections are made via standard pins in the C and D connectors. In addition, the following jumper connections are made via etch on the SC01 board (but not on the standard LSI-11 backplane):

<u>Pins</u>	<u>Signals</u>
CR2 to CS2	BDMGIL to BDMGOL
CM2 to CN2	BIAKIL to BIAKOL

3. Designated spare pins BPl and AB1 are implemented in the SC01 controller with signals designated BIRQ6L and BIRQ7L respectively. These pins are used to permit installation of the SC01 in versions of the LSI-11 which may provide interrupt levels 6 and/or 7.

4. Pins AC1 and AD1 are implemented with extended address bits BAD16L and BAD17L; these signals are used to permit the SC01 to be installed in versions of the LSI-11 which provide extended addressing beyond 32K words (e.g., LSI-11/23).

#### 4.2.3 Initialization and Power Sequencing

The controller responds to an Initialize (INIT) signal on the LSI-11 bus by executing a specific microcode sequence. Generally, this will cause generation of a Control Reset function which will immediately terminate any function being executed by any drive.

Controller hardware monitors the dc power status line on the LSI-11 bus, BDCOKH (DC Power OK). In the event that BDCOKH falls, indicating that system DC power is unstable, the controller will (if able) terminate and clear the controller unconditionally. The SC01 has its own on-board dc power sensing circuit, independent of the bus signal. When dc power to the controller is stabilized, firmware will perform an automatic initialization so that it is ready to execute the initial software commands received.

#### 4.2.4 Electrical Specifications

The SC01 bus interface circuitry conforms to the bus specifications for the LSI-11. The logic levels specified by the manufacturer are:

##### Input Levels

TTL Logical Low: +0.8 Vdc max.

TTL Logical High: +2.0 Vdc min.

##### Output Levels

TTL Logical Low: +0.4 Vdc max.

TTL Logical High: +2.4 Vdc min.

The SC01 uses the following device types of the LSI-11 bus interface:

Receiver: National 8837. Equivalent types include Signetics 8T37, Motorola 3438.

Driver: T1 7438.

Transceiver: National 8641. Equivalent types include Signetics 8T38, Motorola 3438.

A standard unit load as specified by the manufacturer is equal to one receiver and two drivers and less than 10pf of circuit board etch. At nominal termination to 3.4V, this load represents approximately 130ua leakage in the logical high state.

All bidirectional lines terminate in the SC01 to an 8641 transceiver which presents one receiver and one driver load. All unidirectional inputs to the SC01 are terminated to a single 8837 receiver, and all unidirectional outputs from the SC01 are driven by a single open-collector 7438. Thus, the SC01 presents less than a single unit load (as defined) to the LSI-11 bus.



Table 4-2  
LSI-11 Interface Signals (SU0110401)

Bus Pin	Mnemonic	Description
AA1 AB1	BIRQ6L BIRQ7L	} Reserved for interrupt level expansion.
AC1 AD1	BAD16L BAD17L	} Extended address bits (implemented for bus address expansion)
AE1 AF1 AH1		} Unused
AJ1	GND	Ground
AK1 AL1		} Unused
AM1	GND	Ground
AN1	BDMRL	Direct Memory Access (DMA) Request
AP1 AR1 AS1		} Unused
AT1	GND	Ground
AU1 AV1		} Unused
BA1	BDCOKH	DC Power OK
BB1	BPOKH	AC Power CK
BC1 BD1 BE1 BF1 BH1		} Unused
BJ1	GND	Ground

Table 4-2  
LSI-11 Interface Signals (SU0110401) (Continued)

Bus Pin	Mnemonic	Description
BK1 BL1		} Unused
BM1	GND	Ground
BN1	BSACKL	Bus Master
BP1	BIRQ5L	Reserved for interrupt level expansion
BR1 BS1		} Unused
BT1	GND	Ground
BU1		Unused
BV1		Unused
AA2	+5	+5 V Power
AB2		Unused
AC2	GND	Ground
AD2		Unused
AE2	BDOUTL	Data Output
AF2	BRPLYL	Reply
AH2	BDINL	Data Input
AJ2	BSYNCL	Synchronize
AK2	BWTBTL	Write/Byte
AL2	BIRQ4L	Interrupt Request
AM2	BIAKIL	Interrupt Acknowledge Input
AN2	BIAKOL	Interrupt Acknowledge Output
AP2	BBS7L	Bank 7 Select
AR2	BDMGIL	DMA Grant-Input
AS2	BDMGOL	DMA Grant-Output
AT2	BINITL	Initialize
AU2 AV2	BDAL00L BDAL01L	} Data/Address Lines
BA2	+5	+5 V Power
BB2		Unused
BC2	GND	Ground
BD2		Unused

Table 4-2  
LSI-11 Interface Signals (SU0110401) (Continued)

Bus Pin	Mnemonic	Description
BE2	BDAL02L	} Data/Address Lines
BF2	BDAL03L	
BH2	BDAL04L	
BJ2	BDAL05L	
BK2	BDAL06L	
BL2	BDAL07L	
BM2	BDAL08L	
BN2	BDAL09L	
BP2	BDAL10L	
BR2	BDAL11L	
BS2	BDAL12L	
BT2	BDAL13L	
BU2	BDAL14L	
BV2	BDAL15L	
CJ1	GND	
CM1	GND	
CT1	GND	
CV1		Unused
CA2	+5	+5 V Power
CC2	GND	Ground
CR2	BDMGIL	DMA Grant Input (jumpered to CS2 on SC01)
CS2	BDMGOL	DMA Grant Output (jumpered to CN2 on SC01)
CM2	BIAKIL	Interrupt Acknowledge Input (jumpered to CN2 on SC01)
CN2	BIAKOL	Interrupt Acknowledge Output (jumpered to CM2 on SC01)
DJ1	GND	Ground
DM1	GND	Ground
DT1	GND	Ground
DA2	+5	+5 V Power
DC2	GND	Ground
DD2	+12	+12 V Power

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APPENDIX A  
REFERENCE DOCUMENTS

<u>Company</u>	<u>Document No.</u>	<u>Title</u>
CDC	64712400	Flat Cable Interface Specification for the SMD, MMD, and CMD Families
CDC	64709300	Product Specification, Storage Module Drive
CDC	64709700	Product Specification, Mini-Module Drive
CDC	75888221	Product Specification, Cartridge Module Drive
CDC	75888415	Hardware Maintenance Manual, CMD
DEC	1978	PDP-11 Peripherals Handbook
DEC	EK-11034-UG-001	PDP-11/34 System User's Manual
DEC	EK-RP11E-MM-001	RP11-E Disk Pack Drive Controller Maintenance Manual
DEC	EK-RP056-OP	RP05/RP06 User's Manual
DEC	EK-RM023-UG-001	RM02/03 Disk Subsystem User's Guide

APPENDIX B  
OPTION SWITCHES

Table B-1 is a summary of the SW1 and SW2 option switches for most SC01 models. See appropriate User's Manual for a detailed description of the switches and the recommended settings.

Table B-1

	A1	A2	A3	A4	A5	A6	A7	A8	B1	B2
SW1-1	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Not Used	Format Enable	411 Cylinder Select	5 Track Select
SW1-2	CMD Fixed Volume	CMD Fixed Volume	CMD Fixed Volume	Config. Select #1	CMD Fixed Volume	Not Used	Config. Select #1	6/10 Head Select	Checksum Enable	Checksum Enable
SW1-3	Not Used	823 Cylinder Select	12/24 MByte Select	Config. Select #2	Not Used	Not Used	Config. Select #2	Kennedy Addressing Select	815 Cylinder Select	823 Cylinder Select
SW1-4	No ECC Correction	No ECC Correction	No ECC Correction	No ECC Correction	No ECC Correction	No ECC Correction	No ECC Correction	No ECC Correction	19 Track Select	32 Sector Select
SW1-5	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	Alt. ECC Correction	CMD Fixed Volume	Not Used
SW1-6	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Single Port Select	Single Port Select
SW1-7	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	DMA Bandwidth Control	DMA Bandwidth Control
SW1-8	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode
SW2-1	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Extended OP Codes	Extended OP Codes
SW2-2	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.
SW2-3	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	4 Wd.DMA Burst Select	4 Wd.DMA Burst Select
SW2-4	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

APPENDIX C  
LED INDICATORS

There are four LED indicators on the top of the B board. These are used to indicate controller activity and the results of self-test as follows:

- LED 1: LED will flicker during controller operation to indicate activity with the disk and computer. If LED is on after a power up, it indicates the self-test failed in the ECC test.
- LED 2: If LED is on at end of self-test, it indicates that self-test failed buffer test.
- LED 3: If LED is on at end of self-test, it indicates that self-test failed ECC/CRC test.
- LED 4: This LED will be on under any one of the following conditions:
  - a. Self-test failed; or
  - b. No drive has power on; or
  - c. All drives respond to same unit select address; or
  - d. No drive has a unit number 0-3; or
  - e. Either the A cable, or the B cable, or both, is not properly connected.

In most emulations this LED is on steady for condition A only. For conditions B-E the LED will blink.

**BLANK**



## APPENDIX D

### SC01/B3 CONFIGURATION AND ADDRESS SELECTION

#### D.1 INTRODUCTION

To allow the SC01/B3 user maximum flexibility in disk drive selection, the SC01/B3 supports a wide variety of disk types. This appendix provides the switch settings which make possible this flexibility.

#### D.2 CONTROLLER CONFIGURATION

The SC01/B3 unit is capable of supporting a wide variety of disk drives. Switch SW1-1, SW1-2, SW1-3 SW1-4, and SW1-5 define the various drives which are supported, and a list of these drive types and sizes may be found in Table D-1. Table D-2 gives the proper switch settings for each of the various configurations.

##### D.2.1 Drive Configuration Selection

The SC01/B3 emulates three different DEC disk subsystems, the RM02, the RM03, and the RM05. The RM02 and RM03 have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb.

The Drive Configuration table (Table D-2) reflects the number of physical cylinders and tracks assigned to each unit. Those units marked with an asterisk appear to the software as a unit with twice the number of specified cylinders and one half the number of specified tracks. All units have 32 sectors per track.

1. Locate your drive type and size in Table D-1. Note the KEY assigned to each type of drive you intend to use. Make sure your drive is hard sectored and set at 32 sectors.
2. Scan down the KEY column of Table D-2 until you find your drive's number. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.
3. After finding a suitable match for Drive 0, check the drive key and type for Drive 1 for that configuration row. It is not necessary to use both drive ports.
4. When you have found an entire configuration which is suitable, set the configuration switches as indicated.

TABLE D-1  
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
5	64	4	32	9733-5/CDC
30	561	3	32	3350/PRIAM
40	589	4	32	2311/FUJITSU
80	823	5	32	9762,9730-80/CDC, T82RM/CENTURY, 5300-80/KENNEDY, 80/AMPEX
84	589	7	32	2312/FUJITSU
150	411	19	32	9764/CDC
160	1645	5	32	160/AMPEX, BD160/BALL
165	823	10	32	165/AMPEX, 9730-160/CDC, M2284/FUJITSU
300	823	19	32	9766/CDC, T302/CENTURY
675	842	40	32	9775/CDC

TABLE D-2  
DRIVE CONFIGURATIONS

CONF. NO.	SW-					PHYSICAL		Drive Type
	5	4	3	2	1	KEY	Unit	
00	O	O	O	O	O	80	0	RM02
						80	1	RM02
01	O	O	O	O	C	165	0	RM02
						165	1	RM02
02	O	O	O	C	O	165	0*	RM02
						165	1*	RM02
03	O	O	O	C	C	160	0	RM02
						160	1	RM02
04	O	O	C	O	O	300	0	RM05
						300	1	RM05
05	O	O	C	O	C	300	0	RM02
						300	1	RM02
06	O	O	C	C	O	NOT USED		
						NOT USED		
07	O	O	C	C	C	675	0	RM02
						675	1	RM02
08	O	C	O	O	O	675	0*	RM05
						675	1*	RM05
09	O	C	O	O	C	5	0	RM02
						5	1	RM02
0A	O	C	O	C	O	30	0	RM02
						30	1	RM02
0B	O	C	O	C	C	NOT USED		
						NOT USED		
0C	O	C	C	O	O	40	0	RM02
						40	1	RM02

TABLE D-2  
DRIVE CONFIGURATIONS (Con't)

CONF. NO.	SW-					PHYSICAL		Drive Type
	5	4	3	2	1	KEY	Unit	
0D	O	C	C	O	C	84	0	RM02
						84	1	RM02
0E	O	C	C	C	O	150	0	RM02
						150	1	RM02
0F	O	C	C	C	C			
10	C	O	O	O	O			
11	C	O	O	O	C			0F - 14 NOT USED
12	C	O	O	C	O			
13	C	O	O	C	C			
14	C	O	C	O	O			
15	C	O	C	O	C	80	0	RM02
						165	1	RM05
16	C	O	C	C	O	80	0	RM02
						165	1*	RM03
17	C	O	C	C	C	80	0	RM02
						160	1	RM03
18	C	C	O	O	O	80	0	RM02
						300	1	RM05
19	C	C	O	O	C	80	0	RM02
						300	1	RM03
1A	C	C	O	C	O	NOT USED		
						NOT USED		
1B	C	C	O	C	C	80	0	RM02
						675	1	RM03
1C	C	C	C	O	O	80	0	RM02
						675	1*	RM05
1D	C	C	C	O	C	80	0	RM02
						5	1	RM05
1E	C	C	C	C	O	300	0	RM05
						675	1	RM03
1F	C	C	C	C	C	300	0	RM02
						675	1*	RM03

\*See paragraph D.2.1

### D.3 Alternate Address and Vector Selection

The address selections are made via jumper connections on the "B" board (Emulex part number SU010402). The necessary connections for each address are contained in Tables D-3 and D-4.

TABLE D-3  
ALTERNATE ADDRESS SELECTION

Jumper Connections	Starting Address	Address Number
H to J	776300	Alternate #1
H to K	776700	Standard RM
H to L	776100	Alternate #2
H to M	775400	Alternate #3

TABLE D-4  
ALTERNATE VECTOR SELECTION

Jumper Connections	Connection	Address Number
C to D E to F	OPEN OPEN	254 (Standard RM)
C to D E to F	OPEN Jumper In	150
C to D E to F	Jumper In OPEN	370
C to D E to F	Jumper In Jumper In	374

#### D.4 Option Switches

There are two switches on the SC01/B3 microprocessor board (Emulex part number SU1110403). SW1 is located between U63 and U64 near the bottom of the board. SW2 is a "piano type" switch, and is located near the top right corner of the board. Tables D-5 and D-6 list the switch settings.

TABLE D-5  
CONFIGURATION SWITCH SETTINGS

Switch	Open	Closed	Function
SW1-1		See Table D-2	Configuration Select #1
SW1-2		See Table D-2	Configuration Select #2
SW1-3		See Table D-2	Configuration Select #3
SW1-4		See Table D-2	Configuration Select #4
SW1-5		See Table D-2	Configuration Select #5
SW1-6	Disable	Enable	Dual-Port Mode
SW1-7	Disable	Enable	DMA Request Bandwidth
SW1-8	Disable	Enable	Checksum enable for data transfers

TABLE D-6  
OPTION SWITCH SETTINGS

Switch	Open	Closed	Function
SW2-1	Disable	Enable	Century Trident compatibility
SW2-2			Not used <sup>1</sup>
SW2-3	Two Words	Four Words	DMA Burst

<sup>1</sup>All unused switches must be closed.

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