SYSTEM 80

MICROCOMPUTER SYSTEM

PRELIMINARY PRODUCT BROCHURE

JUN 16 1976

ELECTRONIC MEMORIES & MAGNETICS CORPORATION

12621 Chadron Avenue. Hawthorne. California 90250 / Telephone: (213) 644-9881

INTRODUCTION
SYSTEM 80

The SYSTEM 80 is a true OEM general purpose microcomputer system component that offers the best performance available today. With its 175 nanosecond microprocessor cycle time it is faster than most minicomputers on the market. An increment register requires only 650 nanoseconds and a double add only 850 nanoseconds. For real time operations, the SYSTEM 80 can respond to an interrupt as fast as 3.4 microseconds. This includes saving the current program counter, current program status bits, current accumulator content and enabling interrupts for the next higher level device. While others are talking about lower speed at reduced prices, EMM is delivering higher speeds at reduced prices. Now you can develop a microprocessor based product which will have a price/performance advantage for many years. The SYSTEM 80 uses an 8080 compatible instruction set saving any software and training you may already have invested.

The SYSTEM 80 was designed for the most demanding microprocessor applications. Features include:

- Choice of memories
  - Non-volatile Core (650 nsec or 850 nsec)
  - Low-cost NMOS 4K Static RAM (no refresh required)
  - High-speed NMOS 1K Static RAM (no refresh required)
  - Bipolar ROM, PROM
- Intermixing of memories
- Complete 8080 instruction set compatibility
- Memory addressing to one megabyte
- DMA with up to 5.5 megabytes/second
- Programmed I/O to 125K bytes/second
- Serial I/O port
- Vectored priority interrupts
- Real Time Clock
- ROM Bootstrap Loader
- Operator Control Panel
- Power Failure/Auto Restart
- Chassis and Power Supply
- Disk Executive System
- Program Generation Software to One Megabyte

EMM's powerful CPU and long experience building state-of-the-art core and NMOS memories for demanding OEM accounts provides a reliable and capable microcomputer system. This manual provides detailed data on the features of SYSTEM 80 and its capabilities. Based on this data we believe you will choose SYSTEM 80.

SPECIFICATIONS
SYSTEM 80

Processor

Data Word Length	8 Bits
Instruction Word Length	8, 16, 24 Bits
Number of Instructions	78 (8080 Compatible)
Fixed Point Arithmetic	2's Complement and BCD
Programmable Registers	8
Addressing Range	64K Direct 1 Megabyte Extended
Microprogrammed	Yes
Basic Cycle Time	175 nsec

Memory

Type	Core/Semiconductor RAM/ROM
Memory Cycle Time	850 and 650 nsec/450 nsec/ 180 nsec
Memory Access Time	300 nsec/275 nsec/150 nsec
Memory Increments	16K, 32K or 64K bytes

Input/Output

DMA	Standard to 5.5 mbytes/sec
Programmed I/O	Standard to 125K bytes/sec
Interrupt Response	3.4 Microsec*
I/O Bus Levels	+5V and GND
I/O Devices	256

*Interrupt response time includes saving current program counter, status word and accumulator and enabling interrupt for the next cycle.

Environment

Operating Temperature	$0^{o}C$ to $50^{o}C$
Storage Temperature	$-55^{o}C$ to $85^{o}C$
Relative Humidity	to 95% without condensation

Packaging

Chassis Dimensions (With Power Supply)	$5\frac{1}{4}$ or 7 inches By 21 by 17.6
Mechanical Interface	19 inch EIA Rack
Weight (Without Cards)	65 lbs.
Power Required	115 or 230VAC $\pm$10%, 50 or 60HZ single phase, 9 amperes maximum.

DETAILED HARDWARE DESCRIPTION
SYSTEM 80

INPUT/OUTPUT SYSTEM

The SYSTEM 80 Input/Output System can address up to 256 devices and has three basic modes for flexibility and ease of use. They are as follows:

Programmed I/O

Program controlled input/output uses the executing program to transfer bytes between the external device and the CPU A-Register. I/O instructions are used to determine the device's readiness to receive or transfer data. This type of transfer is most effective where data is to be operated on immediately after input or just prior to output. Devices such as keyboard terminals, displays and paper tape readers and punches generally use this I/O mode. The SYSTEM 80 uses this mode for its standard TTY Controller.

Direct Memory Access (DMA)

Where high speed transfer rates are required, the DMA bus allows data to flow directly between the memory and the external device without service by the program. This is accomplished on a cycle-stealing basis and bypasses the CPU. DMA is required when the program could not keep up with the transfer rate or when the programmer does not wish to handle each data transfer. A powerful capability of the DMA is that it allows the external device to communicate directly with up to one megabyte of memory.

Interrupt Control

Interrupt handling is included in the SYSTEM 80 and provides an external device with a means to gain immediate CPU attention. This system, when used by the external device, provides for recognition and identification of an external event as well as automatic vectoring to a unique memory location. Interrupt controlled I/O is generally used for process control applications and allows one sub-routine to service many I/O devices randomly. The SYSTEM 80 contains many unique instructions for interrupt handling such as enable/disable interrupt, stack commands for saving and restoring register and status and special single byte return commands. This allows simple interrupt routines with rapid execution times.

The following table lists the input/output signals available to the user.

Name	Function
A00-A19	Address Bits 00-19 (20 bits)
DB0-DB7	I/O Data Bus Bits 0-7 (8 bits)
INTE	Interrupts Enabled
MSYN	Memory Sync from Requestor
HLTA	Halt Acknowledge
HOLDR	Hold Request
READY	Ready to Transfer Data
I/ORST	I/O and Proccesor Reset
SYNC	Processor Sync
RESET	I/O and Processor Reset
INTR	Interrupt Request
DSTR	Data Strobe
IOSN	I/O Sync
DADR	Data Direction
HOLDAI	Hold Acknowledge In
HOLDAO	Hold Acknowledge Out
INTAI	Interrupt Acknowledge In
INTAO	Interrupt Acknowledge Out

The I/O card slot has all the above signals present plus adequate amounts of +5V, +15V and -15V. 80 pins are available for the user interface.

INSTRUCTION EXECUTION TIMES

The SYSTEM 80 contains an advanced microprogrammed asynchronous bipolar MSI Central Processor (CPU) and standard Control ROM's (CROM's) which provide complete instruction set compatibility with the 8080. Because the CPU is bipolar, the SYSTEM 80 offers much faster execution times than the 8080. A complete list of instructions and times are shown in the following table.

The following abbreviations are used in the table:

WC	With Carry
WB	With Borrow
RG1	Any Register (A, B, C, D, E, H, L)
RG2	Any Register Other Than RG1
SP	Stack Pointer
PC	Program Counter
M	Memory Location Defined by Contents of H and L
EOR	Exclusive OR
IOR	Inclusive OR
B2	Byte 2 of the Instruction
B3	Byte 3 of the Instruction
(X,X)	Memory Location Defined by X, X

INSTRUCTION	DESCRIPTION	EXECUTION TIME 650ns Memory Microsec	EXECUTION TIME 180ns Memory Microsec
ADD RG1	Add RG1 to A	.8	.65
ADC RG1	Add RG1 to A WC	.8	.65
SUB RG1	Subtract RG1 from A	.8	.65
SBB RG1	Subtract RG1 from A WB	.8	.65
ANA RG1	AND RG1 with A	.8	.65
XRA RG1	EOR RG1 with A	.8	.65
ORA RG1	OR RG1 with A	.8	.65
CMP RG1	Compare RG1 with A	.8	.65
INR RG1	Increment RG1	.8	.65
DCR RG1	Decrement RG1	.8	.65
INX B	Increment B and C	1.0	.85

INSTRUCTION	DESCRIPTION	EXECUTION TIME 650ns Memory Microsec	180ns Memory
INX D	Increment D and E	1.0	.85
INX H	Increment H and L	1.2	1.05
INX SP	Increment SP	1.2	1.05
DCX B	Decrement B and C	1.0	.85
DCX D	Decrement D and E	1.0	.85
DCX H	Decrement H and L	1.2	1.05
DCX SP	Decrement SP	1.2	1.05
RRC	Rotate A Right	.8	.65
RLC	Rotate A Left	.8	.65
RAL	Rotate A Left Through Carry	.8	.65
RAR	Rotate A Right Through Carry	.8	.65
MOV RG1, RG2	Move RG2 into RG1	.8	.65
MOV M, RG1	Move RG1 into M	1.40	.90
MOV RG1, M	Move M into RG1	1.50	.90
MVI RG1	Move B2 into RG1	1.40	.90
MVI M	Move B2 into M	2.10	1.15
ADD M	Add M to A	1.43	.90
ADC M	Add M to A WC	1.43	.90
SUB M	Subtract M from A	1.43	.90
SBB M	Subtract M from A WB	1.43	.90
ANA M	AND M with A	1.43	.90
XRA M	EOR M with A	1.43	.90
ORA M	OR M with A	1.43	.90
CMP M	Compare M to A	1.43	.90
INR M	Increment M	2.30	1.30
DCR M	Decrement M	2.30	1.30
ADI	Add B2 to A	1.43	.90
ACI	Add B2 to A WC	1.43	.90
SUI	Subtract B2 from A	1.43	.90
SBI	Subtract B2 from A WB	1.43	.90
ANI	AND B2 with A	1.43	.90
XRI	EOR B2 with A	1.43	.90
ORI	OR B2 with A	1.43	.90
CPI	Compare B2 with A	1.43	.90
STAX B	Move A to (B, C)	1.90	1.30
STAX D	Move A to (D, E)	1.90	1.30
LDAX B	Move (B, C) to A	1.70	1.30
LDAX D	Move (D, E) to A	1.70	1.30
LXI B	Move B2 to C, B3 to B	2.15	1.35
LXI D	Move B2 to E, B3 to D	2.15	1.35
LXI H	Move B2 to L, B3 to H	2.15	1.35
LXI SP	Move B2 to SP (low), B3 to SP (high)	2.15	1.35

INSTRUCTION	DESCRIPTION	EXECUTION TIME 650ns Memory	180ns Memory
		Microsec	
LDA	Move B2 to A	2.83	1.95
STA	Move A to (B2, B3)	3.20	1.95
SHLD	Move L to (B3, B2), H to (B3, B2+1)	3.90	2.15
LHLD	Move (B3,B2) to L, (B3,B2+1) to H	3.75	2.40
XCHG	Swap D and H, E and L	1.00	.85
XTHL	Swap L and (SP), H and (SP+1)	3.60	2.00
SPHL	Move H and L to SP	1.00	.85
PCHL	Move H and L to PC (Jump Indirect)	1.00	.85
DAD B	Add B and C to H and L	1.00	.85
DAD D	Add D and E to H and L	1.00	.85
DAD H	Add H and L to H and L	1.20	1.05
DAD SP	Add SP to H and L	1.20	1.05
JMP	Jump - Move B3, B2 to PC	2.20	1.55
JC	Jump on Carry	2.20/.80	1.55/.65
JNC	Jump on No Carry	2.20/.80	1.55/.65
JZ	Jump on Zero	2.20/.80	1.55/.65
JNZ	Jump on No Zero	2.20/.80	1.55/.65
JP	Jump on Positive	2.20/.80	1.55/.65
JM	Jump on Minus	2.20/.80	1.55/.65
JPE	Jump on Parity Even	2.20/.80	1.55/.65
JPO	Jump on Parity Odd	2.20/.80	1.55/.65
CALL	Call Move B3, B2 to PC	3.55	2.20
CC	Call on Carry	3.55/1.40	2.20/.90
CNC	Call on No Carry	3.55/1.40	2.20/.90
CZ	Call on Zero	3.55/1.40	2.20/.90
CNZ	Call on No Zero	3.55/1.40	2.20/.90
CP	Call on Positive	3.55/1.40	2.20/.90
CM	Call on Minus	3.55/1.40	2.20/.90
CPE	Call on Parity Even	3.55/1.40	2.20/.90
CPO	Call on Parity Odd	3.55/1.40	2.20/.90
RET	Return Unconditional	2.20	1.55
RC	Return on Carry	2.20/.80	1.55/.65
RNC	Return on No Carry	2.20/.80	1.55/.65
RZ	Return on Zero	2.20/.80	1.55/.65
RNZ	Return on No Zero	2.20/.80	1.55/.65
RP	Return on Positive	2.20/.80	1.55/.65
RM	Return on Minus	2.20/.80	1.55/.65
RPE	Return on Parity Even	2.20/.80	1.55/.65
RPO	Return on Parity Odd	2.20/.80	1.55/.65
PUSH B	Move B to (SP-1), C to (SP-2)	2.30	1.30
PUSH D	Move D to (SP-1), E to (SP-2)	2.30	1.30
PUSH H	Move H to (SP-1), L to (SP-2)	2.30	1.30
PUSH PSW	Move A to (SP-1), F to (SP-2)	2.30	1.30

INSTRUCTION	DESCRIPTION	EXECUTION TIME 650ns Memory (Microsec)	180ns Memory (Microsec)
POP B	Move (SP) to C, (SP+1) to B	2.10	1.35
POP D	Move (SP) to E, (SP+1) to D	2.10	1.35
POP H	Move (SP) to L, (SP+1) to H	2.10	1.35
POP PSW	Move (SP) to F, (SP+1) to A	2.10	1.35
CMA	Compliment A	.80	.65
STC	Set Carry	.80	.65
CMC	Compliment Carry	.80	.65
DAA	Decimal Adjust Accumulator	.80	.65
IN	Read Data from Device B2	2.00	1.50
OUT	Output Data to Device B2	2.20	1.70
RST	Restart	2.50	1.44
EI	Enable Interrupts	.80	.65
DI	Disable Interrupts	.80	.65
NOP	No Operation	.80	.65
HLT	Halt Processing	.80	.65

NOTE: Where two times are shown, such as 2.2/.8, the first time is for condition met, the second for condition not met.

OPERATOR CONTROL PANEL

The operator control panel is an integral part of the SYSTEM 80 and is accessible from the front of the system. The control panel contains indicators and switches which allow the operator complete control over the system. The indicators and switches perform the following:

Switches

SS/Cont	Allows single cycle of instructions
Run	Initiates automatic program cycling
Reset	Master resets CPU
Restart	Starts program at address selected by IPL switch
IPL (Rotary)	9 position rotary switch to select restart addresses.

Indicators

Databus In/Out	Two banks of 8 LED indicators each reflecting the contents of the memory Read Data Bus and the system extend I/O Bus.
Address Out	20 LED indicators reflecting the contents of the address bus.
Run	LED indicating "run" mode
Halt	LED indicating "halt" mode

REAL TIME CLOCK

The real time clock (RTC) is an integral part of the CPU. The purpose of the RTC is to interrupt the program on a regular basis to allow monitoring and control of real time activities. The interrupting frequency is 100HZ (once every 10 milliseconds). An enable/disable instruction is provided to allow program control over the clock.

SERIAL I/O PORT

The serial I/O port provides for a teletype, CRT or other serial asynchronous device and is standard with all SYSTEM 80's. Features of the serial port include:

RS232C or 20ma current loop interface for local devices.

Baud rate selection of 110, 300, 1200, 2400, 4800 or 9600 baud.

POWER FAILURE PROTECTION/AUTOMATIC RESTART

The SYSTEM 80 monitors power supply voltages and provides for an orderly shutdown of the system upon detecting a power failure. In the case where non-volatile core memories are used, data and programs are retained. When power is restored, the SYSTEM 80 automatically restarts at a predetermined location in memory for which a 256 byte ROM is supplied. The standard ROM returns the user to the bootstrap loader. Other restart options can be made available.

BOOTSTRAP LOADER ROM

A 256 byte EROM is provided as a standard feature of the SYSTEM 80. The EROM program functions are as follows:

1. Load binary tape from TTY
2. Load hex tape from TTY
3. Load one block from disk
4. Output any memory location within the first 64K bytes of memory to the TTY
5. Output the previous memory location to the TTY
6. Output the next memory location to the TTY
7. Write into the memory location within the first 64K bytes of memory

The EROM occupies memory locations FF00 through FFFF.

MEMORIES

Memory selection is the key to successful microcomputer applications. SYSTEM 80 offers the widest range of memories available in the market. All memories are pin compatible and can be inter-mixed to optimize solutions to specific requirements. This means the user can configure to his current needs and later change the combination to satisfy new requirements. Since the SYSTEM 80 can accommodate up to one full megabyte of memory, the user now has a system which can grow in performance and capacity with his application needs. The following table should make it easy to configure your system. All memories are on a single board and require only one memory slot in the SYSTEM 80. Since the SYSTEM 80 CPU is asychronous, instruction execution time is decreased with the use of faster memory without CPU adjustments.

Memory Type	Cycle Time	Modularity	Programmed Bytes/Sec	DMA Bytes/Sec
Non-volatile core	650ns	16K, 32K	90K	1.54M
Non-volatile core	850ns	64K	77K	1.33M
4K Static RAM	450ns	16K,32K,64K	100K	2.22M
1K Static RAM	180ns	16K, 32K	121K	5.55M
PROM	150ns	8K to 32K	125K	N/A

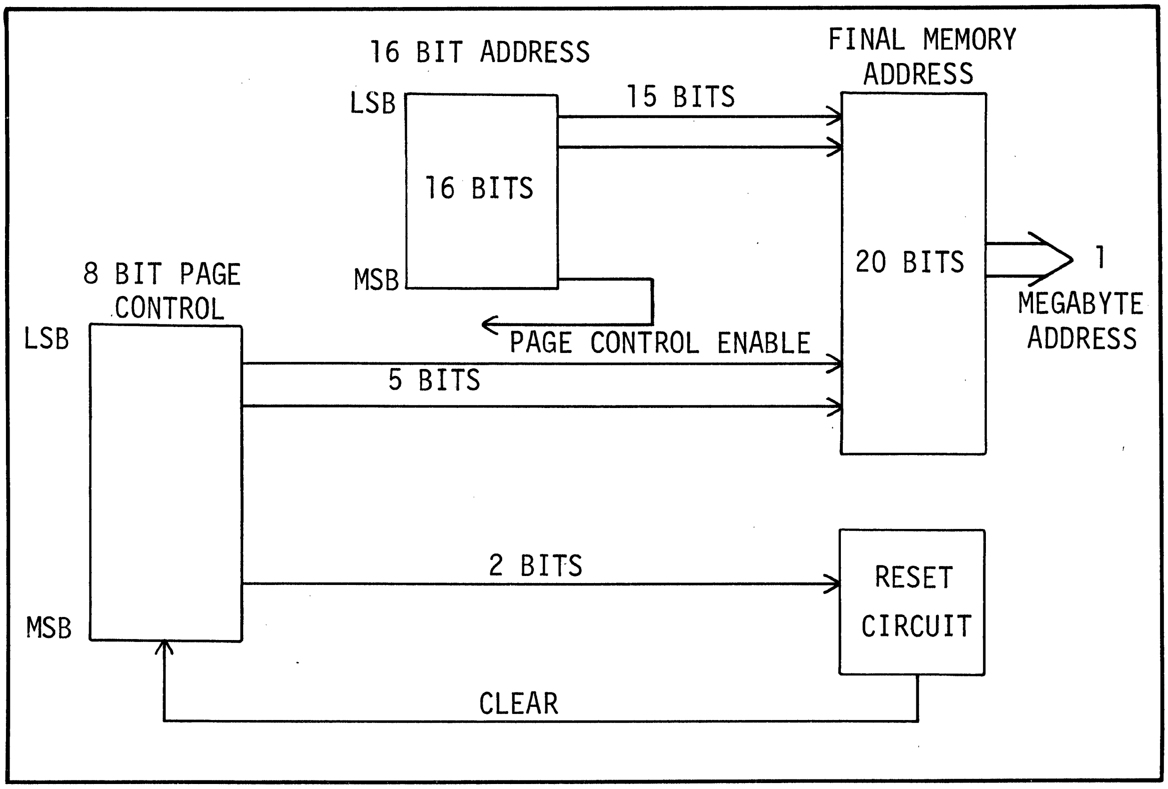
All memories use proven technology and are tested extensively to provide high levels of reliability. Since all memories are static, no throughput is lost due to refresh cycles. This can be a significant factor in both high speed and interrupt driven systems.

MEMORY EXPANSION CAPABILITY

One of the most powerful features of the SYSTEM 80 is its ability to address up to one megabyte of memory. This capability is normally found only in large computer systems. In order to reference memory of one megabyte, two different means to expand the address field to 20 bits can be provided.

Memory Address Extension

Memory address extension provides a simple, low overhead method of addressing one megabyte of memory. In this mode, physical memory is blocked into pages of 32K bytes. The assembler generates addresses up to one megabyte contiguously and then converts each address to a 32K byte relative address and a page relative address providing 32 pages of 32K bytes per page or one megabyte. This is done in the following manner:



The 2 bits used to control the reset circuit represent the number of memory cycles required to execute the statement whose address is higher than 32768_{10}. At the end of the execution, the page control register is cleared leaving control in the first 32K byte page which can be considered fixed. A program residing in the lower 32K bytes of memory can access data in all other pages. In the same manner, jumps can be executed.

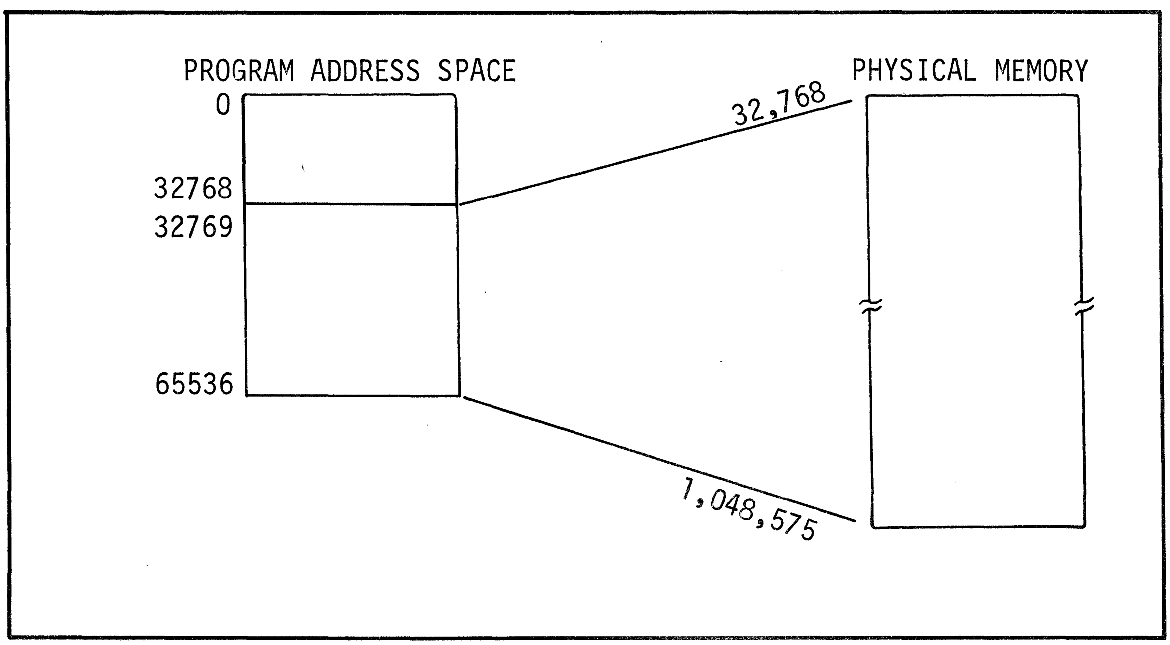
By way of an OUT command, the applications program can load the 8 bit page control register. If the 2 most significant bits are 00 the paging is unconditional and the 5 least significant bits of the register are concatenated to the 15 bit address in all cases. This, of course, can be changed via another OUT command. Thus, operands can be located anywhere within the physical memory. The page control hardware is arranged so that a buffer register is loaded by an OUT command as well as the page control register. If an out of page address is then generated, the system will set up the reset circuitry and reset the page control register. In this case however, rather than resetting the page control register to zero the page control register will be reloaded with the contents of the buffer register. Thus control will always remain in the present page even though references to out of page addresses are made.

This method of address extension, while simple in both concept and execution, provides significant power and flexibility to the user and, for many uses, represents an excellent balance of capability and low overhead.

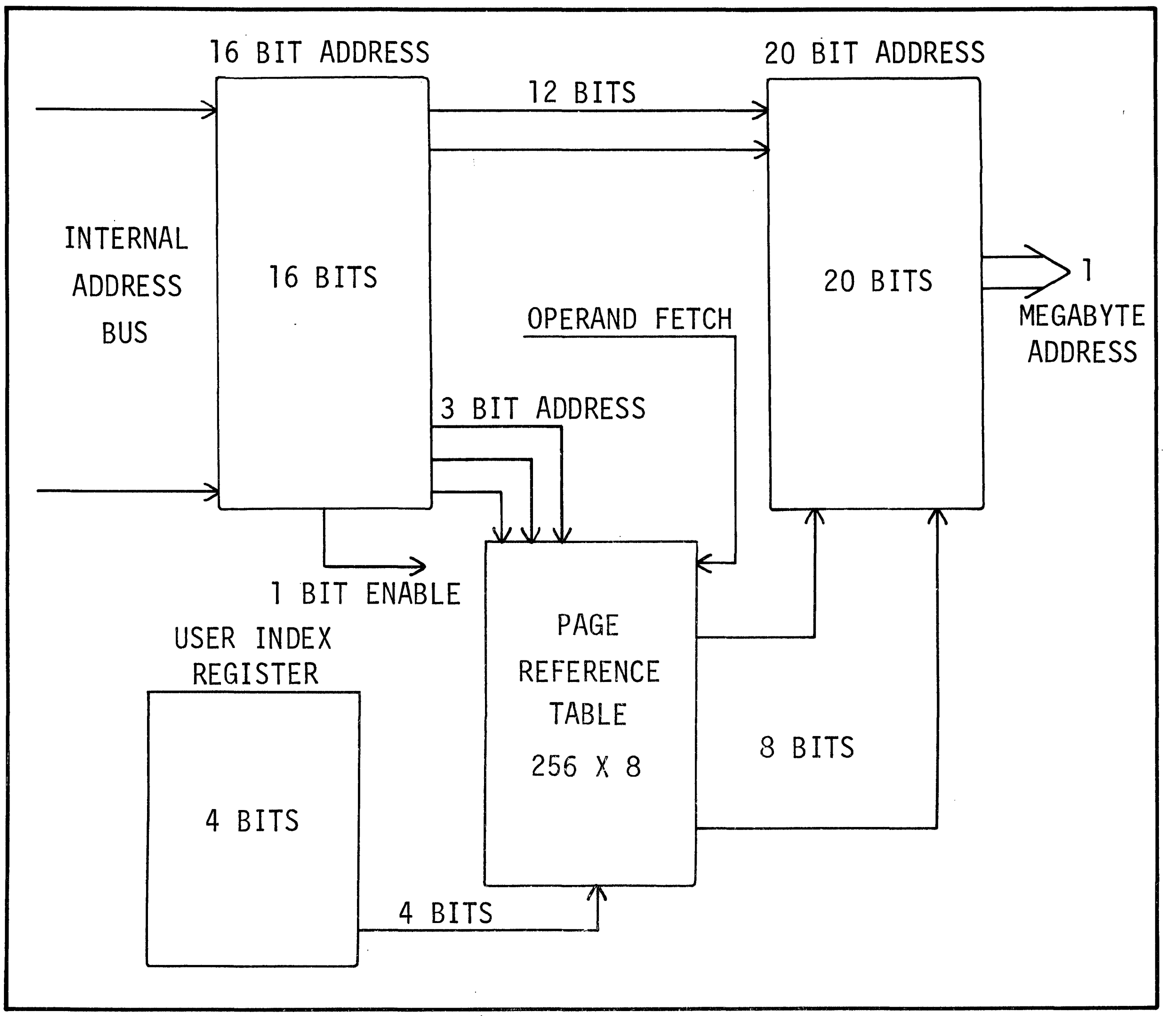
Memory Map

The memory map option amends the extended memory address by using a page reference table to map the physical memory into 4K byte pages. By use of the map, a user's memory need no longer be contiguous since all addresses are made up of 12 bits representing relative location within a 4K byte and 8 bits from the page reference table which represents the offset of the starting address of the page from the memory origin. However, program addresses in the 0 to 32K range are equated to corresponding physical addresses to provide a fixed page.

Program addresses in the 32K to 64K range are translated to physical memory addresses anywhere in the one megabyte range on a 4K block basis.



The translation mechanism is via a special high speed memory called a page reference table. Values stored in the page reference table by the program are used to arrive at the final physical address.



Using this feature, 4K byte pages can be positioned into arbitrary locations in physical memory and references to that page will be automatically mapped to the actual physical address via the page reference table.

The page reference table can best be considered a three dimensional array with 8 map locations per level and 32 levels for a total of 256 pages. Three bits from the 16 bit internal address bus resolve map locations within a level while 4 bits from the user index and OPERAND FETCH resolve 32 levels.

By loading the page reference table, a program can reach 3 32K byte sections of memory. These sections are the fixed 0-32K section, an unrestricted 32K user section and a 32K data only section. By loading a new value into the user index register, different 32K user sections and data sections can be accessed.

SOFTWARE AND PERIPHERAL DESCRIPTION
SYSTEM 80

SYSTEM 80 is offered with a wide range of software. Since the SYSTEM 80 instruction set is compatible with the 8080, the power of the SYSTEM 80's software enhances previously generated programs and training.

Software for the SYSTEM 80 includes a monitor, a debug package, a relocatable assembler and linking loader and a disk executive (DEX) which includes an I/O executive (IOX).

Relocatable Assembler

The assembler generates relocatable object code and provides for generation of addresses up to one megabyte. This software capability, together with the extended memory addressing hardware, makes it easy to effectively utilize large memory capacities.

Linking Loader

The linking loader provides for loading main programs as well as loading and linking subprograms. As a program is loaded, the loader identifies external references and requests that they be satisfied. The loader relocates object code during load to any arbitrary starting location and generates a map at completion. The loader fully supports one megabyte of memory.

Editor

The editor provides for input and maintenance of source code up to the full one megabyte memory limit of SYSTEM 80. The editor provides the capability to read and punch source tapes and to add, delete and change code. In addition, the editor can execute searches for a given string and can substitute a new string or locate a workspace pointer.

Disk Executive System

The disk executive system (S/80-DEX) supports up to 40 megabytes of disk storage and provides for operator control via the system console. Control is in the form of short commands which allow the operator to load and execute system and user programs, assemble or edit disk files, debug programs and save programs on the disk. In addition, S/80-DEX supports program overlays from the disk. The I/O sub-system (S/80-IOX) provides for both character and record oriented I/O services for the S/80-DEX and the user on a named file basis. Files may be either ASCII (data, source, BNPF, HEX) or binary (ABS, PGM, data).

Disk Controller

SYSTEM 80 is offered with a disk controller which supports the following disk drives:

Manufacturer	Model	Capacity
Caelus	203-1	2.5 Megabytes
Caelus	203-2	5.0 Megabytes
Pertec	3341	5 Megabytes
Pertec	3441	10 Megabytes
Diablo	31	2.5 Megabytes
Diablo	33	5 Megabytes

The disk controller, in conjunction with the S/80-DEX provides a powerful program generation tool. Four drives can be daisy chained together for a total cppacity of 40 megabytes. The disk controller transfers data, via DMA, at a rate of 200 Kbytes per second.

THE DATA CONTAINED HEREIN IS PRELIMINARY IN NATURE AND THEREFORE IS SUBJECT TO CHANGE WITHOUT NOTICE. FOR FURTHER INFORMATION PLEASE CONTACT:

NORMAN G. COMPTON		RICHARD S. BROWN
MICROCOMPUTER SALES MANAGER	OR	MICROCOMPUTER PRODUCT MANAGER
(213) 644-9881 Extension 1080		(213) 644-9881 Extension 1387

DATE OF ISSUE, MAY, 1976

ELECTRONIC MEMORIES & MAGNETICS CORPORATION

12621 Chadron Avenue, Hawthorne, California 90250 / Telephone: (213) 644-9881