

**digital**

**DUII**

**Engineering Drawings**

**Digital Equipment Corporation**

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# **CUSTOMER PRINT SET INDEX**

SEQUENCE

SINGLE LINE PGM SYNCH INT  
DULL-DA, EA FIELD INSTALLATION  
AND ACCEPTANCE PROCEDURE  
ACCESSORY LIST  
PGM SYNC INTERFACE  
CABLE MODEM BC05C  
MODEM TEST CONNECTOR  
TTL TO BELL SYSTEM 301 & 303  
HIGH SPEED MODEM CABLE  
CABLE INTERFACE BD. X 1

— 1 —

N B-DD-DU11-Ø  
A-SP-DU11-Ø-4  
  
A-AL-DU11-Ø-3  
D-CS-~~M~~822-Ø-1  
D-UA-BCØ5C-Ø-Ø  
D-CS-H315-Ø-1  
D-CS-M595-Ø-1  
D-UA-BCØIW-Ø-Ø  
D-CS-M970-Ø-1

**SEQUENCE**

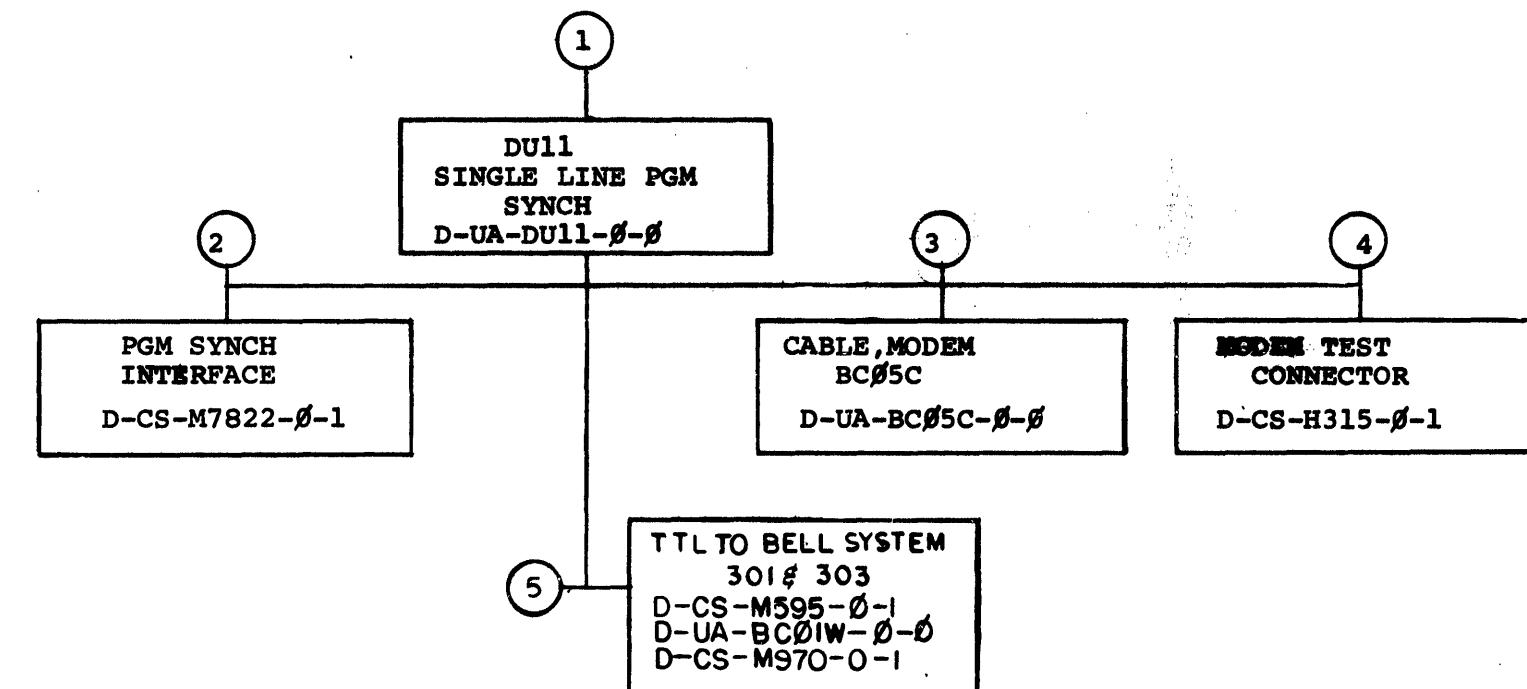
**MFG. PRINT SET  
ACCEPTANCE PROCEDURE  
TEST PROCEDURE**

A-SP-DU11-0-1  
A-SP-DU11-0-2

# THIS IS PRINT SET 1

— 1 —

				USED ON OPTION/MODEL				DRN. K. DAVIS		DATE 9-14-3		TITLE SINGLE LINE PGM SYNCH.INT.			
				DULL				CHK'D. <i>M. L. S.</i>		DATE 10/16/73					
								PROJ. ENG. <i>S. Berezka</i>		DATE 10/29/73					
								PROD. <i>R. Wall</i>		DATE 10/29/73		SIZE B			
								FIELD REV. <i>J. Harg</i>		DATE 10/26/73		CODE DD			
												NUMBER DULL-0		REV D	
												DIST			
REVISIONS		DATE	CHG. NO.	REV											
		5/74	DULL-00001	A											
		8/74	DULL-00002	B											
		10/74	DULL-00003	C											
		7/75	DULL-00004	D											
SHEET 1 OF 3															



TITLE	SHEET 2 OF 3	SIZE CODE	NUMBER	REV
SINGLE LINE PGM SYNCH. INT.	B DD		DU11-Ø	D

ELECTRICAL							MECHANICAL																			
CUSTOMER PRINT SET		MFG. SET		DRAWING NO.			REV	NO OF SHT	DESCRIPTION		OPTION NO./FILE DATE		CUSTOMER PRINT SET		MFG. SET		DRAWING NO.			REV	NO OF SHT	DESCRIPTION		OPTION NO./FILE DATE		
		FIND NO.																								
X		1	D-UA-DULL-Ø-Ø	*	1	SINGLE LINE PGM SYNCH. INT.											1	D-UA-DULL-Ø-Ø	*	1	SINGLE LINE PGM SYNCH INT					
X		X	A-SP-DULL-Ø-1	A	4	ACCEPTANCE PROCEDURE																				
X		X	A-SP-DULL-Ø-2	D	12	TEST PROCEDURE																				
X			A-AL-DULL-Ø-3	A	1	ACCESSORY LIST																				
X			A-SP-DULL-Ø-4	C	9	FIELD INSTALLATION AND ACC.																				
X		2	D-CS-M7822-Ø-1	#	6	PGM SYNC INTERFACE																				
			K-CO-M7822-Ø-4		1	X-Y COORDINATE HOLE LOCATION																				
			D-AH-M7822-Ø-5		1	ASSY/DRILLING HOLE LOCATION																				
			B-MH-M7822-Ø-6		1	MODULE ECO HISTORY																				
X		3	D-UA-BCØ5C-Ø-Ø	#	1	CABLE MODEM BCØ5C											3	D-UA-BCØ5C-Ø-Ø	*	1	CABLE, MODEM BCØ5C					
X		4	D-CS-H315-Ø-1	#	1	MODEM TEST CONNECTOR																				
			K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOCATION																				
			C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT																				
			B-MH-H315-Ø-6		1	MODULE ECO HISTORY																				
X		5	D-CS-M595-Ø-1	#	2	TTL TO BELL SYSTEM 301 & 303																				
X			D-UA-BCØIW-Ø-0	#	1	HIGH SPEED MODEM CABLE																				
X			D-CS-M970-Ø-1	#	1	CABLE INTERFACE BD,*!																				
CUSTOMER PRINT SET CODES		X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED										TITLE		SIZE CODE		NUMBER		REV								
												SINGLE LINE PGM SYNCH		SHEET 3 OF 3		B DD		DULL-Ø		D						

DIGITAL EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE

DULL-DA, EA Field Installation and Acceptance Procedure

This document is divided into two sections; the first section deals with the field installation of a DULL-DA or EA, the second section covers the customer acceptance of the option.

The installation section covers the configuration of jumpers and switches on the module itself. It also has helpful hints that could save aggravation. All references to modems are to the Bell 201 series for the DULL-DA, and to the Bell 303 for the DULL-EA. No attempt has been made to cover other modems, although many have the same characteristics as those cited.

Throughout this document the term DULL, without a suffix, refers to both the DA and EA version. Where information pertains specifically to one version only the appropriate suffix will be added.

Field Installation

1.0 Module Configuration

The DULL module M7822 is configured for the customer's system by cutting jumpers on the module and by setting the switch pack. In most cases only the Unibus address and interrupt vector address need to be reconfigured although all jumpers will be defined.

1.1.0 Unibus Address

The DULL Unibus address falls into the floating address space. The first DULL floating address is 16000. This would be the address of the first DULL in a system if the system consisted of no other devices that preceded the DULL in the floating address scheme. In this floating address scheme the DULL uses four address spaces starting on a zero boundary and is preceded by the DQ11 (i.e., 160040-50). Once the position of the DULL has been determined in the floating address scheme, the Unibus address is selected by the rocker switches on the M7822.

1.1.1 Setting the Unibus Address

Switch pack (SP1) controls the Unibus address of the DULL. Once the Unibus address has been determined, set the rocker switches as follows: For a logical (1) on the Unibus address line, set the rocker switch that corresponds to that particular bit to the OFF position. A switch is in the OFF position when the rocker is depressed on the OFF side of the switch.

SIZE	CODE	NUMBER	REV
A	SP	DULL-0-4	C

DEC FORM NO DEC 16-(381)-1022-N370

SHEET 2 OF 9

DRA 108

ENGINEERING SPECIFICATION					
TITLE DULL-DA, EA FIELD INSTALLATION AND ACCEPTANCE PROCEDURE					
REVISIONS					
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY
A	ECO CHANGE	DULL-00001	REILLY	4/74	J.R. Reilly
B	ECO CHANGE	DULL-00002	ZERESKI	8/74	J.Zereski
C	ECO CHANGE	DULL-00004	ZERESKI	7-75	J.Zereski

Index

- 1.0 Module Configuration
  - 1.1.0 Unibus Address
  - 1.2.0 Interrupt Vector Address
  - 1.3.0 Miscellaneous Jumpers
  - 1.4.0 Mounting Information
  - 1.5.0 Power Requirement and Unibus Loading
  - 1.6.0 Environmental Specifications
  - 1.7.0 Preliminary Testing
  - 1.8.0 Testing with Diagnostics
  - 1.9.0 Systems Test
- 2.0 Customer Acceptance

ENG	J.Zereski	APPD	J.Zereski	SIZE	CODE	NUMBER	REV
DEC 16-(382)-1022-N971				A	SP	DULL-0-4	C

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SHEET 1 OF 9

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE

Example:

To select an address of 160010 switches 1 through 9 would be in the ON position, switch 0 would be OFF. Note that the number of switch does not correspond to the bit position on the Unibus, i.e., SW0 doesn't sample BUS A0.

1.2.0 Interrupt Vector Address

The DULL Vectors also fall into the floating interrupt vector space. The first vector of the floating scheme is address 300. This would be the vector of the first DULL in a system that consisted of devices which did not precede the DULL in the floating vector scheme. In this floating vector scheme the W11-W precedes the DULL. Each DULL in a system occupies two interrupt vectors.

1.2.1 Setting the Interrupt Vector

The vector is determined by the position of jumpers W9 through W14. During an interrupt sequence a BUS D line will be asserted as a logical (1) if a jumper is in place. As cited earlier the DULL occupies two vectors. Only the first vector need be considered and it must start on a zero boundary. The second vector is simply controlled by W9-W14 and BUS D #2 which is controlled by the hardware.

Example:

To select a set of vectors, 300 and 304, cut jumpers W9-W11 and W14. Jumpers W13 and W12 remain in.

1.3.0 Miscellaneous Jumpers--Modify only at customer's request with the exception of W15, W16 & W14-W9.

Drawing #	Jumper #	Function
5	W2	This jumper is normally OUT. If this jumper is in, the receiver logic will synchronize on one sync character instead of the recommended two.
6	W4	This jumper is normally IN. If this jumper is left out, Bits 1-3 of the RXCSR won't be cleared by Master Reset or BUSINIT. In some cases the connection with the Data Set may be required to be excluded from the effects of Master Reset or Bus Init.
4	W14	Sets Vector Bit 8 when installed
	W13	Sets Vector Bit 7 when installed
	W12	Sets Vector Bit 6 when installed
	W11	Sets Vector Bit 5 when installed
	W10	Sets Vector Bit 4 when installed
	W9	Sets Vector Bit 3 when installed

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ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE

1.3.0

Drawing # Jumper #

Function

6	W5	This jumper is normally IN. If this jumper is cut pin 11 of the Berg header (normally SEC REC or unused) will be disconnected from the EIA receiver. In other than the specified modems this pin may be connected to something other than SEC REC in which case it may be necessary to remove the jumper.
6	W6	This jumper is normally IN. If this jumper is cut, pin 11 of the Berg header will be disconnected from the EIA driver. This pin is normally connected to the SEC XMIT or an unused lead of the modem. In modems other than these specified, it may be necessary to remove this jumper.
4	W15	This jumper is normally IN. W15 should only be removed if the processor being used is a KAll without a KAll option. For all other processors, this jumper is in.
8	W16	This jumper is normally OUT. Only in systems where the voltage on pin A11 is at 8V RMS should this jumper be installed. A G855 filter should also be installed in this case. Refer to the installation section of the DULL maintenance manual.

Note: If any of the miscellaneous jumpers have been changed with the exception of W15 and W16, new parameters must be entered into the diagnostic program through its keyboard monitor.

1.4.0 Mounting Information

1.4.1 DULL-DA

The DULL-DA is compatible with all small peripheral controller slots (SPC) to date, with the exception of those internal to the KAll.

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## ENGINEERING SPECIFICATION

## CONTINUATION SHEET

## TITLE

Consideration must be given to the routing of the BC05-C cable or cables. If more than one DULL-DA is mounted in a system unit it would be desirable to have the system unit mounted as close as possible to the port in the cab provided for the cables.

Refer to drawing D-UA-DULL-#-# for the position of the module in a system unit.

## 1.4.2 DULL-EA

The DULL-EA is compatible only with the DD11-B unit. This system unit must have the appropriate ECO installed for correct operation. Slots 2 or 3 are the only slots which the DULL-EA can use in the DD11-B. To install a DULL-EA into a DD11-B refer to Drawing D-UA-DULL-#-# for the position of the modules. INSURE THAT DD11-B ECO #3 IS INSTALLED IN THE DD11-B. Extreme care should be used in the routing of the BC01-W modem cable. INSTALL JUMPERS 202 AND 301 IN M970 ALL OTHER JUMPERS OUT.

## 1.5.0 Power requirements and Unibus loading.

1.5.1 Each DULL places one bus load on the Unibus as defined by the peripherals and interfacing handbook, i.e., one BUS Receiver and 2 BUS Drivers per line.

## 1.5.2 DULL-DA power requirements

+5V @ 1.8 amps  
+15V @ .04 amps  
-15V @ .07 amps

## 1.5.3 DULL-EA power requirements

+5V @ 2.1 amps  
+15V @ .07 amps  
-15V @ .2 amps

## 1.6.0 Environmental Specifications

+10°C to +50°C with a relative humidity of from 20% to 95% (without condensation).

## 1.7.0 Preliminary Testing

## 1.7.1 Voltage Checks

With the DULL plugged into the back panel check the voltages at the following points. A 453 scope should suffice if it's calibrated.

	SIZE	CODE	NUMBER	REV
	A	SP	DULL-#-4	C

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## ENGINEERING SPECIFICATION

## CONTINUATION SHEET

## TITLE

IC & Pin	Voltage	Function
E16 # 1	+5V, +or -250 MV	TTL & MOS supply
E16 16	-12V, +or -600 MV	MOS & EIA level converter supply
*E12 14	+12V, +or -1V	EIA level converter supply

\*Note: If W16 is in place, the voltage on E12 14 will be +8V, +1V or -500 MV.

## 1.7.2 Verification of address recognition logic

With the following test loop the correct operation of the address decoding logic can be verified.

STR: MOV # SWR, R#  
ADD #, (R#); executes the DATI, DATO  
JMP # STR; on the DULL adrs logic

STR: 200	13700
	177570
	62710
	000000
	137
	200

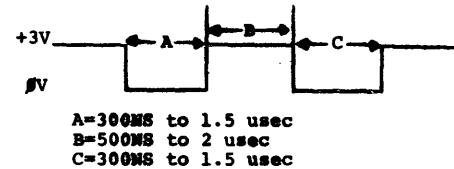
With this loop toggled in at address 200.

A. Load address 200.

B. Place the first register address of the DULL into the console SWR.

C. Press the start key.

D. With a scope monitor point E69#6 on the M7822, the following waveform should be observed. Note that the timing given may not be exactly accurate because of differences in systems.



	SIZE	CODE	NUMBER	REV
	A	SP	DULL-#-4	C

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## ENGINEERING SPECIFICATION

## CONTINUATION SHEET

## TITLE

## 1.7.3 Verification of the Unibus, Bus D line drivers

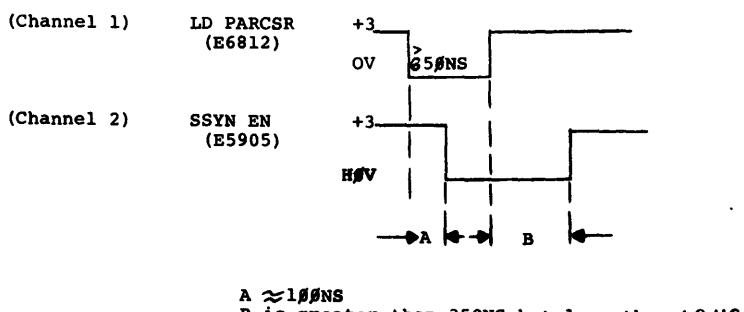
- A. Press Halt
- B. Press Start to issue CLR in the DULL
- C. Examine the last DULL register, TXDBUF, (Sel. 6) The contents should read back as all ones. This proves that all DULL unibus D line drivers turn on.

## 1.7.4 Verification of Slave Sync inhibit delay

With same loop used in 1.7.2 load the PARCSR address (Sel. 2) into the console SWR.

- A. Start the program. With the first scope probe verify the LD PARCSR one shot at E6812. This output should be low for at least 65#NS (Refer Fig. A).
- B. Sync on channel one of the scope, with the second probe verify that BUS SSYN is being inhibited for at least 35#NS after the rising edge of the LD PARCSR pulse. (Refer Fig. A)

Figure A



	SIZE	CODE	NUMBER	REV
	A	SP	DULL-#-4	C

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DRA 108

## ENGINEERING SPECIFICATION

## CONTINUATION SHEET

## TITLE

IC & Pin	Voltage	Function
E16 # 1	+5V, +or -250 MV	TTL & MOS supply
E16 16	-12V, +or -600 MV	MOS & EIA level converter supply
*E12 14	+12V, +or -1V	EIA level converter supply

\*Note: If W16 is in place, the voltage on E12 14 will be +8V, +1V or -500 MV.

## 1.7.2 Verification of address recognition logic

With the following test loop the correct operation of the address decoding logic can be verified.

STR: MOV # SWR, R#  
ADD #, (R#); executes the DATI, DATO  
JMP # STR; on the DULL adrs logic

STR: 200	13700
	177570
	62710
	000000
	137
	200

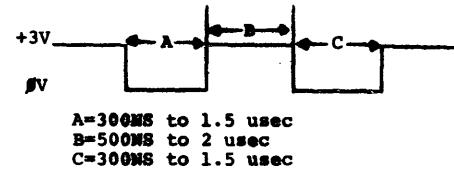
With this loop toggled in at address 200.

A. Load address 200.

B. Place the first register address of the DULL into the console SWR.

C. Press the start key.

D. With a scope monitor point E69#6 on the M7822, the following waveform should be observed. Note that the timing given may not be exactly accurate because of differences in systems.



	SIZE	CODE	NUMBER	REV
	A	SP	DULL-#-4	C

SHEET 8 OF 9

## ENGINEERING SPECIFICATION

## CONTINUATION SHEET

## TITLE

Repeat this same procedure for the LD TEST# one shot, Fig. A and the timing information given is the same with the exception of the signal names and pin designations.

- A. Load Address 200
- B. Place the TXDBUF address into the SWR (Sel.6).
- C. Place channel/scope probe on E68#4.
- D. Place Channel 2 scope probe on E59#5.
- E. Press Start and verify the timing as per Figure A.

## 1.7.5 Verification of Master Reset

Load diagnostic DEDU-AA, refer to the operating instructions of the diagnostic and select and loop on Test #8. Verify the output of the TEST# one shot (E6413). This output should be true for 6 USEC. While this output is true, SSYN EN (E59#5) should be false.

## 1.8.5 Testing with diagnostics.

## 1.8.1 DULL-DA

With the BC#5-C cable connected to the M7822 module and the opposite end of the cable terminated by the H315 test connector, start testing with DEDU-AA. All diagnostics from DEDU-AA to DEDU-FA should run in the external mode. At least 3 passes of each diagnostic should be made. This concludes DULL-DA testing, remove the H315 connector and plug the BC#5-C into the modem.

## 1.8.2 DULL-EA

Starting with DEDU-AA through DEDU-FA, run all diagnostics with the diagnostic running in the internal maintenance mode. At least 3 passes of each diagnostic should be made. Connect the Berg connector of the BC#1-W into the M97# module. If the modem is not a Bell 3#3 or 3#1, special cables might be required to connect to the modem. This must be done through the local office and is not part of the DULL-EA installation.

If the modem in question is something other than those cited, installation testing is concluded here.

With the cited modems, plug the Burndry connector of the BC#1-W into the SYNC connector of the data set. This concludes DULL-EA testing.

	SIZE	CODE	NUMBER	REV
	A	SP	DULL-#-4	C

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# ENGINEERING SPECIFICATION

CONTINUATION SHEET

## TITLE

### 1.9.0 Systems Test

1.9.1 Using the DECX11 DULL module DUA\_, run all DULL's on the system. Up to 8 DULL's may be exercised on a system. At least 3 passes of each DULL should be made.

### 2.0 Customer Acceptance

#### 2.1.0 DULL-DA

Customer acceptance is based on the satisfactory conclusion of Steps 1.8.1 and 1.9.1.

#### 2.1.1 DULL-EA

Customer acceptance is based on the satisfactory conclusion of Steps 1.8.2 and 1.9.1.

	SIZE A	CODE SP	NUMBER DULL-Ø-4	REV C

**DIGITAL EQUIPMENT CORPORATION**  
**MAYNARD, MASSACHUSETTS**

## ACCESSORY LIST

MADE BY K.DAVIS  
DATE 10/26/73

ENG<sup>th</sup> a Zerodki

ENG A Bresacki PROD R Wolff ISSUED S

DATE 10/29/23

**ANSWER** **1** **ANSWER** **2**

**ITEM** DWG NO. & PART

CHECKED K. GLEEZE SECTION

DATE 10/26/73

PROD R 4988 ISSUED S

**DATE** 10/29/73

10. The following table shows the number of hours worked by 1000 workers in a certain industry.

## LEGEND

D	DOCUMENT
DN	DOCUMENT CHANGE NOTICE
PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE READ-IN-MODE

## **QUANTITY / VARIATION**

8

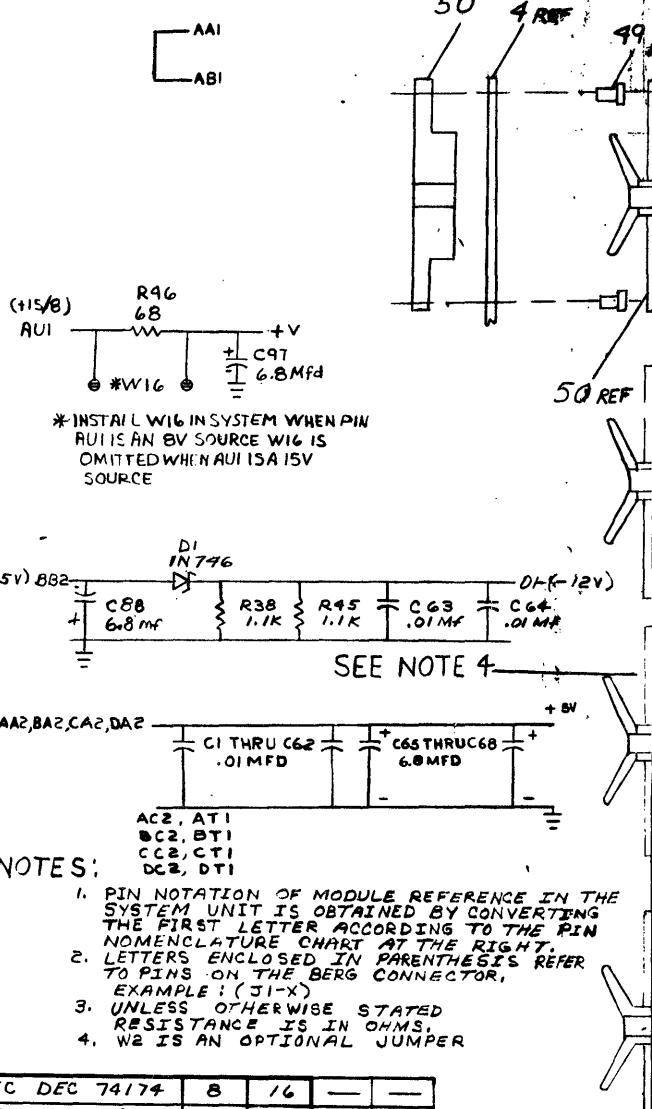
7

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ITEM REF. DES.	DESCRIPTION	PART NO.	ITEM NO.	ITEM REF DESIGNATION
1 CAP 330 PF 100V 5%	TUBING	9107278-11	66	1 R47
1 C58	CAP 330 PF 100V 5%	1000023	67	2 R28, R45
1 C92	CAP 1200 PF 100V 5%	1002424	68	1 R46
1 WIRE, #30 AWG	WIRE, #30 AWG	9107540-55	69	1 R14
1 C54	CAP 220PF 100V 5%	1000021	70	1 R52
1 LEFT LATCH	LEFT LATCH	1209941-03	71	4 D2, D3, D4, D5
1 RIGHT LATCH	RIGHT LATCH	1209941-04	72	1
1,2,3,4				2
16				NR W16
72				4
1				1
1 C100 C87				5
4 REF				6
99				7
4 PLACES				8
10				9

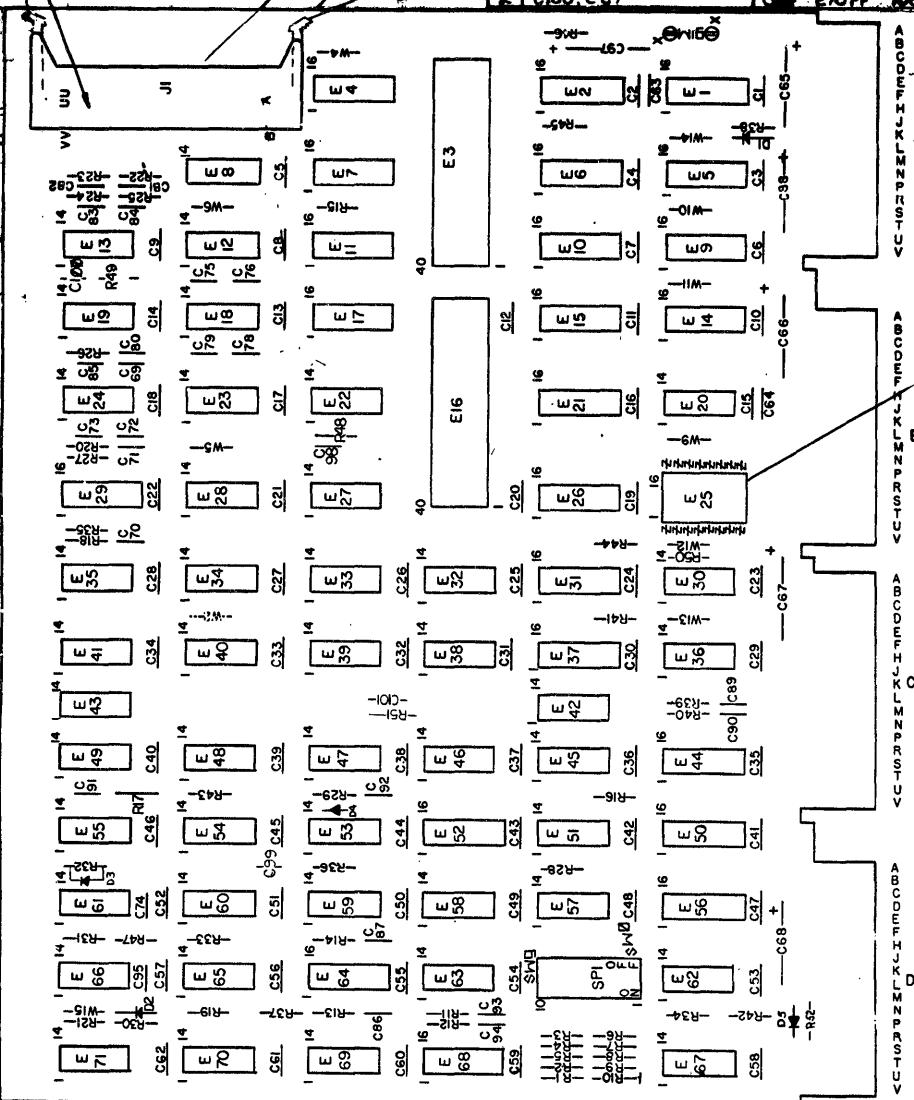


TESTS: DC2, CT1  
DC2, DT1

1. PIN NOTATION OF MODULE REFERENCE IN THE SYSTEM UNIT IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE RIGHT.
2. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR.  
EXAMPLE: (J1-X)
3. UNLESS OTHERWISE STATED RESISTANCE IS IN OHMS.
4. W2 IS AN OPTIONAL JUMPER

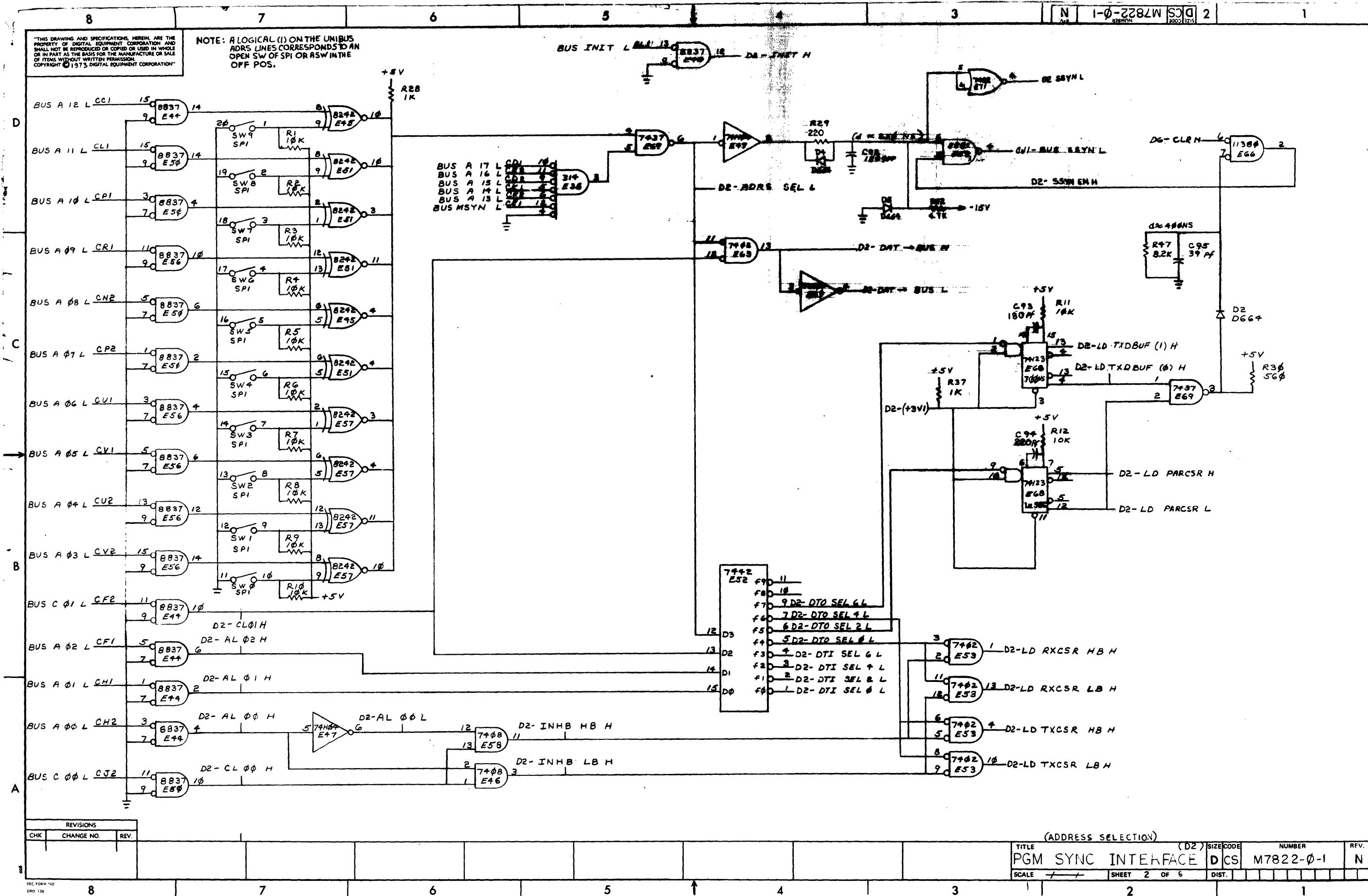
IC DEC 74174	8	16	—	—
IC DEC 8838	8	16	—	—
SAR PR1472B	20	1	—	16
SAT PT1482E	21	1	—	16
IC DEC 1488	7	—	14	1
IC DEC 8837	8	16	—	—
IC DEC 74153	8	16	—	—
IC DEC 11380	1	8	—	—
IC DEC 74175	8	16	—	—
IC DEC 74123	8	16	—	—
IC DEC 7442	8	16	—	—
IC DEC 314	1	8	—	—
IC TYPE	GND	+5V	+V	-12V

IC DEC 314	1
IC TYPE	GND +
GND AND 5V ARE USUALLY PIN 7 AND 1. RESPECTIVELY EXCEPTIONS ARE STATED AS	

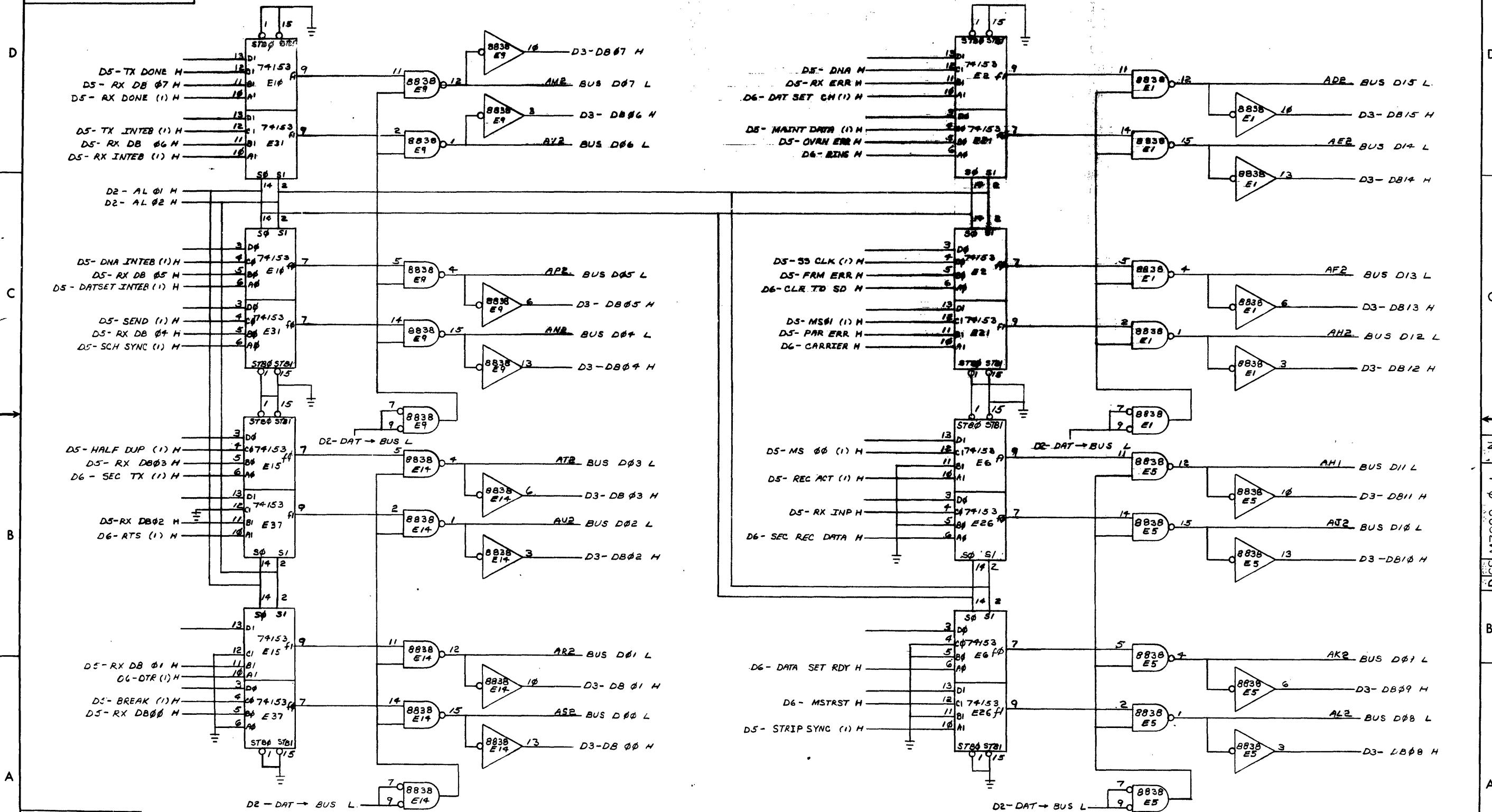


ION	PART NO.	ITEM NO.	REF	X-Y COORDINATE HOLE LOCATION	K-CO-M7822-0-4	
5%	1303179	55	REF	ASST/DRILLING HOLE LAYOUT	D-AH-M7822-0-5	
5%	1304475	56	REF	MURATA ECO HISTORY	B-MH-M7822-0-6	
4W5%	1300219	57	1	ETCHED CIRCUIT BOARD	5010535	
5%	1902394	58	1	C93	CAP 1.80 PF 100V 5%	
5%	1300447	59	3	C70, C71, C86	CAP 100 PF 100V 5%	
1100114	60	2	C79,C90	CAP 120 PF 100V 5%		
1211287-06	61	1	C95	CAP 3.7PF 100V 5%		
1006735	62	1	C101	CAP 600 PF 100V 5%		
9107560-01	63	9	C88,C72,C73,C75,C76,C78-C80,C91	CAP 470 PF 100V 5%		
210244	64	94	C1-C84, C81-C85	CAP .01 UF 100V 20%		
1008778	65	6	C88-C90,C92	CAP 6.8 UF 35V 10%		
1000028	66	1	C94	CAP 22 UF 35V 10%		
PINTOMETER ARKNE		1	DI1	DIODE INFRARED	1104860	
MODULE	SYSTEM UNIT	1	S25	I.C. SOCKET	1209838	
		1	A1	SOHN (BORG HEADER)	1209941	
A	C	1	SPI	SWITCH DIP	1211164-06	
		10	R22,R24,32,R34,R45,R49,R61	RES 100 OHM 1/4W 5%	1300229	
B	D	2	R34,R29	RES 220 OHM 1/4W 5%	1300271	
		1	R35	RES 360 OHM 1/4W 5%	1300309	
C	E	7	R27,R30,R35,R37,R42,R43,R44	RES 1K 1/4W 5%	1300365	
		21	R1-R3,R24,R35,R36,R37,R38,R20,R21	RES 10K 1/4W 5%	1300479	
D	F	8	R51, R50	RES 100 1/4W 5%	1301322	
		1	R80	RES 800 1/4W 5%	1301890	
E	G	5	E32,E36,E38,E46,E8	I.C. DEC 7400	1905575	
		1	E43	I.C. DEC 7410	1905576	
F	H	4	E40,E53,E63,E71	I.C. DEC 7402	1909004	
		7	E29,E37,E53,E71,E55,E24,E67	I.C. DEC 7404	1909667	
G	I	4	E38	I.C. DEC 7474-H52	1909061	
		1	E26	I.C. DEC 314	1909704	
H	J	4	E20,E34,E39,E62	I.C. DEC 8001	1909705	
		4	E13,E45,E51,E57	I.C. DEC 8242	1909712	
I	K	3	E61, E107-E47	I.C. DEC 7404	1909931	
		8	E2,E5, E5, E15,E21,E22, E31, E37	I.C. DEC 74153	1909937	
J	L	1	E52	I.C. DEC 7442	1910046	
		1	E57	I.C. DEC 7437	1910091	
K	M	7	E29,E27,E59,E58,E60,E42,E46	I.C. DEC 7408	1910155	
		2	E12,E70	I.C. DEC 1400	1910322	
L	N	2	E18,E24	I.C. DEC 1400	1910323	
		3	E29,E64,E68	I.C. DEC 74123	1910436	
M	O	3	E4,E7,E11	I.C. DEC 74175	1910851	
		1	E17	I.C. DEC 74174	1910852	
N	P	1	E23	I.C. DEC 7427	1910878	
		3	E44,E50,E56	I.C. DEC 8002	1911116	
O	Q	4	E1,E5,E9,E14	I.C. DEC 8038	1911117	
		1	E66	I.C. DEC 11800	1911113	
P	R	1	E3	SAT PT 14828	2111557	
		1	E16	SAR PR 14728	2111556	
Q	S	8		EYELET (GS-7 STIMPSON)	9008732	
		4		HANDLE (MAGENTA)	9008337-06	
R	T	10	W9,W5,W6,W9-W15	INSULATED JUMPER	9009185	
		1	C89	CAP 1000A 100V 5%	1000022	
S	U	1	R19	RES 7.5K 1/4W	1301422	
		1	E49	IC DEC 7474	1905547	
QTY		REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.	
NUMBER						
SIZE CODE						
REV						

FIRST USED ON OPTION MODEL		REF DESIGNATION		DESCRIPTION		PART NO.	
DUII		ETCH BOARD REV E		PARTS LIST			
M7822-00001 C		DRN. <i>swilson</i>	DATE 6/19/93	digital		EQUIPMENT CORPORATION	
ORIGINATOR D	B	CMD. <i>swilson</i>	DATE 6/19/93			MAYNARD, MASSACHUSETTS	
CHANGE NO. REV		DATA <i>swilson</i>	DATE 6/19/93			TITLE	
REVISIONS						PGM SYNC	
D662 INL45						INTERFACE	
IN746A NA							
D664 IN3606							
DEC NO.		EIA NO.	DEC NO.	EIA NO.	NEXT HIGHER ASSY		
					B-DD-DUII-0.		
					SCALE NONE		
					SHEET 1 OF 6		
					DIST.		
SEMICONDUCTOR CONVERSION CHART							



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(BUS MULTIPLEXORS, RECEIVERS AND DRIVERS)

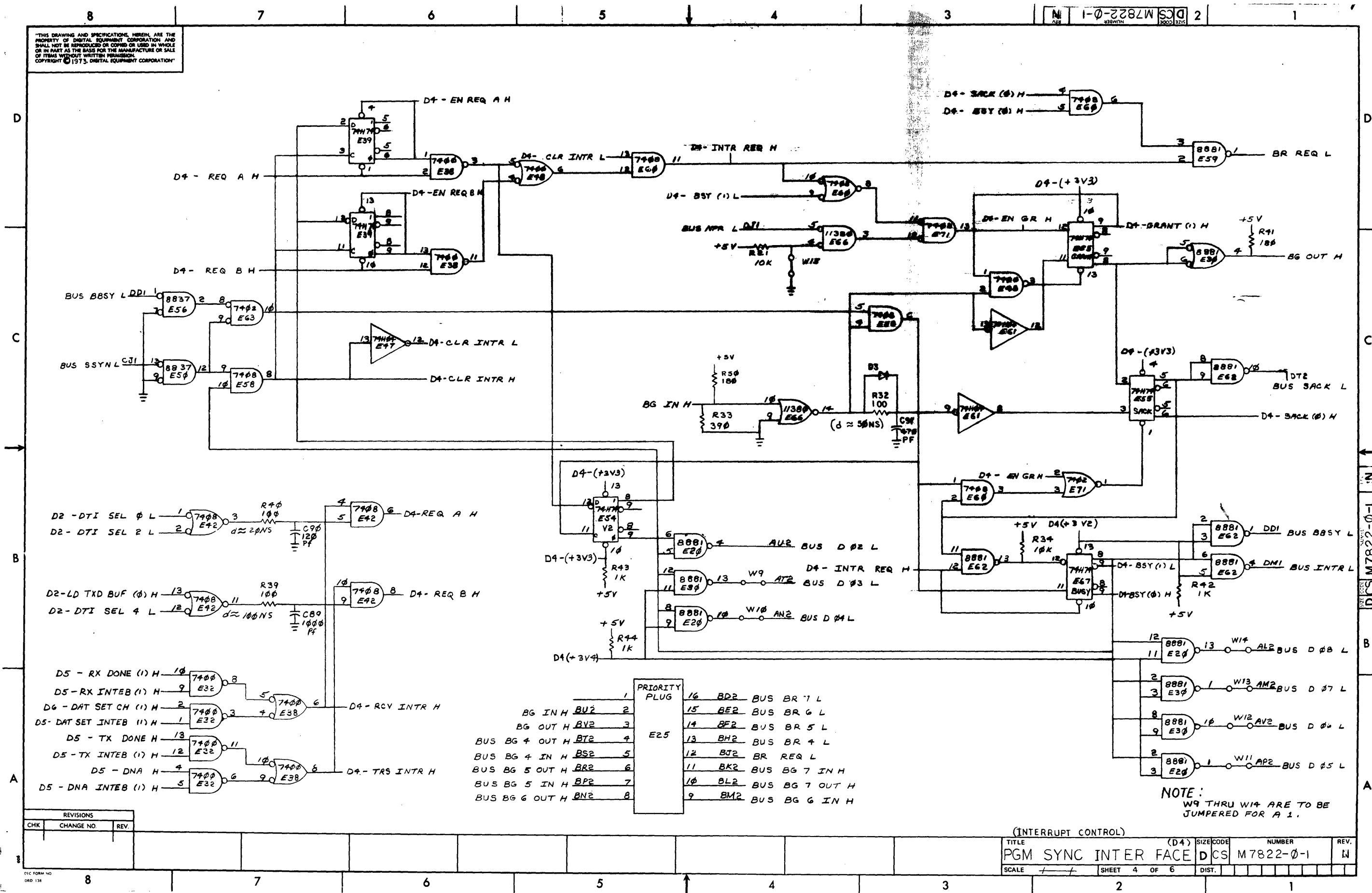
REVISIONS		TITLE		SIZE	CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.		(D3)			N

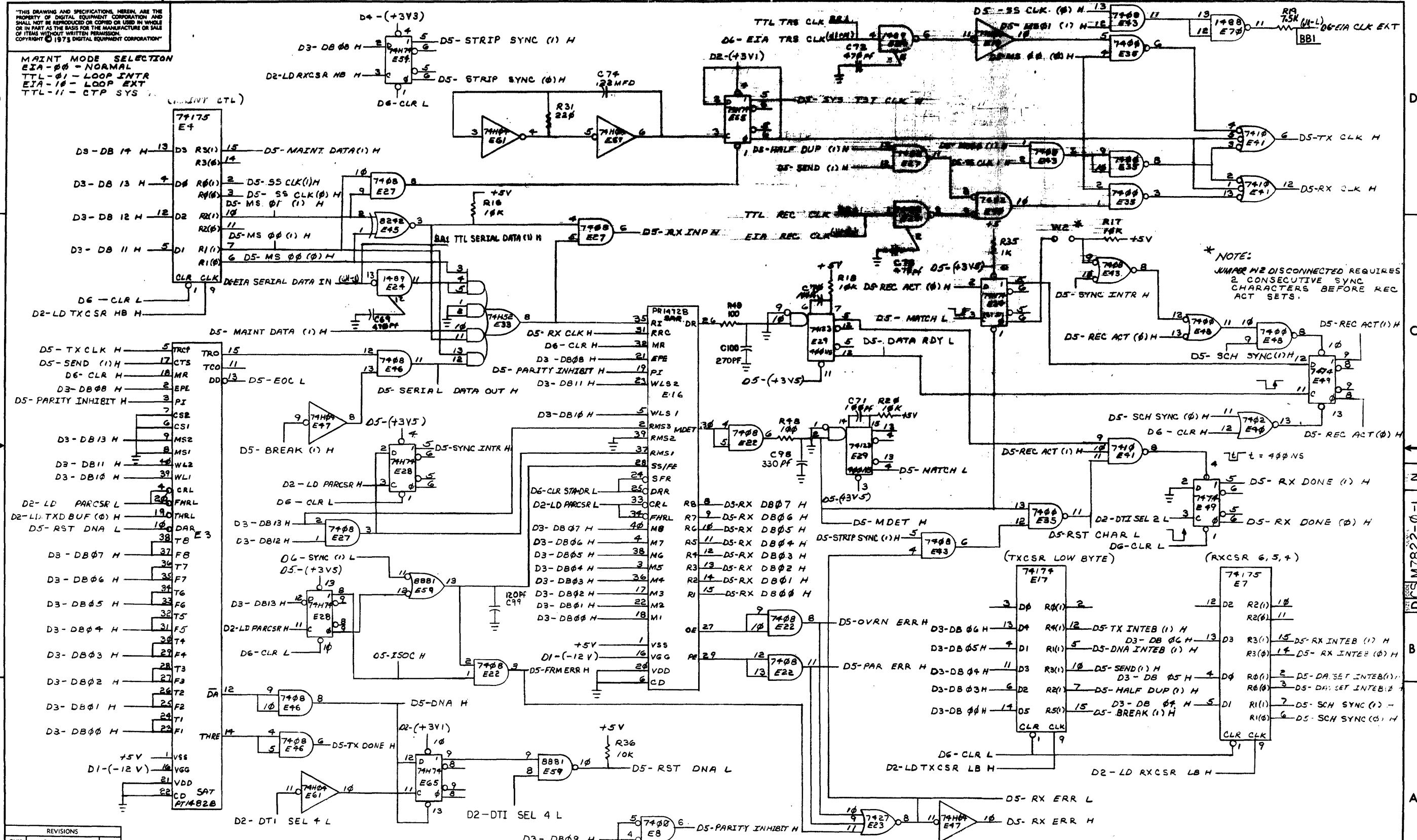
PGM SYNC INTERFACE DCS M7822-0-1 N

SCALE 1/1 SHEET 3 OF 6 DIST.

8

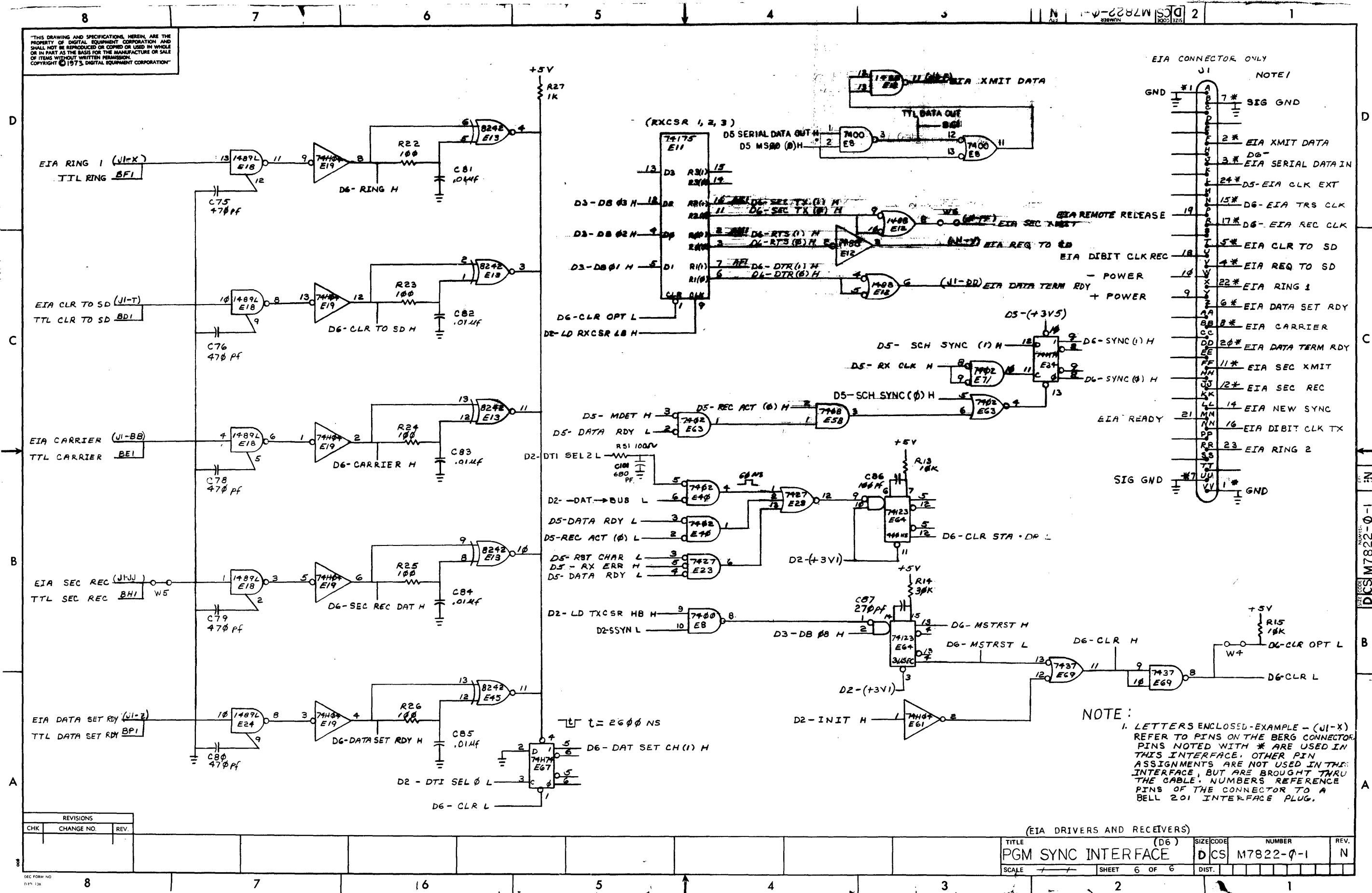
1





( XMIT RCV STATUS MAINT, AND CLK)

REVISIONS	CHANGE NO.	REV.	TITLE	(D5)	SIZE CODE	NUMBER	REV.
CHK			PGM SYNC INTERFACE	DCS	M7822-Φ-1		N
8			SCALE	+	SHEET 5 OF 6	DIST.	



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1

1

5

1

## OTES:

1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
  2. ONLY DEC PART #1210090-0-0 MAY BE USED AS JI.
  3. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #6 (BERG HOUSING) AS SHOWN.
  4. USE ITEM #13 (9107302-11) IN TWO PLACES (PI-1, PI-7) TO PREVENT SHORTING.
  5. USE ITEM #12 (9107295-11) ON ALL REMAINING SOLDER CUPS TO PREVENT SHORTING.
  6. DUE TO TOLERANCES WITH DIFFERENT VENDORS, THE HOOD (ITEM #8) MAY VARY IN OUTSIDE DIAMETER CAUSING POTENTIAL STRAIN RELIEF GRIPPING PROBLEM. SHOULD THIS CONDITION BE PRESENT USE ITEM #4 (9107034) AT JUNCTION OF CABLE AND HOOD.
  7. PLACE ITEM #4 (9107256) OVER SHIELD WIRE JI-A, JI-B, PI-1, PI-7.

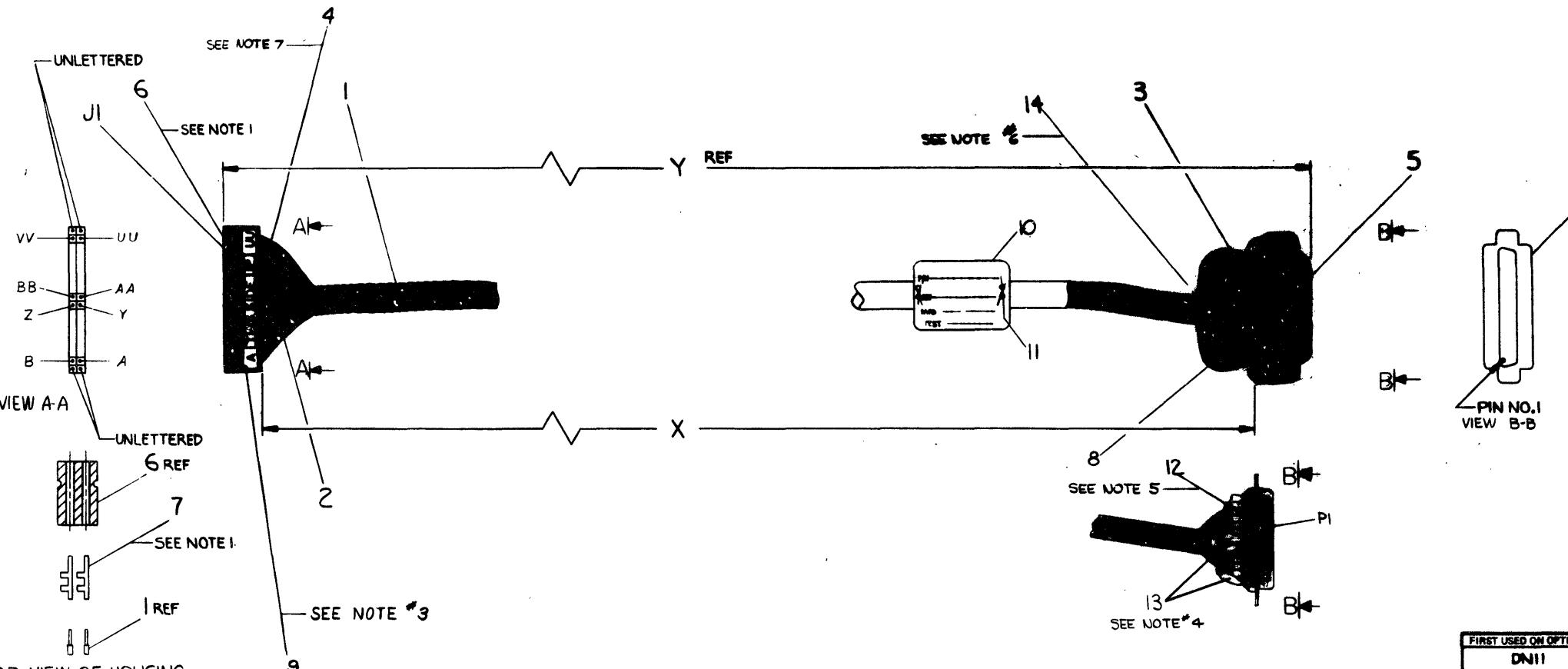
## WIRE TABLE

WIRE						
ITEM NO.	DESCRIPTION		FROM		TO	
	AWG	COLOR	CONNECTION	WITH	CONNECTION	WI
1 26	BLU/WHT	PI-1	*	SOLDER	J1-WV	7
	WHT/BLU	PI-2			J1-F	
	ORN/WHT	PI-3			J1-J	
	WHT/ORN	PI-4			J1-V	
	GRN/WHT	PI-5			J1-T	
	WHT/GRN	PI-6			J1-Z	
	BRN/WHT	PI-7	**		J1-UU	
	WHT/BRN	PI-8			J1-BB	
	SLV/WHT	PI-9			J1-Y	
	WHT/SLA	PI-10			J1-W	
	BLU/RED	PI-11			J1-FF	
	RED/BLU	PI-12			J1-JJ	
	ORN/RED	PI-13			J1-D	
	SLA/RED	PI-14			J1-LL	
1 26	SLA/GRN	PI-15	SOLDER		J1-N	7

ITEM NO.	DESCRIPTION	FROM	TO	WITH
AVG	COLOR	CONNECTION	WITH	CONNECTION
1 26	RED/RED	PI-16	SOLDER	J1-NN
	SLA	PI-17		J1-R
	RED/SLA	PI-18		J1-U
	BLU/BLU	PI-19		J1-P
	BLK/BLU	PI-20		J1-DD
	ORNG/BLK	PI-21		J1-MM
	BLK/BLK	PI-22		J1-X
	SWALK	PI-23		J1-RR
	SWALK	PI-24		J1-L
	RED/ORN	PI-25		J1-C
	SHIELD	PI-1	*	J1-A
	SHIELD	PI-7	55	55
2 26	BLK	PI-1		J1-SS
	RED	J1-E		J1-M

**LEGEND**

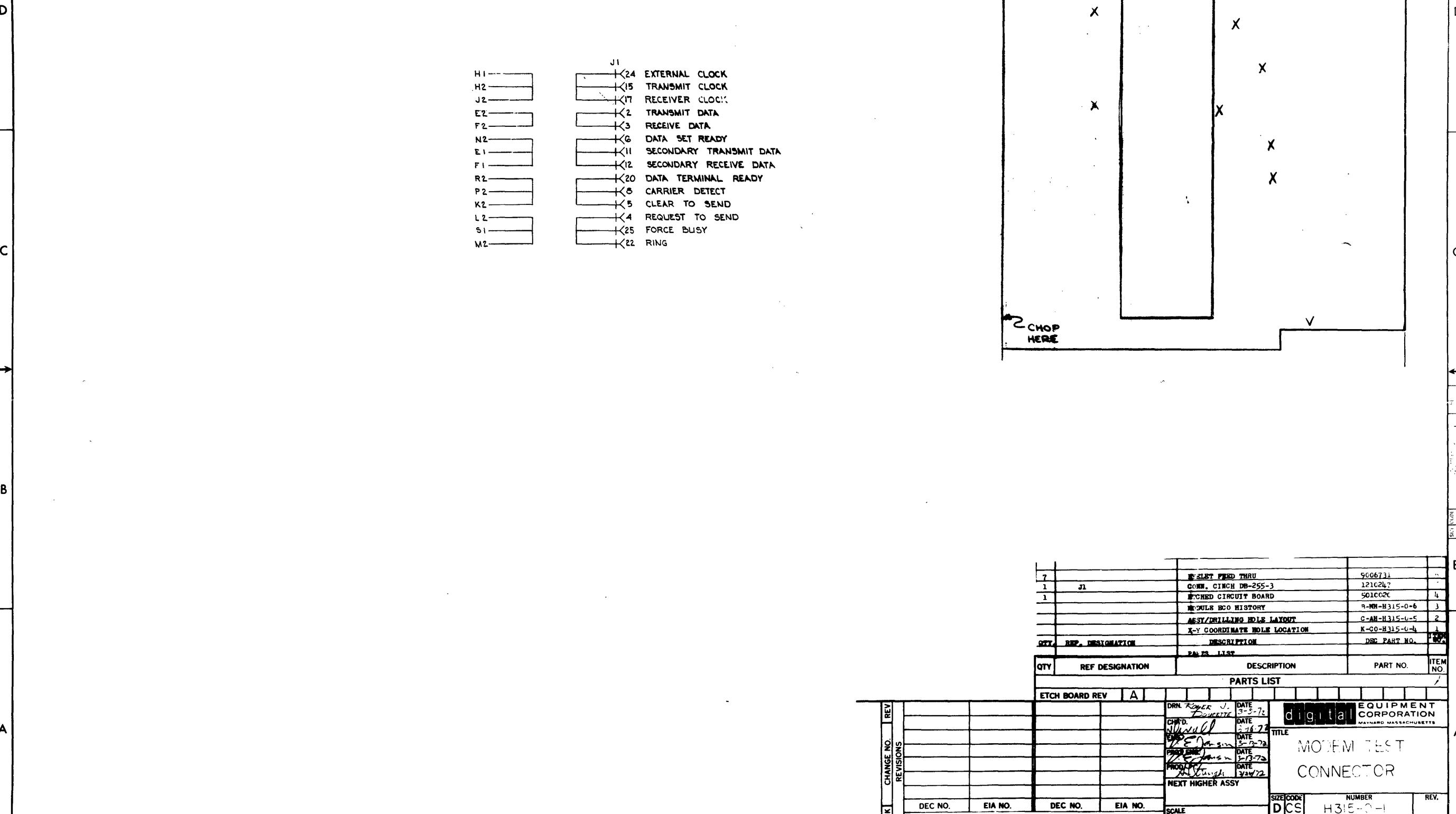
LEGEND		
NUMBER	VARIATION	
BC05C-25	DIM X	DIM Y (PRECUT)
	25' 3"	25' 1.8"
BC05C-50	25' ± 2%	56' 4.8"
BC05C-69	9' 2 3"	9' 1.8"



A/R	ITEM	QTY	SIZE CODE
A/R	TAPE, DOUBLE SIDED	9007834	14
A/R	TUBING, 10 AWG, CLEAR	9107302-11	13
A/R	TUBING, 14 AWG, CLEAR	9107295-11	12
2	tie wraps	9007031	11
1	CABLE, LABEL	9009532	10
1	LABEL, THIS SIDE UP	3611567	9
1	WOOD, #DB51226-1 CINCH	1205885	8
29	SOCKET, "HT-68	1210589-5	7
1	HOUSING, #20303 BERG	1210590-0-0	6
1	PLUG, #DB-25P CINCH	1205886	5
A/R	TUBING, .022 AWG TEF BLK	9107256-00	4
A/R	WIRE, #26 AWG STRD TEF BLK	9107636-00	3
A/R	WIRE, #26 AWG STRD TEF RED	9107636-22	2
A/R	CABLE, 25 CONDUCTOR #26 AWG	9107736	1

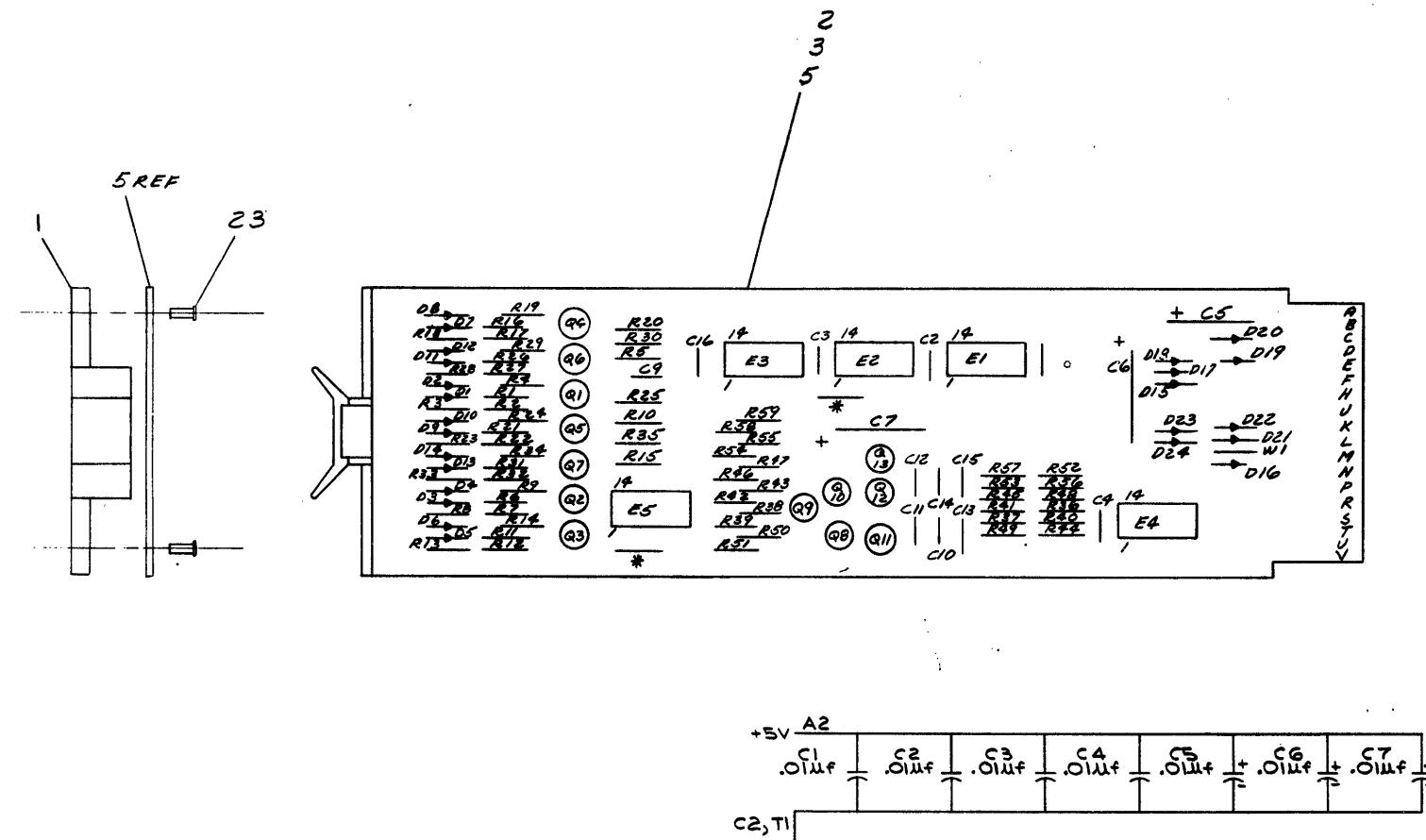
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8 7 6 5 4 3 2 1



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**NOTES:**

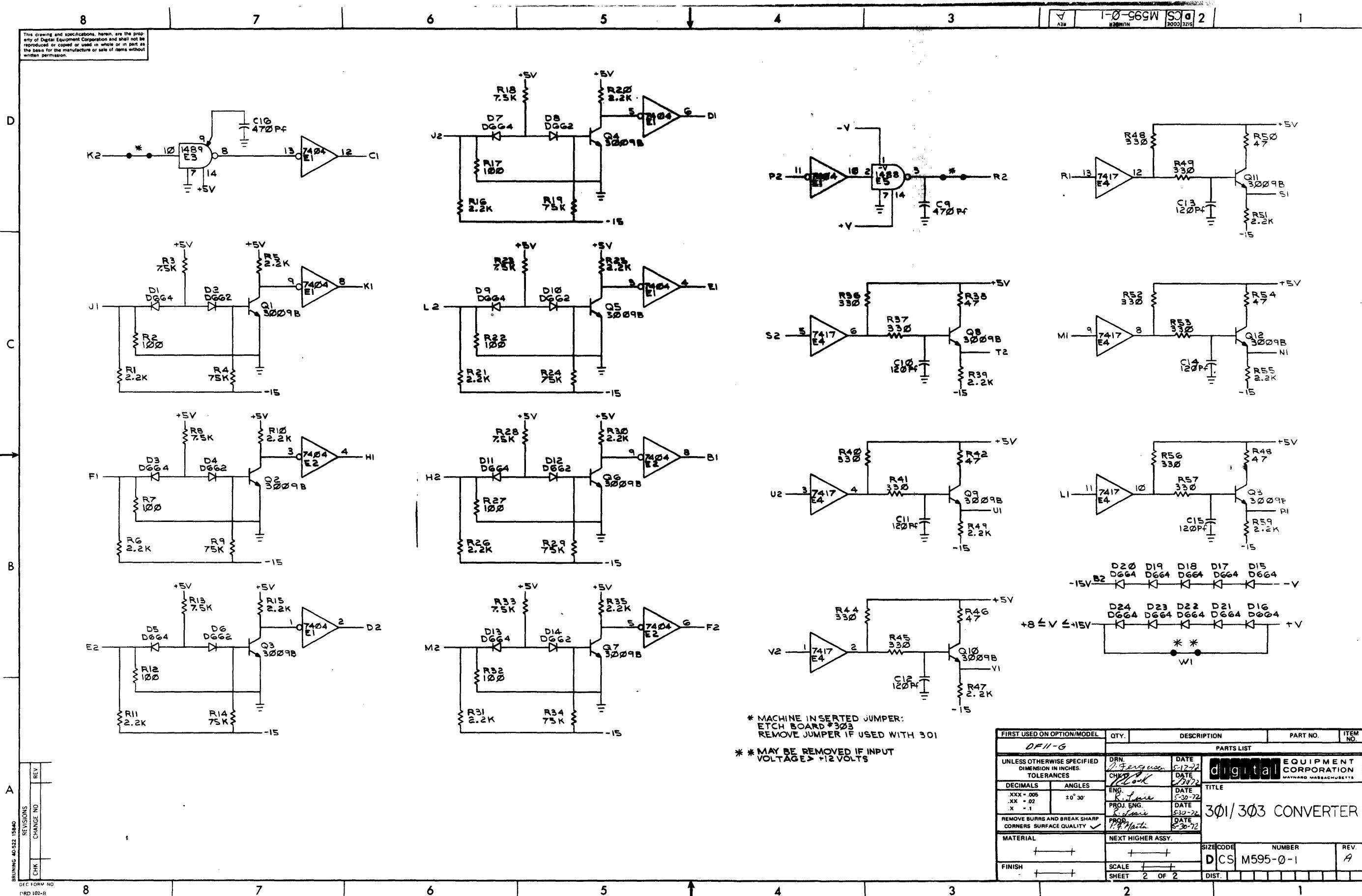


N/A  
+ 5V

DEC FORM NO. 10-100-1

FIRST USED ON OPTION MODEL		QTY	REF DESIGNATION	DESCRIPTION	PART NO.	NO.
DF11-G					PARTS LIST	
			ETCH BOARD REV B			
CHK	REV				DBN: <i>Signature</i> PL-61	DATE 5-22-72
	REVISIONS				CHKD:	DATE 5-22-72
				ENG:	DATE 5-22-72	
				PROL. ENG:	DATE 5-22-72	
				PROD:	DATE 5-22-72	
			DEC 3009B	2N3646	NEXT HIGHER ASSY	
			D664	IN3606		
			D662	IN645		
	DEC NO.	EIA NO.	DEC NO.	EIA NO.	SIZE CODE NUMBER REV	
	SEMICONDUCTOR CONVERSION CHART				D C S M 595-0-1	A
				SHEET 1 OF 2	DIST.	
301/303 CONVERTER						

## 3ØI/3Ø3 CONVERTER



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8 7 6 5 4 3 2 1

FUNCTION	WIRE	CONNECTION	WIRE	LOCATION
CLEAR TO SEND (CS)	C COND	P1 - 2		
SEND REQUEST (SR)	D COND	P1 - 3		
SEND DATA (SD)	E COND	P1 - 4		
DATA SET READY (DSR)	F COND	P1 - 5		
RING INDICATOR (RI)	F SHIELD	P1 - 6		
LOCAL TEST (LT)	G COND	P1 - 7		
SERIAL CLOCK TRANSMITTER	H COND	P1 - 8		
SERIAL CLOCK RECEIVER	I COND	P1 - 9		
RECEIVE DATA (RD)	K COND	P1 - 10		
SERIAL CLOCK RECEIVE ISOLATION	L COND	P1 - 11		
ASynch CLOCK	M COND	P1 - 12		
DATA TERMINAL READY (DTR)	M SHIELD	P1 - 13		
	C SHIELD	P1 - 14		
	D SHIELD	P1 - 15		
	E SHIELD	P1 - 16		
	F SHIELD	P1 - 17		
	G SHIELD	P1 - 18		
	H SHIELD	P1 - 19		
	I SHIELD	P1 - 20		
	K SHIELD	P1 - 21		
	L SHIELD	P1 - 22		
	M SHIELD	P1 - 23		
	A	P1 - 24		
	B	P1 - 25		

ATTACHED PAIR WIRE (IN LONG) WILL BE ATTACHED TO EACH CONDUCTOR OF EACH WIRE (1 WIRE TO INNER CONDUCTOR, 1 WIRE TO THE SHIELD). THE WIRES WILL THEN BE CRIMPED TO THE BERG PINS AS INDICATED.

WHEN SUPPLIED BY A VENDOR THIS CABLE WILL BE FULLY TESTED BY VENDOR. TESTED AND INSPECTED BY INCOMING INSPECTION PRIOR TO ACCEPTANCE.

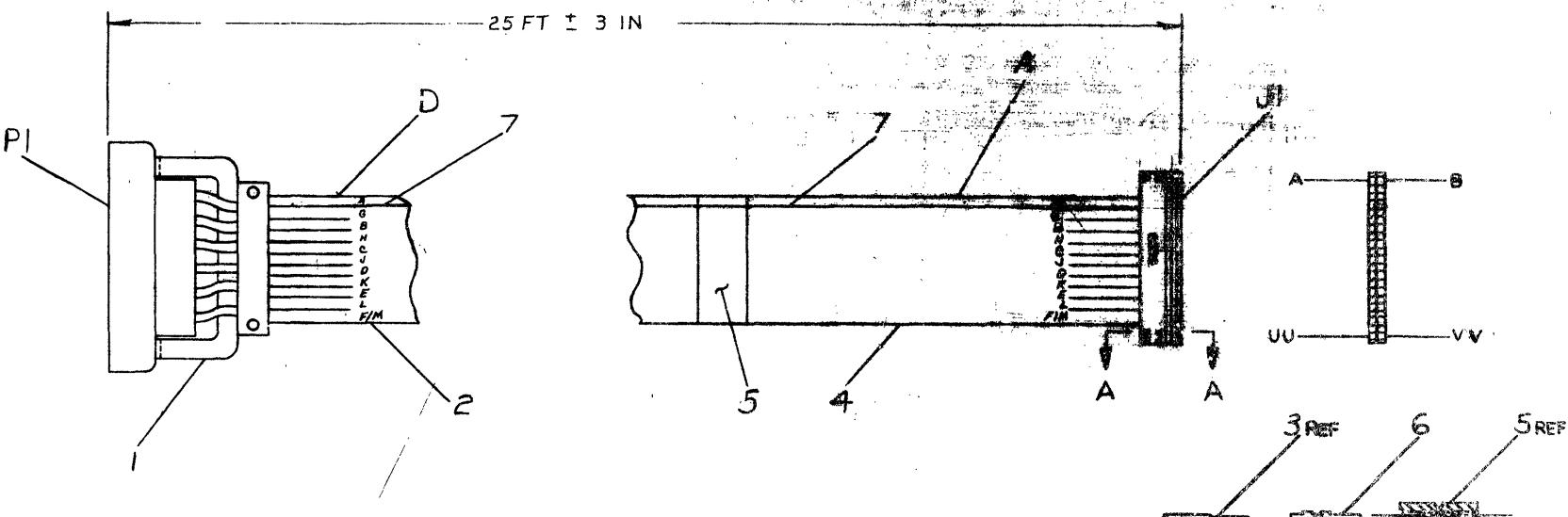
C. THIS IS THE CABLE DESCRIBED BY PURCHASE SPECIFICATION 11-00019. A COLORED TRACER WILL BE WOVEN INTO THE CABLE BETWEEN WIRES 'H' AND 'G'.

RG 183 A/U CAN BE USED TO DIRECTLY REPLACE RG 180U. NO SUBSTITUTIONS, OTHER THAN THOSE SPECIFIED IN THIS PRINT, MAY BE MADE WITHOUT PRIOR APPROVAL.

SIZE CODE NUMBER REV  
D U A B C O I W - 0 - 0 A

B

A



SECTION A-A

SECTION B-B

REVISIONS	CHANGE NO.	REV.
CHN	BCOIW-00001	A
SP	2-1-72	
SMITH		

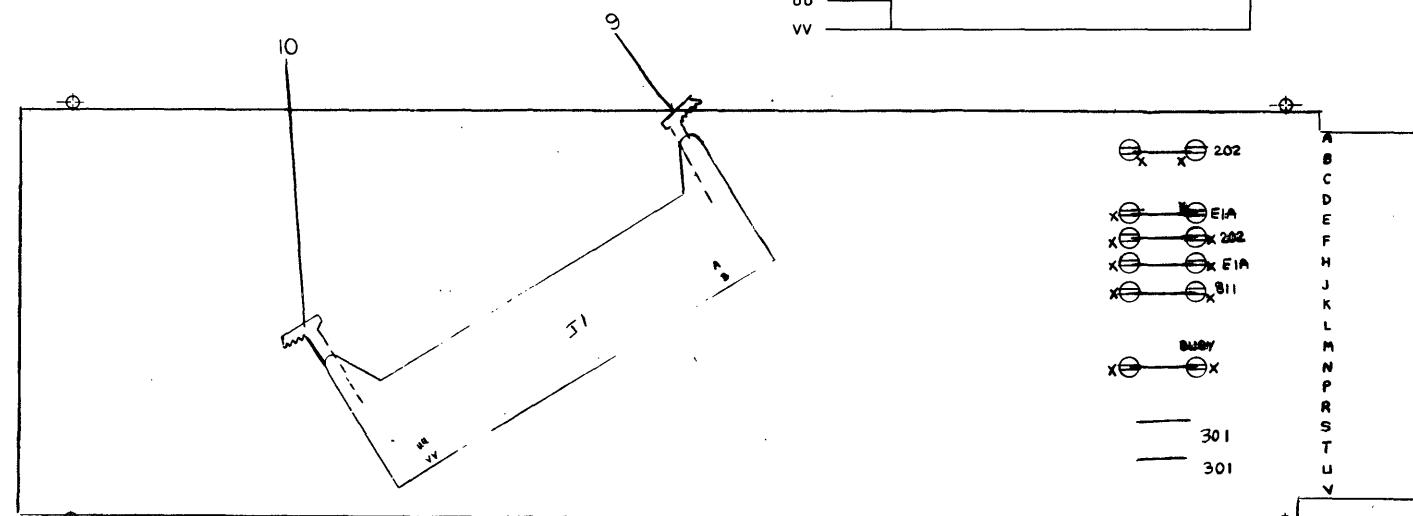
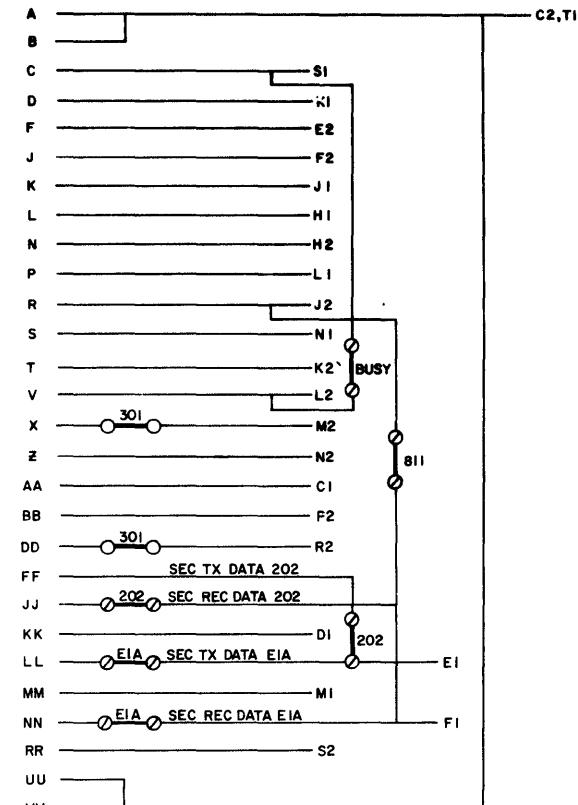
DFC FORM NO.  
DD FORM 100-A

8 7 6 5 4 3 2 1

FIRST USED ON OPTION/Model		DATE 2-1-72	DATE 3-25-74	DATE 3-22-74	DATE 3-27-74
PARTS LIST		EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS			
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES		TITLE HIGH SPEED MODEM CABLE			
DECKALS ANGLES XNN = .005 XN = .02 X = .1 REMOVE DURS AND BREAK SHARP CORNERS SURFACE QUALITY ✓ MATERIAL		NEXT HIGHER ASY.			
FINISH		SCALE 1 OF 1	REV. A	DIST. G	
SIZE CODE NUMBER		D U A B C O I W - 0 - 0	REV. A		

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- I. FUNCTIONS OF MODEM JUMPERS (WHEN INSTALLED)
- EIA — SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA PINS 14 & 16
  - 202 — SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA PIN 11 & 12
  - 301 — ALLOW OPERATION OF RING AND DATA TERMINAL READY FUNCTIONS WITH BELL 303 SERIES
  - BII — BELL 8IIB RESTRAINT FUNCTION IS MONITORED BY SECONDARY RECEIVE.
  - BUSY — BELL 8IIB FORCE BUSY FUNCTION ANDED WITH REQUEST TO SEND
  - 301 — REMOVE FOR BELL 301 USE ONLY



REVISIONS
CHG CHG NO REV
572 0001 D
10/10/71
ENG. 10/10/71
PROD. 10/10/71

DRN 5 Cooper	DATE 10-5-71
CHG CHG NO REV	DEC EIA DEC EIA
572 0001 D	
10/10/71	
ENG. 10/10/71	DATE 10/10/71
PROD. 10/10/71	DATE

TRANSISTOR & DIODE CONVERSION CHART
digital
EQUIPMENT CORPORATION
MARLBOROUGH, MASSACHUSETTS

QTY.	REP. DESIGNATION	DESCRIPTION	PARTS LIST
X-Y COORDINATE HOLE LOCATION			
		ASSY/DRILLING HOLE LOCATION	D-AH-M970-0-5
		X-Y COORDINATE HOLE LOCATION	K-CO-M970-0-4
		DESCRIPTION	DESC PART NO.
			10
1	LEFT LATCH	1209941-03	10
1	RIGHT LATCH	1209941-04	9
1	HANDLE, PLIP CHIP - MAGENTA	9008337-06	8
12	SPLIT LUGS	9006735	7
2	EYESETS	9006732	6
1	J1	CONN 4OP RT ANG HEADER	1209941
1		ETCHED CIRCUIT BOARD	5009752
		MODULE ECO HISTORY	B-MH-M970-0-6
		ASSY/DRILLING HOLE LOCATION	D-AH-M970-0-5
		X-Y COORDINATE HOLE LOCATION	K-CO-M970-0-4
		DESCRIPTION	DESC PART NO.
			10