Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-9
Maintenance Manual

KG09B

Memory Extension Control

DEC-09-I1AA-D

KG09B
MEMORY EXTENSION CONTROL MAINTENANCE MANUAL

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual contains operation and maintenance information for the memory extension options KG09B and MM09A/B/C of the PDP-9 Digital Data Processor. For complete understanding of the options and their relation to the basic PDP-9 system, the user should be thoroughly familiar with the contents of the PDP-9 Maintenance Manual, Document No. F-97.

1.2 PURPOSE

The KG09B Memory Extension Control allows expansion of the basic 8192-word PDP-9 core memory to 32,768 words in increments of 8192 words, using the MM09A, MM09B, and MM09C Memory Modules, respectively.

The KG09B option includes a 2-bit extended program counter (EPC), a 2-bit extended memory address register (EMA), and associated control logic. The KG09B is installed in the two DEC Type 1943D Mounting Panels located above the basic PDP-9 tape reader/punch, Figure 1-1. The mounting panels comprise the ME09B chassis which also houses the MP09C Memory Parity and KX09A Memory Protection options. An indicator panel, supplied as part of the ME09B and installed above the marginal check panel, contains indicator lamps for all three options.

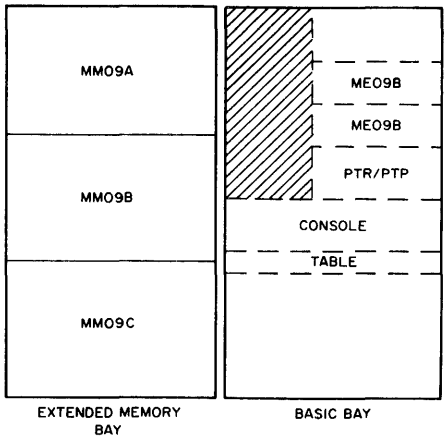


Figure 1-1 Extended Memory Configuration, Front View

The MM09/A/B/C Memory Modules are installed in a separate DEC Type CAB-31 cabinet bolted to the basic cabinet. Each memory module is assigned its own memory bank designation as follows:

MC70B	Basic Memory	Bank 0
MM09A	First added 8K module	Bank 1
MM09B	Second added 8K module	Bank 2
MM09C	Third added 8K module	Bank 3

1.3 RELATED DOCUMENTS

In addition to certain documents listed in Chapter 1 of the PDP-9 Maintenance Manual, the KG09B and MM09A/B/C options are supported by the test tapes indicated in Table 1-1. Refer to Chapter 4 for test conditions.

Table 1-1
Related Test Programs

Number	Title	Form
MAINDEC-9A-D1CC-PH	KG09A/B Extended Memory Control Test	Hardware Read-In(HRI) paper tape
MAINDEC-9A-D1DA-LA-PH	Extended Memory Test	Hardware Read-In(HRI) paper tape
MAINDEC-9A-D1FA-PH	Extended Memory Address Test	Hardware Read-In(HRI) paper tape

1.4 POWER REQUIREMENTS

The KG09B option draws its +10, -15V logic power from the basic PDP-9's 709 Power Supply. The MM09A/B/C modules take their -30V memory power from the 709 supply. Additionally each module requires a separate 783 Power Supply for its +10, -15V logic power. These 783 supplies are located in the memory module cabinet.

1.5 ENGINEERING DRAWING REFERENCES

Throughout this manual all references to option drawings and basic PDP-9 drawings are abbreviated. Refer to Chapter 5 of the PDP-9 Maintenance Manual for descriptions of drawing number codes. Chapter 5 of this manual contains a set of option drawings and circuit schematics of all logic modules.

1.6 SPECIFICATIONS

1.6.1 KG09B

Heat Dissipation	94 BTU/hr
Power Dissipation	0.030 kW

1.6.2 MM09A/B/C

Cabinet Height	69-1/8 in.
Cabinet Width	32-1/2 in.
Cabinet Depth	27-3/4 in.
Door Clearance (rear)	31 in.
Cabinet Weight	400-800 lb.
Heat Dissipation	421 BTU/hr/8K
Power Dissipation	0.134 kW/8K

CHAPTER 2
INSTALLATION AND OPERATION

2.1 INSTALLATION

PDP-9 systems which include the extended memory options are shipped with the ME09B chassis and associated panel installed, and the memory module cabinet bolted to the basic system cabinet. No special installation instructions are required. Certain jumpers in the basic cabinet must be removed when the KG09B and MM09A/B/C options are installed:

EXD (1) B from F36C to F37E (drawing KC27)
EPC03 (1) from F37C to F37K (drawing KC27)
EPC04 (1) from F37M to F38C (drawing KC27)
Indicator wiring from D26C to D25A (drawing ME3)
Indicator wiring from D25A to D25B (drawing ME3)
Indicator wiring from D25B to D25C (drawing ME3)

2.2 INTERFACE CABLING

2.2.1 Memory Extension Control KG09B

Eight flex-print cables carry signals between the KG09B and the CP, I/O bus, and the first MM09A memory extension module. Drawing KG6 presents a pictorial view of the cabling configuration and a listing of the cable connectors.

The two memory module cables carry the EMA03-04 bits to the memory control circuits from the KG09B option, and the MB01, MB03, MB04 bits to the KG09B from the memory module interface. The connectors are shown on drawing KG3. These are chain-connected from the basic MC70B memory, Section 2.2.2.

Two cables connect the standard I/O bus to the KG09B, drawing KG4, three cables interconnect the CP/KG09B signals, drawing KG3, and one cable carries the indicator drive power to the associated indicator panel supplied as part of the ME09B hardware.

2.2.2 Memory Modules MM09A/B/C

Each memory module is chain-connected to the previous one by means of six flex-print cables as shown on drawing MM2. A full complement of three memory modules therefore requires 18 cables, with MM09C connected to the MC70B as shown. Not shown on drawing MM2 are the two cables which connect EMA03-04 and MB01, MB03-04 from MM09A to the KG09B, Section 2.2.1.

2.2.3 Level Terminators

Two G795 Level Terminators are normally furnished and installed in locations D38, E38 of the basic MC70B memory. These provide proper termination for bits MB00-17, as shown on drawing MC9. Installation of extended memory modules requires that the terminators be removed and replaced by the W033 Flexprint Cable Connectors as listed on drawing MM2. The terminators are then relocated to D38, E38 of the last memory module in use. For example, a fully extended, 32K memory system requires the relocation of the terminators to D38, E38 of MM09A, the last chain-connected module.

2.3 POWER WIRING

2.3.1 Memory Extension Control KG09B

Drawing ME2 shows the wiring to the power terminals on the ME09B chassis and the associated indicator panel. The logic power is distributed from the terminals to all modules installed in the chassis via the marginal check switches on the 1943D mounting panels. Both the fixed +10V, -15V and the marginal checking +10V, -15V power come from the matching color-coded terminals as indicated on drawing IC-9-0-1. The power is controlled from the basic system's 841A Power Control as explained in Section 3.7, PDP-9 Maintenance Manual.

2.3.2 Memory Modules MM09A/B/C

Memory module power wiring is shown on drawing MM1. Primary ac power switched on from the basic system's 841A unit energizes the 783 Power Supplies and the fans in the MM09 fan housings. The 783 Power Supplies provide the fixed +10V, -15V logic power to the MM09 memory modules. The marginal checking +10V, -15V power comes from the basic system's 709 Power Supply, as controlled by the marginal check panel. The 709 supply also provides the -30V memory stack power to the MM09 modules. The color coding scheme for the power terminals on the fan housings is the same as that shown for the basic system, drawing IC-9-0-1.

2.4 MANUAL CONTROLS AND INDICATORS

2.4.1 Basic System Console

The basic PDP-9 console contains a prewired EXD mode switch and indicator lamp. The switch is used in conjunction with the START key to enter or leave the extend mode at the start of a program.

Thereafter, the programmed IOT instructions control the status of the extend mode regardless of the EXD switch position. The indicator illuminates when the PDP-9 is in the extend mode, regardless

of the setting of the EXD switch. In the off (down) position the EXD switch is grounded. The LOCK position of the maintenance panel switch has no effect on the EXD switch.

The memory extension control logic permits the console DEPOSIT, EXAMINE, READ IN, and I/O RESET functions to operate within the extended memory system as described for the basic system in the PDP-9 Maintenance Manual.

2.4.2 Indicator Panel

The ME09B includes an indicator panel installed above the marginal check panel of the basic PDP-9 system. This panel contains prewired indicator driver transistors and lamps for all three options assigned to the ME09B chassis, including six lamps for the KG09B: EPC03-04, EMA03-04, EMIR, and EXD. All illumination signals come from connector W018-D25 in the ME09B chassis. The KG09B indicators show the status of the respective flip-flops in the control logic.

2.5 PROGRAMMING CONSIDERATIONS

The KG09B logic adds four IOT instructions to the basic PDP-9 repertoire and makes use of the DBR instruction existing in program interrupt (PI) and automatic priority interrupt (API) service routines. Table 2-1 briefly describes these functions.

Table 2-1
Extended Memory IOT Instructions

Octal Code	Mnemonic	Description
707701	SEM	Skip next instruction if extend mode enabled
707702	EEM	Enter the extend mode.
707704	LEM	Leave the extend mode.
707742	EMIR	Extend mode interrupt restore.
703344	DBR	Debreak and restore.

Execution of the EEM instruction enables the extend mode, and LEM disables the mode. If the mode is enabled, execution of the SEM instruction increments the PC contents by 1, causing the program to skip the next sequential instruction.

The PI, API, and DCH/RTC breaks trap to their proper locations in bank 0 regardless of the extend mode status. In trapping to bank 0, a PI break stores the existing status of the LINK, extend mode, memory protect mode, and EPC along with the current program count (PC) in location 00000,

then disables the mode. An API break transfers program control to the appropriate channel entry location in bank 0. The instruction present in the channel location should be a JMS or a JMS I, which stores the existing status of the LINK, etc., in the location referenced by the JMS instruction. With the extend mode enabled, JMS I permits this storage location to reside in any bank. For this reason in particular, the API break does not disable the extend mode.

A DCH break traps to bank 0 for the WC cycle. During the CA cycle the CA register contains a 15-bit address of the data entry or retrieval location, in which case bits 03-04 may point at any bank. An RTC break of course is a one-cycle (WC) break which remains in bank 0.

A DMA break does not effect the extend mode operations since its control logic employs a separate addressing scheme to access any bank.

A memory protect violation from the Memory Protection option KX09A causes an immediate fetch of a JMS 20 instruction if the PI facility is disabled, or a JMS 0 instruction if the facility is enabled, with a trap to bank 0 in either case. The current program count and program status information is stored in location 00020 or 00000, and a monitor program begins from 00021 or 00001. This is true regardless of extend mode status.

EMIR primes the computer to restore the status of the extend mode and EPC along with the interrupted program count upon completion of the PI, API, or protect violation breaks. Like EMIR, DBR also restores the status of the extend mode and EPC. Additionally it restores the status of the LINK and the memory protect mode. Normally the next to the last instruction in the PI/API/protect violation routine, DBR or EMIR is followed by a JMP I to the storage location. JMP I performs the actual program and status restoration. As for all IOT instructions, another interrupt cannot occur until completion of the subsequent instruction, i.e., completion of JMP I. The following sequence, for example, re-establishes the interrupted conditions upon completion of the PI service routine:

```
ION             /REENABLE THE PI FACILITY
EEM*            /ENABLE EXTEND MODE
DBR or EMIR     /PRIME SYSTEM TO RESTORE PROGRAM
JMP I           /RESTORE PROGRAM
```

* If the interrupt occurred in other than bank 0 with extend mode disabled.

While the extend mode is enabled, any operand in the memory system can be indirectly accessed. The effective address in an indirectly addressed location in the current memory bank must be a 15-bit address. Bits 03-04 in the effective address indicate the memory bank that is to be accessed, and bits 05-17 indicate the operand location in that bank. The EPC indicates the current bank and does not change. Because the EPC cannot count in conjunction with the PC, the PC does not increment across memory bank boundaries (i.e., the location addressed after 17777 is 00000, not 20000).

To change the currently active bank, the program must include a jump instruction with indirect address (JMP I, or JMS I if the exit point is to be preserved for subsequent restoration). The extend mode must be enabled. Execution of the jump instruction enters bits 03-04 of the effective address into the EPC to select the new memory bank. Bits 05-17 enter the starting address of the new bank in the PC.

The CAL instruction addresses location 00020 in bank 0 when the extend mode is enabled and the relative location 00020 in the current memory bank when the mode is disabled. (A CAL I instruction in any case is invalid and will be treated like a JMS I 20).

The XCT instruction always functions as if the referenced instruction was fetched. Thus an XCT I reference to a skip instruction in another bank effects a skip of the instruction immediately following XCT I if the skip condition is satisfied. Similarly, XCT I reference to a JMS or CAL instruction in another bank effects the appropriate storage of the PC and EPC contents, which represent the address of the location following XCT I and not the location following the referenced instruction.

While the extend mode is disabled, all instructions and operands to be executed must be stored in the same (current) memory bank. This current bank is addressed by both the PC and the EPC. It is impossible to enter other banks with the extend mode disabled, except as noted for traps to bank 0 above, and for traps to autoindex registers 00010-17 in bank 0.

Regardless of extend mode status, an instruction which indirectly addresses an autoindex register traps to bank 0. When the extend mode is enabled the 15-bit effective address in the autoindex location points to any bank. When the extend mode is disabled, the effective address in the autoindex location points to memory bank 0. That is, only 13 bits of the effective address in the autoindex register are accepted by the control logic. The EMA which was zeroed in order to address the autoindex location is restored from the EPC at the end of the instruction. To load an autoindex register from any memory bank other than 0, the extend mode must be enabled. In this case a DAC I instruction references an effective address location in the current bank (other than 00010-17), and the effective address points to bank 0.

CHAPTER 3
PRINCIPLES OF OPERATION

This chapter describes the Memory Extension Control option KG09B in terms of its instruction repertoire and the logic that implements the instructions. The discussions include references to the logic drawings in Chapter 5 and to pertinent drawings in the basic PDP-9 system.

The MM09A/B/C Memory Module options are exact duplicates of the basic PDP-9 memory system MC70B. Refer to Section 3.6 of the PDP-9 Maintenance Manual for control logic details.

3.1 MANUAL OPERATIONS

3.1.1 START Key

The on (up) position of the console EXD switch enables the extend mode in conjunction with the START key. Regardless of the setting of the switch, a program can be started in any memory bank by setting the ADDRESS switches and pressing START. The negative SW EXD level goes from the switch to W034-F37 on drawing KC28, to G796-A06 and W034-B06, drawing KG3. From B06 the level goes to the control logic on drawing KG2.

With the console ADDRESS switches set to the program's starting address, the operator depresses the START key to start the program as described in Section 3.7.4.2, PDP-9 Maintenance Manual. The START operations involve the extraction of process word 06 from control memory as described. Process word 06 contains the processes ADS0, PCI, MBI, SM, and CMA21. The first three processes gate the 15-bit starting address from the ADDRESS switches into the MB and the 13 least-significant bits into the PC.

ADS0 (1), PCI (1) B, and the SW EXD level produce EXD (1) on drawing KG2, which sets the EXD flip-flop via collector pulling and lights the EXD indicator on the console via W018-D25, also shown on drawing KG2. The absence of both PC0 (1) and EXT (1) allows MB03-04 to appear at the jam input gates of the EPC and EMA flip-flops. MB03-04 represent the extended address bits set earlier into ADDRESS switches 03-04.

ADS0 (1) B triggers the 65 ns delay B310-CD24. This delay allows the MB03-04 bits to settle before the delay output triggers pulse amplifiers C21 and D21 to strobe the EPC and EMA jam input gates. The EPC will be strobed from pulse amplifier C21 because of ADS0 (1) and PCI (1). Thus the extended address bits get into the flip-flops at some time before the CP's RUN flip-flop sets to permit the issuance of the first CLK pulse. The time, of course, depends on the REPEAT SPEED switch selection.

EMA03-04 go from W033-B07 on drawing KG3 to W033-F40 on drawing MC8 for comparision with the bank selection switches in the basic MC70B memory (bank 0), drawing MC2. The bits are also chain-connected from F38 of the basic memory to F40 of the next (MM09) memory bank, etc., so that SM (1) and the CLK pulse activate the appropriate bank as selected by the EMA bits. SM(1) and CLK thus start the core memory and control memory to fetch the addressed instruction and to extract the fetch entry process word (21).

3.1.2 DEPOSIT/EXAMINE Keys

The DEPOSIT and EXAMINE operations described in Sections 3.7.4.5 through 3.7.4.8 in the PDP-9 Maintenance Manual hold true for any memory bank as selected by ADDR SW03-04. For these operations neither the PC nor the EPC is involved. ADSO (1) appears in process word 01 to strobe the MB03-04 bits into the EMA as for the START operations above. The absence of PCI (1) in the process word precludes the strobing of the EPC flip-flops and the production of the EXD (1) level. Thus the use of the EXD switch is ineffective and the extend mode remains unchanged.

3.1.3 READ IN Key

The READ IN operations described in Section 3.7.4.9 of the PDP-9 Maintenance Manual hold true for any memory bank as selected by ADDR SW03-04. ADSO (1) appears in process word 01 to strobe the MB03-04 bits into the EMA as for the START operations above. The absence of PCI (1) in the process word precludes the strobing of the EPC flip-flops at this time and inhibits the EXD (1) signal. Thus the use of the EXD switch is ineffective and the extend mode remains unchanged.

During this time the tape reader logic is issuing RD START RQ, which conditions the DCD input gate to pulse amplifier R603-C18. On the subsequent process word 25 ADSO (1) is removed, so that $\overline{\text{ADSO (1) B}}$ triggers the amplifier to strobe the EPC. Thus the EPC contains MB03-04, representing the ADDR SW03-04 selection. This is done to accommodate the execution of the last word read into memory from the tape. As described, the last word is usually a JMP instruction to the starting address of the program just read into memory. The PCO (1) level at the end of the JMP execution gates the EPC status into the EMA jam input gates and PCO (1) B strobes the gates. In this manner the program continues in the current memory bank.

3.1.4 I/O RESET Key

The I/O RESET key clears all flip-flops in the KG09B logic in addition to the basic system flip-flops as explained in Section 3.7.4.10, PDP-9 Maintenance Manual.

3.2 IOT INSTRUCTIONS

3.2.1 SEM (707701)

The SEM instruction (skip on extend mode enabled) is decoded in the I/O control logic, drawing KD3, to produce the IOT7701 pulse at the device selector W103-CD14, drawing KG2. If the extend mode is enabled, IOT7701 sets the EX SKIP flip-flop. EX SKIP (1) generates SKIP RQ at R111-D16U which goes back to the I/O control logic via the I/O bus. SKIP RQ results in IO SKIP which sets the SKIP flip-flop on drawing KC14. See Section 3.8.1.6, PDP-9 Maintenance Manual.

The IO SYNC level resets the EX SKIP flip-flop. IO SYNC is obtained on each computer CLK POS pulse where no AM request has been received, drawing KD3 (2), and where no IOT instruction is in progress, drawing KD3 (1).

3.2.2 EEM (707702)

The EEM instruction (enter the extend mode) is decoded in the I/O control logic, drawing KD3, to produce the IOT7702 pulse at the device selector W103-CD14, drawing KG2. IOT7702 sets the EXD flip-flop to enable the extend mode.

3.2.3 LEM (707704)

The LEM instruction (leave the extend mode) is decoded in the I/O control logic, drawing KD3, to produce the IOT7704 pulse at the device selector W103-CD14, drawing KG2. IOT7704 resets the EXD flip-flop to disable the extend mode.

3.2.4 EMIR (707742)

The EMIR instruction (extend mode interrupt restore) is included to provide compatibility from the PDP-7 to the PDP-9. Its use is described in the PDP-7 User Handbook. EMIR is decoded in the I/O control logic, drawing KD3, to produce the IOT7703 pulse at the device selector W103-CD14, drawing KG2. Additionally, bit 12 in the instruction word produces the SD00 level which conditions the DCD set gate to the EMIR flip-flop. The IOT7702 pulse therefore sets the EXD and EMIR flip-flops simultaneously.

EMIR always precedes a JMP I instruction to the program storage location upon completion of a PI or API break. During the JMP I fetch cycle, the IR04 (1) bit is detected on drawing KC12 to cause the computer to go into a defer cycle. The defer cycle fetches the effective address word previously stored by the PI or API break entry processes, now indirectly addressed by the JMP I instruction. The effective address word contains the interrupted program count in bits 05-17 plus the interrupted LINK, extend mode, memory protect mode, and EPC status in bits 00-04.

DEI (1) in the defer cycle entry process word (31) sets the EXCY flip-flop, conditioned by EXD (1) and IR04 (1). The CLR pulse which follows process word 31 gates the effective address word into the MB.

DEI (1) also resets IR04 so that the JMP op code produces REP on drawing KC12, causing the computer to enter the JMP execute cycle. The JMP execute process word 74 contains MBO, PCI, DONE, LI, CONT, and CMA10. MBO (1) and PCI (1) place the effective address word (bits 05-17) in the PC. At the same time PCI (1) B samples the original extend mode status bit MB01 (0) B in conjunction with EXCY (1) and EMIR (1) at R111-D15H. If MB01 was at 0 when stored, then EXD (0) ensues to reset the EXD flip-flop via collector pulling. If MB01 was a 1, then the EXD flip-flop remains set.

EXCY (1) and PCI (1) B trigger pulse amplifier W612-C21 to strobe the EPC jam input gates. The MB03-04 bits are thus restored to the EPC.

The main program count and the extend mode and EPC status are now fully restored. Process word 10 (BGN) prepares the computer for the resumption of the main program by gating the PC contents into the MB with processes PCO and MBI. PCO (1) B strobes the EMA jam input gates which now receive the EPC bits from B169 AND/NOR gates. When the first instruction has been fetched, IRI (1) in the fetch cycle process word 12 resets the EMIR and EXCY flip-flops.

3.2.5 DBR (703344)

The DBR instruction (debreak and restore) which always precedes a JMP I instruction, is decoded in the I/O control logic, drawing KD3, to produce the DBR level as described in Section 3.8.1.7, PDP-9 Maintenance Manual. The DBR pulse occurring during process 74 of JMP I causes restoration of the interrupted LINK, memory protect mode, and PC status as described. Additionally, DBR samples the interrupted extend mode status bit on drawing KG2 as reflected in MB01 of the effective address word. If 0, DBR∧MB01 (0) produce EXD (0) at R111-D17 to hold the EXD flip-flop in the reset state. If 1, DBR∧MB01 (1) produce EXD (1) and EXCY (1) at R002-C25 to set the respective flip-flops. Thereafter, these flip-flops act to restore the EPC as for EMIR.

3.3 ADDRESSING ANOTHER BANK

With the extend mode enabled, all memory reference instructions in a currently active bank can indirectly address a location in any other bank.

During process word 12 of the instruction fetch cycle the instruction word containing the indirect address is placed in the MB and the op code portion is placed in the IR. The IRI (1) process which gates the op code into the IR also resets the EXCY flip-flop, drawing KG2. IR04 (1), indicating an indirect address, conditions the DCD set gate to the flip-flop in conjunction with EXD (1).

Process word 24 detects IR04 (1) to force the computer into a defer cycle. At the start of the defer cycle the DEI (1) process sets EXCY (1) and resets IR04. The core memory read half-cycle reads out the effective address word, and other processes place it in the MB. MB03-04 designate the memory bank to be accessed. These bits are presented to the EPC and EMA jam input gates via the B169 AND/NOR gates in the absence of the PCO (1) and EXT (1) levels.

MEM STROBE occurs in core memory at the same time that STROBE SAR and STROBE SAL read out the effective address word into the MB. MEM STROBE, DEI(1), and EXCY(1) produce EMA STROBE, which strobes the MB03-04 bits into the EMA. The EPC retains the current bank designation because of the absence of a strobing pulse at this time.

Process word (24) determines if the computer shall go into an execute cycle or into the special IA0 cycle, as indicated by the op code in the IR. The execute or the IA0 cycle fetches the operand from the memory bank designated by the EMA, and the instruction is executed. In either case, the BGN process word (10) at the end of the cycle transfers the next sequential instruction address from the PC to the MB for the next fetch cycle. PCO (1) of the BGN word also gates the EPC bits into the EMA. Therefore, the program returns to the current bank from which the indirect address word was originally fetched.

3.4 CHANGING THE CURRENTLY ACTIVE BANK

3.4.1 JMP I (Op Code 60)

With the extend mode enabled, a JMP I instruction fetched from the currently active bank may change the EPC contents and consequently activate another bank. During the JMP I fetch cycle IR04 (1) is detected on drawing KC12 to cause the computer to go into a defer cycle. The defer cycle fetches the effective address word addressed by JMP I. The effective address word contains a 15-bit address, with MB03-04 designating the new memory bank to be accessed and MB05-17 containing the starting address in that bank.

DEI (1) in the defer entry process word 31 sets the EXCY flip-flop, conditioned by EXD (1) and IR04 (1), while other processes gate the effective address word into the MB. DEI (1) also resets IR04 (1) so that the JMP op code produces REP on drawing KC12, causing the computer to enter the JMP execute cycle.

The JMP execute process word 74 contains MBO, PCI, DONE, LI, CONT, and CMA10. MBO (1) and PCI (1) place the effective address bits MB05-17 in the PC. At the same time PCI (1) B and EXCY (1) trigger pulse amplifier W612-C21 to strobe the MB03-04 bits into the EPC.

Processes PCO (1) and MBI (1) in process word 10 (BGN) gate the PC contents into the MB for the start of the next fetch cycle. PCO (1) B also strobes the EMA jam input gates which now receive the new EPC information from the B169 AND/NOR gates. Thus the next fetch cycle takes its

instruction word from the newly activated memory bank at the address jammed into the MA from the MB. When the instruction is fetched, IRI (1) in the fetch cycle process word 12 resets the EXCY flip-flop. Thereafter the EPC remains set to the new bank designation as long as the program continues in that bank.

3.4.2 JMS I (Op Code 10)

With the extend mode enabled, a JMS I instruction fetched from the currently active bank may change the EPC contents and consequently activate another bank. During the JMS I fetch cycle, IR04 (1) is detected to cause the computer to go into a defer cycle. The defer cycle fetches the effective address word addressed by JMS I. The effective address word contains a 15-bit address, with MB03-04 designating the new memory bank to be accessed, and MB05-17 containing the address in that bank in which the current program count and status information is to be stored. A later JMP I to this address returns the program sequence to the currently active bank.

DEI (1) of the defer entry process word 31 sets the EXCY flip-flop, drawing KG2, while other processes gate the effective address word into the MB. DEI (1) also resets IR04 so that TI (1) in the next process word (24) detects JMS to force the computer into the IA0 cycle. During the defer cycle, MEM STROBE (B), DEI (1), and EXCY (1) produce EMA STROBE which jams the contents of MB03 and MB04 into EMA03 and EMA04, respectively.

The IA0 entry process word 32 gates the current program count and program status information into the AR as the core memory read half-cycle starts. During read the contents of the addressed location are ignored (lost), the MB contents are incremented by 1, then placed in the PC by a 1 → PCI signal evolved from process word 23. On drawing KG2 EXCY (1) and 1 → PCI strobe the MB03-04 bits into the EPC.

During write, the contents of the AR, containing the disrupted program count and status information, are stored in the addressed location by process word 62. The next process word is BGN (10), which gates the new address in the PC into the MB, while PCO (1) B and RUN (1) strobe the new EPC contents into the EMA. Thus the next fetch cycle addresses the newly-activated memory bank and the program continues from there.

3.4.3 CAL (Op Code 00)

With the extend mode enabled, a CAL instruction in the currently active bank traps to location 00020 in bank 0, storing the current program count and status information at that location and taking the next instruction from location 00021. A later DBR or EMIR and JMP I to 00020 returns the program sequence to the currently active bank.

During the third process word (24) of the CAL fetch cycle, CAL (1), TI (1), and EXD (1) are all present to produce TI·EXD·CAL at R111-D15N, drawing KG2. This level clears the EMA flip-flops. At CLK time a short time later, address 00020 is placed in the MB.

The decoded CAL (1) signal leads the computer into a subsequent IA0 cycle. The IA0 entry process word 32 gates the current program count and status information into the AR as the IA0 core memory read half-cycle starts. During read the contents of location 00020 are ignored (lost), the MB contents (address 00020) are incremented by 1, then placed in the PC by a 1 → PCI signal evolved from process word 23. On drawing KG2 this 1 → PCI signal in NANDed with CAL (1) and EXD (1) to clear the EPC flip-flops.

During memory write, the contents of the AR, containing the disrupted program count and status information, are stored in location 00020 by process word 60. The next process word is BGN (10) which gates address 00021 from the PC into the MB, with EMA and EPC remaining reset to address bank 0. The new program sequence continues from there.

With the extend mode disabled the operations are basically the same except the EMA and EPC are not cleared; the CAL instruction references location 00020 in the current memory bank.

3.5 AUTOINDEXING

An instruction word in the current memory bank which indirectly addresses an autoindex register (00010-17) traps to bank 0 regardless of extend mode status. During the third process word (24) of the fetch cycle, TI (1) detects IR04 (1) to force the computer into a defer cycle. At the same time, TI (1) and IR04 (1) detect bits MB05-17 to set the AUT INX flip-flop on drawing KC14. AUT INX (1) immediately clears the EMA flip-flop, drawing KG2. Thus the defer cycle will address bank 0.

During defer, the core memory read half-cycle reads out the effective address word from the autoindex location, the effective address word is incremented by 1, then placed in the MB. The write half-cycle writes the incremented address back into the autoindex location. The incremented address also remains in the MB for the upcoming execute or IA0 cycle.

During defer, if the extend mode is enabled, EMA STROBE occurs at MEM STROBE time to strobe the effective address bits MB03-04 into the EMA. If the extend mode is disabled, the EMA flip-flops remain cleared. In this case the upcoming execute or IA0 cycle remains in bank 0. The EPC retains the current bank designation in either case because of the absence of a strobing pulse at this time.

The subsequent process word in the defer cycle (24, 70, or 74) determines if the computer shall go into an execute cycle or into the special IA0 cycle as indicated by the op code in the IR. TI (1)$\wedge$IR04 (0) resets AUT INX during process word 24 or 70, and PCI (1) resets it during process word 74. The execute or IA0 cycle fetches the operand from the bank designated by the EMA, and the instruction is executed. The BGN process word (10) at the end of the cycle transfers the next sequential instruction address from the PC to the MB for the next fetch cycle. PCO (1) of the BGN word also gates the EPC bits into the EMA, so that the program returns to the currently active bank for the instruction fetch.

3.6 MEMORY PROTECTION VIOLATIONS

A protect violation forces the computer into a fetch cycle to fetch a JMS 20 or JMS 0 instruction, depending on the on/off status of the PI facility. During the JMS fetch, TI (1) of process word 24 turns on a PV0 EMA signal in conjunction with a PV level in the KX09A option. PV0 EMA clears the EMA flip-flops so that the subsequent IA0 cycle addresses bank 0 to store the current program count and program status information in location 00020 or 00000.

The 1 → PCI signal in process word 23 of the IA0 cycle produces PV0 EPC in the KX09A option. PV0 EPC occurs as address 00020 or 00000 is incremented by 1 and placed in the PC for the next computer fetch cycle. This signal clears the EPC so that the computer continues in bank 0 with a monitor program starting from location 00021 or 00001. Refer to the KX09A manual for details.

3.7 PI BREAKS

When a PI break is entered, the break entry word (11) places address 00000 in the MB, clears the IR for a pseudo CAL op code, and leads the computer into an IA0 cycle, as described in Section 3.8.1.7, PDP-9 Maintenance Manual.

EXT (1) of the break entry process word sets the BK flip-flop, drawing KD3 (2), gates IO ADDR 03, IO ADDR 04 onto the EPC, EMA jam input gates, and strobes the gates to clear the EMA (00 from IO ADDR 03-04). The EPC retains the current bank designation. The IA0 cycle will address bank 0 as designated by the cleared EMA.

BK (1) sets the PROG SYNC flip-flop. This places a negative PROG SYNC (1) B level at the DCD input gate to pulse amplifier R603-C18, drawing KG2. The IA0 cycle performs the pseudo CAL execution, storing the PC contents and program status information in location 00000 in bank 0.

An IO CLR pulse, 500 ns after IA0 entry, resets PROG SY, PROG SYNC, BK, and PIE, drawing KD3 (2). Reset PROG SYNC triggers the pulse amplifier R603-C18 to produce the IOT PWR CLR (B) V PICY pulse. This pulse clears (disables) the extend mode control flip-flops and the EPC, so that the program continues from 00001 in bank 0 at PCO (1) time of the BGN process word in the IA0 cycle.

At the conclusion of the PI break, an EMIR or DBR and JMP I sequence retrieves the stored program count and status information for a return to the current bank.

3.8 API BREAKS

When an API break is entered, the break entry process word (11) places the API channel address in the MB, clears the IR, and leads the computer into an XCT cycle, as described in the API option manual.

EXT (1) gates IO ADDR 03 and IO ADDR 04 onto the EPC and EMA jam input gates, and strobes the gates to clear the EMA (00 for IO ADDR 03-04). The EPC retains the current bank designation. The XCT cycle will address bank 0 as designated by the cleared EMA.

The XCT cycle fetches the instruction located in the API channel address. This instruction is either a JMS or a JMS I. For JMS the computer goes into an execute cycle to store the current program and status information at the addressed location in bank 0.

At DONE (1) time in the JMS execution, DONE (1) and 0 EPC LATCH generate PV0 EPC which clears the EPC and generates 0 → EPC UNLATCH. Thus at the BGN process word, PCO (1) B strobes the EPC bits into the EMA, so that the API service routine continues in bank 0 from the next sequential location after the JMS storage. 0 → EPC UNLATCH disables PV0 EPC.

These events occur regardless of the extend mode status. If the API channel location contains a JMS I instruction, the extend mode must be enabled so that the effective address obtained from bank 0 during the defer cycle can point to a storage location in any bank. Processor word (23) which produced 1 → PCI will generate the 0 → EPC UNLATCH pulse which loads MB03 and 04 into EPC. 0 → EPC UNLATCH prevents PV0 EPC from being generated at DONE (1) time. API service will now continue in the bank designated by the JMS I instruction. At the conclusion of the API break, JMP I retrieves the stored program count and status information for a return to the current bank.

3.9 DCH/RTC BREAKS

When a DCH/RTC break is entered, the break entry word (11) places the device's WC register address in the MB, clears the IR, and leads the computer into a WC cycle, as described in Section 3.8.2, PDP-9 Maintenance Manual.

EXT (1) of the break entry word gates IO ADDR 03, IO ADDR 04 (normally, both in the 0 state) onto the EPC, EMA jam input gates and strobes the gates to load the EMA flip-flops. The EPC retains the current bank designation. The WC cycle will address the bank designated by the EMA (bank 0).

The WC cycle fetches the word count in the WC register, increments both the word count and its reference address, checks for word count overflow, and steps the break counter to 10 (BK0 = 1, BK 1 = 0). The incremented address is stored in the AR and represents the address of the next sequential location in memory bank 0. This location is the current address register (CA) which is initialized to the address -1 of the data transfer location. The CA register is referenced during the CA cycle to increment its contents and to place them in the MB.

An RTC break, of course, ends with the WC cycle, in which case the last process word is BGN (10). PCO (1) B from BGN strobes the current bank designation into the EMA from the EPC, and the program thus returns to the currently active bank for the next fetch cycle.

For DCH breaks, the CA cycle steps the break counter to 11 (BK0 = 1, BK1 = 1). On drawing KC10 (1), BK1 (1) B and ARI (1) of process word 13 produce BK CA as the device data is transferred from the I/O bus to the AR (for input data operations), or as 0s are placed in the AR (for output data operations).

BK CA occurs while the CA register contents are in the MB. BK CA strobes MB03-04 into the EMA so that the subsequent input/output data cycle accesses the designated memory bank.

The last process word in the data cycle(s) is BGN, during which PCO (1) B strobes the EMA with the EPC bits to return the program to the currently active bank.

3.10 DMA BREAKS

A DMA break does make use of the memory extension control. When the DMA channel steals a memory cycle, the control logic in the DMA multiplexer option issues its own AM EMA bits to each memory bank for bank selection in conjunction with the MODE flip-flop in the memory control circuits. Refer to the DM09A option manual for details.

CHAPTER 4
MAINTENANCE

4.1 GENERAL MAINTENANCE

The general maintenance practices described in the PDP-9 Maintenance Manual also apply to the KG09B and MM09A/B/C options.

4.2 TEST PROGRAMS

The KG09B and MM09A/B/C options can be tested using MAINDEC-9A-D1CC-PH, MAINDEC-9A-D1FA-PH, and MAINDEC-9A-D1DA-LA-PH respectively under marginal check conditions of +10 ±4V and -15 ±2.5V. Refer to the associated program documents.

4.3 MODULE REPLACEMENT

Tables 4-1 and 4-2 list the full complement of logic modules comprising the KG09B and one MM09 option respectively. The spare modules kit SP09A offered by DEC as a replacement stock level for the entire PDP-9 system provides at least one spare of all module types used in the KG09B and MM09 options. It is recommended that the user maintain this minimum stock level to avoid equipment down-time due to repair of faulty modules.

Table 4-1
Module Complement, KG09B

DEC Type	Module Type	Quantity
B169	AND/NOR Gate	1
B213	Dual Flip-Flop	2
B310	Delay	1
G795	Level Terminator	2
G796	Level Terminator	2
R002	Diode Network	3
R111	NAND/NOR Gate	9
R603	Pulse Amplifier	1
S107	Inverter	2
S205	Dual Flip-Flop	2
W005	Clamped Load	1
W103	Device Selector	1
W612	Pulse Amplifier	3

Table 4-2
Module Complement, MM09

DEC Type	Module Type	Quantity
B104	Inverter	5
B105	Inverter	5
B169	AND/NOR Gate	15
B213	Dual Flip-Flop	14
B310	Delay	2
B360	Delay	5
B602	Pulse Amplifier	1
G008	Master Slice Control	1
G009	Sense Amplifier	18
G010	Sense Amplifier Selector	2
G219	Address Selector	44
G622	Resistor Board	8
G795	Level Terminator	3*
G796	Level Terminator	2**
G804	Power Control	1
G805	Power Regulator	4
R002	Diode Network	1
R111	NAND/NOR Gate	3
S107	Inverter	1
W005	Clamped Load	1
W612	Pulse Amplifier	14

*Including 2 for last MM09 in use.

**If parity option not installed.

CHAPTER 5
ENGINEERING DRAWINGS

This chapter contains a set of KG09B, MM09A/B/C, and ME09B engineering drawings along with circuit schematics of all logic modules used in the KG09B. DEC engineering drawings are encoded as to drawing type, major assembly, and series. These drawing number codes are explained in Chapter 5 of the PDP-9 Maintenance Manual.

5.1 DRAWING LIST

Below is a list of all drawings included in this chapter. Other related drawings are included in the Chapter 5 drawings of the PDP-9 Maintenance Manual, as part of the prewired, basic system.

Memory Extension Control KG09B

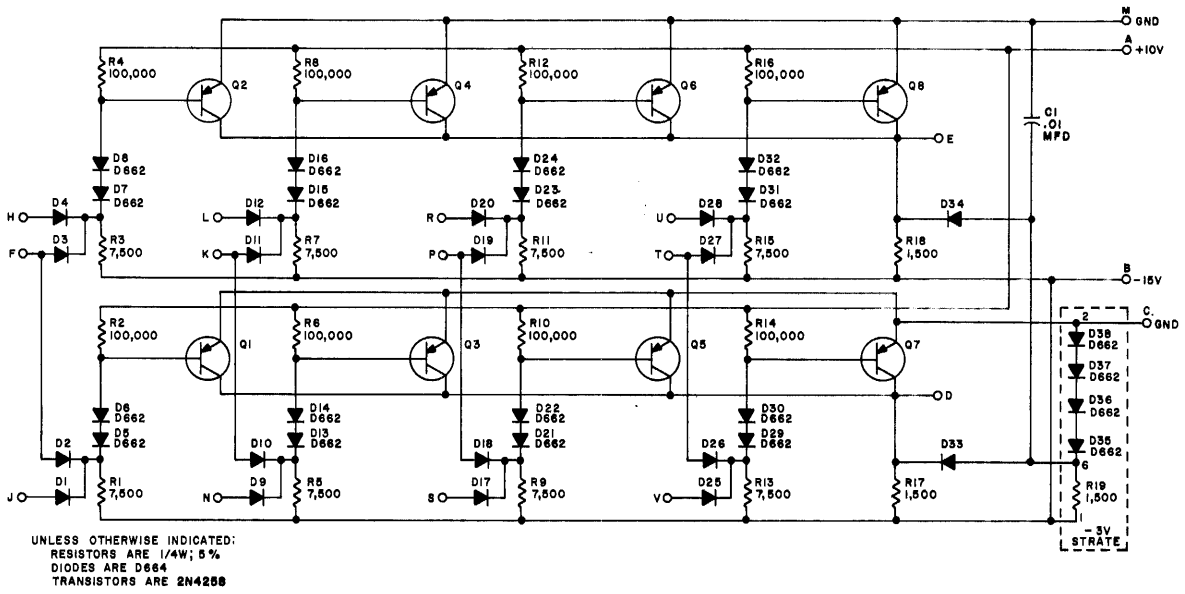
Drawing Number	Title	Revision	Page
B-CS-B169-0-1	AND/NOR Gate B169, Circuit Schematic	C	5-3
B-CS-B213-0-1	Flip-Flop B213, Circuit Schematic	F	5-3
B-CS-B310-0-1	Delay B310, Circuit Schematic	B	5-4
B-CS-G795-0-1	Level Terminator G795, Circuit Schematic	A	5-4
B-CS-R002-0-1	Diode Network R002, Circuit Schematic	A	5-5
B-CS-R111-0-1	NAND/NOR Gate R111, Circuit Schematic	F	5-5
B-CS-R603	Pulse Amplifier R603, Circuit Schematic	6	5-6
B-CS-S107-0-1	Inverter S107, Circuit Schematic	D	5-6
B-CS-S205-0-1	Flip-Flop S205, Circuit Schematic	D	5-7
B-CS-W005-0-1	Clamped Load W005, Circuit Schematic	B	5-7
C-CS-W103-0-1	Device Selector W103, Circuit Schematic	D	5-8
B-CS-W612-0-1	Pulse Amplifier W612, Circuit Schematic	D	5-9
D-BD-KG09-B-1	Extended Memory Control, Block Diagram	-	5-11
D-BS-KG09-B-2	Extended Memory Control, Block Schematic	A	5-13
D-IC-KG09-B-3	Cable Connections	-	5-15
D-IC-KG09-B-4	IO Interface	-	5-17
D-MU-KG09-B-5	Module Utilization	-	5-19
A-PL-KG09-B-5	Parts List	-	5-21
D-IC-KG09-B-6	Cable Diagram	A	5-23

Extended Memory Modules MM09A/MM09B/MM09C

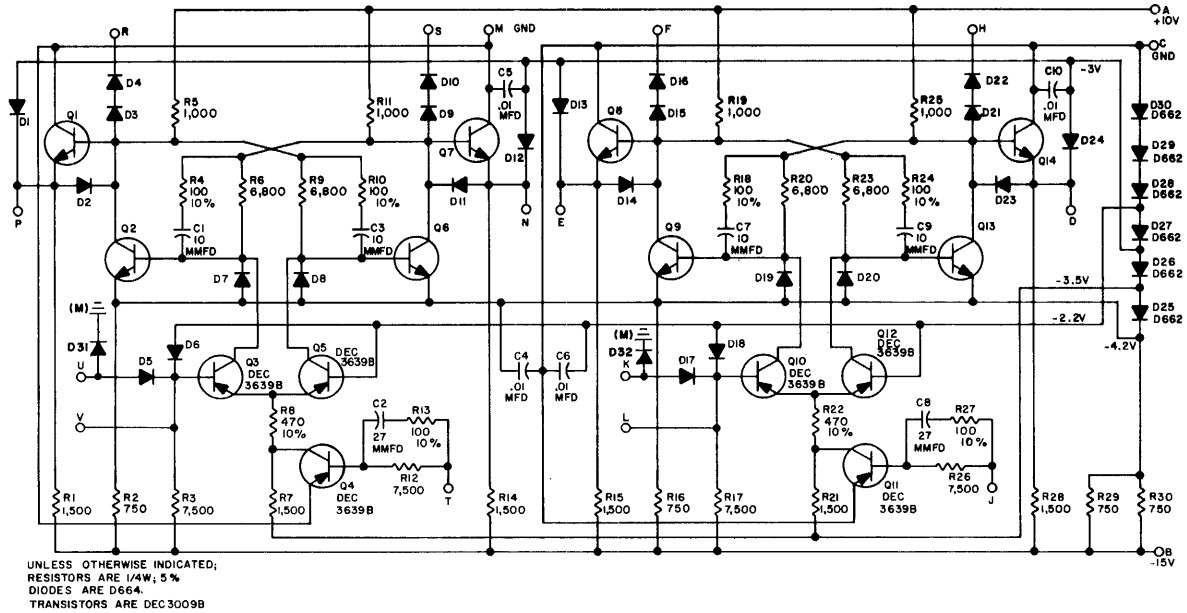
Drawing Number	Title	Revision	Page
B-CS-783-0-1	Power Supply 783, Circuit Schematic	C	5-25
C-CS-G796-0-1	Level Terminator G796, Circuit Schematic	A	5-26
C-UA-MM09-A-0	Unit Assembly	-	5-27
A-PL-MM09-A-0	Parts List	-	5-28
D-IC-MM09-A-1	Power Wiring	-	5-29
D-IC-MM09-A-2	Cable Diagram	A	5-31
C-UA-MM09-B-0	Unit Assembly	-	5-33
A-PL-MM09-B-0	Parts List	-	5-34
C-UA-MM09-C-0	Unit Assembly	-	5-35
A-PL-MM09-C-0	Parts List	-	5-36
MC70-B-0 through MC70-B-20	Memory Module Logic Drawings (included in Chapter 5, PDP-9 Maintenance Manual)		

Memory Parity, Protection, and Extension Chassis ME09B

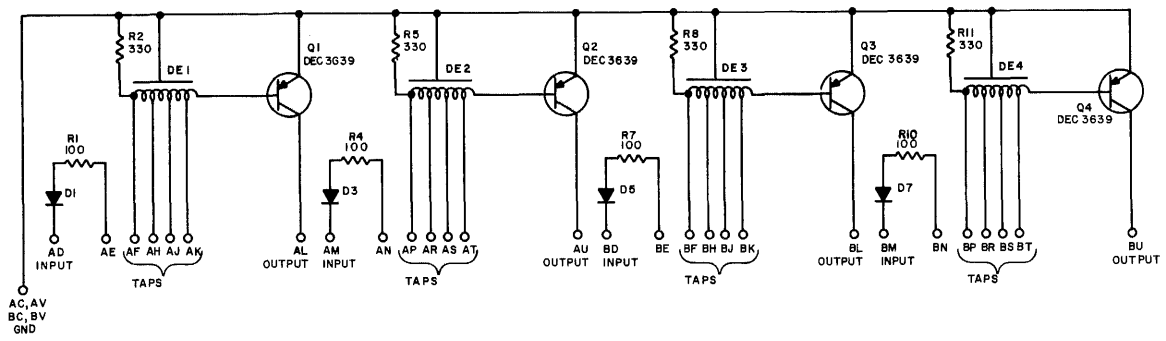
D-UA-ME09-B-0	Unit Assembly	A	5-37
A-PL-ME09-B-0	Parts List	A	5-39
A-WL-ME09-B-1	Wiring List	C	5-40
D-IC-ME09-B-2	Power Wiring	-	5-41
A-CP-ME09-B-3	External Components List (Sheet 1)	D	5-43
A-CP-ME09-B-3	External Components List (Sheet 2)	D	5-44
D-AD-7005684-0-0	Assembly Drawing	-	5-45
A-PL-7005684-0-0	Assembly Parts List	-	5-47



B-CS-B169-0-1 AND/NOR Gate B169,
Circuit Schematic

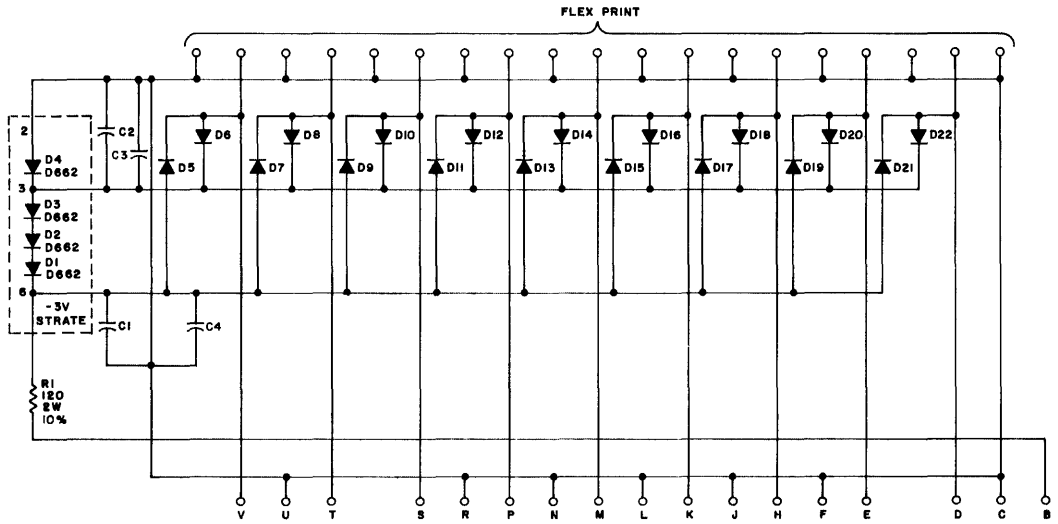


B-CS-B213-0-1 Flip-Flop B213, Circuit Schematic



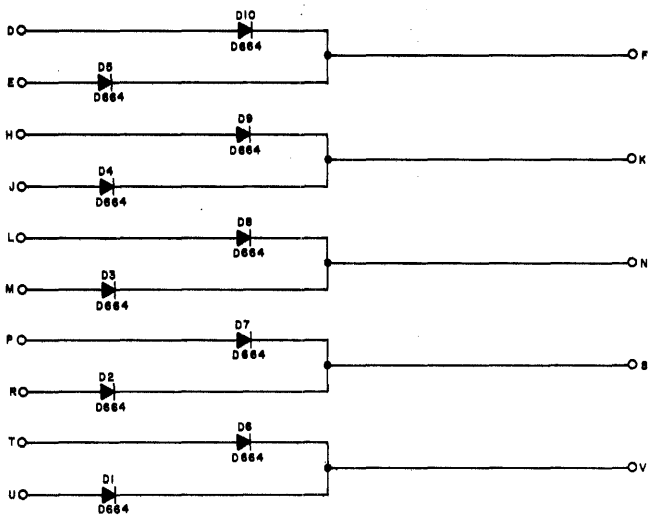
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
DIODES ARE D-664
DE1 - DE4 ARE TECHNITROL, .05 usec,
330 Ω TAPS AT .0125 usec, DD-330-5-1, 6012

B-CS-B310-0-1 Delay B310, Circuit Schematic

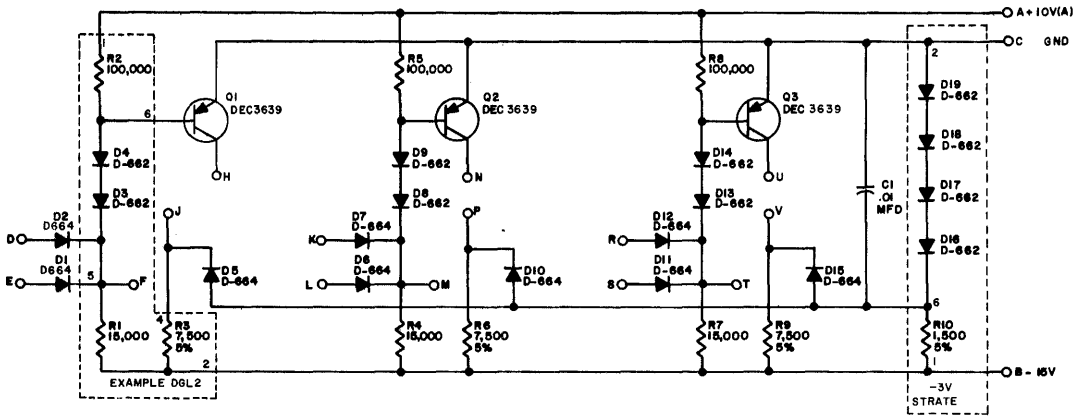


UNLESS OTHERWISE INDICATED:
DIODES ARE D664
CAPACITORS ARE .01 MFD, 50V

B-CS-G795-0-1 Level Terminator G795,
Circuit Schematic



B-CS-R002-0-1 Diode Network R002,
Circuit Schematic



UNLESS OTHERWISE INDICATED:
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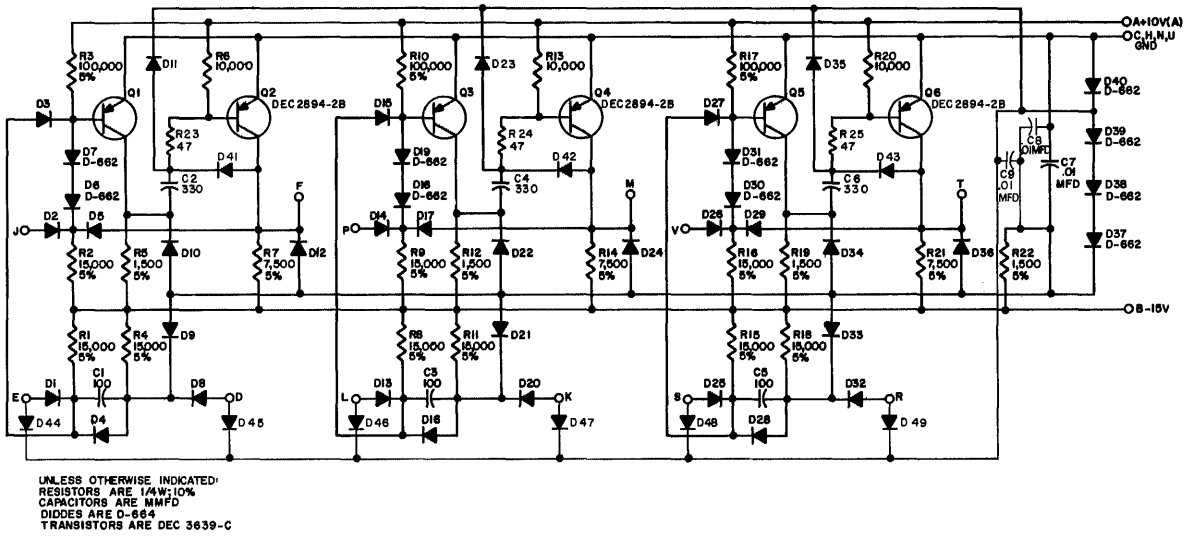
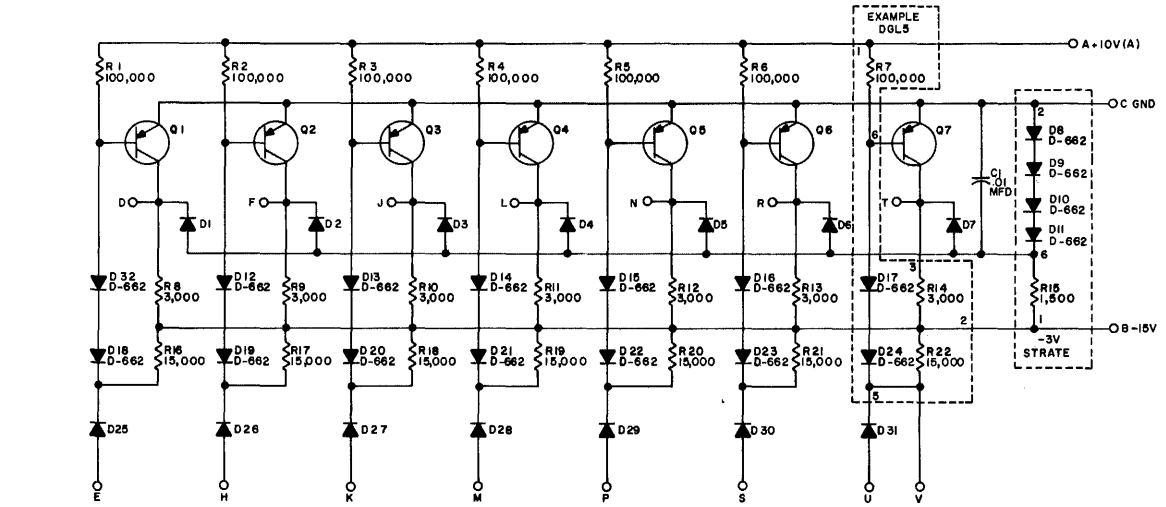
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

B-CS-R111-0-1 NAND/NOR Gate R111,
Circuit Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-C

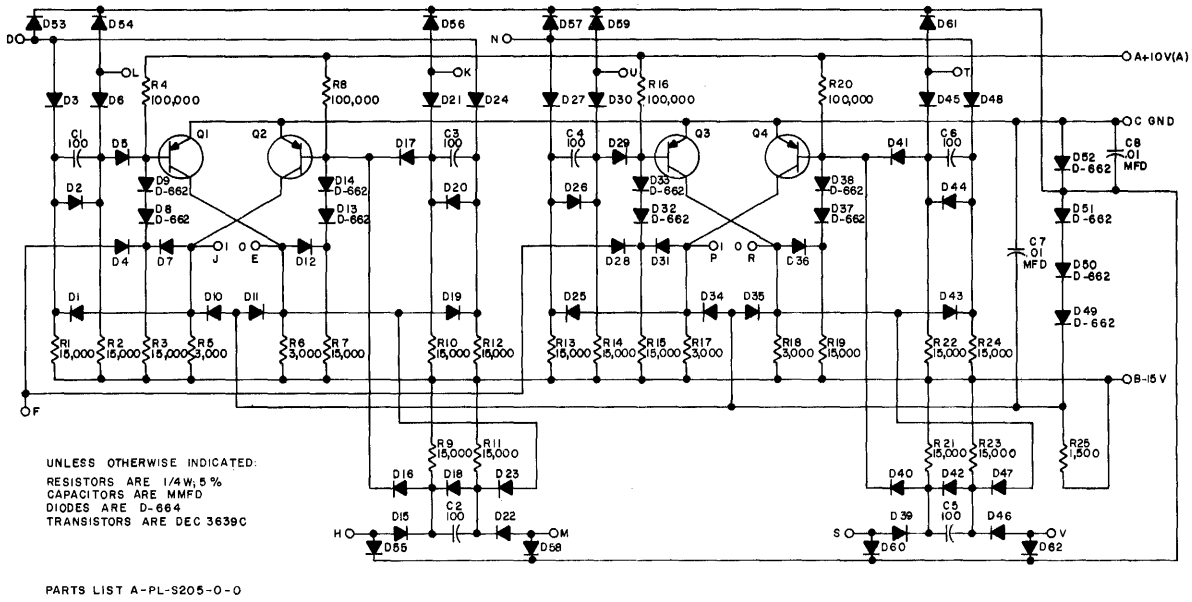
B-CS-R603 Pulse Amplifier R603,
Circuit Schematic



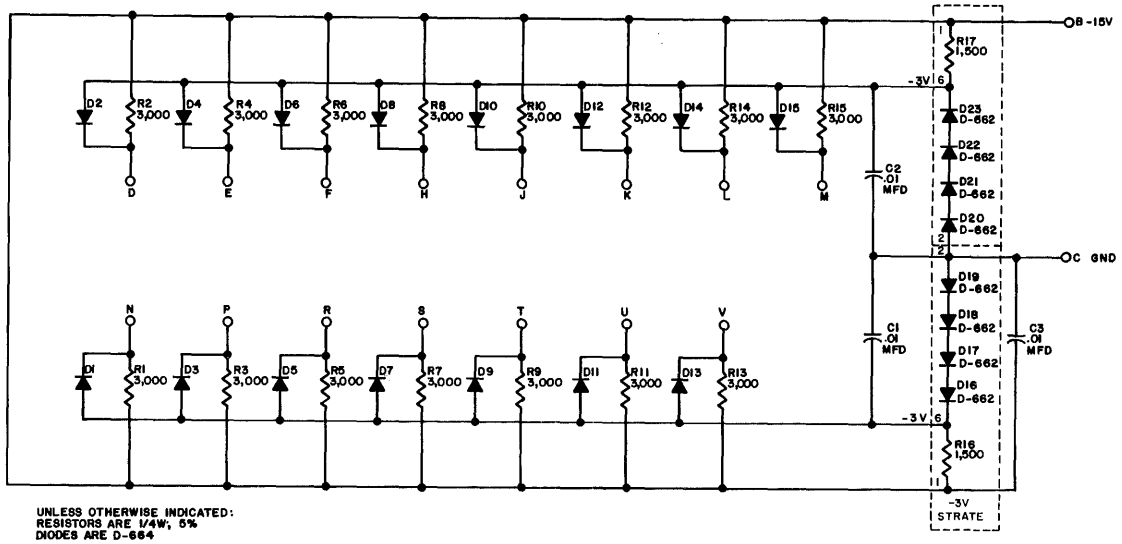
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS S1A

PARTS LIST A-PL-S107-0-0

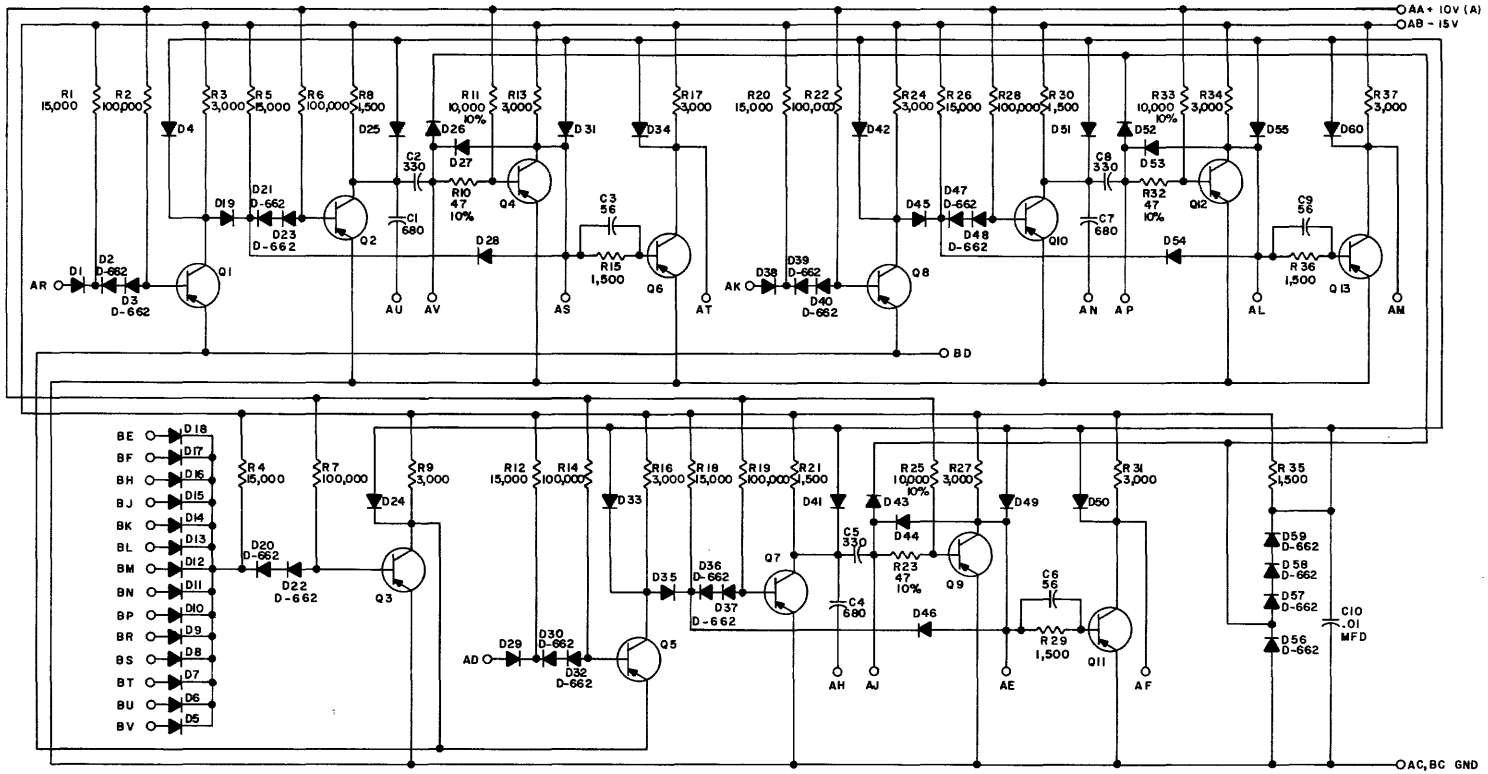
B-CS-S107-0-1 Inverter S107, Circuit Schematic



B-CS-S205-0-1 Flip-Flop S205, Circuit Schematic



B-CS-W005-0-1 Clamped Load W005,
Circuit Schematic



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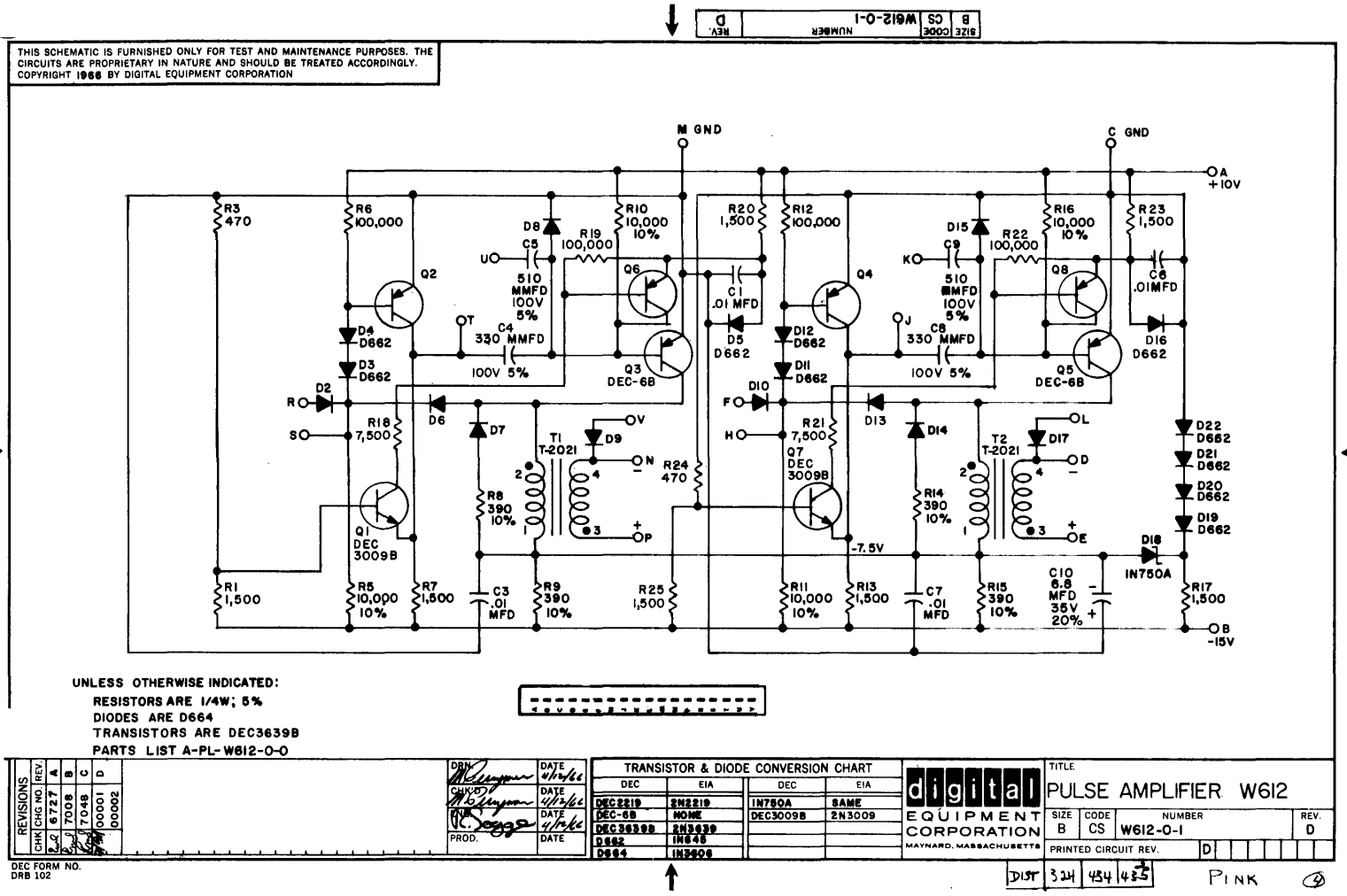
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

C-CS-W103-0-1 Device Selector W103,
Circuit Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664
TRANSISTORS ARE DEC3639B
PARTS LIST A-PL-W612-0-0

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2219	2N2219	IN750A	SAME
DEC-6B	NONE	DEC3009B	2N3009
DEC3639B	2N3639		
D662	IN646		
D664	IN3604		

REVISIONS				
REV.	A	B	C	D
CHG NO.	6727	7008	7048	00001
CHK				00002

DRN. DATE 4/17/66
CHK'D DATE 4/17/66
ENG. DATE 4/17/66
PROD. DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PULSE AMPLIFIER W612

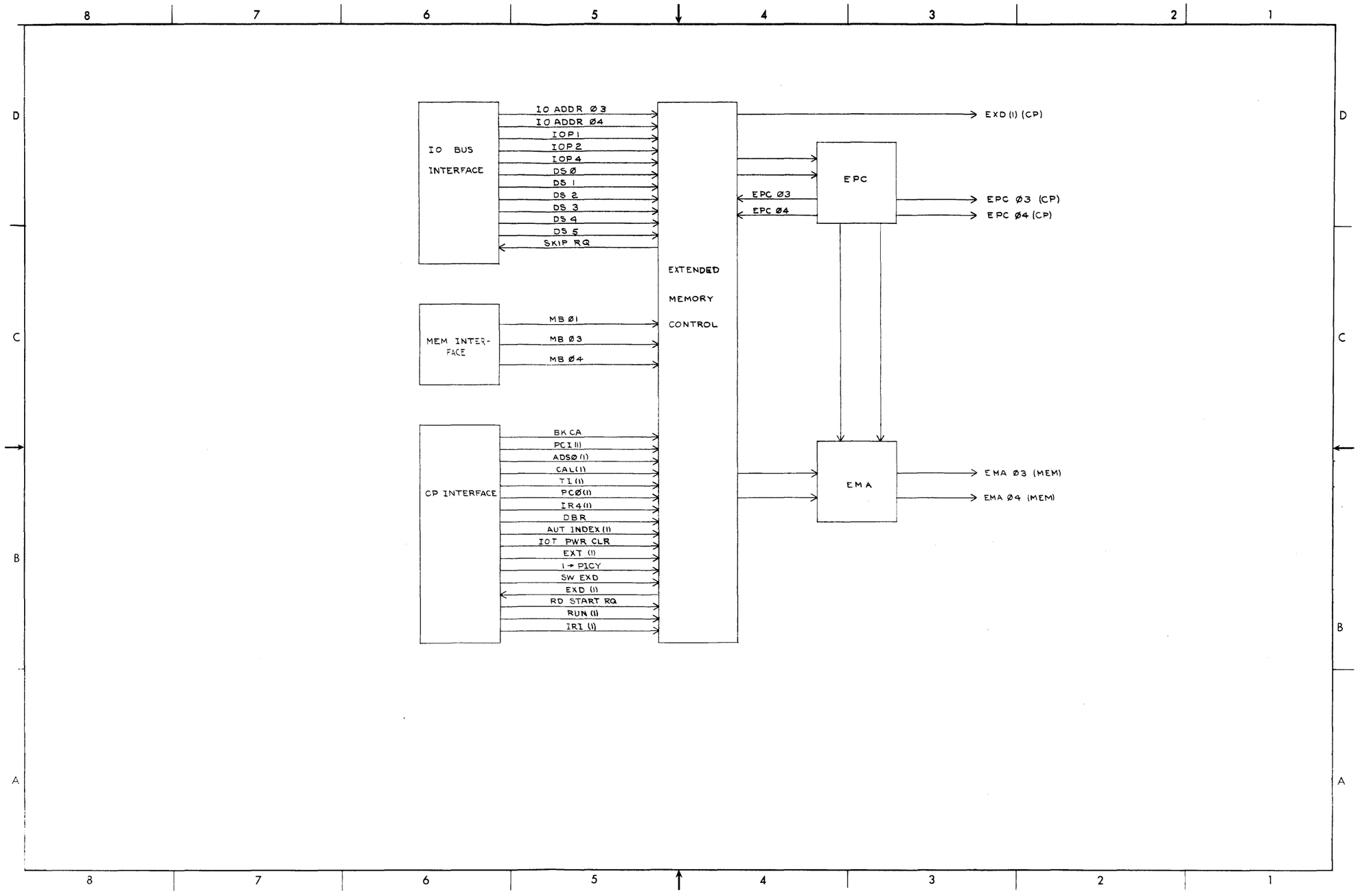
SIZE	CODE	NUMBER	REV.
B	CS	W612-0-1	D

PRINTED CIRCUIT REV. D

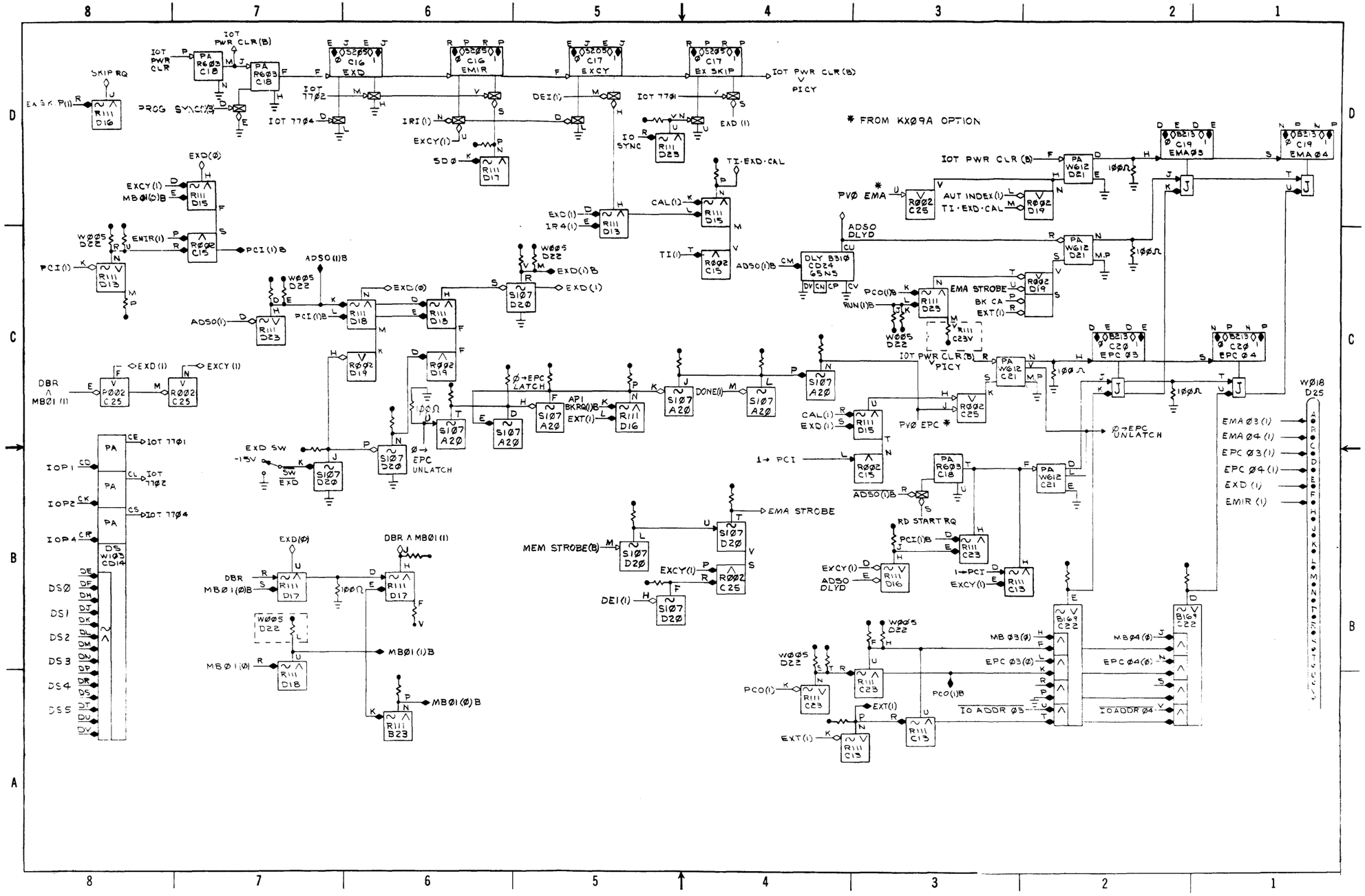
DEC FORM NO. DRB 102

DIST 324 454 435 PINK 4

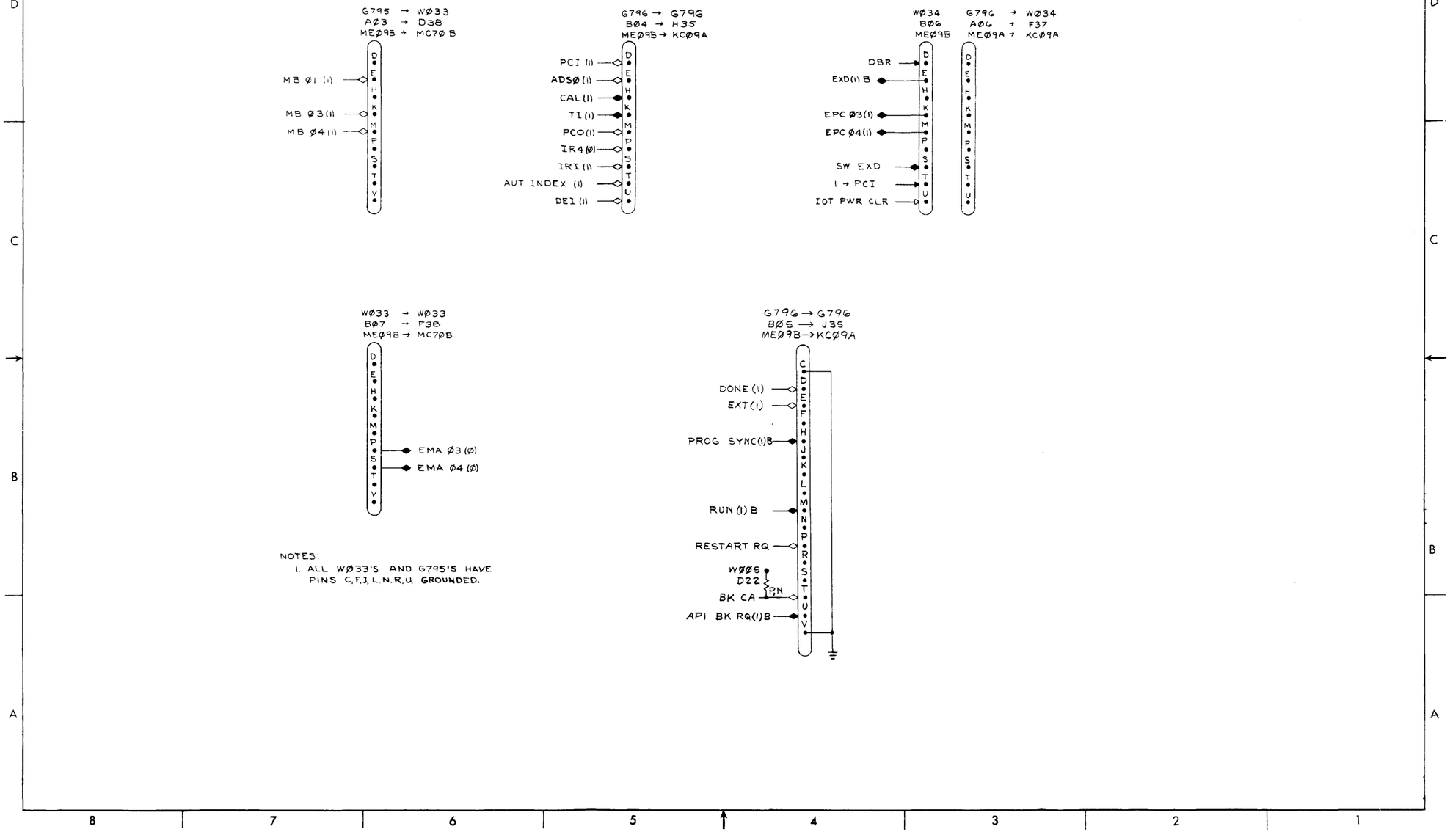
B-CS-W612-0-1 Pulse Amplifier W612,
Circuit Schematic



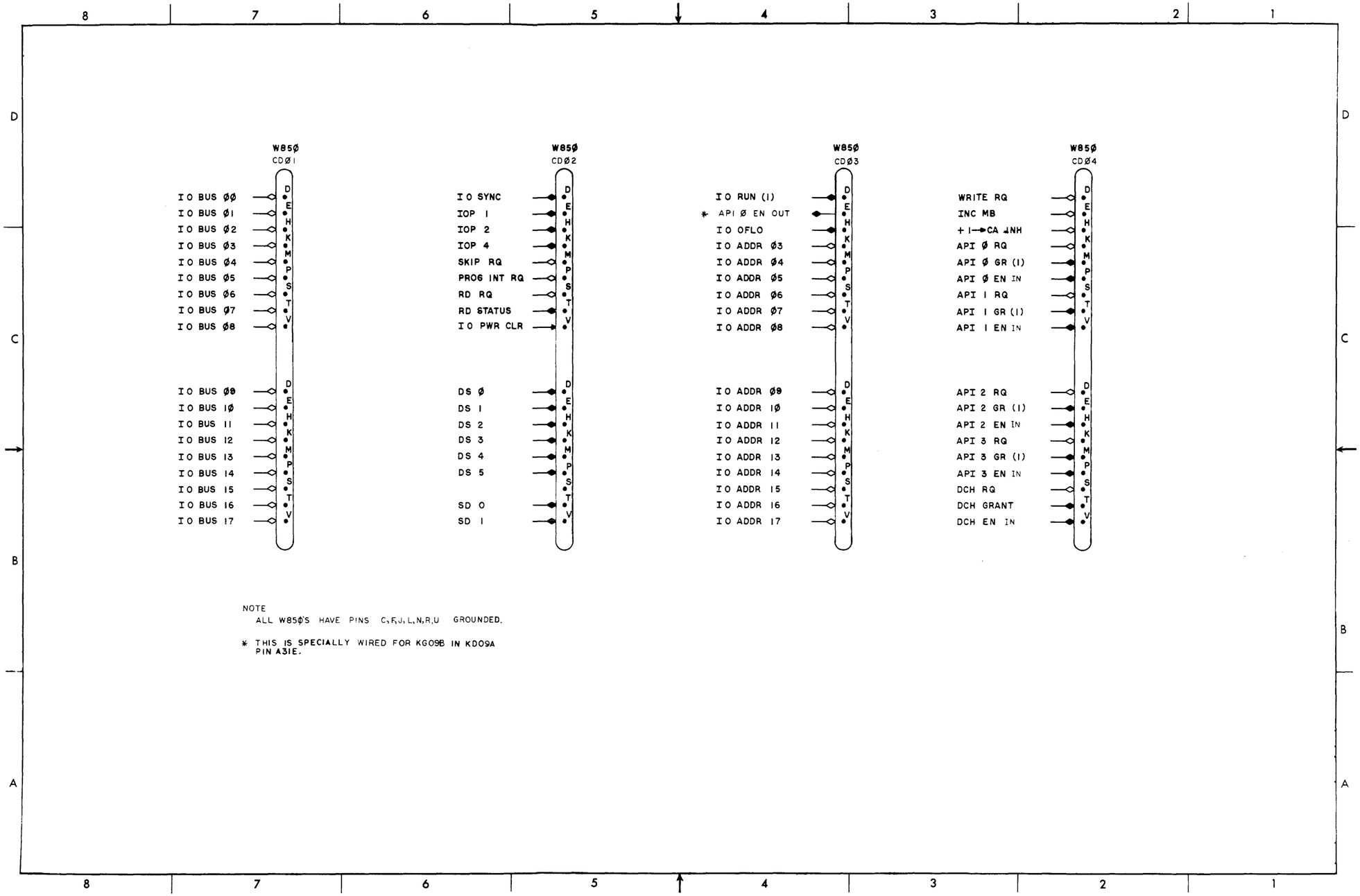
D-BD-KG09-B-1 Extended Memory Control, Block Diagram



D-BS-KG09-B-2 Extended Memory Control, Block Schematic



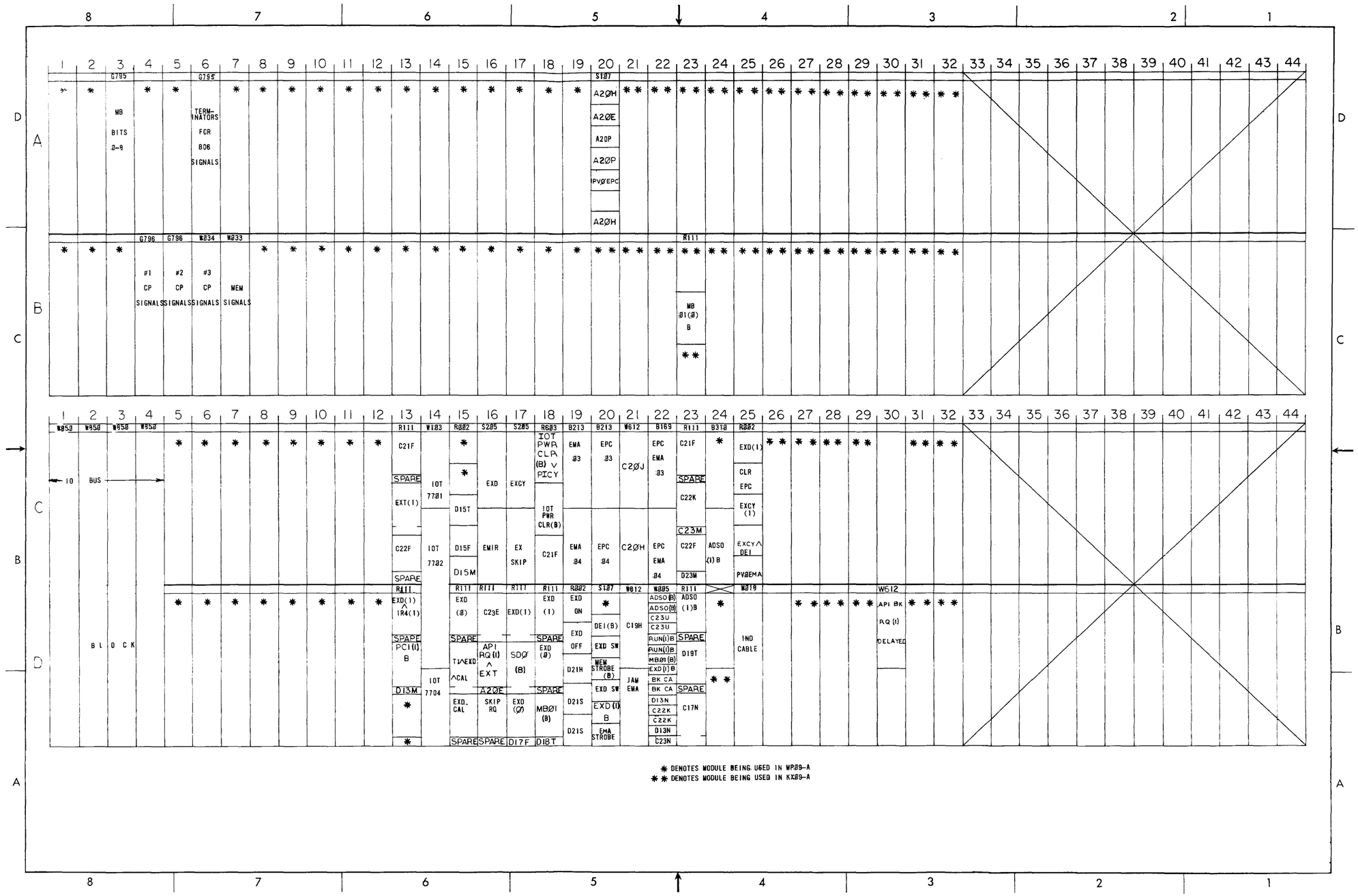
NOTES:
1. ALL WØ33'S AND G795'S HAVE PINS C, F, J, L, N, R, U, GROUNDED.



NOTE
ALL W85Ø'S HAVE PINS C,F,J,L,N,R,U GROUNDED.

* THIS IS SPECIALLY WIRED FOR KG09B IN KD09A PIN A31E.

D-IC-KG09-B-4 IO Interface

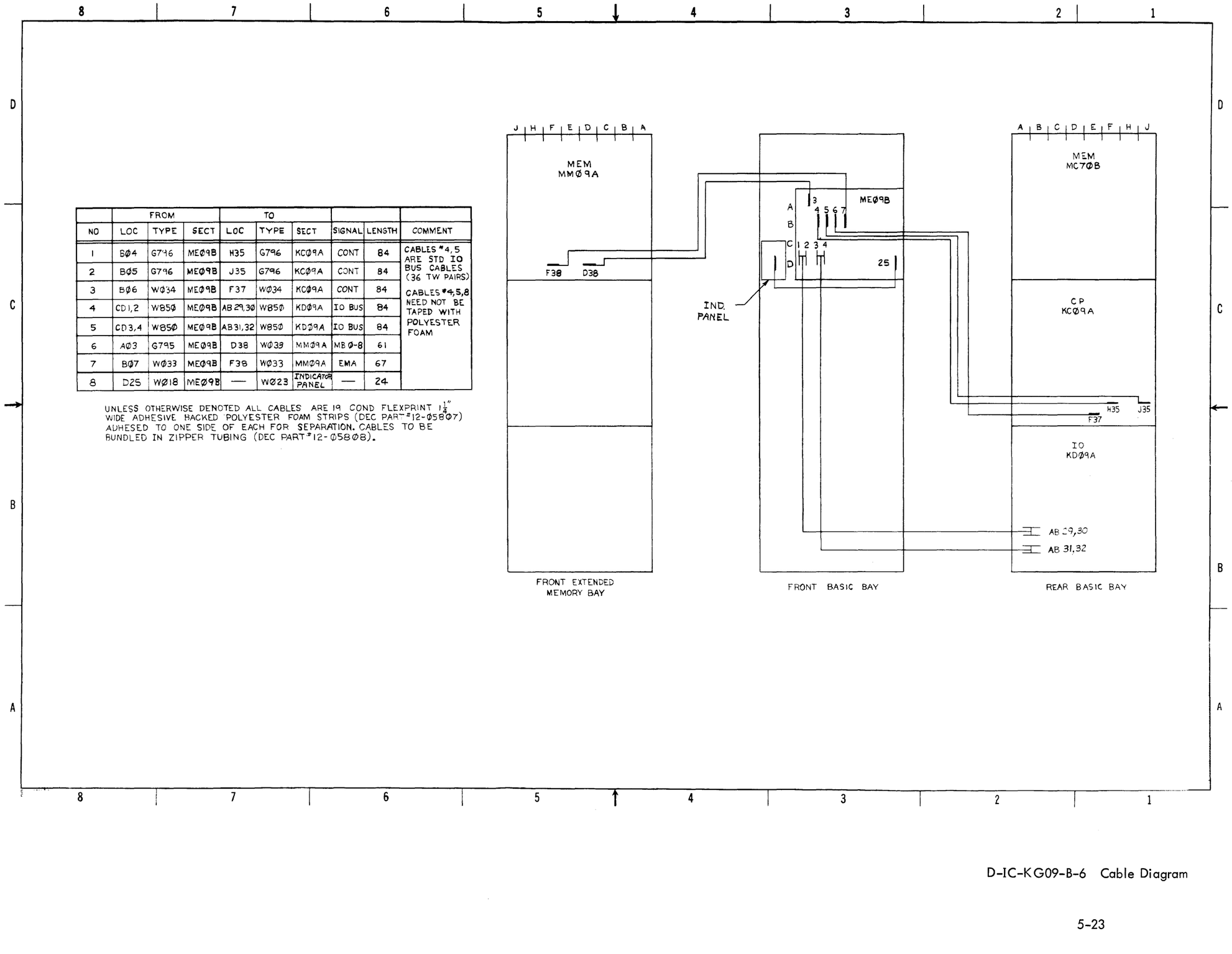

G795
G795
MB BITS Ø-9
TERM-INATORS FOR BØ6 SIGNALS
S1Ø7
A2ØH
A2ØE
A2ØP
A2ØP
PVØEPC
A2ØH
G796
G796
W834
W833
#1 CP SIGNALS
#2 CP SIGNALS
#3 CP SIGNALS
MEM SIGNALS
R111
MB Ø1(Ø) B
W85Ø
W85Ø
W85Ø
W85Ø
IO BUS
BLOCK
R111
C21F
SPARE
EXT(1)
C22F
SPARE
R111
EXD(1) ^ IR4(1)
SPARE
PCI(1) B
D13M
W1Ø3
IOT 7701
IOT 7702
IOT 7704
R1Ø2
D15T
D15F
D15M
R111
EXD (Ø)
SPARE
TIMEXD
^CAL
EXD. CAL
SPARE
S2Ø5
EXD
EMIR
C23E
SPARE
SKIP RQ
S2Ø5
EXCY
EX SKIP
EXD(1)
SDØ (B)
EXD (Ø)
SPARE
D17F
R6Ø3
IOT PWR CLR (B) V PICY
IOT PWR CLR(B)
C21F
R111
EXD (1)
SPARE
EXD (Ø)
MBØ1 (B)
SPARE
D18T
B213
EMA Ø3
EMA Ø4
EMA
D21H
D21S
D21S
B213
EPC Ø3
EPC Ø4
EPC
S1Ø7
DEI(B)
EXD SW
MEM STROBE (B)
EXD SW
EXD (1) B
EMA STROBE
W612
C2ØJ
C2ØH
C19H
JAM EMA
B169
EPC EMA Ø3
EPC EMA Ø4
EPC EMA Ø4
D23M
W885
ADSO(B)
ADSO(B)
C23U
C23U
RUN(1)B
RUN(1)B
MBØ1(B)
EXD(1)B
BK CA
BK CA
DI3N
C22K
C22K
DI3N
C23N
R111
C21F
SPARE
C22K
C23M
C22F
SPARE
D19T
C17N
B31Ø
ADSO (1)B
ADSO (1)B
R1Ø2
EXD(1)
CLR
EPC
EXCY (1)
EXCY ^ DEI
PVØEMA
W819
IND CABLE
W612
API BK RQ (1) DELAYED
* DENOTES MODULE BEING USED IN WPØ9-A
** DENOTES MODULE BEING USED IN KXØ9-A

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
		1	W005 CLAMPED LOAD	
		9	R111 DIODE GATE	
		1	W103 DEVICE SELECTOR	
		3	R002 DIODE CLUSTER	
		2	S205 DUAL FLIP-FLOP	
		1	R603 PULSE AMP.	
		2	B213 FLIP-FLOP	
		3	W612 PULSE AMP.	
		1	B169 INVERTER	
		1	B310 DELAY LINE	
		2	S107 INVERTER	
		15	G795 CLAMPED CABLE CONN	

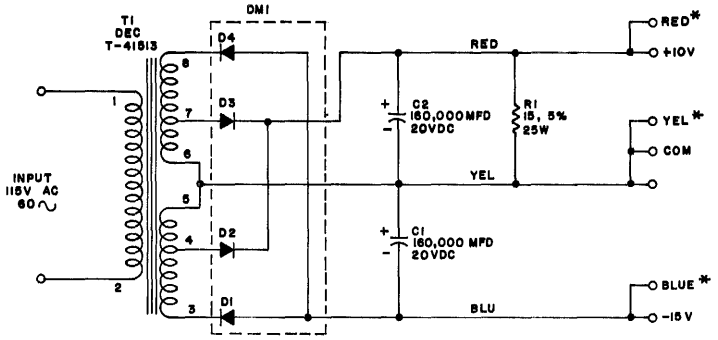
A-PL-KG09-B-5 Parts List

NO	FROM LOC	FROM TYPE	FROM SECT	TO LOC	TO TYPE	TO SECT	SIGNAL	LENGTH	COMMENT
1	BØ4	G796	MEØ9B	H35	G796	KCØ9A	CONT	84	CABLES #4,5 ARE STD IO BUS CABLES (36 TW PAIRS)
2	BØ5	G796	MEØ9B	J35	G796	KCØ9A	CONT	84	
3	BØ6	WØ34	MEØ9B	F37	WØ34	KCØ9A	CONT	84	CABLES #4,5,8 NEED NOT BE TAPED WITH POLYESTER FOAM
4	CD1,2	W85Ø	MEØ9B	AB29,3Ø	W85Ø	KDØ9A	IO BUS	84	
5	CD3,4	W85Ø	MEØ9B	AB31,32	W85Ø	KDØ9A	IO BUS	84	
6	AØ3	G795	MEØ9B	D38	WØ33	MMØ9A	MB Ø-8	61	
7	BØ7	WØ33	MEØ9B	F38	WØ33	MMØ9A	EMA	67	
8	D25	WØ18	MEØ9B	—	WØ23	INDICATOR PANEL	—	24	

UNLESS OTHERWISE DENOTED ALL CABLES ARE 19 COND FLEXPRINT $1\frac{1}{4}$" WIDE ADHESIVE BACKED POLYESTER FOAM STRIPS (DEC PART #12-Ø58Ø7) ADHESED TO ONE SIDE OF EACH FOR SEPARATION. CABLES TO BE BUNDLED IN ZIPPER TUBING (DEC PART #12-Ø58Ø8).



D-IC-KG09-B-6 Cable Diagram



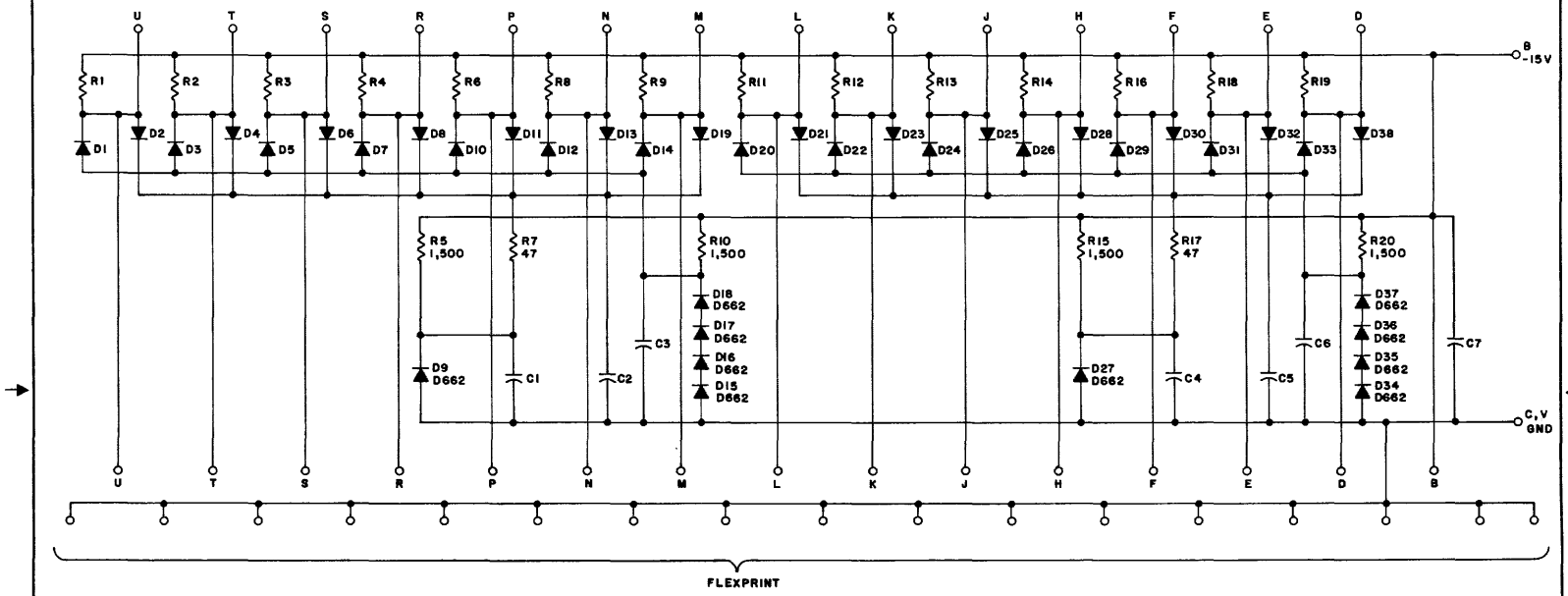
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16 V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 6.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 6.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE EQUATION: $5I_{10}+6I_{15} \leq 53$

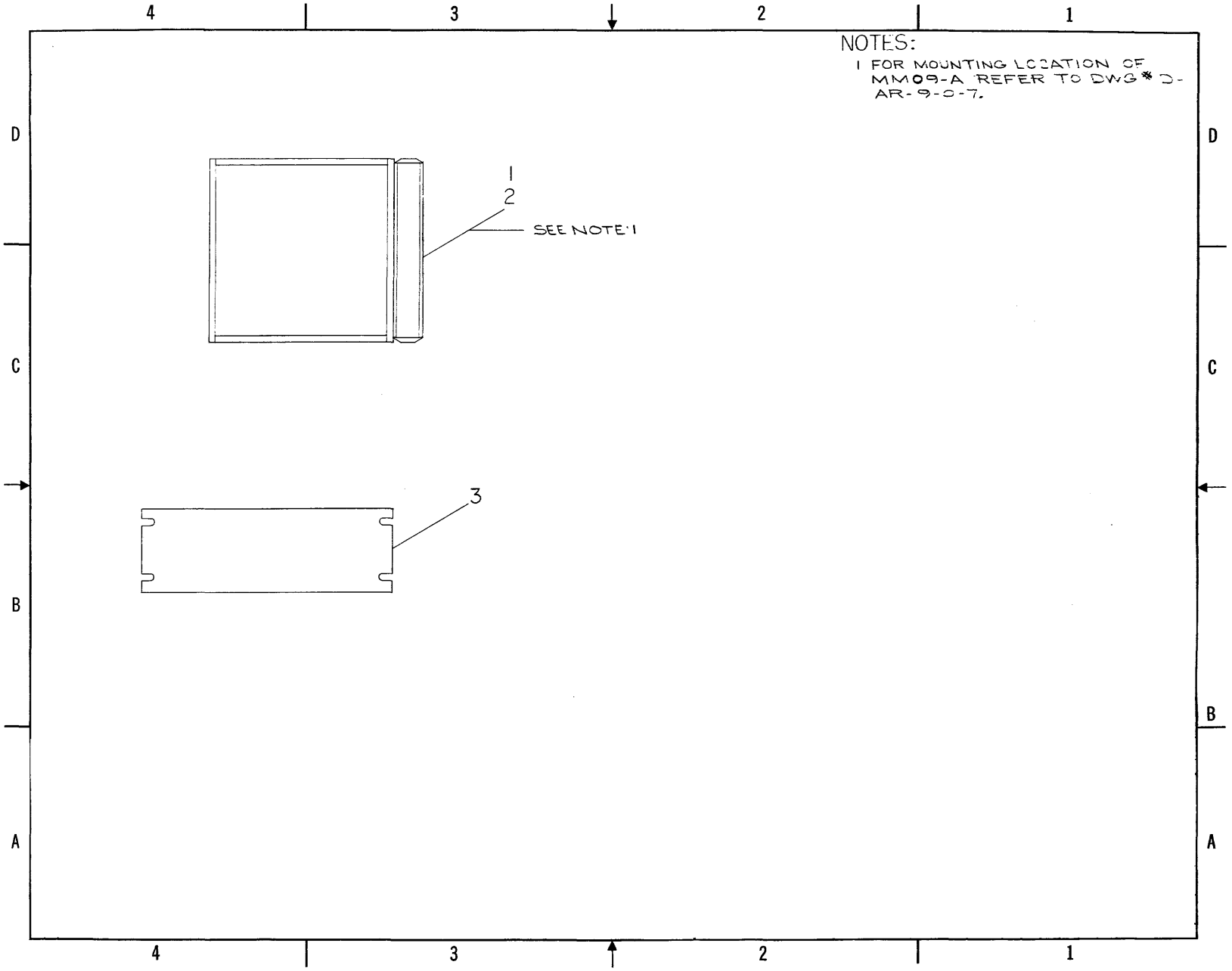
* HEYMAN MFG. CO. TAB TERMINALS

B-CS-783-0-1 Power Supply 783,
Circuit Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
RESISTORS ARE 7,500
CAPACITORS ARE .01 MFD
DIODES ARE D664

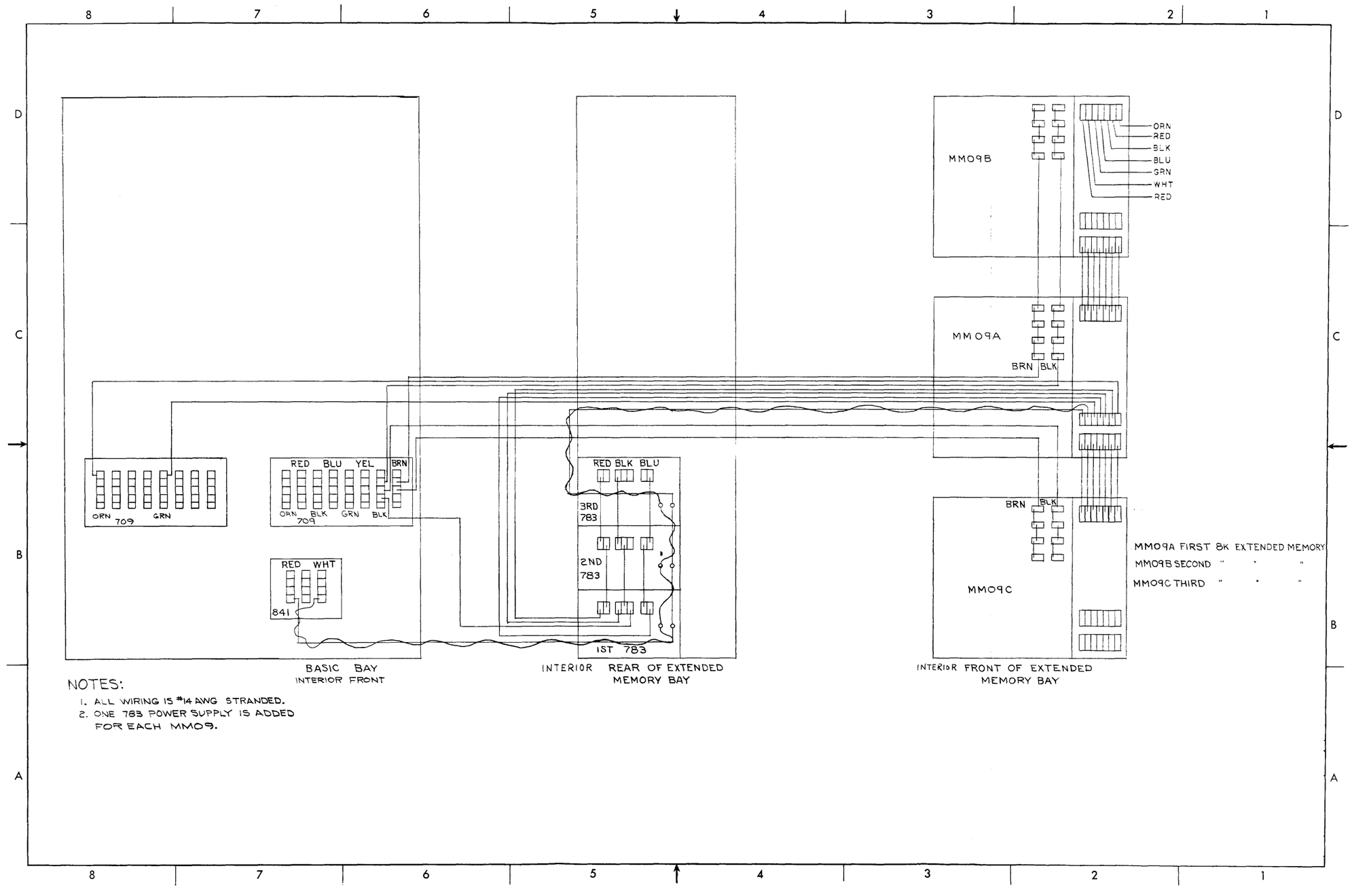
C-CS-G796-0-1 Level Terminator G796,
Circuit Schematic



C-UA-MM09-A-0 Unit Assembly

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
1	A-PL-MC70-B-0	1	MC70-B MEMORY UNIT	
2	A-PL-7005450-0-0	1	CABLE SET MM09-A	
3	A-PL-783-0-1	1	783 POWER SUPPLY	

A-PL-MM09-A-0 Parts List



D-IC-MM09-A-1 Power Wiring

16K (MM09A)

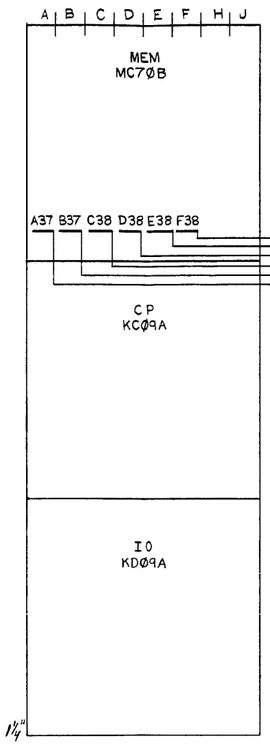
NO.	FROM LOC	FROM TYPE	FROM SECT.	TO LOC	TO TYPE	TO SECT.	SIGNAL	LENGTH IN.	COMMENT
1	C38	WØ33	MC7ØB	C4Ø	WØ33	MMØ9A	CONT	75"	
2	D38			D4Ø			MB Ø-8	81"	
3	E38			E4Ø			MB 9-17	86"	
4	F38			F4Ø			CONT	91"	
5	A37	↓	↓	A4Ø	↓	↓	SA Ø-8	64"	
6	B37	WØ33	MC7ØB	B4Ø	WØ33	MMØ9A	SA 9-17	7Ø"	

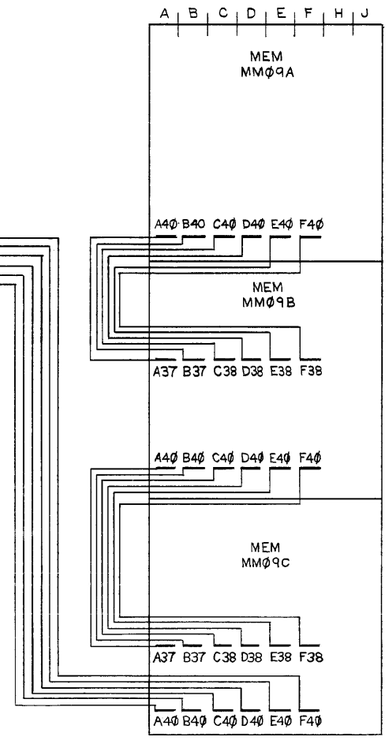
24K(MMØ9A + MMØ9B)

NO.	FROM LOC	FROM TYPE	FROM SECT.	TO LOC	TO TYPE	TO SECT	SIGNAL	LNS. LENGTH IN.	COMMENT
1	C38	WØ33	MC70B	C4Ø	WØ33	MMØ9B	CONT	75"	
2	D38			D4Ø			MB Ø-8	81"	
3	E38			E4Ø			MB 9-17	86"	
4	F38			F4Ø			CONT	91"	
5	A37		↓	A4Ø		↓	SA Ø-8	64"	
6	B37		MC7ØB	B4Ø		MMØ9B	SA 9-17	7Ø"	
7	C38		MMØ9B	C4Ø		MMØ9A	CONT	33"	
8	D38			D4Ø			MB Ø-8	38½"	
9	E38			E4Ø			MB 9-17	44"	
1Ø	F38			F4Ø			CONT	5Ø"	
11	A37	↓	↓	A4Ø	↓	↓	SA Ø-8	21½"	
12	B37	WØ33	MMØ9B	B4Ø	WØ33	MMØ9A	SA 9-17	27"	

NOTES:

1. UNLESS OTHERWISE DENOTED ALL CABLES ARE 19 COND FLEXPRINT WITH 1¼" ADHESIVE BACKED POLYESTER FOAM STRIPS (DEC PART #12-05807) ADHESED TO ONE SIDE OF EACH CABLE FOR SEPARATION. CABLES TO BE BUNDLED IN ZIPPER TUBING (DEC PART #12-05808).
2. MEM STROBE MUST BE TERMINATED WITH A 150Ω FROM E32L TO E32C IN THE MMØ9A ONLY.
3. WHEN THE MEMORY PARITY (MPØ9A) IS NOT USED A37 AND B37 OF THE MMØ9A REQUIRE A G797.

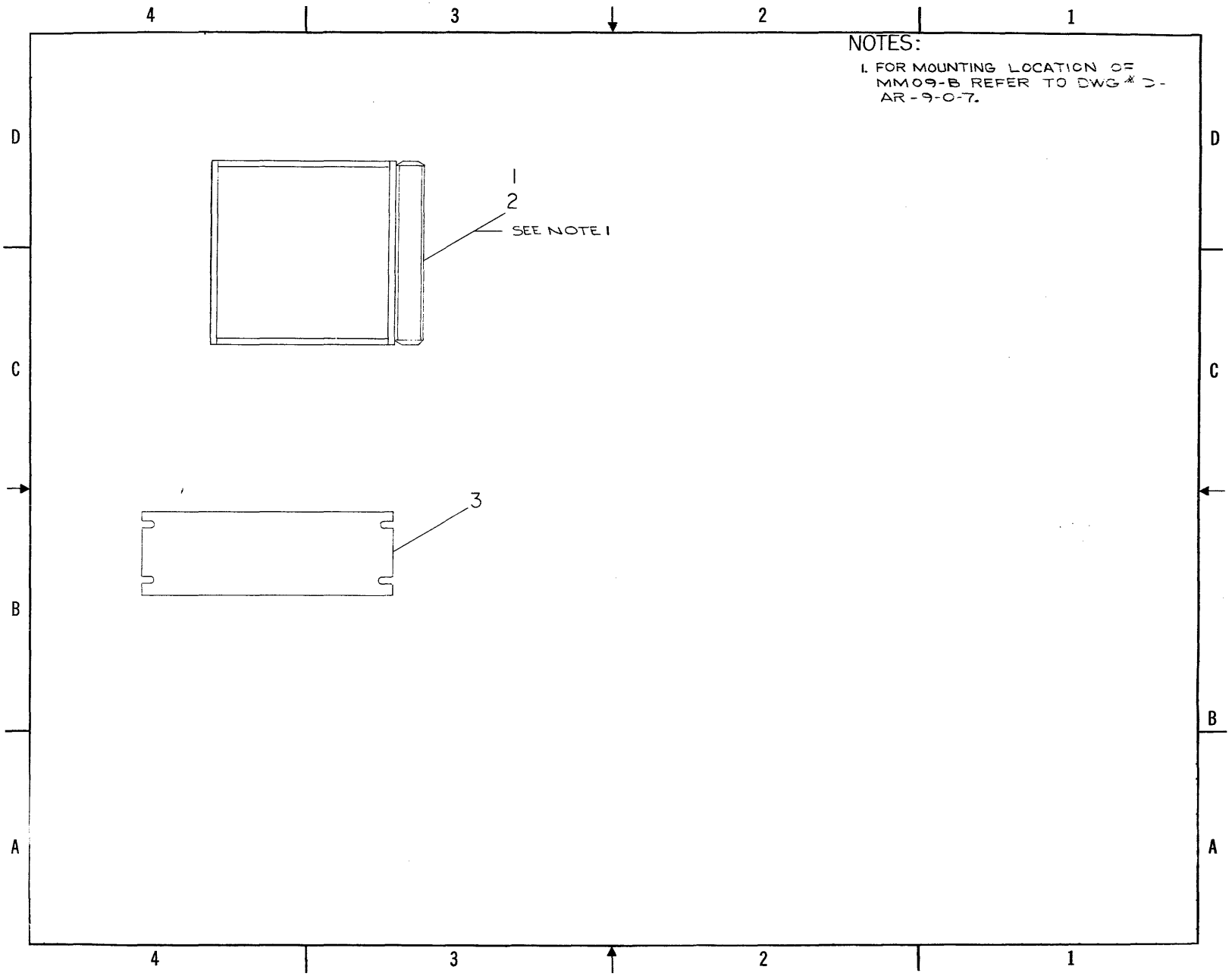




32K (MMØ9A + MMØ9B + MMØ9C)

NO.	FROM LOC	FROM TYPE	FROM SECT.	TO LOC	TO TYPE	TO SECT.	SIGNAL	LNS LENGTH	COMMENT
1	C38	WØ33	MC7ØB	C4Ø	WØ33	MMØ9C	CONT	75	
2	D38			D4Ø			MBØ-8	81	
3	E38			E4Ø			MB 9-17	86	
4	F38			F4Ø			CONT	91	
5	A37		↓	A4Ø		↓	SAØ-8	64	
6	B37		MC7ØB	B4Ø		MMØ9C	SA 9-17	7Ø	
7	C38		MMØ9C	C4Ø		MMØ9B	CONT	33	
8	D38			D4Ø			MB Ø-8	38½	
9	E38			E4Ø			MB 9-17	44	
1Ø	F38			F4Ø			CONT	50	
11	A37		↓	A4Ø		↓	SAØ-8	21½	
12	B37		MMØ9C	B4Ø		MMØ9B	SA 9-17	27	
13	C38		MMØ9B	C4Ø		MMØ9A	CONT	33	
14	D38			D4Ø			MBØ-8	38½	
15	E38			E4Ø			MB 9-17	44	
16	F38			F4Ø			CONT	5Ø	
17	A37	↓	↓	A4Ø	↓	↓	SAØ-8	21½	
18	B37	WØ33	MMØ9B	B4Ø	WØ33	MMØ9A	SA 9-17	27	

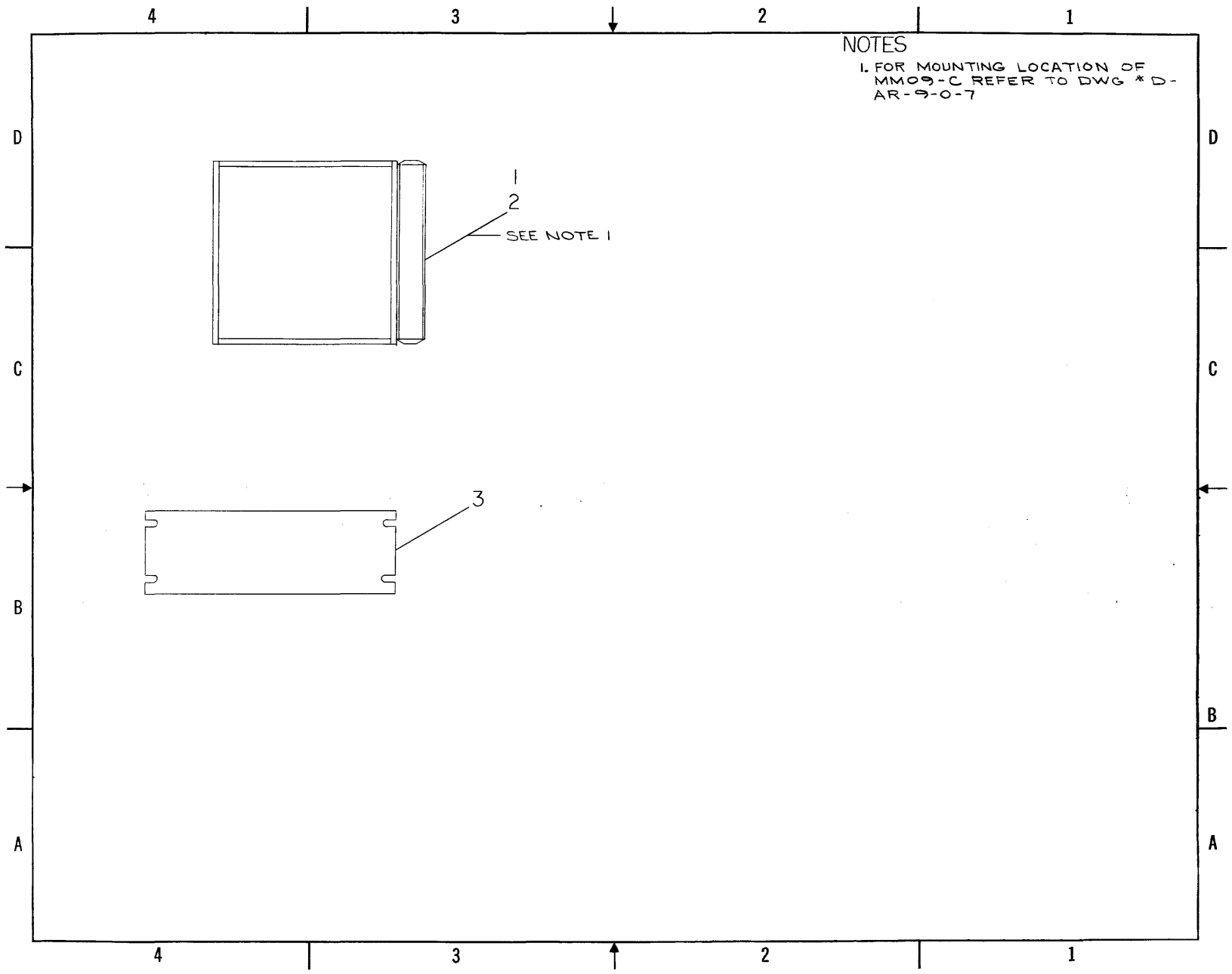
D-IC-MM09-A-2 Cable Diagram



C-UA-MM09-B-0 Unit Assembly

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
1	A-PL-MC70-B-0	1	MC70-B MEMORY UNIT	
2	A-PL-7005451-0-0	1	CABLE SET MM09-B	
3	A-PL-783-0-1	1	783 POWER SUPPLY	

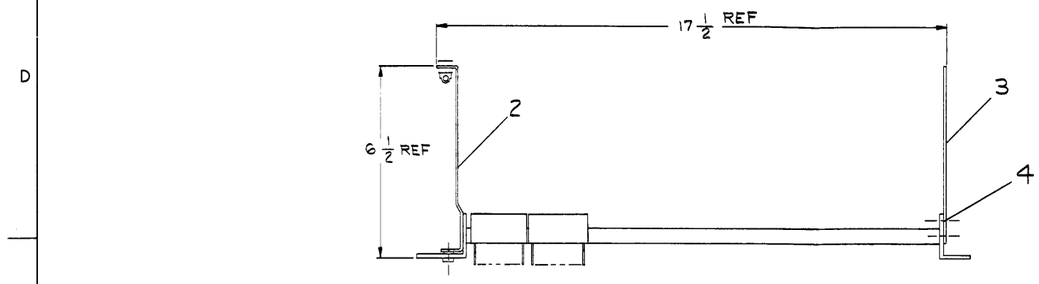
A-PL-MM09-B-0 Parts List

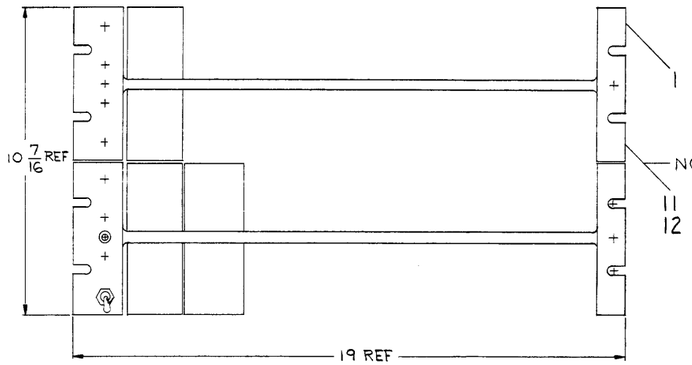


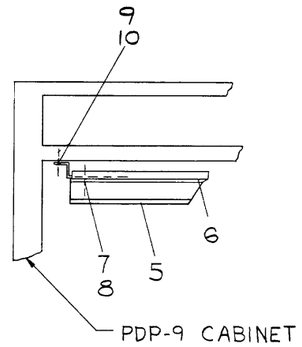
C-UA-MM09-C-0 Unit Assembly

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
1	A-PL-MC70-B-0	1	MC70-B MEMORY UNIT	
2	A-PL-7005452-0-0	1	CABLE SET MM09-C	
3	A-PL-783-0-1	1	783 POWER SUPPLY	

A-PL-MM09-C-0 Parts List







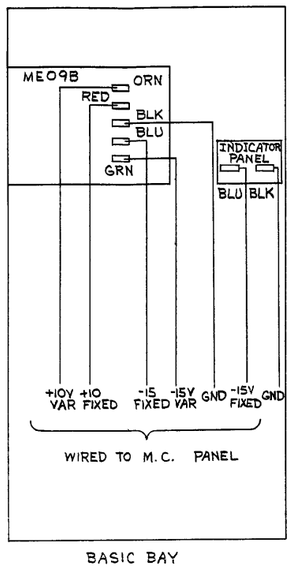
D-UA-ME09-B-0 Unit Assembly

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
1	D-AD-7005684-0-0	1	WIRED ASS'Y ME09-B	7005864
2	C-IA-5402526-0-0	2	MARGINAL CHECKING PANEL	5402526
3	C-MD-5302486-0-0	2	RIGHT END PANEL	5302486
4		8	POP RIVET 1/8D #AD43ABS U.S.M.C.	90-06509
5	C-MD-7405633-0-0	1	CABLE DUCT #1	7405633
6	D-MD-7405327-0-0	1	CABLE HOLD DOWN BRACKET	7405327
7		2	SCR PHL HD PAN #8-32 x 1/2 SST	9006039-1
8		2	NUT KEPS #8-32 SST	90-06563
9		2	SCR PHL HD TRUSS #10-32 x 3/4 SST	9006075-1
10		2	WASH EXT TOOTH #10	90-06635
11	D-AD-7005320-0-0	1	INDICATOR PANEL ASS'Y ME09B	7005320
12	B-AD-7005449-0-0	1	CABLE SET	7005449

A-PL-ME09-B-0 Parts List

REVISIONS			
REV LTR	ECO NO	DATE	ENG
A	167	12-21-67	
B	186	1-26-68	
C	209	3-15-68	

A-WL-ME09-B-1 Wiring List



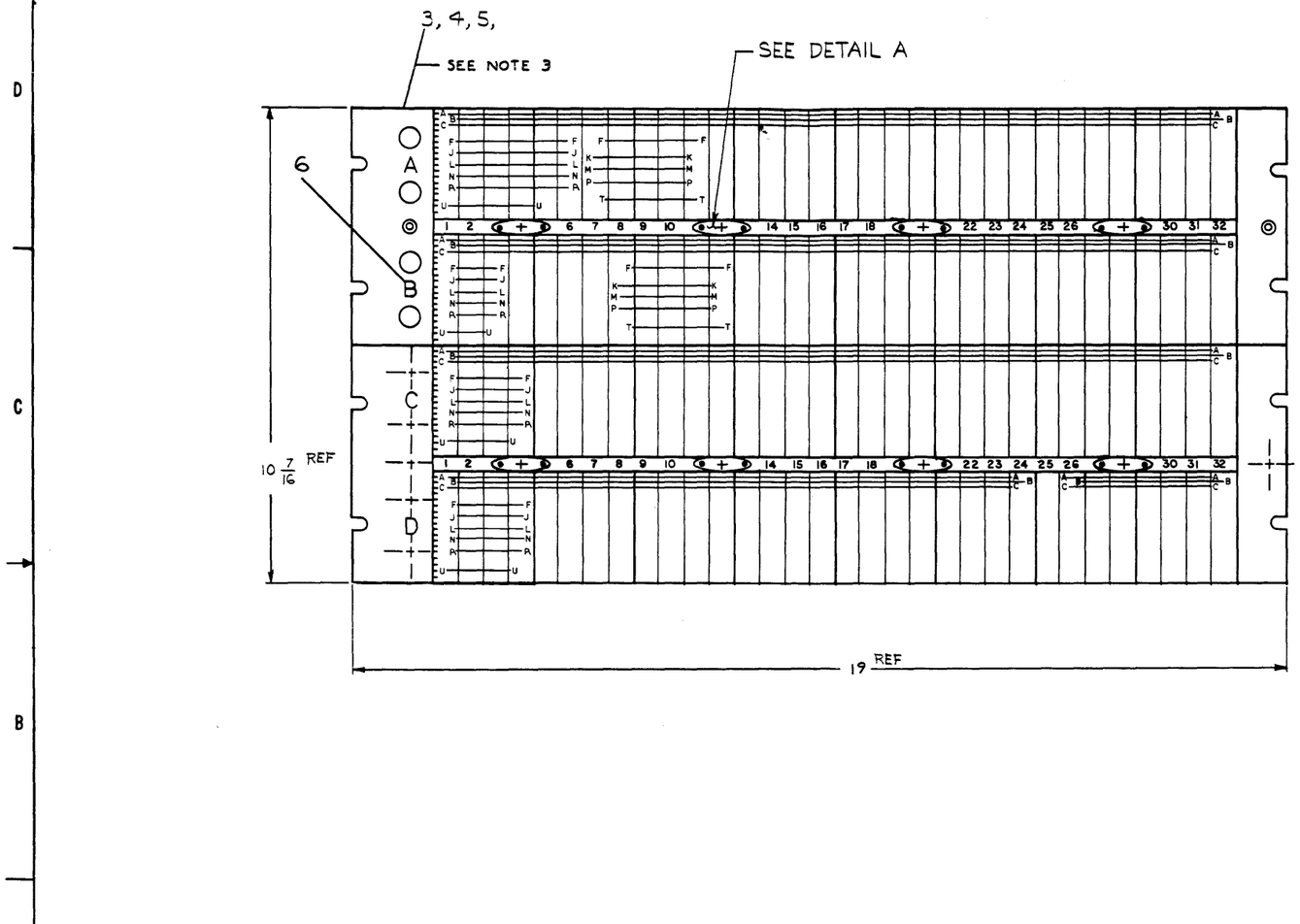
NOTES:

1. BASIC BAY POWER WIRING IS AWG #14 STRANDED.

D-IC-ME09-B-2 Power Wiring

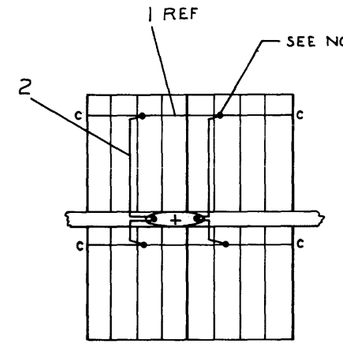
COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
	MP09-C				
RES (CLKD)	1KOHM ¼W±10%		B05R	B05A	
RES (IO PWR CLR MEM DONE)	100 OHM ¼W±10%		C07F	C07M	
RES (STROBE READ PARITY)			C07T	D07C	
(IO PWR CLR (B))			D11T	D11C	
(WRITE DATA EN)			C08H	C08C	
(READ DATA EN)			C08F	C08M	
(SA18)			C07U	C06C	
(STR WR PAR)			B19J	B19C	
(CLKD)			D32R	D32C	
(MA JAM PAR)	47 OHM		J38T	J38M	
WIRE (INDICATORS)	JUMPER *		D24C	D25H	
			D25H	D25J	
			D25J	D25K	
			D25K	D25L	
PARITY MEM DONE	100 OHM		D2ØE	D2ØC	
	KG09-B				
RES(Ø→EPC UNLATCH)	100 OHM		A2ØU	A2ØC	
RES (CLR EMA)	100 OHM ¼W±10%		C19H	C19M	
(CLR EPC)			C20H	C20M	
(JAM EMA)			C19J	C19C	
(JAM EPC)			C20J	C20C	
(DBR)			D32K	D31C	
WIRE (INDICATORS)	JUMPER *		D26C	D25A	
			D25A	D25B	
			D25B	D25C	

A-CP-ME09-B-3 External Components List
(Sheet 1)



NOTES:

1. CONNECTIONS ON ITEMS #1 & #2 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
3. USE YELLOW WIRE (ITEM #3) FOR MACHINE WRAPPED & BLUE WIRE (ITEM #4) FOR HAND WRAPPED WIRING.



DETAIL A
8 PLACES
SEE NOTE 2

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM —— STOCK SIZE —— CAT. NO. —— MFG.	DEC. STOCK NO.
	SEE ML	REF	WIRE LIST	
	SEE ML	REF	EXTERNAL COMPONENTS LIST	
1		A/R	CHAIN VOLTAGE	1202188
2		A/R	#24 AWG SOLID KYNAR WHT	
3		A/R	#24 AWG SOLID TEF YEL	
4		A/R	#24 AWG SOLID KYNAR BLU	
5	D-AD-1943-D-0	2	1943D MTG PANEL	1943-D
6	A-DC-7406371-0-0	A/R	LOGIC FRAME DECALS (CLEAR)	7406371

A-PL-7005684-0-0 Assembly Parts List

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.