MS8-C/MS8-D MOS Memory
Technical Manual

EK-MS8CD-TM-001

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CONTENTS

CHAPTER 5 MEMORY CYCLE CONTROL AND TIMING

CHAPTER 6 MEMORY REFRESH, POWER UP, AND ADDRESS LOGIC

CHAPTER 7 TROUBLESHOOTING

APPENDIX A 555 TIMER IC

FIGURES

TABLES

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This manual discusses the installation, operation, and maintenance of the MS8-C/MS8-D MOS memory system. It also provides recommended troubleshooting procedures.

1.2 GENERAL

The MS8-C/MS8-D memory system (Figure 1-1) is an MOS, semiconductor, random access memory designed to interface with the PDP-8/A Omnibus. It is mounted on a hex module, but uses only five of the six sets of fingers (backplane pins A – E). There are two versions of the MS8-C module available and four of the MS8-D (Table 1-1).

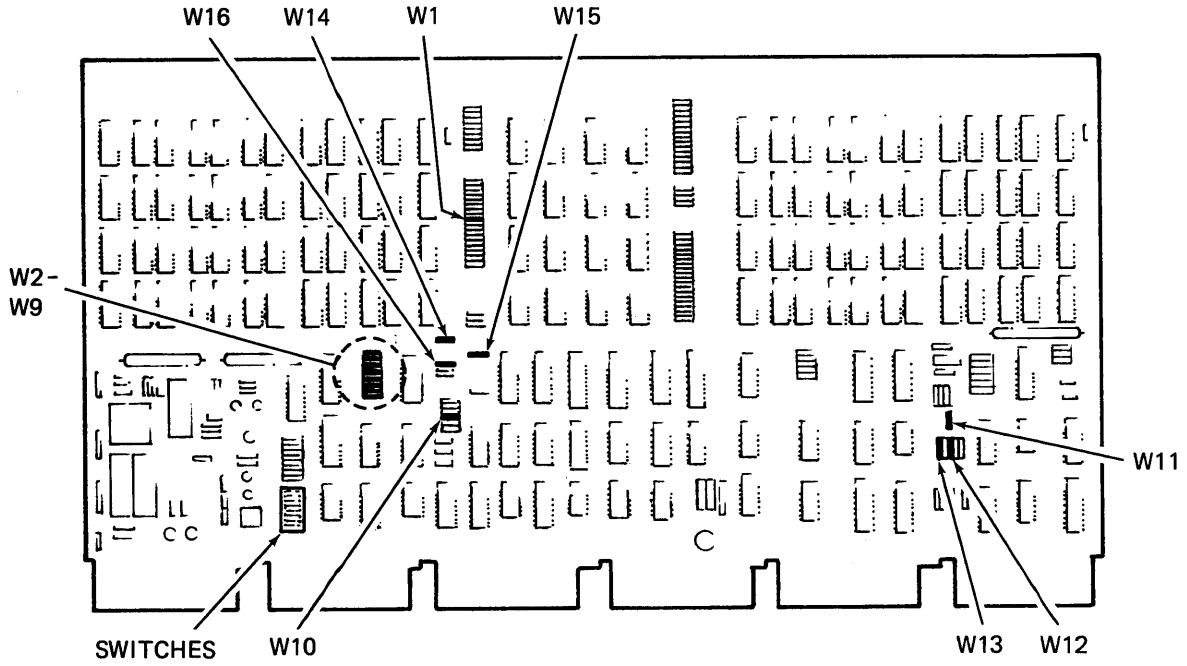

Figure 1-1 MS8-C/MS8-D Memory

Table 1-1 MS8-C/MS8-D Configurations

Option	Memory Size	MOS RAM Size	Populated
MS8-CA	16K X 12 bits	4K	1/2
MS8-CB	32K X 12 bits	4K	full
MS8-DB	32K X 12 bits	16K	1/4
MS8-DD	64K X 12 bits	16K	1/2
MS8-DF	96K X 12 bits	16K	3/4
MS8-DJ	128K X 12 bits	16K	full

The processor signals which control the MS8-C/MS8-D are the same as those which control the PDP-8/A core memory systems. Therefore, differences between core memory and MS8-C/MS8-D memory are not apparent to the processor. Since the contents of the MOS RAM chips are volatile, the memory performs a refresh cycle every 14 μs. A single cycle refreshes 1 of 64 rows of cells on each chip for the MS8-C, and 1 of 128 rows of cells on each chip for the MS8-D. Thus, the entire memory is refreshed approximately every 900 μs for MS8-C and 1.8 ms for MS8-D.

The MS8-C/MS8-D memory can be placed in any slot in the PDP-8/A backplane with five sets of fingers (A – E). Any PDP-8/A system with 32K maximum of memory must include a KM8-A module. A system with more than 32K of memory, however, must include a memory management option (KT8-A) instead of a KM8-A.

Switches on the MS8-C/MS8-D enable the user to select any 16K boundary as a starting address for memory. For more information, refer to the *KT8-A Memory Management Control User's Guide* (EK-KT08A-UG-001).

1.3 SPECIFICATIONS

1.3.1 Omnibus Interface

The MS8-C/MS8-D memory interfaces directly with the PDP-8/A Omnibus. Each memory data line has two drivers and one receiver. All other signals have either one driver or one receiver.

1.3.1.1 Backplane Pins – The MS8-C/MS8-D memory uses backplane pins as shown in Table 1-2.

1.3.2 Power Supply Requirements

Power supply requirements for the MS8-C/MS8-D memory are listed in Table 1-3.

The +5 V line provided by the power supply generates +12 V on the module. The −15 V line provided by the power supply generates −5 V on the module.

Table 1-2 MS8-C/MS8-D Omnibus Pin Connections

Pin	A1	A2	B1	B2	C1	C2	D1	D2	E1	E2
A	T Margin 1 H	+5 V	T Margin 2 H	+5 V	T RAS L	+5 V	-5 V Margin		REF DIS L	
B	T MUX L		TD STB 1 L		LOCKOUT L	-15 V	REF OSC H		Position 7 H	BANK SEL 0 L
C	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
D	MA 0 L	EMA 0 L	MA 4 L				MA 8 L		Position 6 H	BANK SEL 1 L
E	MA 1 L	EMA 1 L	MA 5 L				MA 9 L		Position 5 H	
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	MA 2 L	EMA 2 L	MA 6 L			TP 3 H	MA 10 L		Position 4 H	
J	MA 3 L		MA 7 L				MA 11 L		Position 3 H	
K	MD 0 L	MD DIR L	MD 4 L				MD 8 L		Position 2 H	
L	MD 1 L	SOURCE H	MD 5 L				MD 9 L		Position 1 H	BANK SEL 2 L
M	MD 2 L	STROBE H	MD 6 L		Not Last Xfer L		MD 10 L		Position 0 H	
N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
P	MD 3 L		MD 7 L			TS 4 L	MD 11 L		+12 V MARGIN	
R				NTS STALL L					-5 V	BANK SEL 3 L
S		WRITE H								
T	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
U		ROM ADDRS L		Run L						
V				POWER OK H					+12 V	

Table 1-3 Maximum Power Supply Requirements

Voltage	Option	Memory Size	Operating Current	Standby Current
+5 V (±5%)	MS8-CA	16K	3.3 A	2.6 A
	MS8-CB	32K	3.5 A	2.8 A
	MS8-D	All	3.5 A	2.8 A
-15 V (±10%)	MS8-C and MS8-D	All	.07 A	0.07 A

1.3.3 Access and Cycle Times

Access time to the MS8-C/MS8-D is 285 ns. Cycle times are processor dependent as follows.

Cycle Time	Cycle	CPU Configuration
1.2 μs	Read/write cycle	8E
1.4 μs	Read/modify/write cycle	8E
1.5 μs	Read/write cycle	8A

CHAPTER 2
INSTALLATION

2.1 GENERAL

The MS8-C/MS8-D memory module can be installed in any PDP-8/A system. Before it is shipped, the appropriate jumpers are removed or installed in accordance with the memory size (Table 4-1). The jumpers should not be altered.

2.2 ADDRESS SELECTION SWITCHES

There are eight switches located near the lower-left corner of the MS8-C/MS8-D module. Field Service should set these switches to reflect the address space that memory occupies within the PDP-8/A. Table 2-1 shows the most common module configurations used in a PDP-8/A system and the proper switch settings. Although other module configurations may be developed, at present, the three shown in the table are the only ones used.

Each switch enables a different 16K segment of the memory address. More than one module may be used in a system; for example, two or more MS8-CBs, two or more MS8-DBs, or some combination of both. If more than one module is used, and if memory contains more than 16K, then only one of each numbered switch should be left open (off) on all the modules. To maintain contiguous address space, the off switches must be in consecutive positions starting with S1 and moving toward S8 as required.

2.3 BACKPLANE CONFIGURATION

Any of three backplane configurations can be used with the MS8-C/MS8-D memory module (Figures 2-1 and 2-2). In a 12-slot (H9300 chassis) backplane, Field Service should place the module in any one of slots 4 through 8. In a 20-slot (BA8-C chassis) backplane, Field Service should place the module in any one of slots 4 through 11.

Table 2-1 Switch Settings

Module Configuration	Address Space	Switches S1	S2	S3	S4	S5	S6	S7	S8
MS8-DJ	0–128K	X	X	X	X	X	X	X	X
MS8-CB/MS8-DB	0–32K	X	X	–	–	–	–	–	–
	16–48K	–	X	X	–	–	–	–	–
	32–64K	–	–	X	X	–	–	–	–
	48–80K	–	–	–	X	X	–	–	–
	64–96K	–	–	–	–	X	X	–	–
	80–112K	–	–	–	–	–	X	X	–
	96–128K	–	–	–	–	–	–	X	X

X = Switch off
– = Switch on

NOTE

A KT8-A memory management option must be used if the system has more than 32K of memory.

Make sure that system power is off before removing or installing the module.

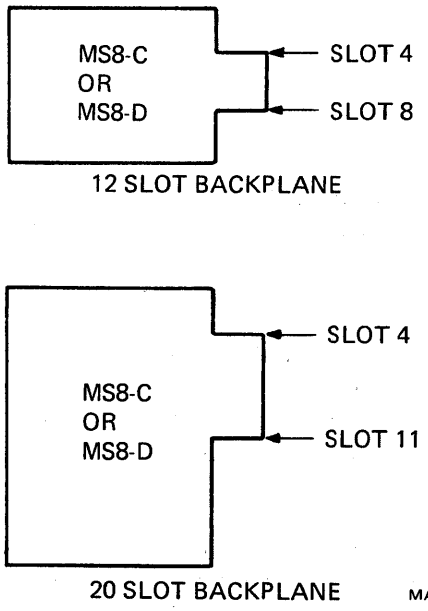

Figure 2-1 Configuration with One Backplane

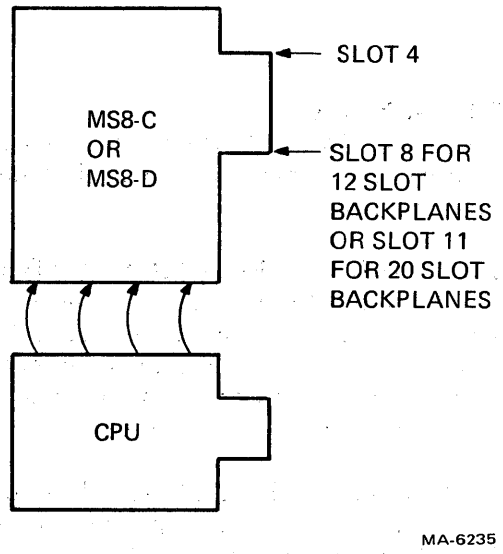

Figure 2-2 Typical Configuration with Two Backplanes

Use the following steps to configure the backplane. For more information on expanded systems, refer to Paragraph 3.2 in the *PDP-8 Family Configuration Guide* (EK-0PDP8-SP-001).

1. Due to the priority sequence, it is preferable for memory and the CPU to reside in separate boxes. However, if they are in the same box (that is, if memory is in both boxes), then they should be placed at the maximum allowable distance from each other.

2. In an expanded system containing a KT8-A option, an M9020 terminator module must be installed (using any E connector) in the box *not* containing the KT8-A option. Use a cable (70-11411-1J) to connect the bank select signals between the KT8-A and M9020 in the two boxes.

2.4 RUNNING DIAGNOSTICS

After memory has been installed, the user should verify memory operation by running the following diagnostic programs.

1. PDP-8/A Extended Memory Address Test (MAINDEC-08-DHKMC-D)
2. PDP-8/E Extended Memory Data and Checkerboard Test (MAINDEC-08-DHKMA-D-D)

Refer to Chapter 7 for details on program loading and execution.

CHAPTER 3
MOS CHIP DESCRIPTION

3.1 PHYSICAL DESCRIPTION

The MOS memory device used with the MS8-C is a 4096-bit, dynamic, random access memory circuit. The MOS memory device used with the MS8-D is a 16384-bit, dynamic, random access memory circuit. These circuits are packaged in a standard 16-pin DIP. The DIP provides high system bit density and is compatible with available automatic testing and insertion equipment. Figure 3-1 shows the chip pin connections. Table 3-1 lists the chip supply voltages.

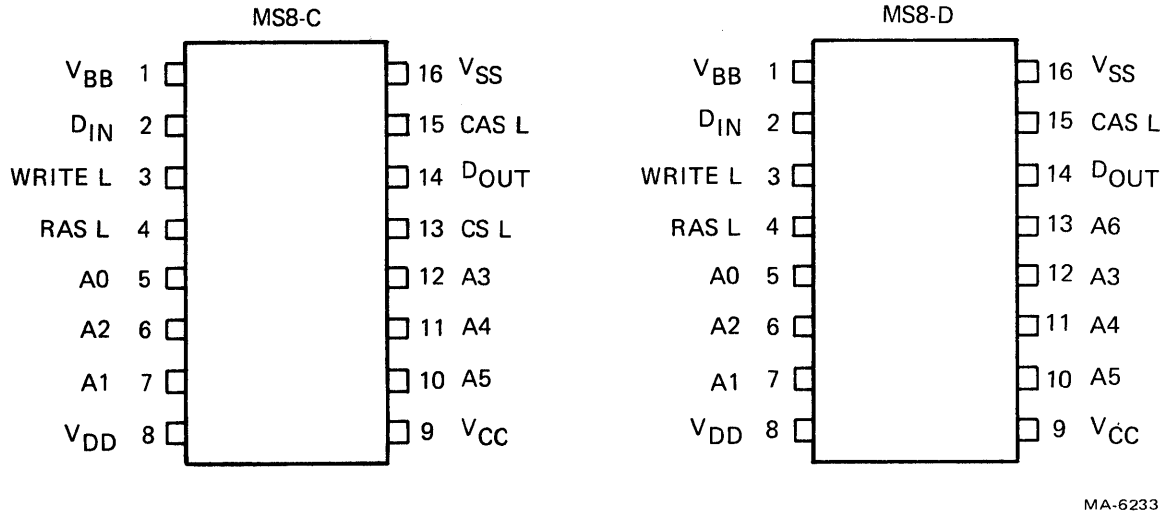

Figure 3-1 MOS RAM Chip Pin Connections

Table 3-1 Chip Supply Voltages

Voltage	Operation
V_{DD}	+12 Vdc
V_{CC}	+5 Vdc
V_{SS}	Ground
V_{BB}	-5 V

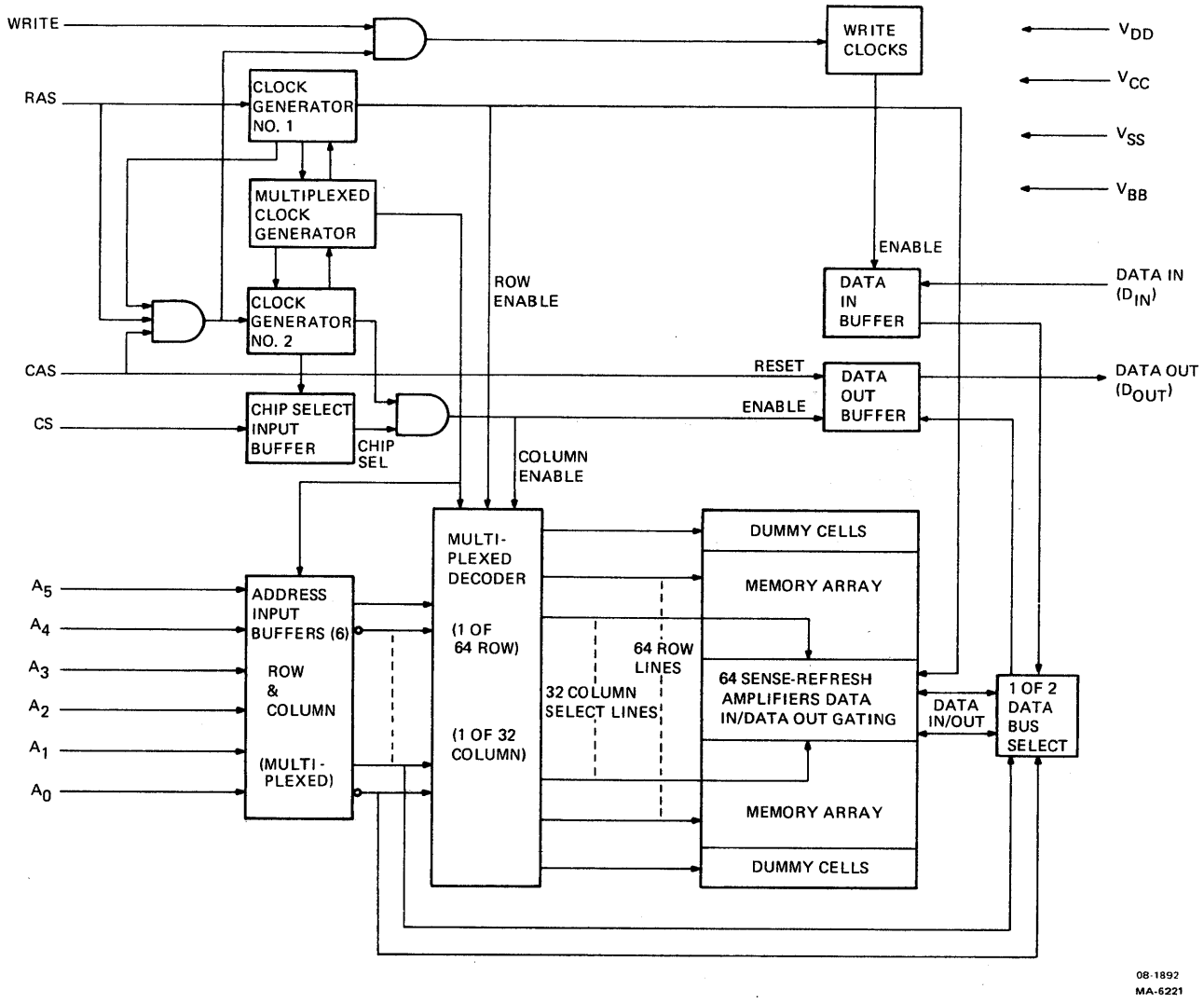

Figure 3-2 4096 × 1 Bit MOS RAM Block Diagram

3.2 FUNCTIONAL DESCRIPTION

Functional block diagrams of the chips are shown in Figure 3-2 for the MS8-C module and Figure 3-3 for the MS8-D module. The 4096 storage locations for the MS8-C are arranged in a 64 row by 64 column array. The 16384 storage locations for the MS8-D are arranged in a 128 row by 128 column array. Thus, a cell location for either memory can be specified by a row address and a column address. Since address information latches into on-chip registers, row and column addresses can be multiplexed onto a common set of address lines.

3.2.1 MS8-C Addressing

The MS8-C logic multiplexes 12 address bits (6 at a time) onto lines A0 – A5. The RAS L (row address strobe) signal latches row address information into a 6-bit register. The CAS L (column address strobe) signal latches column address information and the CS L (chip select) signal into a 7-bit register. Applying enable signals to 1 of the 64 decoders results in the selection of 1 of the 4096 cell locations for a data transfer.

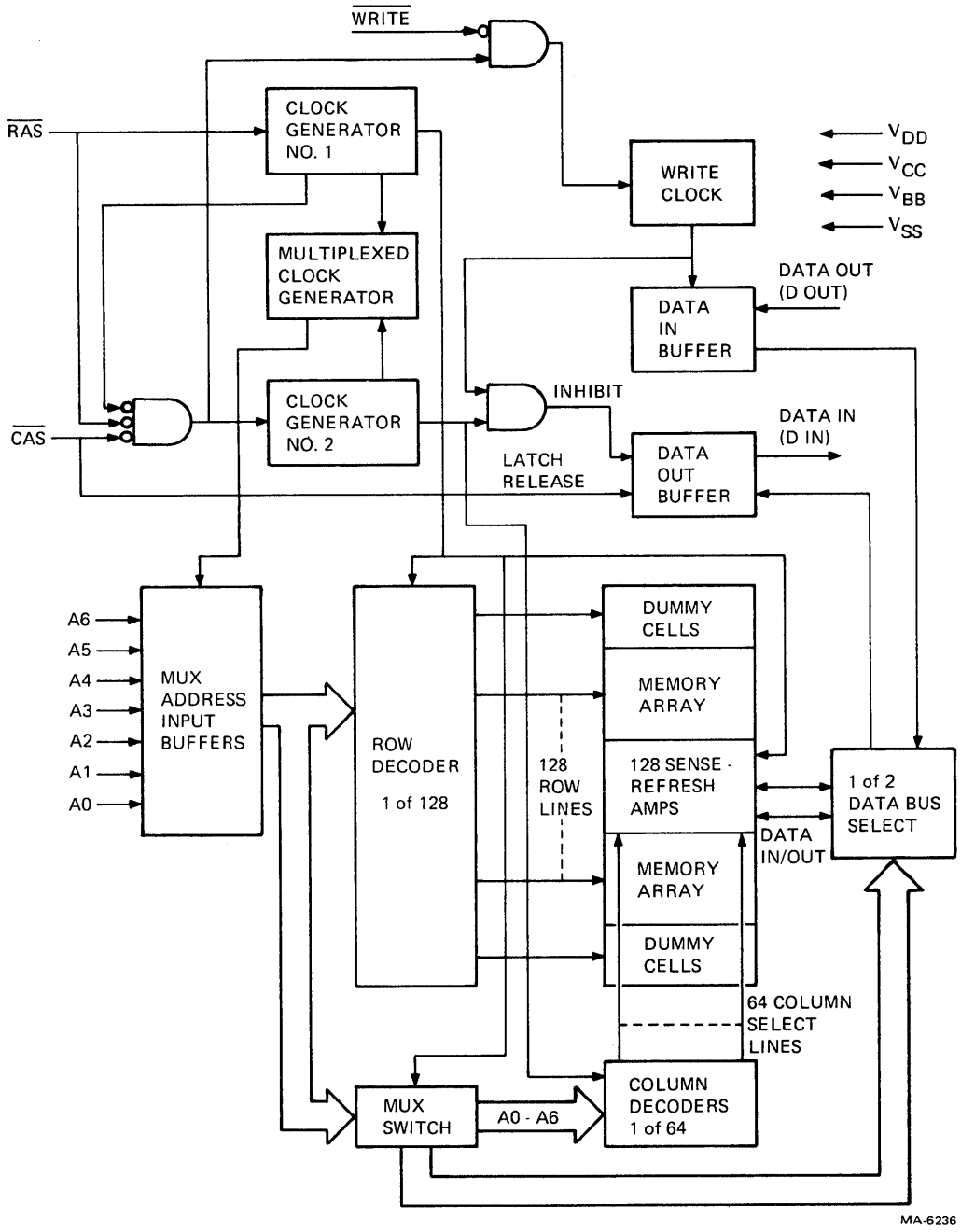

Figure 3-3 16384 × 1 Bit MOS RAM Block Diagram

3.2.2 MS8-D Addressing

The MS8-D logic multiplexes 14 address bits (7 at a time) onto lines A0 – A6. The RAS L signal latches row address information into a 7-bit register. The CAS L signal latches column address information into a 7-bit register. Applying enable signals to 1 of the 128 decoders results in the selection of 1 of the 16384 cell locations for a data transfer.

3.2.3 Cell Storage Element

Figure 3-4 is a simplified representation of the MOS chip. (Switches are symbolic of a more detailed chip operation.) The basic cell storage element is a capacitor. A charge of 0 – 6 V represents logic 0, and a charge of 6 – 12 V represents logic 1. Since the charge on the capacitor dissipates with time, it must be continually refreshed for the data to remain valid. All read and write cycles refresh data in the addressed locations. During these cycles, the row address is latched first, and then 1 of the 64 (MS8-C)

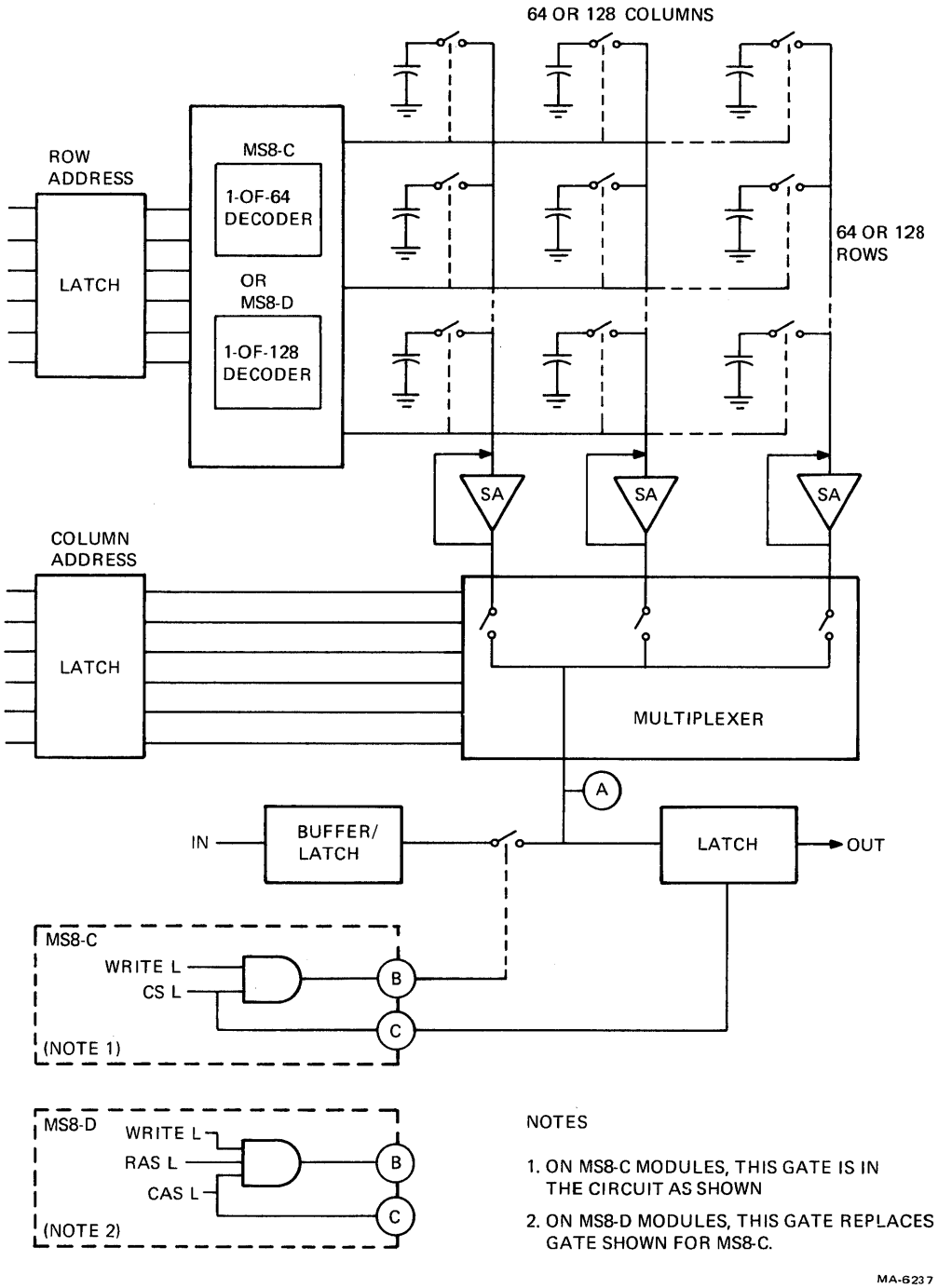

Figure 3-4 MOS Chip (Simplified Data Gating)

or 128 (MS8-D) decoders closes all switches in the selected row. The charge voltage on each capacitor in the row is applied to a sense amplifier (SA), which refreshes data by restoring the charge voltage to its original level. For example, the maximum charge voltage on a cell capacitor is 12 V, representing logic 1. When the cell is addressed, a portion of the full charge may dissipate so that the voltage decreases, for example, to 8 V. The SA restores the voltage to its full charge of 12 V. Similarly, any voltage between 0 and 6 V is restored to a logic 0 level of 0 V.

3.2.4 Read, Write, and Refresh

After data in the selected row is accessed and refreshed, the column address is latched. The multiplexer selects 1 of the 64 (MS8-C) or 128 (MS8-D) columns and applies the amplified charge voltage on a single capacitor (point A in Figure 3-4). If it is a read cycle (Figure 3-5), data is strobed into the tri-state output latch and remains valid until the next time CAS L goes low. If it is a write cycle (Figure 3-6), the input buffer/latch drives point A (Figure 3-4), overriding the SA output and charging the selected cell capacitor.

Since it is possible that a cell may be addressed only infrequently (if at all) during normal read/write operations, a special refresh cycle (Figure 3-7) is performed at regular intervals. In MS8-C/MS8-D memory, this cycle occurs approximately every 14 μs. The memory module logic supplies a different row address for each refresh cycle. Therefore, for the MS8-C, data in all 64 row addresses is refreshed about every 900 μs; for the MS8-D, data in all 128 row addresses is refreshed about every 1800 μs. The refresh operation is similar to a read or write cycle, except that it does not generate column addresses and CAS L. For the MS8-C only, the refresh cycle disables the CS L signal so that neither the input circuit nor the output circuit is enabled. The output latch goes to its high impedance state, providing minimal power consumption.

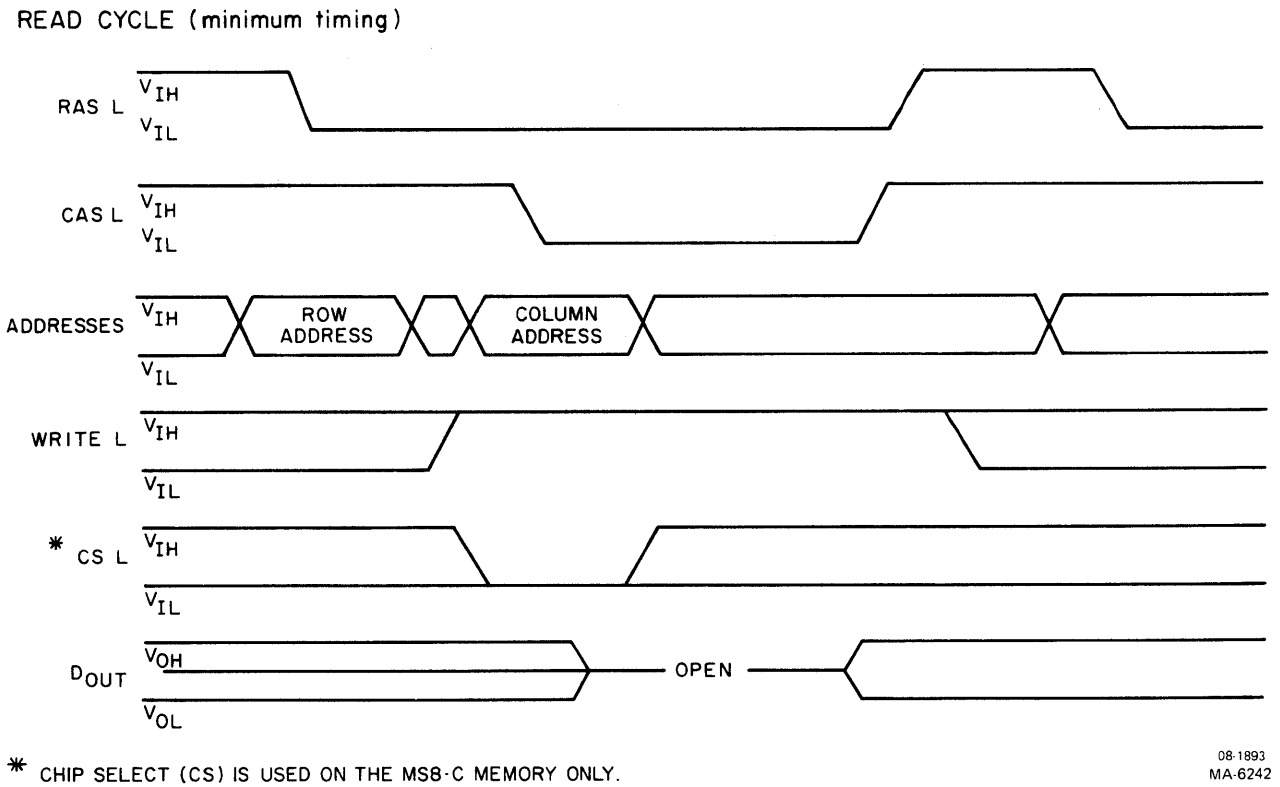

Figure 3-5 Chip Read Timing

3.2.5 Timing

Figures 3-5 and 3-6 illustrate the timing for the read and write cycles. The RAS L signal starts the timing cycle internally. In order to reduce the overall system power, the MS8-C/MS8-D logic decodes RAS L and supplies it only to the selected bank of chips. The CAS L signal is supplied to all chips, but chips that do not receive a RAS L signal go to their high impedance output states.

For a read cycle at the addressed location, the WRITE L signal must be high and the CS L signal (MS8-C only) must be asserted. Data is strobed into the output latch/buffer at access time (after RAS L is asserted). The data remains valid until CAS L goes low during a subsequent timing cycle. For a write cycle at the addressed location, the WRITE L signal must go low before access time. The chip accepts the WRITE L command only if CS L (MS8-C only) has been asserted. The low transition of the CAS L signal strobes data on the D_{IN} line into an input latch. The output latch/buffer goes to logic 1 at access time.

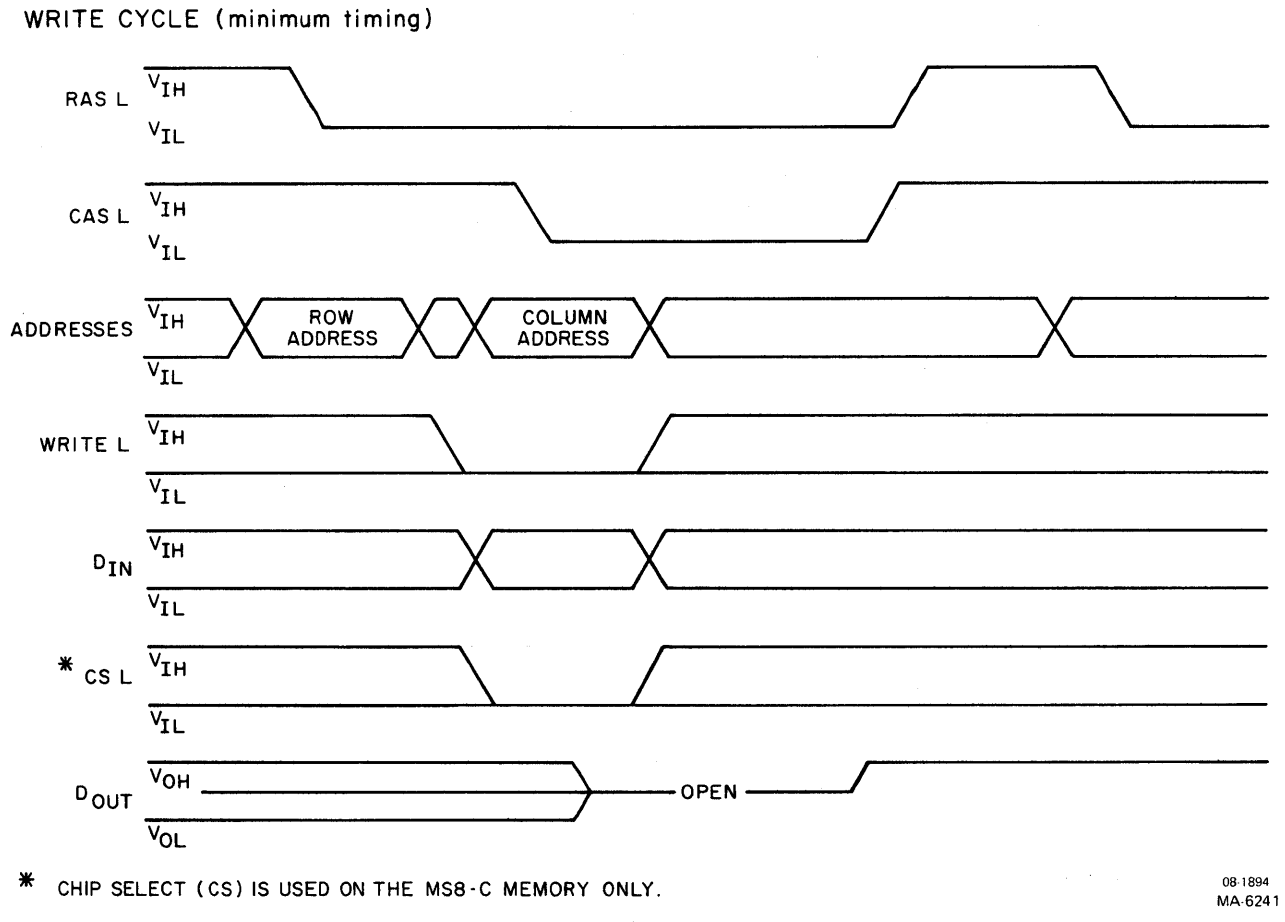

Figure 3-6 Chip Write Timing

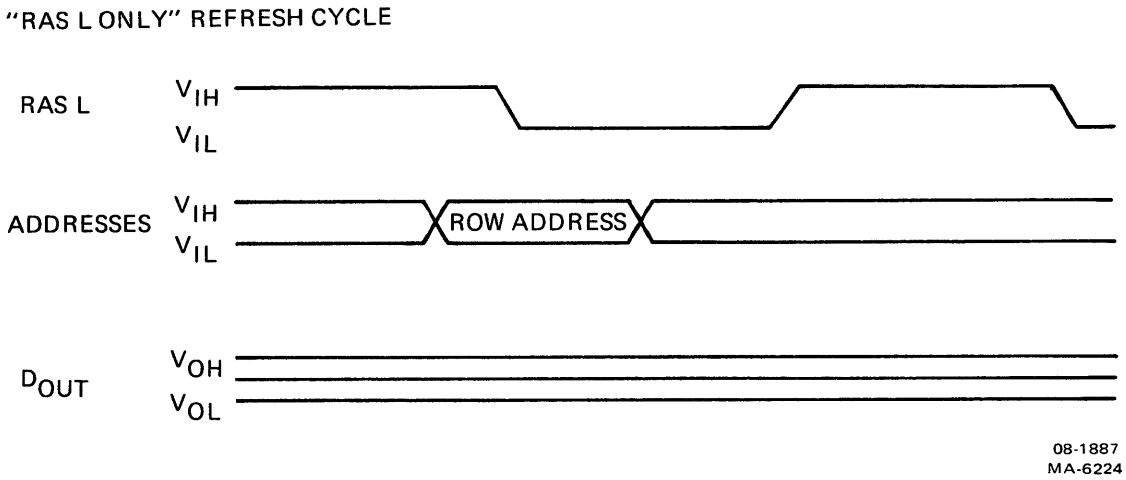

Figure 3-7 Chip Refresh Timing

CHAPTER 4
MEMORY AND POWER DETAILED DESCRIPTION

4.1 GENERAL

After the PDP-8/A initiates a memory cycle, the MS8-C/MS8-D control logic accesses the location addressed. The control logic then gates the selected data from the Omnibus to the memory array, or from the memory array to the Omnibus. The cycle is synchronized with the processor timing signals. Figure 4-1 shows the basic circuits which make up the memory.

When the processor initiates a memory cycle, it asserts a memory address on the memory address Omnibus lines at timing pulse T4. The address lines settle before SOURCE H goes high and starts the memory timing sequence. The address asserted remains valid on the Omnibus for the duration of the processor cycle (approximately 1.5 μs). Refer to the Omnibus timing diagram (Figure 5-2).

In a read cycle, the data is read during the first third of the processor cycle. During a write cycle, the memory always performs a read/modify/write routine; it reads the data in the location addressed and then writes the modified or new data back into the same location. The time between the read and write portions of the memory cycle may be used for a memory refresh cycle, depending on the condition of the Refresh Go flip-flop.

4.2 MEMORY ARRAY

4.2.1 MOS RAM Chip Configuration

The fully configured memory array on the MS8-C consists of 96 4K $\times$ 1-bit MOS RAM chips. For the MS8-D, the memory array consists of 96 16K $\times$ 1-bit MOS RAM chips. In the circuit schematic, the array forms an 8 $\times$ 12 matrix. Twelve chips constitute a 4K word field on the MS8-C, and a 16K word field on the MS8-D. A row address describes each field. Eight fields are available on the array, providing 32K (MS8-C) and 128K (MS8-D) memory locations. Each of the 12 chips in a field represents one data bit position in that field.

Figure 4-2 shows the relation of the individual MOS RAM chips to the word fields and data bit positions.

4.2.2 Row and Column Addressing

At row address time, one of the eight fields is selected for memory reference. The lower six memory address signals (MA06 – MA11) on the MS8-C, as well as a seventh (EMA2) on the MS8-D, are gated to the address pins of each chip in the selected field. The signals are then latched into the row address register of the chips.

At column address time, the upper six memory address signals (MA00L – MA05L) on the MS8-C, as well as a seventh (EMA1) on the MS8-D, are gated to the address pins of the same selected chips. These signals are then latched into the column address registers of the chips in the selected field. At this point, the memory location addressed by the processor is available for data transfer.

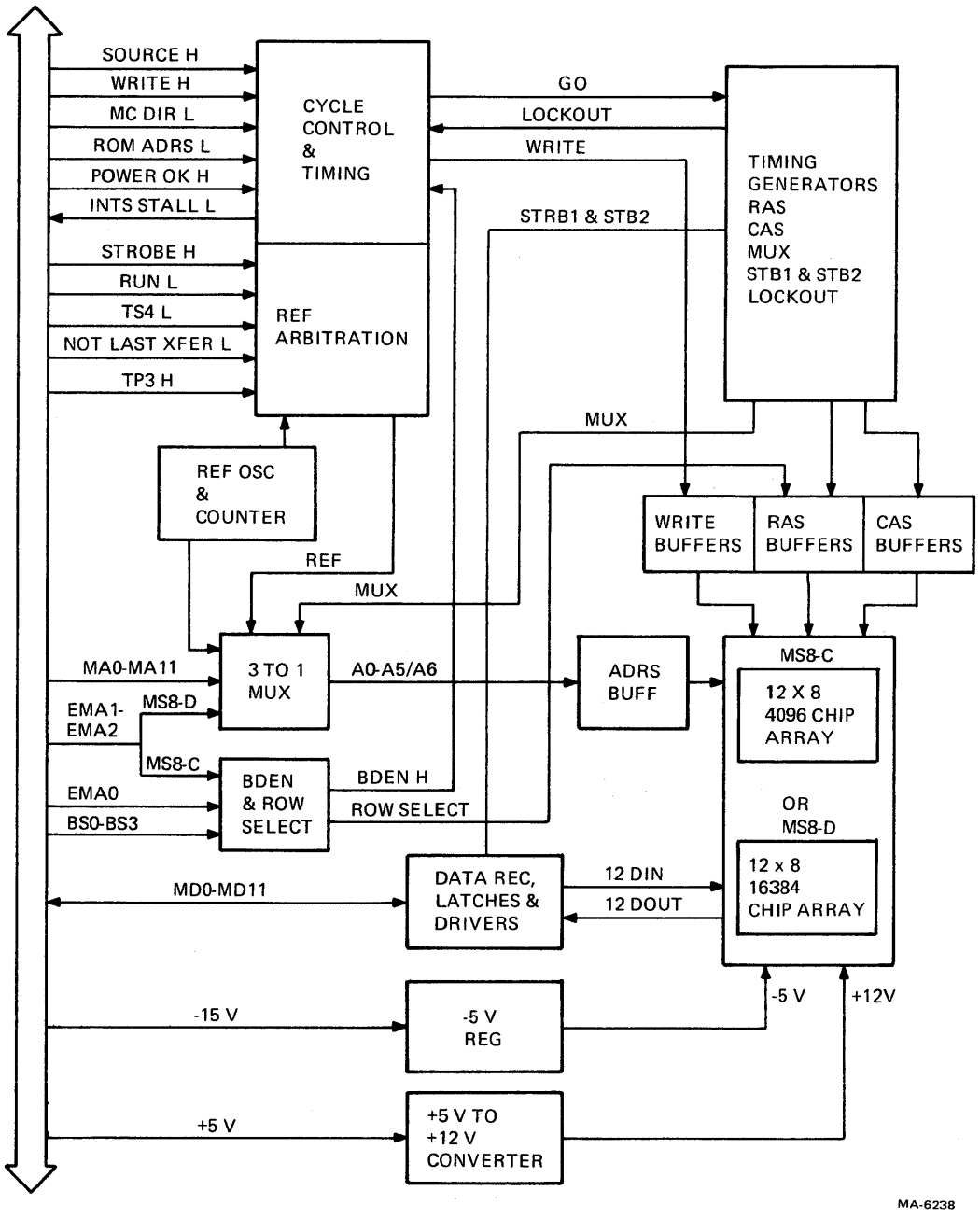

Figure 4-1 MS8-C/MS8-D Block Diagram

4.3 FIELD AND BANK ADDRESS SELECTION LOGIC

4.3.1 Extended Memory Address Signals

The three extended memory address signals for MS8-C (EMA0L – EMA2L) are channeled through the jumpers to a pair of 2:4 decoders. This produces eight row select signals (row 0 L – row 7 L). Refer to Figure 4-3 and sheet 6 of the MS8-C prints.

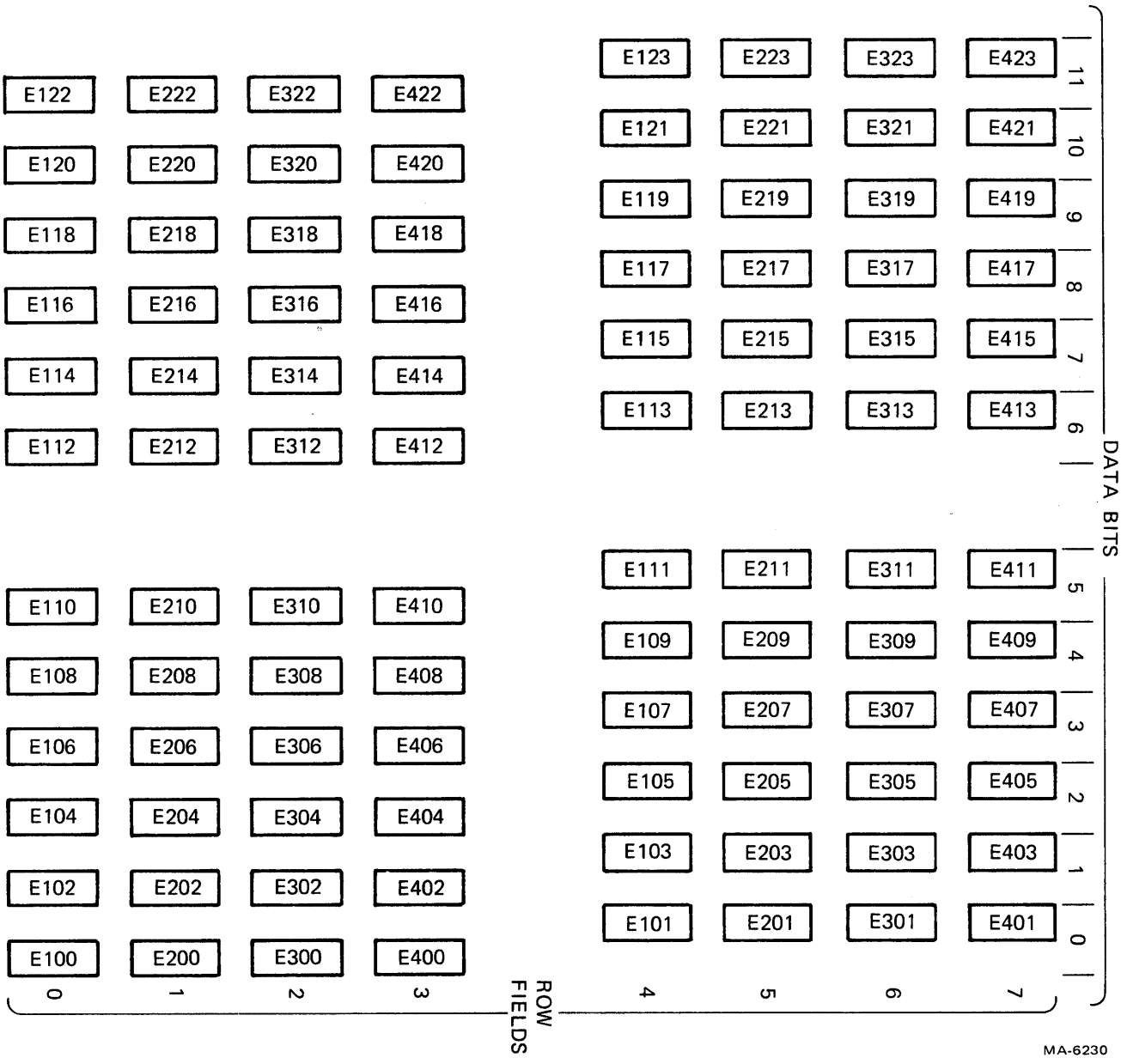

Figure 4-2 MOS RAM Chip Matrix

The row select signals are NANDed first with REF ADR L and then with T RAS L. This produces eight row address select signals (RAS 0 – 7 L). Only one of these signals is true (low) at any given time, except on a refresh cycle when all are true (low).

Two of the extended memory address signals for the MS8-D module (EMA1, EMA2) are gated to the seventh address line of the 16K MOS RAM chips (Paragraph 4.2.2). The third signal (EMA0) is still used for row select decoding.

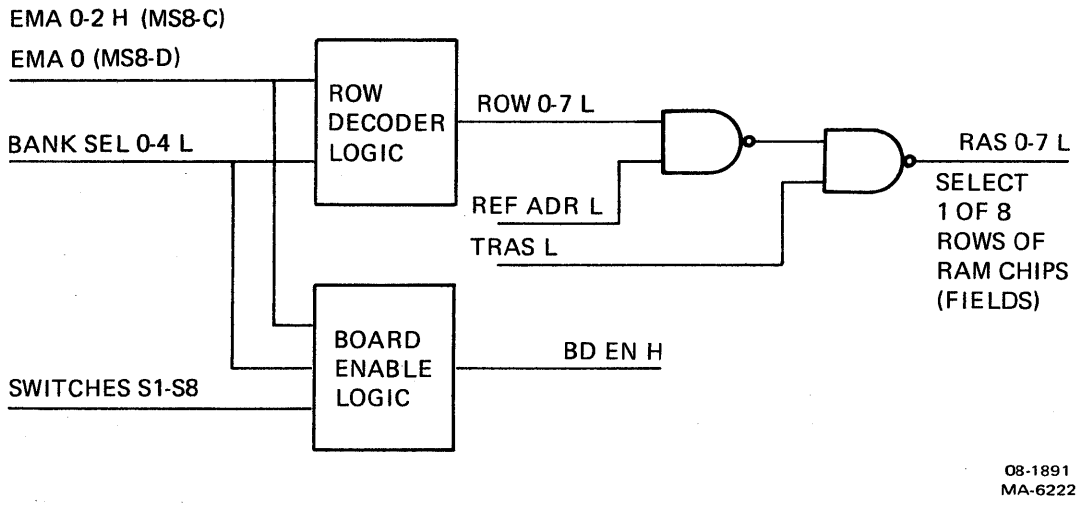

Figure 4-3 Field and Bank Address Selection

4.3.2 Bank Select Lines

Bank select lines 0 – 3 and EMA0 produce ROW signals on the MS8-D module. Each bank select line (0 – 3) enables a 32K segment of memory or a particular MS8-C module. The address selection switch(es) (Paragraph 2.2) enable these lines. The EMA0 signal selects either the upper or lower 16K sector. Refer to Figure 4-3 and sheet 6 of the MS8-D prints.

4.3.3 Jumper Installation

Table 4-1 shows the jumpers that exist on the various module configurations.

Table 4-1 Jumper Installation

	Module Configurations					
Jumper	MS8-CA 16K	MS8-CB 32K	MS8-DB 32K	MS8-DD 64K	MS8-DF 96K	MS8-DJ 128K
W1	–	–	X	X	X	X
W2	X	X	–	–	–	–
W3	X	X	–	–	–	–
W4	X	X	–	–	–	–
W5	–	–	X	X	X	X
W6	–	–	X	X	X	X
W7	–	–	X	X	X	X
W8	–	–	X	X	X	X
W9	X	X	–	–	–	–
W10	X	–	X	X	X	–
W11	X	X	–	–	–	–
W12	–	–	X	X	X	X
W13	–	–	X	X	X	X
W14	–	–	–	X	–	X
W15	–	–	–	–	X	–
W16	–	–	X	X	–	–

X = Jumper installed
– = Jumper not installed

4.3.4 Starting Address Selection Switches

Refer to Paragraph 2.2.

4.4 ARRAY POWER SUPPLY (+12 V, −5 V)

The MS8-C/MS8-D contains a power supply circuit which provides +12 V and −5 V operating voltages to the MOS RAM chips.

4.4.1 −5 V Supply

A zener diode (D28) and a −5 V regulator (Q11) reduce the −15 V from the system power supply to a −5 V, as shown on sheet 8 of the prints.

4.4.2 +12 V Supply

+5 V system power supply generates the +12 V level. On the refresh address counter, RA0H forms a square wave with a 28 μs period. This is ANDed with REF OSC H, and negated to turn on and off the output transistors of E64 (pins 3 and 5).

The collectors of these transistors are tied to a voltage sensing network. When the −5 V supply rises significantly, or the +5 V supply falls significantly, transistors Q9 and Q8 turn on, thus pulling the outputs of E64 to ground. This process effectively disables the +12 V generation circuit whenever −5 V is lost, protecting the RAM chips in accordance with the manufacturer's specifications.

Square waves generated at E64 (pins 3 and 5) feed the bases of Q6 and Q7, producing a +5 V to ground swing across the primary coil of transformer T1.

Thus, a 30 V swing is produced on the secondary coil of T1. This square wave is then rectified. Q10 regulates the rectified signal to produce a steady +12 V. A second inductor (PC) is connected to the center tap of both the transformer windings. This reduces noise injected back into the +5 V supply. PC is an etch inductor, not a discrete component.

CHAPTER 5
MEMORY CYCLE CONTROL AND TIMING

5.1 FETCH, DEFER, AND EXECUTE

There are three types of processor cycles used to access memory for data transfer: fetch, defer, and execute. During both the fetch and defer cycles, the processor reads an instruction or data word from a memory location. During the execute cycle, the processor may read a memory location, or it may require the memory to perform a read/modify/write routine at the location addressed.

Consider the following example.

```
0200/     DCA I    377
0377/     7000
7000/
```

First, the processor performs a fetch cycle to location 0200_8. This brings the DCA I instruction into the instruction decoder. The processor then performs a defer cycle, reading location 0377_8. This finds the address of the operand location. Next, the processor performs an execute cycle, writing the contents of the accumulator into location 7000_8, the location addressed by the word in location 0377_8. However, memory first performs a read cycle when it accesses location 7000_8, before it performs the write cycle. Thus, although they are ignored, the original contents of location 7000_8 are placed on the memory data lines of the Omnibus, during the read cycle. At the end of the read cycle, the MD drivers on the MS8-C/MS8-D memory are disabled and the processor asserts data to be written on the memory data lines.

5.2 DATA CYCLE INITIALIZATION

When the board enable signal (BDEN H) is high (indicating that a memory location on the module is being addressed), the MS8-C/MS8-D module responds to timing and control signals on the Omnibus. At the beginning of a processor cycle, the Omnibus signal WRITE H is low, making READ H high. READ H is ANDed with BDEN H, producing READ A H. Then, READ A H is ANDed with STALL SET L (high), which puts a high level on the J input of the T RAS flip-flop (Figure 5-1).

The memory timing sequence begins following timing pulse T4. The processor drives the Omnibus line SOURCE H high. This signal is inverted to clock and set the T RAS flip-flop (Figure 5-1). Figure 5-2 shows memory cycle timing.

Figure 5-3 is a memory cycle flowchart. It shows the various conditions necessary for the initiation of read, refresh, and write cycles.

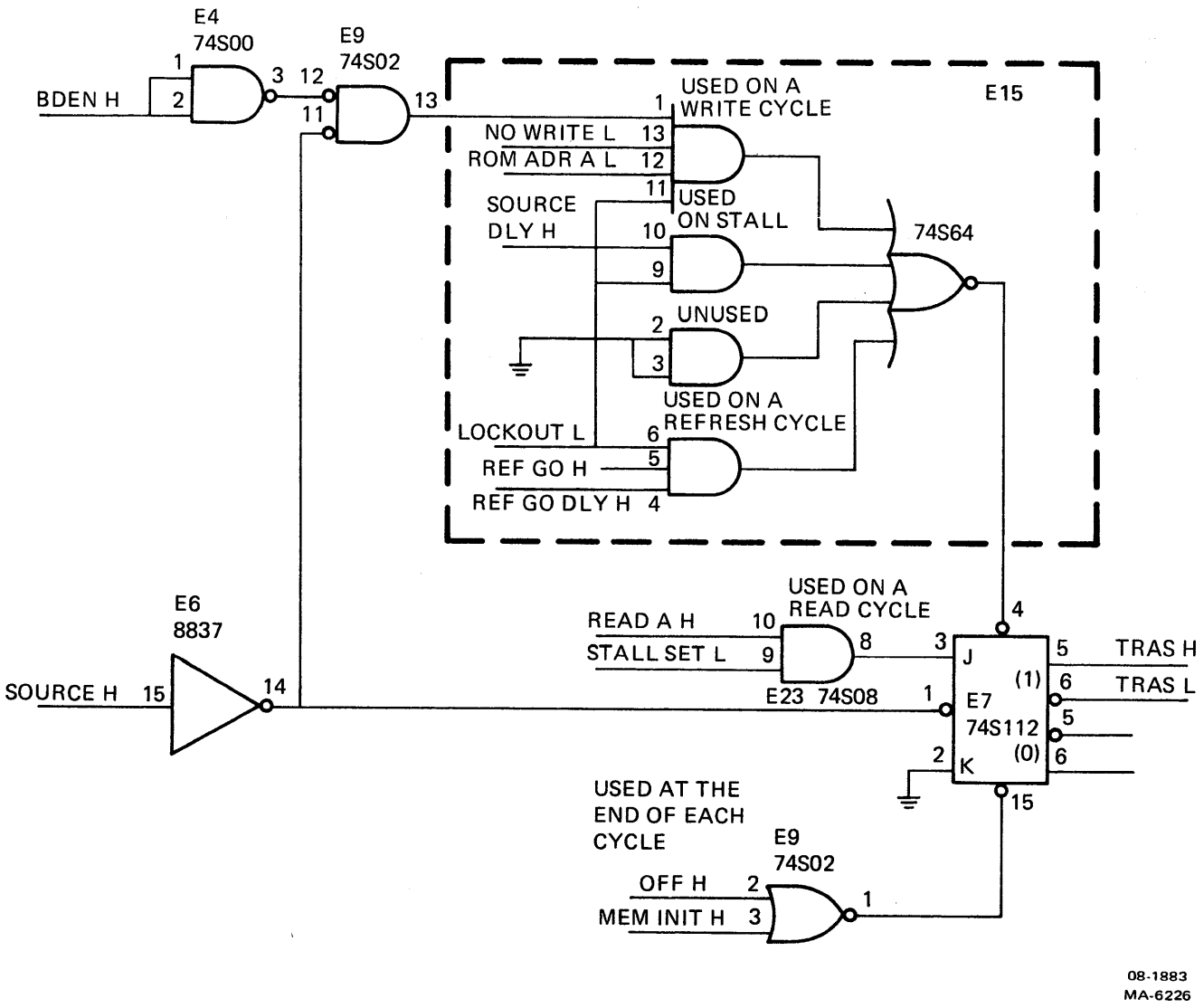

Figure 5-1 T RAS Flip-Flop and Associated Logic

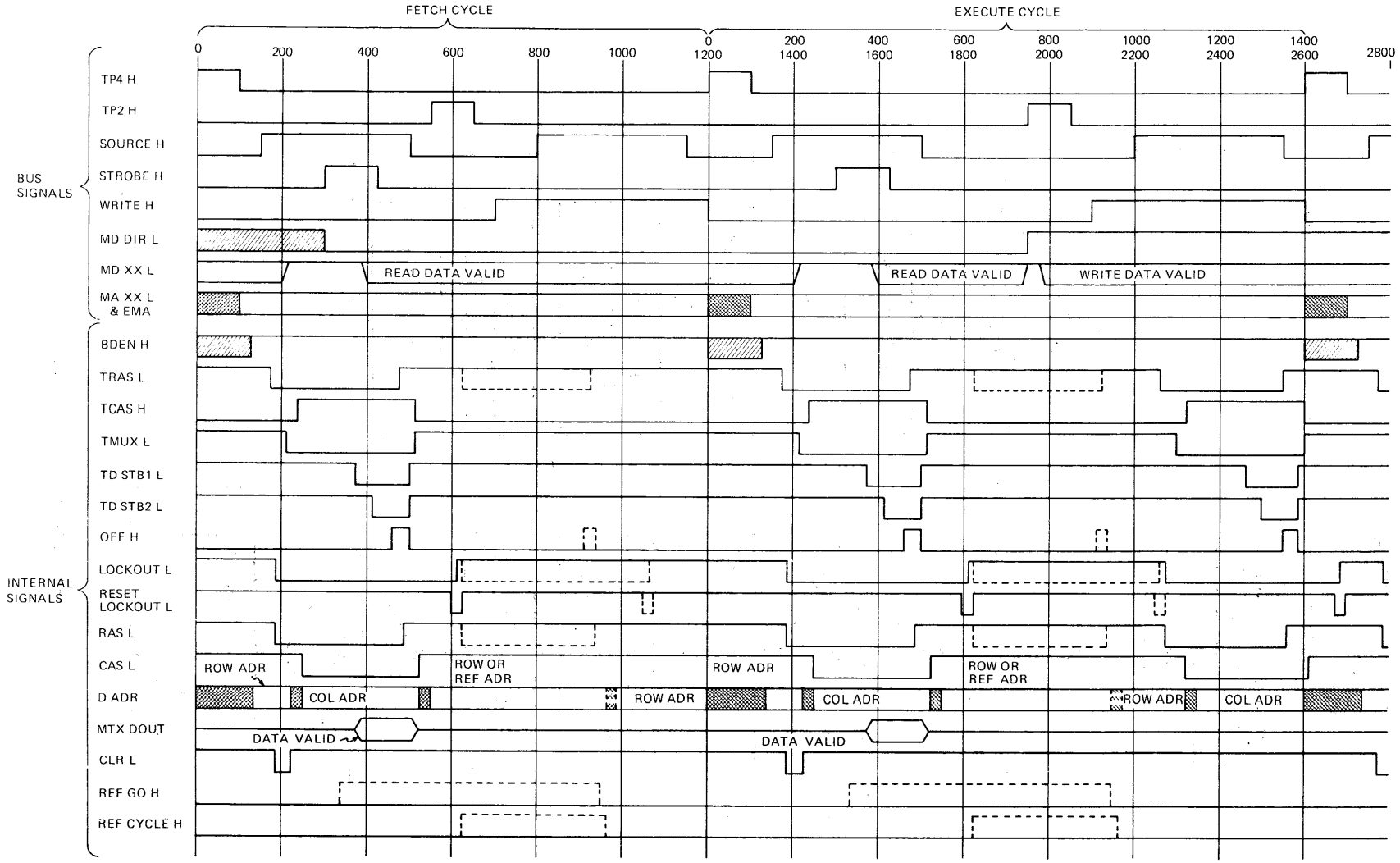

Figure 5-2 Memory Data Cycle (Typical Timing)

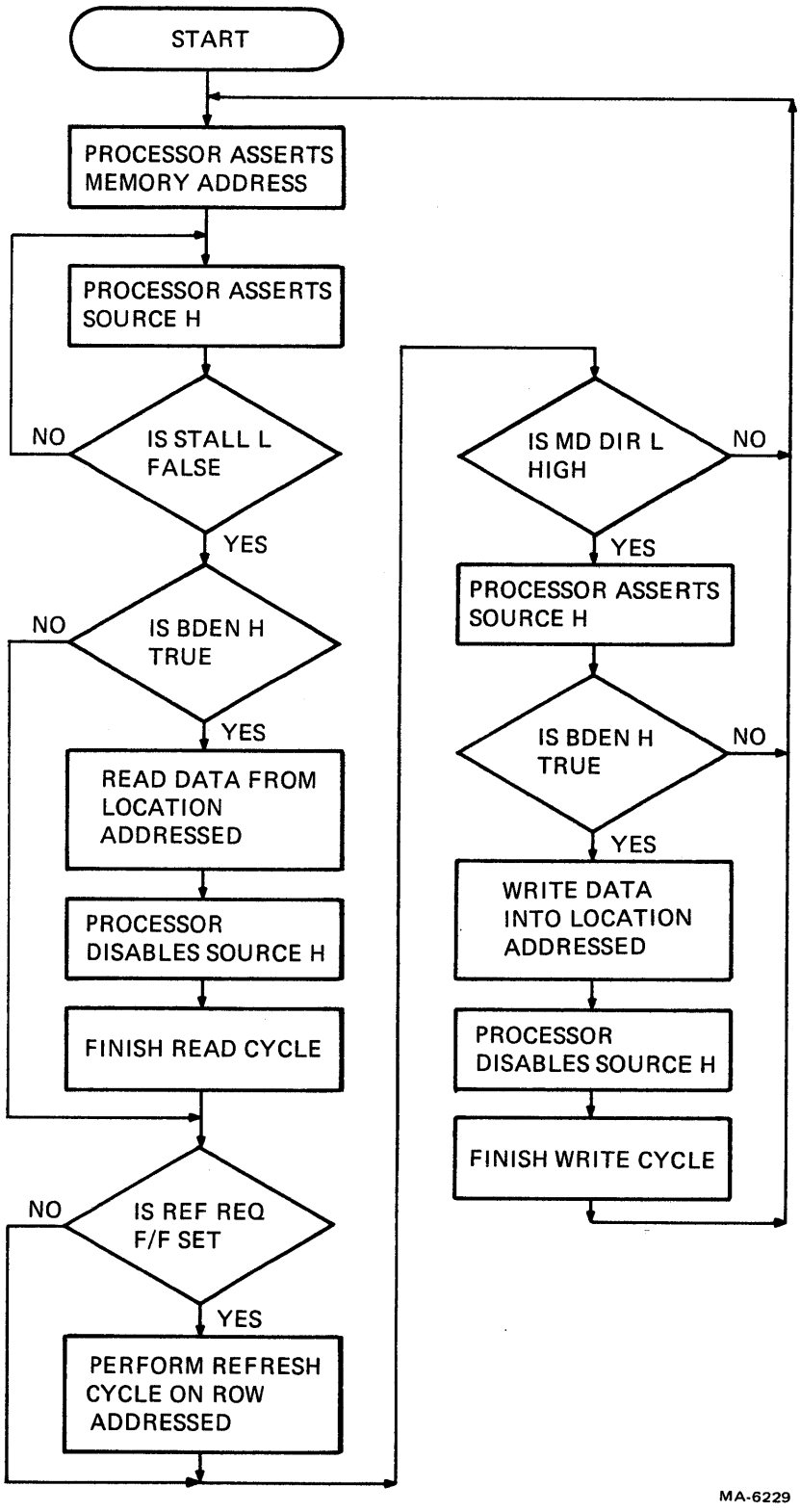

Figure 5-3 Memory Cycle Flowchart

5.3 ROW ADDRESS TIME

T RAS L feeds a group of five delay circuits (Figure 5-4 and sheet 3 of the prints). Table 5-1 shows the initial output conditions of these delay circuits at the beginning of the timing sequence, before the T RAS flip-flop sets.

When the T RAS flip-flop sets (8 ns plus SOURCE H), it enables one of eight signals (RAS 0 – 7 L). This selects the row of 12 chips identified by the extended address and bank select lines (sheet 4 of the prints). T RAS L is ORed with the output of the Lockout Hold flip-flop and OFF AL. This produces LOCKOUT L (sheet 3 of the prints).

Refer to Figure 5-5. T RAS L (initially high) is NANDed with STB 1 L (which should be high) to feed an RC network. Also, T RAS L inverts directly to form another RC network. The two RC networks provide ramp input voltages to five 75107 line receiver gates (sheet 3 of the prints). The line receiver produces T MUX L, which is the first signal to change its state (46 ns after SOURCE H).

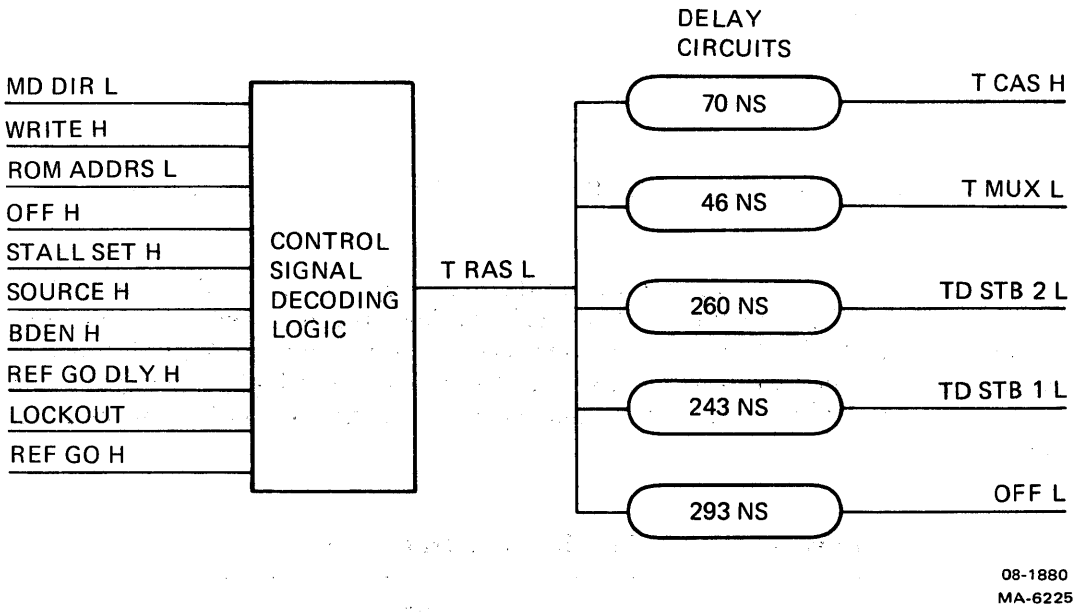

Figure 5-4 Control and Timing Signals Block Diagram

Table 5-1 Signals Triggered by T RAS L: Initial Conditions

OFF H	Low
TB STB 1 L	High
TB STB 2 L	High
T MUX L	High
T CAS H	Low

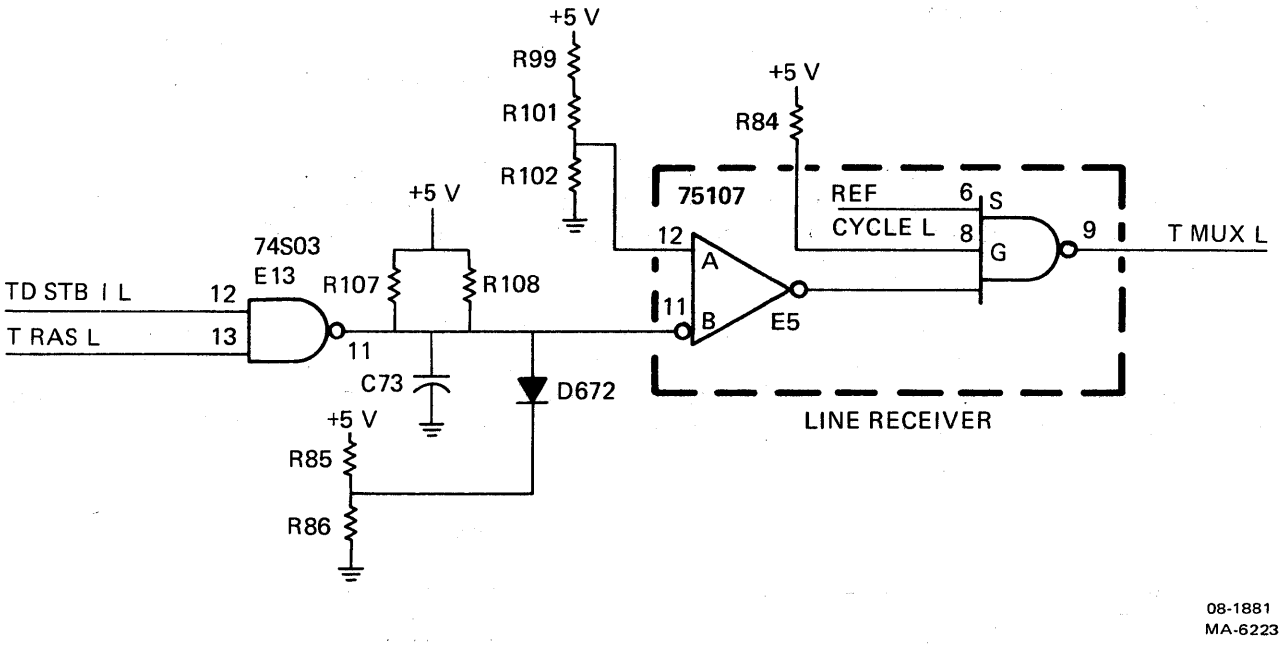

Figure 5-5 T MUX L Line Receiver (75107) and Associated Ramp

Since T RAS L and TD STB 1 L are high before the cycle begins, the initial output of NAND gate E13 at pin 11 is low. Also, the B input of the line receiver is low. Resistors R99, R101, and R102 form a voltage divider which holds the A input of the line receiver at a steady 1.8 V level. Since there is no refresh cycle at this time, the two strobe inputs (pins 8 and 6) are both high, enabling the line receiver output. Table 5-2 is a truth table for the 75107 line receiver. Figures 5-6 and 5-7 illustrate the dynamic nature of the line receiver.

Table 5-2 75107 Line Receiver Truth Table

A-B	Strobes G	Strobes S	Output
(A-B) $\geq$+25 mV	X	X	H
	L	X	H
-25 mV $<$(A-B) $<$+25 mV	X	L	H
	H	H	*
	H	H	L
(A-B) $\leq$-25 mV	X	L	H
	L	X	H

L = Low
H = High
X = L or H
* = Indeterminate

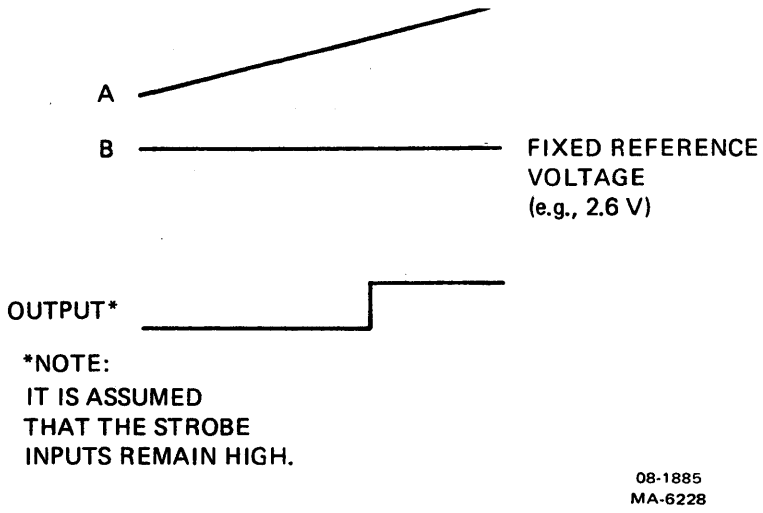

Figure 5-6 Line Receiver, Ramp on A

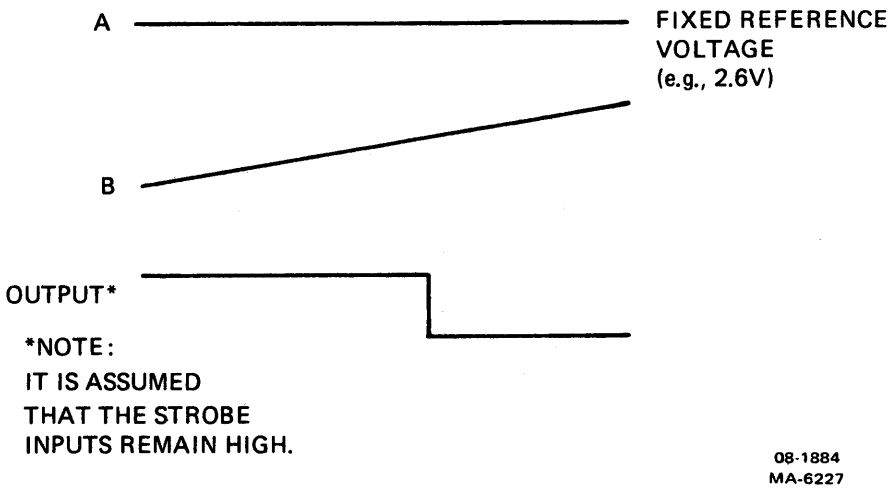

Figure 5-7 Line Receiver, Ramp on B

T MUX L is initially high. When T RAS L is enabled, the NAND gate at switch E13 and capacitor C73 begins to charge. When the voltage level on the B input of the line receiver goes 25 mV above the A input, the line receiver switches. This produces a low level on the line receiver output. The delay time achieved is a function of both the resistor values in the voltage divider circuit, and the resistor and capacitor values in the RC network. The delay circuits which feed OFF H, TD STB 1 L, TD STB 2 L, and T CAS H function in a manner similar to the T MUX L delay circuit. This timing chain is more stable under varying temperature conditions than conventional one-shot or delay line circuitry.

The T MUX L signal feeds the row and column address multiplexer circuit (sheet 5 of the prints). The initial high level on T MUX L causes the B inputs on the two multiplexer chips (E33 and E26) to be selected. Thus, the low order addresses (MA11 – 6L on MS8-C or MA11 – 6L and EMA2 on MS8-D) are selected first. REF ADR H is low, enabling multiplexers and causing the outputs of the E37 and E42 NAND gates to go high. Seven groups of four NAND gates each are used to drive the address lines which feed the array. The seventh group is used as a chip select signal on MS8-C, and as the seventh address line on MS8-D. The six MS8-C and seven MS8-D selected memory address lines are then gated to the MOS RAM chips as the row address bits. They are loaded into the row address registers on the chips in the field selected. These row address bits are not to be confused with signals ROW 0 – 7 L and RAS 0 – 7 L.

5.4 COLUMN ADDRESS TIME

When T MUX L goes high (46 ns after SOURCE H), it causes the address multiplexer chips to select the A inputs (sheet 5 of the prints). Memory address signals MA5-0L (MS8-C) or MA5-0L EMA1 (MS8-D) are gated through the address line drivers to the MOS RAM chips. When T CAS H goes high (70 ns after SOURCE H), it enables the four column address drivers: CAS AL, CAS BL, CAS CL, and CAS DL (sheet 4 of the prints). These signals clock the column address bits into the column address registers on the chips in the selected field.

5.5 CLR L AND REFRESH REQUEST SIGNALS

Another important timing signal changes state in this portion of the memory cycle. SOURCE H feeds a delay circuit which causes a 38 ns low pulse on CLR L, beginning at SOURCE H plus 43 ns (sheet 3 of the prints). This clears the MDR Hold flip-flop at E20, which in turn disables the data drivers E51, E11, and E1, and the data latches (sheet 7 of the prints).

5.6 CHIP SELECT (MS8-C ONLY)

In the MS8-C memory module jumper W11 should be installed to connect EMA 1 H to ground. This signal is selected by address multiplexer chip E26 at column address time, enabling one leg of each of the four address drivers A06A – D L (sheet 5 of the prints). Jumper W1 is open, pulling signal RA6 H high. Thus, the condition of REF ADR H controls the second leg of each of the A06 drivers. (If REF ADR H is low, the four A06 drivers will be enabled.) These drivers feed the chip select input pins of the MOS RAM chips, enabling the 12 MOS RAM chips in the selected memory field at column address time.

NOTE

This CHIP SELECT signal functions only on the MS8-C. On the MS8-D, a seventh MOS RAM address is used. This seventh address (Paragraph 4.2.2) is selected by multiplexer E26 and is driven by the four address drivers A06A – D L.

5.7 READ CYCLE

The MS8-C/MS8-D memory always performs a read function in the first third of a memory data cycle. The data from the location addressed is available on the output pins of the MOS RAM chips in the selected field and valid 140 ns after CAS L goes low.

5.7.1 Getting Data

Data is fed to the input pins of the memory data register 214 ns after SOURCE H goes high; 29 ns after this (243 ns after SOURCE H) TD STB 1 L goes low. This resets the Source DLY flip-flop if it is not already in the reset state and ensures that the input to the RC network (which forms T CAS H and T MUX L) stays high even if T RAS L is disabled (Figure 5-5 and sheet 3 of the prints). TD STB 1 L is ANDed with MD DIR AL, enabling memory data to the MD lines through E44, E14, and E3 (sheet 7 of the prints). Then the ramp which produces TD STB 2 L reaches the critical voltage, causing TD STB 2 L to go low 260 ns after SOURCE H. This causes the MD Bus Latch Control flip-flop to set, strobing data into the memory data latches and enabling one leg of each of the bus driver chips E51, E11, and E1. Data is then latched on the MD lines.

5.7.2 Finishing Read Timing

Data remains latched in the MDR and asserted on the Omnibus until MD DIR A L goes high or CLR L resets the MD Bus Latch Control flip-flop.

The ramp which feeds the OFF H circuit reaches the critical level 293 ns after SOURCE H. OFF H switches high (sheet 2 of the prints) and is ORed with MEM INIT H. This clears the T RAS flip-flop. When T RAS L goes high, it drives low the ramp which feeds OFF L, TD STB 1 L, and TD STB 2 L. These three signals switch high after a 31 ns delay (324 ns after SOURCE H).

When the T RAS flip-flop resets, it sets the Lockout Hold flip-flop (sheet 3 of the prints). This holds LOCKOUT L low for an additional 130 ns after resetting T RAS, allowing time for the memory timing logic to shut down. The 1L side of the Lockout Hold flip-flop drives an RC network which forms a ramp input to a line receiver circuit. When the line receiver switches from high to low, it resets the Lockout Hold flip-flop, disabling LOCKOUT L 439 ns after SOURCE H.

While LOCKOUT L is still enabled, TD STB 1 L goes high, forcing low the ramp which feeds the T MUX L and T CAS H signals. T MUX L then goes high 339 ns after SOURCE H, and T CAS H goes low at 342 ns after SOURCE H. Finally, T RAS L, which will have gone high 309 ns after SOURCE H, disables the selected RAS L lines, thus disabling the memory field which has been accessed. The processor disables SOURCE H 350 ns after enabling it.

5.8 REFRESH CYCLE WITHIN DATA CYCLE

The refresh oscillator completes a cycle every 14 μs, setting the Refresh Request flip-flop and incrementing the refresh address counter. Refresh logic is shown on sheet 2 of the prints. If the Refresh Request flip-flop was set during or before the first 150 ns of a memory data cycle, STROBE H causes the Refresh Go flip-flop to set 159 ns after SOURCE H. REF GO L feeds a delay circuit which causes the assertion of REF GO DLY H.

REF GO H and REF GO DLY H are ANDed with LOCKOUT L. When LOCKOUT L goes high at the end of the read portion of the cycle, the AND gate is enabled, setting the T RAS flip-flop through the preset input. T RAS L then enables LOCKOUT L, clocking the Refresh Cycle flip-flop high.

REF GO H is ANDed with T MUX L (high) to enable REF ADR L (sheet 2 of the prints). This signal combines with T RAS L to enable the eight RAS lines (sheet 4 of the prints). Thus, all eight rows of chips in the array (eight fields) are refreshed with each refresh cycle.

REF ADR H disables the address multiplexers, forcing the outputs high. REF ADR H is also ANDed separately with the seven refresh address counter signals. The first six (MS8-C) or seven (MS8-D) groups of the MOS RAM chip address drivers go high or low in accordance with the state of the six (MS8-C) or seven (MS8-D) refresh address counter lines (sheet 5 of the prints). This combination of signals asserts 1 of the 64 (MS8-C) or 128 (MS8-D) row addresses on the input pins of the MOS RAM chips. Once the row address is latched on each MOS RAM chip, the 64 (MS8-C) or 128 (MS8-D) cells in the selected row on each chip are refreshed.

The seventh group of MOS RAM address drivers is disabled during the refresh cycle on the MS8-C module. Jumper W1 should be open, causing signal RA6 H to go high (sheet 5 of the prints). When REF ADR H goes high with the setting of the REF GO flip-flops, it puts a low level on one leg of each A06 driver, thus disabling them. When the A06 line on the MS8-C module is high, the chip select function on the MOS RAMs is disabled, assuring data integrity in the storage array. On the MS8-D module, the A06 line varies in accordance with the state of the seventh refresh address counter line, in the same manner as the A00 – A05 address lines.

OFF H switches high 280 ns after the T RAS flip-flop sets. This signal resets the T RAS flip-flop after 21 ns, disabling the eight RAS field select lines. OFF L then goes high 31 ns after going low, clocking the Refresh Done flip-flop high (sheet 2). REF DONE H is then ANDed with REF CYCLE H to clear the Refresh Go flip-flop. When REF GO H goes low, it resets the Refresh Cycle flip-flop, ending the refresh cycle.

5.9 WRITE CYCLE

Shortly after the beginning of the refresh cycle, the WRITE H signal goes high, forcing READ L high (sheet 3 of the prints). This enables the four write signals WA L, WB L, WC L, and WD L (sheet 4 of the prints).

T RAS L and OFF AL go high. T RAS H goes low, clocking the Lockout Hold flip-flop high. When the Lockout Hold delay circuit times out, resetting the Lockout Hold flip-flop, LOCKOUT L goes high.

When the processor asserts SOURCE H, the signal is ANDed with BDEN H, NO WRITE L (high), ROM ADR L (high), and LOCKOUT L (high) to set the T RAS L flip-flop through the preset input. T RAS L then starts the write cycle timing sequence.

The memory location address referenced during the cycle is still asserted on the address and extended memory address lines of the Omnibus. The five timing signals, triggered by T RAS L, function the same way for a write cycle as they do for a read cycle. OFF H and T CAS H are initially low. TD STB 1 L, TD STB 2 L, and T MUX L are initially high. The three extended memory address lines are decoded and one of eight RAS L signals is enabled by T RAS L (sheet 3 of the prints). This selects one 4K (MS8-C) or 16K (MS8-D) memory field (12 MOS RAM chips). The high level on T MUX L causes the address multiplexer circuit to select the low order address bits (MA6 L – MA11 L for MS8-C and MA6 L – MA11 L and EMA2 for MS8-D). These signals are latched in the row address register of the selected chips. When T MUX L goes low, the high order memory address signals (MA5 L – MA00 L for MS8-C and MA5 L – MA00 L and EMA1 for MS8-D) are gated to the MOS RAM chips. These signals are loaded into the column address register of the selected chips when T CAS H goes high, enabling CAS A – D L.

On the MS8-C module, EMA 2 H is high and EMA 1 H is low. Jumper W11 is installed while jumpers 12 and 13 are open (sheet 6 of the prints). The four lines A06 A – D L are then high when T MUX L is high and low with the assertion of T MUX L.

On the MS8-D module, four lines A06 A – D L are the seventh MOS RAM address line.

On the MS8-C module, the processor asserts the data to be written on the memory data lines before the beginning of the write cycle. This data remains valid throughout the cycle and is written into the addressed location with the assertion of the chip select (A06 A – D L) and write enable (W A – D L) signals.

On the MS8-D module, data is written only by the assertion of T CAS H when the write enable (W A – D L) signals are asserted.

The write cycle is completed in the same way as the read cycle. When the Lockout Hold flip-flop resets, disabling LOCKOUT L, the MS8-C/MS8-D has completed one memory cycle and is ready to perform another.

CHAPTER 6
MEMORY REFRESH, POWER UP, AND ADDRESS LOGIC

6.1 STALL LOGIC

In two cases it is possible for the processor to request a memory data transfer during a refresh cycle: if processing begins after being halted, or if the processor has stalled its timing and control signals in order to accommodate an I/O transfer, in which case more time is available than in a normal processor cycle.

When an I/O device extends the timing cycle, it asserts NOT LAST XFER L. This puts a high level on the J input of the I/O Stall flip-flop before the assertion of timing pulse TP3 H (sheet 2 of the prints). Timing pulse TP3 H clocks I/O STALL high. When the last transfer takes place and NOT LAST XFER L goes high, it is inverted and ANDed with the next TS4 L to clear the I/O Stall flip-flop.

If a refresh cycle is in progress at this point, the processor must be stalled so that it does not attempt to interrupt the refresh process. When I/O STALL L goes high, it is ANDed with an inverted RUN L to clock the Stall Set flip-flop. If either the Refresh Request or Refresh Cycle flip-flop is set, or if LOCK-OUT L is enabled, Stall Set is set when clocked.

If the processor attempts to initiate a memory data cycle READ H goes high. This signal is ANDed with STALL SET H to put a high level on the J input of the Source DLY flip-flop (sheet 3 of the prints). When SOURCE H goes high the Source DLY flip-flop sets. If ROM ADR A L is high, STALL L is asserted on the Omnibus. This stalls the processor timing chain until the refresh cycle is finished.

When the refresh cycle finishes and OFF H goes high, the T RAS flip-flop resets. When LOCKOUT L goes high, it is ANDed with SOURCE DLY H (high) to set the T RAS flip-flop through the preset input. A normal read cycle follows, except that TD STB 1 L goes low, enabling RESET L. RESET L resets the Source DLY flip-flop, disabling STALL L. At this point, the processor continues its timing chain.

6.2 STANDBY REFRESH REQUEST

When the processor halts, the MS8-C/MS8-D memory cannot synchronize its refresh cycle with the processor timing chain. STROBE L stays high, leaving the clock input to the REF GO flip-flop disabled.

When the refresh oscillator times out, it sets the Refresh Request flip-flop. The Q side of the flip-flop is inverted and fed through an RC network. The delayed output of the RC network is ANDed with MEM RUN L, which is high if the processor is not running, setting the REF GO flip-flop through the preset input. REF GO H is ANDed with T MUX L to produce REF ADR H and REF ADR L. REF GO L feeds an RC network to produce REF GO DLY H (sheet 2 of the prints).

When the three signals LOCKOUT L, REF GO H, and REF GO DLY H are high, they are ANDed to set the T RAS flip-flop through the preset input. From this point on, the refresh cycle (with the processor halted) proceeds in the same way as the normal refresh cycle.

6.3 POWER-UP

The Omnibus signal POWER OK H is generated on the power supply to indicate the condition of the dc voltages to the CPU and memory. In the event of a power-up or momentary power failure and recovery, a low to high transition is produced on POWER OK H (sheet 3 of the prints). This results in a brief positive pulse on MEM INIT H and a negative pulse on MEM INIT L and on CLR L.

MEM INIT H clears the T RAS flip-flop, the Refresh Request flip-flop, and the I/O Stall flip-flop. MEM INIT L clears the Source DLY flip-flop and CLR L clears the MDR Hold flip-flop, initializing the MS8-C/MS8-D memory.

6.4 ROM ADDRESS LOGIC

When the processor addresses ROM memory, and a ROM memory resides in that location, ROM ADR L disables the read/write random access memories in the PDP-8/A system. When ROM ADR A L goes low, it holds low pin 12 of E15, the AND/OR INVERT gate (sheet 3 of the prints), preventing the MS8-C/MS8-D memory from performing a write function. ROM ADR A L also disables MD DIR AL, inhibiting the Omnibus memory data line bus drivers. Thus, it prevents memory from performing a read function.

In addition, ROM ADR L disables TD STB 2 L, inhibiting the clock input of the MDR Hold flip-flop. Thus, it ensures that the MDR remains clear.

CHAPTER 7
TROUBLESHOOTING

7.1 GENERAL

Digital Equipment Corporation recommends module replacement as the repair method for the MS8-C/MS8-D memory. Component replacement is not recommended. However, this chapter is designed to aid those customers who prefer to repair the module by replacing components. This discussion assumes that a system fault has already been traced to the MS8-C/MS8-D memory.

If the diagnostic program can be loaded and executed, the problem should be readily identifiable. However, it might not be possible to load the diagnostic, or the diagnostic might not execute correctly after being loaded.

7.2 VOLTAGE LEVELS

First check the +5 V and −15 V levels supplied to the memory module, and the −5 V and +12 V levels developed on the module. Refer to Table 1-2.

7.3 32K TO 128K MOS MEMORY DIAGNOSTIC (AKVTFA0)

The 32K to 128K MOS memory diagnostic tests MS8 MOS memory by writing and reading various data patterns from memory. It uses a moving inversion (MOV I) pattern. At present, this diagnostic is only available on the WS200 diagnostic diskette (AJRXH-J).

The following procedure is used for running the 32K to 128K MOS memory diagnostic. Display examples are included.

1. Boot diagnostic media. The menu shown in Example 1 appears on your console screen.

Example 1

```
**************************************************************

        WORD PROCESSING DIAGNOSTICS SUPERVISOR PROGRAM
        ----------------------------------------------

THIS PROGRAM IS AN AID TO LOADING AND RUNNING WORD PROCESSOR

DIAGNOSTICS.  INSTRUCTIONS ARE ARRANGED IN A MENU FORMAT.

IF THIS TERMINAL IS A VT100, JUMP SCROLL SHOULD BE SET.

> PRESS RETURN TO DISPLAY DIAGNOSTIC MENU SELECTIONS.

> OR PRESS CTRL C  TO EXIT TO THE MONITOR.

**************************************************************
```

2. Press <CR>. The diagnostic selection menu is displayed (Example 2).

Example 2

```
**************************************************************

        PROCESSER AND MEMORY TESTS
        --------------------------

SELECTIONS ARE:

        A -  4K TO 32K PROCESSER EXERCISER              (AJEXCC)

        B -  32K TO 128K MOS MEMORY TEST                (AKVTFA)

        C -  KT8-A MEMORY MANAGEMENT DIAGNOSTIC         (AJKTAB)



> TYPE THE LETTER AND RETURN TO SELECT A TEST.

> JUST TYPE RETURN TO DISPLAY MORE MENU SELECTIONS.

> OR PRESS CTRL C  TO EXIT TO THE MONITOR.

**************************************************************
```

3. Type B followed by <CR> to select the 32K to 128K MOS memory test. The memory test menu (Example 3) is now displayed.

Example 3

```
**************************************************************

        32K TO 128K MOS MEMORY TEST     (AKVTFA)

OPTIONS ARE:
             1 -  SELECT WHICH MEMORY BANKS TO TEST.

             2 -  BEGIN TESTING THE SELECTED MEMORY.

             3 -  DISPLAY STATISTICS FROM THE PREVIOUS TEST.

> TYPE THE NUMBER TO SELECT THE OPTION.

> OR PRESS CTRL C  TO EXIT TO THE MONITOR.
**************************************************************
```

4. To select which memory banks to test, press 1. This displays a sub-menu (Example 4) that lists the four memory banks and corresponding numbers. (The following steps pertain to selecting Bank 0.)

Example 4

```
**********************************************************************

       MEMORY BANKS SELECTED FOR TESTING
       ---------------------------------

BANK 0 IS SELECTED.

BANK 1 IS NOT SELECTED.

BANK 2 IS NOT SELECTED.

BANK 3 IS NOT SELECTED.

> TYPE THE BANK NUMBER TO SELECT/DESELECT THAT BANK.

> OR PRESS CTRL R  TO RETURN TO THE MEMORY TEST MENU.

**********************************************************************
```

5. Press 0. A new sub-menu (Example 5) appears indicating that Bank 0 has been selected.

Example 5

```
**********************************************************************

       MEMORY BANKS SELECTED FOR TESTING
       ---------------------------------

BANK 0 IS NOT SELECTED.

BANK 1 IS NOT SELECTED.

BANK 2 IS NOT SELECTED.

BANK 3 IS NOT SELECTED.

> TYPE THE BANK NUMBER TO SELECT/DESELECT THAT BANK.

> OR PRESS CTRL R  TO RETURN TO THE MEMORY TEST MENU.

**********************************************************************
```

6. To start the test, press and hold the CTRL key while you type the R key (CTRL/R). The diagnostic again displays the memory test menu (Example 6) so that Bank 0 can be tested.

Example 6

```
B*****************************************************************

        32K TO 128K MOS MEMORY TEST     (AKVTFA)

OPTIONS ARE:
              1 -  SELECT WHICH MEMORY BANKS TO TEST.

              2 -  BEGIN TESTING THE SELECTED MEMORY.

              3 -  DISPLAY STATISTICS FROM THE PREVIOUS TEST.


> TYPE THE NUMBER TO SELECT THE OPTION.

> OR PRESS CTRL C  TO EXIT TO THE MONITOR.
*****************************************************************
```

7. Press 2. This starts the selected test. Another sub-menu appears shortly (Example 7).

Example 7

```
*****************************************************************

PASS #1, PROGRAM IS LOCATED IN BANK 0  FIELD 0

TESTING BANK(S)  0

PRESS CTRL T  TO INTERRUPT TESTING.

- ADDRESS TEST DONE.  STARTING FIRST PATTERN TEST.
- FIRST PATTERN TEST DONE.  STARTING SECOND PATTERN TEST.
- SECOND PATTERN TEST DONE.  STARTING THIRD PATTERN TEST.
- THIRD PATTERN TEST DONE.  STARTING FOURTH PATTERN TEST.
- FOURTH (LAST) PATTERN TEST DONE.
- PROGRAM RELOCATED TO BANK 0  FIELD 1
*****************************************************************
```

8. Allow two to three minutes for the diagnostic to run. Observe that after one sub-test has completed, another begins (Example 7).

NOTE

The diagnostic runs five tests. One is an address test, and four are pattern tests. The address test checks that all locations in memory can be addressed correctly. The pattern tests check that data can be written into and read from memory without errors.

A DONE MESSAGE is displayed as each sub-test is completed (Example 7). If an error is detected during a test, an error message lists the memory bank and field where the error was detected.

At any time during testing, you may interrupt the test. This allows a display of errors that the diagnostic may have found. The following steps explain how to interrupt the test.

9. To interrupt testing, type CTRL/R. After a few seconds, a sub-menu (Example 8) appears which gives you two options.

Example 8

```
**************************************************************

        32K TO 128K MOS MEMORY TEST      (AKVTFA)

OPTIONS ARE:
              1 -  DISPLAY CURRENT STATISTICS, THEN CONTINUE.

              2 -  STOP TESTING; RETURN TO THE MEMORY TEST MENU.


> TYPE THE NUMBER TO SELECT THE OPTION.

**************************************************************
```

NOTE

If you choose to display the total error statistics, press 1. The diagnostic displays the errors found and then continues testing. Example 9 shows an error display.

Example 9

```
**********************************************************************

         STATISTICS FOR THIS RUN
         -----------------------

BANK 0      ERRORS DETECTED = 0
------
BANK 1      NOT SELECTED
------
BANK 2      NOT SELECTED
------
BANK 3      NOT SELECTED
------
**********************************************************************
```

If you choose to stop testing, press 2 (Example 8). The diagnostic returns to the memory test menu (Example 6) and you can start from the beginning of the diagnostic.

A complete test for one bank of memory takes about 15 to 20 minutes. If more banks are selected for testing, the program run time increases accordingly.

7.4 TROUBLESHOOTING WITHOUT DIAGNOSTIC

If memory does not respond to attempts to load the diagnostic, use the following troubleshooting procedures to trace and repair the fault.

7.4.1 Timing and Control

It might be that memory is unable to perform a write operation. Check the timing and control circuitry as follows.

Place the MS8-C/MS8-D module on an extender board. Verify that the T RAS flip-flop is set through the J input following the assertion of SOURCE H. Check that the BDEN H, T MUX L, T CAS H, TD STB 1 L, TD STB 2 H, OFF H, and LOCKOUT L signals are asserted in the correct order, that is in accordance with the timing diagram in Figure 5-2. If these signals are functioning correctly, check the receiver gates on the Omnibus memory data lines. Finally, verify that the T RAS flip-flop is set through the preset input when WRITE H becomes true (high).

7.4.2 Data Not Retained

It is also possible that the data is written into memory but not retained. To determine this, check the refresh oscillator circuit (sheet 2 of the prints), the seven output signals of the refresh address counter, and the refresh logic circuitry.

7.4.3 Data Bits Dropped or Picked Up

If data bits are dropped or picked up on read and write cycles, check that the bus drivers and receivers, and the data latches (sheet 7 of the prints) are functioning properly. Check the data circuits by depositing and examining all 1s, and then all 0s at location 00000. If unexpected results occur, follow up on the symptoms.

Again, using memory location 00000, check for shorts by depositing and examining successively the following data words: 0001, 0002, 0004, 0010, 0020, 0040, 0100, 0200, 0400, 1000, 2000, 4000.

7.4.4 Double Addressing

If any address lines are disabled or shorted, the user may be addressing one location but reading or writing data to another. To determine this, perform the procedures described below.

1. Deposit data word 0000 into the following locations: 00000, 00002, 00004, 00010, 00020, 00040, 00100, 00200, 00400, 01000, 02000, 04000, 10000, 20000, 40000, 00000.

2. Deposit data word 7777 into location 00000.

3. Examine location 00002. The data should be 0000 as deposited in step 1. If the data is 7777, address bit 1 is stuck high or low, or shorted to a lower address bit.

4. Deposit data word 7777 into location 00002.

5. Examine location 00004. The data should be 0000 as deposited in step 1. If the data is 7777, address bit 2 is stuck high or low or shorted to a lower address bit.

6. Follow through the sequence outlined in steps 2 – 5. Deposit 7777 into the locations listed in step 1. Examine each following location to make sure that the data is still 0000.

7.4.5 Dropping Fields

If any of the 4K memory fields are inaccessible for data transfer, check the three extended memory address signals and/or the four bank select lines.

7.4.6 STALL L Held

It is possible that the STALL L signal developed on the memory module is held low. If this is the case, the processor stalls, inhibiting all PDP-8/A system functions. Check the STALL assertion logic (sheets 2 and 3 of the prints).

7.4.7 Faulty MOS RAM Chips

If a data bit at a specific location or group of locations is in error, the corresponding MOS RAM chip can be identified and replaced. For example, if data bit 3 in field 5 (row 5) is consistently wrong, the MOS RAM chip E207 should be replaced. (Refer to Figure 4-2.)

7.4.8 Memory Test Toggle

The following program detects memory locations which fail. This program can be toggled into the PDP-8/A memory using the console switch register.

The program writes data contained in the switch register to all memory locations in the data field set by the operator. The program then reads the data back and checks it. Unless it detects an error, the program runs continuously.

Load the program at address 0020. Then load address 0020 and start. If a halt occurs at address 0047, examine address 10. The number in address 10 is the failing PC plus 1, in the data field selected. The failing word can be found at that address. The expected data is address 0054.

Allow the program to run for about 30 seconds with random patterns. Then halt the CPU. Set another data field and restart the program at location 0020. The user may change the pattern in the switch register while the program is running.

```
*0020

00020   7300    START,  CLA CLL
00021   7421            MQL
00022   3010            DCA 10
00023   6214            RDF
00024   7640            SZA CLA
00025   5031            JMP .+4         /THE DF IS NOT ZERO
00026   1055            TAD K55
00027   7421            MQL
00030   7701            ACL
00031   3010            DCA 10
00032   7604            LAS
00033   3054            DCA WORD
00034   1054            TAD WORD
00035   3410            DCA I 10
00036   1010            TAD 10
00037   7640            SZA CLA
00040   5034            JMP .-4
00041   7701            ACL
00042   3010            DCA 10
00043   1410            TAD I 10
00044   7041            CIA
00045   1054            TAD WORD
00046   7640            SZA CLA
00047   7402            HLT
00050   1010            TAD 10
00051   7640            SZA CLA
00052   5043            JMP .-7
00053   5020            JMP START
00054   0000    WORD,   0000
00055   0055    K55,    0055
        7701    ACL=7701
                $$
```

APPENDIX A
555 TIMER IC

The 555 timer (Figure A-1) contains two voltage comparators used to set and reset flip-flops. The bias voltage (V_{CC}) or the control voltage at pin 5 determines the reference for the comparators. The timer has an open collector output at pin 7 and a buffered output at pin 3. Pin 3 can source or sink up to 100 mA.

When the trigger input at pin 2 goes below one-third V_{CC}, or one-half the control voltage, the flip-flop is set (pin 3 goes high and the discharge transistor turns on). The flip-flop is reset when the voltage at pin 6 exceeds either the control voltage or two-thirds V_{CC}.

The timer is also reset by a low voltage level at pin 4. The timer ignores the trigger input if pin 4 is held low.

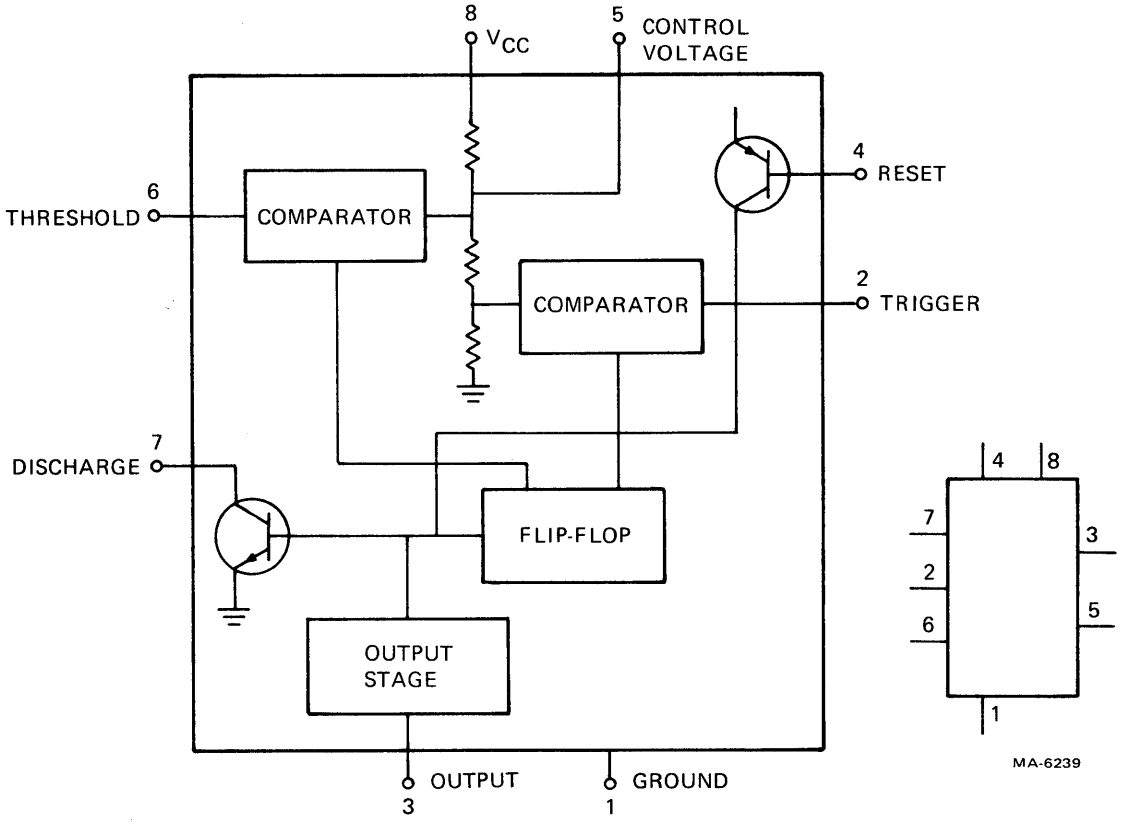

Figure A-1 555 Timer

MS8-C/MS8-D MOS MEMORY
OPERATION AND MAINTENANCE MANUAL
EK-MS8CD-TM-001

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