

M9301-YH

ROM BOOTSTRAP/TEST PROG
MD-11-DQM9A-A

EPDQM9A-A
COPYRIGHT © 1977
FICHE 1 OF 1

JUN 1977
digital
MADE IN USA

The table contains 15 small diagrams or data blocks arranged in a grid. Each block appears to be a technical drawing or a small table of data, possibly representing different memory locations or test patterns for the ROM. The diagrams are too small to read clearly but seem to contain various labels and bit patterns.

801

EOF1DERSDCSEQ

00010000

770526

POP10 411

NEHDR100M9AASEQ

00010000

770526

.MAIN. MACY11 27(1006) 25-APR-77 08:26
 DQM9AA.P11 13-APR-77 11:11 TABLE OF CONTENTS

344	TEST1	THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
359	TEST2	TEST "CLR", MODE "0", AND "BHI", "BVS", "BHI", "BLOS"
376	TEST3	TEST "DEC", MODE "0", AND "BPL", "BEQ", "BGE", "BGT", "BLE"
398	TEST4	TEST "ROA", MODE "0", AND "BVC", "BHS", "BHI", "BNE"
419	TEST5	TEST "BHI", "BLT" AND "BLOS"
439	TEST6	TEST "BLE" AND "BGT"
457	TEST7	TEST REGISTER DATA PATH
484	TEST10	TEST "PL", "BCC", "BLT"
503	TEST11	TEST "A 0", "INC", "COM", AND "BCS", "BLE"
526	TEST12	TEST "R 0", "BIS", "ADD", AND "BLO", "BGE"
549	TEST13	TEST "DEC" AND "BLOS" "BLT"
568	TEST14	TEST "COM", "BIC", AND "BGT", "BGE", "BLE"
593	TEST15	TEST "ADC", "CMP", "BIT", AND "BNE", "BGT", "BEQ"
619	TEST16	TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
646	TEST17	TEST "RSR", "ASL"
677	TEST20	TEST ASH, AND S 08
700	TEST21	TEST "JSR", "RTS", "RTI" & "JMP"
738	TEST22	TEST MAIN MEMORY FROM VIRTUAL 001000 TO LAST ADDR.
786		CACHE MEMORY DIAGNOSTIC TESTS
801	TEST23	TEST CACHE DATA MEMORY
852	TEST24	TEST MEMORY WITH THE DATA CACHE ON
913		BOOTSTRAP ENTRY POINT IS AT 17773000
943		THIS IS THE CODE TO READ THE SWITCH REGISTER AND SWITCHES
977		THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
989		THIS IS THE START OF THE TH11/TU10 BOOT STRAP (MAGNETIC TAPE, TH11)
1007		CODE TO CLEAN UP WORLD AND TRY BOOTSTRAP AGAIN
1013		THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
1020		THIS IS THE START OF THE COMMON READ CODE
1052		THIS IS THE START OF THE RK00/RK06 BOOT STRAP (DISK DUMMY)
1058		THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RP04)
1067		THIS IS THE MEMORY SIZING CODE
1079		THIS IS THE START OF THE RH11/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM, TU16)
1098		THIS IS THE START OF THE PC11 BOOTSTRAP (HIGH SPEED PAPER TAPE READER)
1119		THIS IS THE START OF THE RH11/RM04 BOOT STRAP (FIXED HEAD DISK, RM04)
1124		THIS IS THE START OF THE COMMON RH-70 CODE
1130		THIS IS THE START OF THE RX11/RX01 BOOT STRAP (FLOPPY DISK)
1158		THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)
1166		FUNCTION CODES FOR THE ALL OF THE DEVICES
1198		COMMAND AND STATUS REGISTER ADDRESS TABLE
1211		FUNCTION POINTER TABLE
1223		STARTING ADDRESS TABLE

.REM %

IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DQM9A-A-D
PRODUCT NAME:	POP11/60,POP11/70 ROM BOOTSTRAP/TEST PROGRAM
PROGRAM DATE:	JANUARY 1977
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	JIM KAPADIA

THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE AND SHOULD NOT BE CONSTRUED AS A COMMITMENT BY DIGITAL EQUIPMENT CORPORATION. DIGITAL EQUIPMENT CORPORATION ASSUMES NO RESPONSIBILITY FOR ANY ERRORS THAT MAY APPEAR IN THIS DOCUMENT.

THE SOFTWARE DESCRIBED IN THIS DOCUMENT IS FURNISHED UNDER A LICENSE AND MAY ONLY BE USED OR COPIED IN ACCORDANCE WITH THE TERMS OF SUCH LICENSE.

DIGITAL EQUIPMENT CORPORATION ASSUMES NO RESPONSIBILITY FOR THE USE OR RELIABILITY OF ITS SOFTWARE ON EQUIPMENT THAT IS NOT SUPPLIED BY DIGITAL.

COPYRIGHT (C) 1977 BY DIGITAL EQUIPMENT CORPORATION

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50

67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122

1.0 ABSTRACT

THE M9301-Y-H IS DESIGNED TO PROVIDE BOOT STRAPPING CAPABILITIES FOR THE PDP 11/60 AND PDP 11/70 COMPUTERS. IN ADDITION TO THAT THE M9301-Y-H ALSO INCLUDES ROUTINES THAT PROVIDE BASIC TESTS FOR THE CPU, MEMORY AND THE CACHE.

THE BOOTSTRAP/TEST PROGRAM HAS BEEN DESIGNED FOR FLEXIBILITY OF OPERATION. ITS FUNCTIONS MAY BE INITIATED AUTOMATICALLY ON POWER-UP, OR BY DEPRESSING THE CONSOLE "BOOT" SWITCH OR BY A LOAD ADDRESS AND START SEQUENCE.

A SET OF MICRO-SWITCHES ARE LOCATED ON THE M9301 MODULE. THEY ARE USED BY THE ROUTINES TO DETERMINE WHAT ACTION IS TO BE TAKEN.

2.0 DEVICES SUPPORTED

1. RK11/RK05 DISK
2. RK611/RK06 DISK
3. TC11/TU56 DECTAPE
4. TM11/TU10 MAGTAPE
5. RP11/RP03 DISK
6. RH11/RP04 DISK
7. RH11/TU16 MAGTAPE (800 BPI, NRZI)
8. RH11/RS04 FIXED HEAD DISK
9. RX11/RX01 DISKETTE
10. PC11 HIGH SPEED READER

3.0 INITIATION

THE BOOTSTRAP TEST PROGRAM CAN BE INITIATED IN ONE OF THE FOLLOWING WAYS:

1. AUTOMATICALLY ON POWER UP
2. DEPRESSING "BOOT" SWITCH ON THE CONSOLE
3. LOAD ADDRESS AND START SEQUENCE FROM THE CONSOLE

3.1 POWER-UP START

3.1.1 PDP 11/6X

ON THE PDP 11/6X THERE IS A THREE-POSITION SLIDE SWITCH (BOOT/RUN/HALT) ON THE CONSOLE. IF THIS SWITCH IS LEFT IN THE "BOOT" POSITION AND POWER-UP OCCURS, AN AUTOMATIC BOOTING WILL OCCUR FROM THE PERIPHERAL SPECIFIED IN THE MICRO-SWITCHES (SEE SEC. 5.0). UNIT 0 OF THE DEVICE WILL BE BOOTED. THE TEST ROUTINES WILL BE EXECUTED PRIOR TO BOOTING DEPENDING ON THE SETTING OF MICRO-SWITCHES, SEE SEC. 5.0.

3.1.2 PDP 11/70

IF MICRO-SWITCH 1 ON THE M9301 MODULE IS ON, THEN

123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178

AUTOMATIC BOOTSTRAPPING WILL OCCUR ON POWER UP.
 THE BOOTING WILL BE DONE FROM THE DEVICE SPECIFIED
 IN THE MICRO-SWITCHES. SEE SEC 5.0.

3.2 "BOOT" SWITCH

WHEN THE BOOT SWITCH ON THE CONSOLE IS DEPRESSED,
 BOOTING WILL OCCUR FROM THE PERIPHERAL SELECTED IN
 THE MICRO-SWITCHES, UNIT 0 WILL BE USED. THE TEST
 ROUTINES WILL BE EXECUTED DEPENDING ON THE SETTING OF
 MICRO-SWITCHES, SEE SEC. 5.0.

3.3 CONSOLE

THIS MODE OF OPERATION ALLOWS THE USER TO BOOT FROM
 ANY DEVICE, ANY UNIT NUMBER; (INDICATED
 IN THE CONSOLE SWITCH REGISTER). IF THE CONSOLE SWITCH REGISTER
 IS CLEAR (ONLY THE LOW BYTE NEED TO BE CLEARED), THEN
 THE BOOTING WILL OCCUR FROM THE DEFAULT DEVICE SPECIFIED
 IN THE MICRO-SWITCHES (SEE SEC 5.0). UNIT 0 OF THE
 DEFAULT DEVICE WILL BE USED.

ON THE 11/6X, LOAD ADDRESS 773000.
 ON THE 11/70, LOAD ADDRESS 17773000.

IF THE BOOTING IS TO BE DONE FROM THE DEFAULT DEVICE
 SPECIFIED IN THE MICRO-SWITCHES, THEN CLEAR THE LO-BYTE
 OF THE SWITCH REGISTER AND PRESS START.

IF THE BOOTING IS TO BE DONE FROM ANY DEVICE, THEN
 SWREG<2=0> SHOULD CONTAIN THE DRIVE NUMBER AND
 SWREG<6=3> SHOULD CONTAIN THE DEVICE CODE (SEE SEC 5.0).

AS BEFORE, THE DIAGNOSTIC TESTS WILL BE EXECUTED
 (PRIOR TO BOOTING) DEPENDING ON THE POSITION OF
 MICRO-SWITCHES, SEE SEC. 5.0.

4.0 SWITCH REGISTER--DEVICE CODES, UNIT NUMBER

WHEN THE "LOAD ADDRESS, START" SEQUENCE DESCRIBED IN
 SEC. 3.3 IS USED TO INITIATE THE BOOTSTRAP, THE
 BOOTING WILL OCCUR EITHER FROM THE DEFAULT
 DEVICE SPECIFIED IN THE MICRO-SWITCHES OR THE DEVICE,
 UNIT SPECIFIED IN THE SWITCH REGISTER. THE PROCEDURE
 IS TO LOAD ADDRESS, THEN LOAD THE SWITCH REGISTER PROPERLY
 (SEE TABLE BELOW) AND PRESS START. (CONTROL, START FOR 11/60).

STARTING ADDRESS

 17773000
 773000

PDP 11/70
 PDP 11/6X

SWREG (LO BYTE)

 0
 NON-ZERO

FUNCTION

 BOOT FROM DEFAULT DEVICE, DRIVE 0
 BOOT FROM DEVICE AND DRIVE NUMBER

23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90

- 03 IF OFF, EXECUTE MEMORY-MODIFYING TESTS BEFORE BOOTING (SEE SEC 6.0) (JSR,RTS,RTI, MEMORY TESTS, CACHE TESTS) NOTE: THIS MICRO-SWITCH IS LOOKED AT, ONLY IF 9 IS ON.
- 02 SWITCH SHOULD BE OFF FOR 11/60 SWITCH SHOULD BE ON FOR 11/70 IF BOOT ON POWER UP IS TO BE USED.
- 01 IF OFF, THE LOW ROM (XXX65000-XXX65776) IS DISABLED IF ON, THE LOW ROM IS ENABLED NORMAL POSITION OF SW 01 IS ON.

MICRO-SWITCH OPTION B IS PROVIDED TO PROTECT THE USER AGAINST UNINTENTIONAL OR NON-AUTHORIZED SETTING OF THE CONSOLE SWITCH REGISTER. NORMALLY, ON POWER-UP (SUBSEQUENT TO POWER-FAIL) BOOTING WILL BE DONE FROM THE DEVICE CODE SPECIFIED IN THE MICRO-SWITCHES (ON M9301 MODULE), PROVIDED THE CONSOLE SWITCH REGISTER IS CLEAR. IF THE CONSOLE SWITCH REGISTER IS NOT CLEAR, THE PROGRAM WILL USE THE CODE SPECIFIED IN THE SWITCH REGISTER FOR SELECTING THE DEVICE TO BOOT FROM. IF THE MICRO-SWITCH IS LEFT IN THE OFF POSITION, THE BOOT STRAP PROGRAM WILL NOT SENSE THE CONSOLE SWITCH REGISTER; THUS ELIMINATING THE POSSIBILITY OF ATTEMPTING TO BOOT FROM AN UNDESIRED OR NON-EXISTENT PERIPHERAL IN CASE CONSOLE SWITCH REGISTER IS SET RANDOMLY.

6.0 TEST ROUTINES IN M9301-YH

THE M9301-YH HAS TESTS TO CHECK OUT THE CPU (INSTRUCTIONS), CACHE AND MEMORY (UP TO 28K). THERE ARE TWO TYPES OF TESTS.

1. NON-MEMORY MODIFYING TESTS
2. MEMORY-MODIFYING TESTS

THE CPU INSTRUCTION TESTS ARE NON-MEMORY MODIFYING AND ARE EXECUTED PRIOR TO BOOTING IF MICRO-SWITCH 9 IS ON. SEE SEC 5.0.

THE MEMORY-MODIFYING TESTS CONSTITUTES THE TESTS FOR RTS,RTI,JSR INSTRUCTIONS, TESTS FOR THE CACHE AND THE TESTS FOR THE MEMORY. THESE TESTS ARE EXECUTED PRIOR TO BOOTING IF MICRO-SWITCHES 9 IS ON AND MICRO-SWITCH 3 IS OFF. SEE SEC. 5.0.

6.1 CPU TESTS

THIS SECTION CONSISTS OF SEVERAL SUB-TESTS WHICH CHECK THE CPU DATA PATH AND CONTROL LOGIC USING VARIOUS INSTRUCTIONS.

6.2 MAIN MEMORY TEST

THIS TEST CHECKS OUT THE MAIN MEMORY (UP TO 28K), WITH THE CACHE DISABLED. PARITY ERROR VECTOR HAS BEEN

291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327

SET UP, HENCE PARITY ERRORS IF FOUND WILL BE DETECTED.

6.3 CACHE TEST

THIS SECTION HAS TESTS TO CHECK THE CACHE. THE TEST CHECKS IF THE CACHE HITS CAN BE OBTAINED ALL THE WAY THROUGH THE MEMORY. ALSO, THE DATA MEMORY OF THE CACHE IS CHECKED. DIFFERENT TEST PARAMETERS ARE USED (WHERE NEEDED) TO TEST THE PDP 11/60 AND THE PDP 11/70 CACHE.

7.0 ERROR RECOVERY AND RETRY:

7.1 ERRORS DURING BOOTING

IF A DEVICE ERROR IS DETECTED, WHILE TRYING TO BOOT, A "RESET" WILL BE ISSUED AND THE BOOTSTRAP WILL TRY AGAIN. THIS WOULD ALLOW DEVICES TO COME ON-LINE (INTO LOAD POSITION) AFTER A POWER-UP SUBSEQUENT TO POWER-FAIL.

7.2 ERRORS DURING TESTING

IF AN ERROR IS DETECTED DURING THE EXECUTION OF THE TEST ROUTINES THE PROCESSOR WILL HALT, INDICATING TO THE USER THAT A MALFUNCTION HAS BEEN DETECTED. THE CONSOLE LIGHTS WILL INDICATE THE "PC" AT WHICH THE "HALT" OCCURRED. MORE INFORMATION ABOUT THE FAILURE CAN BE OBTAINED BY REFERENCING THE BOOTSTRAP/TEST LISTINGS AT THE ERROR "PC".

IF AN ERROR OCCURS IN CACHE TESTS, THE USER HAS AN OPTION TO CONTINUE AND BOOT BY PRESSING THE "CONTINUE" SWITCH ON THE CONSOLE. HOWEVER, IN THE ABOVE CASE CACHE MISSES WILL BE FORCED, TO PREVENT FURTHER ERRORS FROM CACHE.

%

K01

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 8
DOMSRA.P11 13-APR-77 11:11

328
329
330
331
332
333
334
335
336
337
338
339

340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395

165000

165000
165000
165000 000401
165002 000000

165004
165004 005006
165006 100403
165010 102402
165012 101001
165014 101401
165016 000000

165020
165020 005306
165022 100004
165024 001403
165026 002002
165030 003001
165032 003401
165034 000000

```

      = BASE1
;:*****
      .SBTTL TEST1 THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
;:
;: THE REGISTER AND CONDITION CODES ARE ALL UNDEFINED WHEN
;: THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
;: THE COMPLETION OF THIS TEST.
;:*****
TST1:
DIAG:
      BR      TST2          ; * BRANCH ALWAYS
      HALT
;:*****
      .SBTTL TEST2 TEST "CLR", MODE "0", AND "BMI", "BVS", "BHI", "BLOS"
;:
;: THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
;: THIS TEST IS ENTERED. UPON COMPLETION OF THIS TEST THE "SP"
;: (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
;:*****
TST2:
      CLR      SP          ; N=0, Z=1, V=0, C=0, SP=000000
      BMI      1$          ; V BRANCH IF N=1
      BVS      1$          ; V BRANCH IF V=1
      BHI      1$          ; V BRANCH IF Z AND C ARE BOTH 0
      BLOS     TST3        ; * BRANCH IF (Z XOR C)=1
1$:
      HALT
;:*****
      .SBTTL TEST3 TEST "DEC", MODE "0", AND "BPL", "BEQ", "BGE", "BGT", "BLE"
;:
;: UPON ENTERING THIS TEST THE CONDITION CODES ARE:
;: N = 0, Z = 1, V = 0, AND C = 0.
;: THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
;: R3 = ?, R4 = ?, R5 = ? SP = 000000
;: UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
;: N = 1, Z = 0, V = 0, AND C = 0
;: THE REGISTERS AFFECTED BY THE TEST ARE:
;: SP = 177777
;:*****
TST3:
      DEC      SP          ; N=1, Z=0, V=0, C=0, SP=177777
      BPL      1$          ; V BRANCH IF N=0
      BEQ      1$          ; V BRANCH IF Z=1
      BGE      1$          ; V BRANCH IF (N XOR V)=0
      BGT      1$          ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
      BLE      TST4        ; * BRANCH IF [Z OR (N XOR V)]=1
1$:
      HALT

```

MO1

398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451

165036
165036 006006
165040 102003
165042 103002
165044 101001
165046 001001
165050 000000

165052
165052 000264
165054 101003
165056 000270
165060 002401
165062 101401
165064 000000

165066
165066 000244

.SBTTL TEST4 TEST "ROR", MODE "0", AND "BVC", "BHIS", "BHI", "BNE"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 177777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 0, Z = 0, V = 1, AND C = 1
THE REGISTERS AFFECTED BY THE TEST ARE:
SP = 077777

†ST4:
ROR SP ;N=0,Z=0,V=1,C=1,SP=077777
BVC IS ;V BRANCH IF V=0
BHIS IS ;V BRANCH IF C=0
BHI IS ;V BRANCH IF C AND Z ARE BOTH 0
BNE †ST5 ;* BRANCH IF Z=0
IS: HALT

.SBTTL TEST5 TEST "BHI", "BLT", AND "BLOS"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 077777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 1, Z = 1, V = 1, AND C = 1
THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

†ST5:
SEZ ;N=0,Z=1,V=1,C=1
BHI IS ;V BRANCH IF Z AND C ARE BOTH 0
SEN ;N=1,Z=1,V=1,C=1
BLT IS ;V BRANCH IF (N XOR V)=1
BLOS †ST6 ;* BRANCH IF (Z OR C)=1
IS: HALT ;STOP HERE IF A BRANCH FAILED

.SBTTL TEST6 TEST "BLE" AND "BGT"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 1, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 077777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 1, Z = 0, V = 1, AND C = 1
THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

†ST6:
CLZ ;N=1,Z=0,V=1,C=1

452 165070 003401
453 165072 003001
454 165074 000000

BLE IS ; V BRANCH IF (Z OR (N XOR V))=1
BGT TST7 ; * BRANCH IF Z AND (N XOR V) ARE BOTH 0
IS: HALT ; STOP HERE IF A BRANCH FAILED

.SBTTL TEST7 TEST REGISTER DATA PATH

* WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
* N = 1, Z = 0, V = 1, AND C = 1.
* THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
* R3 = ?, R4 = ?, R5 = ?, SP = 077777.
* UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
* N = 0, Z = 1, V = 0, AND C = 0.
* THE REGISTERS ARE LEFT AS FOLLOWS:
* R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
* R4 = 125252, R5 = 125252, AND SP = 125252

470 165076
471 165076 012706 125252
472 165102 010600
473 165104 010001
474 165106 010102
475 165110 010203
476 165112 010304
477 165114 010405
478 165116 160501
479 165120 002401
480 165122 001401
481 165124 000000

TST7:
MOV #125252, SP ; N=1, Z=0, V=0, C=1, SP=125252
MOV SP, R0 ; N=1, Z=0, V=0, C=1, R0=125252
MOV R0, R1 ; N=1, Z=0, V=0, C=1, R1=125252
MOV R1, R2 ; N=1, Z=0, V=0, C=1, R2=125252
MOV R2, R3 ; N=1, Z=0, V=0, C=1, R3=125252
MOV R3, R4 ; N=1, Z=0, V=0, C=1, R4=125252
MOV R4, R5 ; N=1, Z=0, V=0, C=1, R5=125252
SUB R5, R1 ; N=0, Z=1, V=0, C=0, AND R1=000000
BLT IS ; V BRANCH IF (N XOR V)=1
BEQ TST10 ; * BRANCH IF Z=1
IS: HALT

.SBTTL TEST10 TEST "ROL", "BCC", "BLT"

* WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
* N = 0, Z = 1, V = 0, AND C = 0.
* THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
* R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
* UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
* N = 0, Z = 0, V = 1, AND C = 1.
* THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
* R2 WHICH SHOULD NOW EQUAL 052524.

496 165126
497 165126 006102
498 165130 103001
499 165132 002401
500 165134 000000

TST10:
ROL R2 ; N=0, Z=0, V=1, C=1, AND R2 = 052524
BCC IS ; V BRANCH IF C=0
BLT TST11 ; * BRANCH IF (N XOR V)=1
IS: HALT

.SBTTL TEST11 TEST "ADD", "INC", "COM", AND "BCS", "BLE"

* WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
* N = 0, Z = 0, V = 1, AND C = 1.
* THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524

501
502
503
504
505
506
507

TEST11 TEST "ADD", "INC", "COM", AND "BCS", "BLE"

R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000

TST11:

```
ADD R2,R3 ;(R2 = 052524) + (R3 = 125252)
INC R3 ;N=1,Z=0,V=0,C=0, AND R3=177776
COM R3 ;N=1,Z=0,V=0,C=0, AND R3=177777
ADD R3,R1 ;N=0,Z=1,V=0,C=1, AND R3 = 000000
BCS IS ;N=0,Z=1,V=0,C=0, AND R1 = 000000
BLE TST12 ; V BRANCH IF C=1
HALT ; * BRANCH IF (Z OR (N XOR V))=1
```

.SBTTL TEST12 TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R3 WHICH SHOULD BE MODIFIED TO 000000, AND
R4 WHICH SHOULD NOW EQUAL 052525

TST12:

```
ROR R4 ;N=0,Z=0,V=1,C=0, AND R4 = 052525
BIS R4,R3 ;N=0,Z=0,V=0,C=0, AND R3 = 052525
ADD R5,R3 ;N=1,Z=0,V=0,C=0, AND R3 = 177777
INC R3 ;N=0,Z=1,V=0,C=0, AND R3 = 000000
BLO IS ; V BRANCH IF C=1
BGE TST13 ; * BRANCH IF (N XOR V)=0
HALT
```

.SBTTL TEST13 TEST "DEC" AND "BLOS", "BLT"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R1 WHICH SHOULD NOW EQUAL 177777

TST13:

```
DEC R1 ;N=1,Z=0,V=0,C=0,R1=177777
BLOS IS ; V BRANCH IF (Z OR C)=1
```

508
509
510
511
512
513
514
515 165136
516
517 165136 060203
518 165140 005203
519 165142 005103
520 165144 060301
521 165146 103401
522 165150 003401
523 165152 000000
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561 165172
562 165172 005301
563 165174 101401

TEST13 TEST "DEC" AND "BLOS", "BLT"

564 165176 002401
565 165200 000000

BLT TST14 ; * BRANCH IF (N XOR V)=1
1S: HALT

.SBTTL TEST14 TEST "COM", "BIC", AND "BGT", "BGE", "BLE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 052524
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R0 WHICH SHOULD NOW EQUAL 052525, AND
R1 WHICH SHOULD NOW EQUAL 052524

TST14:

COM R0 ; N=0, Z=0, V=0, C=1, AND R0 = 052525
BLOS 2S ; * BRANCH IF (Z OR C)=1

2S: BIC R0,R1 ; STOP HERE IF BRANCH FAILED
ADD R1,R1 ; N=1, Z=0, V=0, C=1, AND R1 = 125252

BGT 1S ; N=0, Z=0, V=1, C=1, AND R1 = 052524
BGE 1S ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0

BLE TST15 ; V BRANCH IF (N XOR V)=0
1S: HALT ; * BRANCH IF (Z OR (N XOR V))=1

.SBTTL TEST15 TEST "ADC", "CMP", "BIT", AND "BNE", "BGT", "BEQ"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 052524
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE NOW:
R0 = 052525, R1 = 000000, R2 = 052524, R3 = 000000
R4 = 052525, R5 = 052525, SP = 125252.

TST15:

ADC R1 ; N=0, Z=0, V=0, C=0, AND R1 = 052525
CMP R4,R1 ; N=0, Z=1, V=0, C=0

607 165224 005501
608 165226 020401
609 165230 001005

BNE 1S ; V BRANCH IF Z=0
R1 = 052525 R5 = 125252

611 165232 030105
612 165234 003003
613 165236 005105

BIT R1,R5 ; N=0, Z=1, V=0, C=0
BGT 1S ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
COM R5 ; N=0, Z=0, V=0, C=1, AND R5 = 052525

614 165240 160501
615 165242 001401
616 165244 000000

SUB R5,R1 ; N=0, Z=1, V=0, C=0, AND R1 = 000000
BEQ TST16 ; * BRANCH IF Z=1
1S: HALT

.SBTTL TEST16 TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"

617
618
619

620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675

165246 112700 177401
165246 100001
165252 000000
165254 077002
165256 005001
165262 005201
165264 077002
165266 005700
165270 001002
165272 005701
165274 001401
165276 000000

165300 012700 100000
165304 005201
165306 012702 000020
165312 006200
165314 005500
165316 006301
165320 005501
165322 077205

165324 060001
165326 003401
165330 003001
165332 000000

```
*****
*
* WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
* N = 0, Z = 1, V = 0, AND C = 0.
* THE REGISTERS ARE: R0 = 052525, R1 = 000000, R2 = 052524
* R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
* UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
* N = 0, Z = 1, V = 0, AND C = 0.
* R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
* R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
*
*****
TST16:
MOVB #177401, R0 ; N=0 Z=0 V=0 C=0 AND R0 = 000001
BPL 2$ ; * BRANCH IF N=0
HALT ; STOP IF "BPL" FAILED
1$: SOB R0, 1$ ; DO NOT LOOP SINCE (R0 - 1) = 0
2$: CLR R1 ; N=0, Z=1, V=0, C=0, AND R1 = 000000
3$: INC R1 ; INCREMENT 64K TIMES (2 ** 16)
SOB R0, 3$ ; LOOP BACK TO "INC" 64K TIMES
TST R0 ; N=0, Z=1, V=0, C=0, AND R0 = 000000
BNE 4$ ; V BRANCH IF Z=0
TST R1 ; N=0 Z=1 V=0 C=0 AND R1 = 000000
PEQ TST17 ; * BRANCH IF Z=1
4$: HALT

*****
.SBTTL TEST17 TEST "ASR", "ASL"
*
* WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
* N = 0, Z = 1, V = 0, AND C = 0.
* THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 052524
* R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
* UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
* N = 0, Z = 0, V = 0, AND C = 0.
* THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
* R0 WHICH IS NOW EQUAL TO 000000,
* R1 WHICH IS NOW 000001, AND
* R2 WHICH IS NOW 000000.
*
*****
TST17:
MOV #100000, R0 ; R0=100000
INC R1 ; R1=000001
MOV #1016, R2 ; SET COUNTER TO 16 DECIMAL
1$: ASR R0 ; RIGHT SHIFT R0, SIGN EXTEND (16 TIMES)
ADC R0 ; ADD CARRY (0 UNTIL LAST TIME)
ASL R1 ; LEFT SHIFT R1 (16 TIMES)
ADC R1 ; ADD CARRY (0 UNTIL LAST TIME)
SOB R2, 1$ ; LOOP BACK 16 DECIMAL TIMES
; AT THE END OF THE LOOP
R0 = 000000 AND R1 = 000001
2$: ADD R0, R1 ; N=0 Z=0 V=0 C=0 R1=000001, R0=000000
BLE 2$ ; V BRANCH IF [Z OR (N XOR V)]=1
BGT TST20 ; * BRANCH IF Z AND (N XOR V) ARE BOTH 0
2$: HALT
```

TEST17 TEST "ASR", "ASL"

676
677
678
679
680
681
682
683
684
685
686
687
688
689 165334
690 165334 072127 000015
691
692 165340 000301
693
694 165342 072127 177770
695
696 165346 001401
697 165350 000000
698
699
700
701
702
703
704
705
706
707
708
709
710 165352
711
712 165352 032737 000400 173024
713
714
715 165360 001001
716 165362 000571
717 165364 012706 000776
718 165370 004767 000002
719 165374 000000
720 165376 022716 165374
721 165402 001401
722 165404 000000
723 165406 012716 165416
724 165412 000207
725 165414 000000
726 165416 005046
727 165420 012746 165430
728 165424 000002
729 165426 000000
730 165430 000137 165436
731 165434 000000

: .SBTTL TEST20 TEST ASH, AND SWAB

: *
: * WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
: * N = 0, Z = 0, V = 0, AND C = 0.
: * THE REGISTERS ARE: R0 = 000000, R1 = 000001, R2 = 000000
: * R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
: * UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
: * N = 0, Z = 1, V = 0, AND C = 1.
: * THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
: * R1 WHICH SHOULD NOW EQUAL 000000
: *

: TST20:
: ASH #15,R1 ;LEFT SHIFT BIT0 INTO BIT15
: ;N=1,Z=0,V=1,C=0, AND R1 = 100000
: SWAB R1 ;SWITCH BYTES OF R1, R1 = 000200
: ;N=1,Z=0,V=0,C=0
: ASH #-10,R1 ;RIGHT SHIFT R1 8 PLACES
: ;N=0,Z=1,V=0,C=0, R1 = 000000
: BEQ TST21 ; * BRANCH IF Z=1
: HALT ;EITHER "SWAB" OR "ASH" FAILED

: .SBTTL TEST21 TEST "JSR", "RTS", "RTI", & "JMP"

: * THIS TEST FIRST SETS THE STACK POINTER TO 776,
: * AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
: * ALL WORK PROPERLY.
: *
: * ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
: * TO 00776 AND IS LEFT THAT WAY ON EXIT.
: *

: TST21:
: BIT #400, @#173024 ;DO THE MEMORY-MODIFYING
: ;GROUP OF TESTS? (THIS TEST,
: ;MEMORY TEST, CACHE TEST)
: YES
: BR JUMPO ;SKIP, GO DIRECTLY TO BOOT
: 11\$: MOV #776, SP ;SET UP THE STACK POINTER
: JSR PC, 1\$;TRY TO JSR TO 1\$
: 10\$: HALT ;THE "JSR" MUST HAVE FAILED
: 1\$: CMP #10\$, (SP) ;WAS THE CORRECT ADDRESS PUSHED?
: BEQ 2\$;BRANCH IF YES
: HALT ;WRONG THING PUSHED ON STACK
: 2\$: MOV #3\$, (SP) ;CHANGE THE ADDRESS ON THE STACK
: RTS PC ;TRY TO RETURN TO 3\$
: HALT ;DID NOT RETURN PROPERLY
: 3\$: CLR -(SP) ;PUSH A ZERO ON THE STACK
: MOV #4\$, -(SP) ;PUSH THE RETURN ADDRESS ON STACK
: RTI ;SEE IF AN "RTI" WORKS
: HALT ;THE "RTI" FAILED
: 4\$: JMP @#5\$;TRY TO "JMP"
: HALT ;THE "JMP" FAILED

F02

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 16
 DQM9AA.P11 13-APR-77 11:11

TEST21 TEST "JSR", "RTS", "RTI", & "JMP"

732 165436

5\$: ;ADDRESS TO "JMP" TO

733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783

165436
165436 012700 165446
165442 000137 173310
165446 012737 165750 000114
165454 005037 000116
165460 012703 177746
165464 012713 000014
165470 012702 001000
165474 010200
165476 010010
165500 005720
165502 020005
165504 101774
165506 010200
165510 011001
165512 020001
165514 001401
165516 000000
165520 005120
165522 020005
165524 101771
165526 014001
165530 005101
165532 020001
165534 001401
165536 000000
165540 020002
165542 001371

 .SBTTL TEST22 TEST MAIN MEMORY FROM VIRTUAL 001000 TO LAST ADDR.

 THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
 VIRTUAL ADDRESS 001000 TO LAST ADDR. IF THE DATA DOES NOT COMPARE
 PROPERLY THE TEST WILL HALT AT EITHER 165516 OR 165536. IF A
 PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165750, WITH
 THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE.

 IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
 R0 = 001000, R1 = DATA READ, R2 = 001000, R3 = 177746 (CACHE CONTROL REG.)
 R4 = COUNT VALUE, R5 = LAST MEMORY ADDRESS SP = 000776

TEST22:
 MOV #105,R0 ;SAVE RETURN ADDRESS
 JMP @#SIZE ;GO SIZE MEMORY, RETURN WITH R5 CONTAINING
 ;THE LAST MEMORY ADDRESS
 10\$: MOV #CONT,@#114 ;SET UP PARITY VECTOR
 CLR @#116 ;SET PROCESSOR STATUS WORD TO ZERO
 MOV #177746,R3 ;CACHE CONTROL REGISTER ADDRESS
 MOV #MISS,(R3) ;FORCE MISS BOTH GROUPS
 MOV #1000,R2 ;FIRST ADDRESS STORAGE
 MOV R2,R0 ;SETUP FIRST ADDRESS
 1\$: MOV R0,(R0) ;LOAD EACH ADDRESS WITH ITS
 ;OWN ADDRESS
 TST (R0)+
 CMP R0,R5
 BLOS 1\$
 MOV R2,R0 ;SET STARTING ADDRESS IN R0
 2\$: MOV (R0),R1 ;GET THE DATA
 CMP R0,R1 ;IS IT CORRECT?
 BEQ 3\$;BRANCH IF YES
 HALT ;DATA ERROR ON READING MEMORY LOCATION
 ;R0=ADDRESS, R1=DATA RECEIVED, R0=DATA EXPECTED
 3\$: COM (R0)+ ;COMPLEMENT DATA AND INCREMENT ADDRESS
 CMP R0,R5
 BLOS 2\$
 4\$: MOV -(R0),R1 ;READ THE DATA (IT SHOULD NOW BE THE
 ;COMPLEMENT OF THE ADDRESS)
 COM R1 ;COMPLEMENT BEFORE CHECKING
 CMP R0,R1 ;IS THE DATA CORRECT?
 BEQ 5\$;BRANCH IF YES
 HALT ;DATA ERROR ON READING MEMORY LOCATION
 ;R0=ADDRESS, R1=DATA RECEIVED, R0=DATA EXPECTED
 5\$: CMP R0,R2
 BNE 4\$

840	165614	000457		BR	BOOTMISS		;ABORT REST OF TEST IF "CONTINUE" PRESSED
841	165616	105116		4S: COMB	(SP)		
842	165620	001362		BNE	3S		
843	165622	005720		TST	(R0)+		;MOVE TO NEXT ADDRESS
844	165624	077220		SOS	R2,3S		;BRANCH IF NOT DONE
845	165626	012713	000044	MOV	#GRP1,(R3)		;FORCE REPLACE GROUP 1 AND FORCE MISS GROUP 0 (ON 11/70)
846							;FORCE MISS LOWER 1/2 K OF CACHE ON 11/60
847	165632	012700	005000	MOV	#6000,R0		
848	165636	105166	000001	COMB	1(SP)		;COMPLEMENT THE CYCLE FLAG
849	165642	001347		BNE	1S		;LOOP IF NOT DONE

;*****

.SBTTL TEST24 TEST MEMORY WITH THE DATA CACHE ON

THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU LAST ADDRESS TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN MEMORY. ON THE PDP 11/70, IT STARTS WITH GROUP 1 ENABLED, THEN TESTS GROUP 0, AND FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED. ON THE PDP 11/60, THE TEST IS DONE WITH THE WHOLE CACHE ENABLED.

UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = (FIRST ADDRESS),
R3 = 177746 (CONTROL REG.),
R5 = (LAST MEMORY ADDRESS), SP = 776

UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS 001000 THRU LAST ADDRESS WILL CONTAIN ITS OWN VIRTUAL ADDRESS.

;*****

TEST24:

870	165644			MOV	#1000,R2		;SETUP FIRST ADDRESS
871	165644	012702	001000	MOV	R2,R0		;FIRST ADDRESS IS 1000 OCTAL
872	165650	010200		1S: MOV	R0,(R0)		;FILL MEMORY WITH ADDRESSES
873	165652	010010		TST	(R0)+		
874	165654	005720		CMP	R0,R5		
875	165656	020005		BLOS	1S		
876	165660	101774		MOV	#3,R1		;SET PASS COUNT TO THREE
877	165662	012701	000003	CLR	(SP)		
878	165666	005016		BIT	#2,#173024		;MICRO-SWITCH 2 INDICATES PDP 11/60 OR 11/70
879	165670	032737	000002	BEQ	6S		;IT IS PDP 11/60
880	165676	001420		MOV	#GRP0,(SP)		;LOAD CODE TO FORCE GROUP 0 ONTO STACK
881	165700	012716	000030	2S: MOV	R2,R0		;FIRST ADDRESS
882	165704	010200		3S: COM	(R0)		;DOUBLE COMPLEMENT DATA AND
883	165706	005110		COM	(R0)		;MAKE SURE IT IS IN THE CACHE.
884	165710	005110		CMP	R0,(R0)		;COMPARE DATA, AND SET BIT 0 IN HIT/MISS REG
885	165712	020010					;ALSO POINT TO NEXT ADDRESS
886				BEQ	5S		;BRANCH IF DATA MATCHES
887	165714	001401		HALT			;DATA DIDN'T MATCH R0 = ADDRESS + 2
888	165716	000000		5S: TST	(R0)+		
889	165720	005720		ROR	#177752		;WAS THE LAST MEMORY REFERENCE A HIT?
890	165722	006037	177752	BCS	4S		;BRANCH IF YES
891	165726	103402		HALT			;HIT FAILED TO OCCUR R0 = ADDRESS + 2
892	165730	000000		BR	BOOTMISS		;ABORT REST OF TEST IF "CONTINUE" PRESSED
893	165732	000410		4S: CMP	R0,R5		
894	165734	020005		BLOS	3S		
895	165736	101763					

K02

MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 21
 DQM99A.P11 13-APR-77 11:11 THIS IS THE CODE TO READ THE SWITCH REGISTER AND SWITCHES

```

969
970
971 173112 032737 000010 173024 CHKSWR: BIT      #10,2#173024 ; IS MICRO-SWITCH SET TO
972                                     ; DISABLE LOOKING AT SWITCH REGISTER?
973 173120 001340                                     BNE      START1 ; IF OFF, DONT LOOK AT SWR
974 173122 000734                                     BR       START  ; IF ON, SENSE THE CONSOLE SWREG
975
976
977                                     .SBTTL THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
978                                     ;COMMAND REGISTER ADDRESS IS 177342
979
980 173124 010211 TU56:  MOV      R2,(R1) ; LOAD UNIT NUMBER INTO C.S.R.
981 173126 052311     BIS      (R3)+,(R1) ; 'OR' REWIND COMMAND INTO C.S.R.
982 173130 075711 1S:   TST      (R1) ; SEE IF ERROR BIT IS SET
983 173132 100376     BPL      1S ; WAIT UNTIL BIT 15 OF C.S.R. IS SET
984 173134 005761 177776 TST      -2(R1) ; IS THE ERROR 'END ZONE'
985 173140 100017     BPL      AGAIN ; BRANCH IF NOT 'END ZONE'
986 173142 000420     BR       RPO3
987
988
989                                     .SBTTL THIS IS THE START OF THE TM11/TU10 BOOT STRAP (MAGNETIC TAPE, TM11)
990                                     ;COMMAND REGISTER ADDRESS IS 172522
991
992 173144 010211 TU10:  MOV      R2,(R1) ; LOAD UNIT NUMBER INTO C.S.R.
993 173146 006061 177776 1S:   ROR      -2(R1) ; IS THE SELECTED DRIVE ON LINE
994 173152 103375     BCC      1S ; WAIT FOR BIT TO BE SET BY DRIVE
995 173154 052311     BIS      (R3)+,(R1) ; 'OR' REWIND COMMAND INTO C.S.R.
996                                     ; THIS COMMAND ALSO SETS 800 BPI 9 CHAN.
997 173156 105711 2S:   TSTB     (R1) ; SEE IF THE REWIND IS COMPLETE
998 173160 100376     BPL      2S ; WAIT FOR READY BIT OF C.S.R. TO BE SET
999 173162 012761 177777 000002 MOV      #-1,2(R1) ; SET RECORD COUNTER TO SKIP ONE RECORD
1000 173170 112311     MOVB     (R3)+,(R1) ; LOAD SPACE FORWARD COMMAND INTO C.S.R.
1001 173172
1002 173172 030511 TU10A: 3S:   BIT      R5,(R1) ; TEST FOR 'ERROR' AND 'READY' BITS
1003 173174 001776     BEQ      3S ; BRANCH IF NEITHER SET
1004 173176 100003     BPL      CMNSGO ; BRANCH TO COMMON READ IF NO ERRORS
1005
1006
1007                                     .SBTTL CODE TO CLEAN UP WORLD AND TRY BOOTSTRAP AGAIN
1008
1009 173200 000005 AGAIN:  RESET ; CLEAR ALL DEVICES AFTER ERROR
1010 173202 000743     BR       CHKSWR ; GO SET UP MEMORY MANAGEMENT AND UNIBUS MAP
1011                                     ; AND ATTEMPT TO BOOT AGAIN.
1012
1013                                     .SBTTL THIS IS THE START OF THE RP11/RPO3 BOOT STRAP (DISK PACK, RP11-C)
1014                                     ;COMMAND REGISTER ADDRESS IS 176714
1015
1016 173204 010211 RPO3:  MOV      R2,(R1) ; LOAD THE UNIT NUMBER INTO THE COMMAND REG.
1017
1018
1019
1020                                     .SBTTL THIS IS THE START OF THE COMMON READ CODE
1021
1022 173206 012761 177000 000002 CMNSGO: MOV      #-512,2(R1) ; LOAD WORD COUNT OF 256 WORDS
1023 173214 112302     MOVB     (R3)+,R2 ; LOAD READ FUNCTION INTO LO BYTE
1024                                     ; & THEN LOAD READ FUNCTION INTO C.S.R.

```


L02

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 22
 DQM9AA.P11 13-APR-77 11:11

THIS IS THE START OF THE COMMON READ CODE

1025						
1026						;NOTE: THE ABOVE IS DONE BECAUSE RK611 ;DOES NOT RECOGNIZE BYTE OPERATIONS ;ON THE BUS. ;CLEAR OUT LO BYTE OF THE C.S.R.
1027						
1028	173216	042711	000377	BIC	#377,(R1)	
1029	173222	000402		BR	CMN1	
1030						
1031						
1032		173224		.=BASE4		;ASSEMBLED AT 773224 & 773226 ;VECTOR TO THE START OF M9301 BOOTSTRAP ;PROCESSOR STATUS TO ASSUME AT BOOT TIME
1033	173224	173000		.WORD	173000	
1034	173226	000340		.WORD	000340	
1035						
1036	173230	050211		CMN1:	BIS R2,(R1)	;MOVE THE READ FUNCTION INTO C.S.R.
1037	173232	105711		G01:	TSTB (R1)	;TEST FOR 'READY' BIT
1038	173234	100376			BPL G01	;WAIT UNTIL READY IS SET
1039	173236	005711			TST (R1)	;TEST FOR ERROR BIT
1040	173240	100005			BPL CLRCS	;NO ERROR
1041	173242	105713			TSTB (R3)	;IS IT TU16?
1042	173244	001355			BNE AGAIN	;NO
1043	173246	021361	000014		CMP (R3),14(R1)	;IF YES, WAS THE ERROR A FRAME COUNT EROR?
1044	173252	001352			BNE AGAIN	;IF NOT, TRY TO BOOT AGAIN
1045						
1046	173254	105011		CLRCS:	CLRB (R1)	;CLEAR COMMAND REGISTER. THIS WILL ;STOP DECTAPE MOTION IF DEVICE WAS ;TUS6 - DON'T CLEAR HIGH BYTE ;START SECONDARY BOOT AT 0
1047						
1048						
1049	173256	005007			CLR PC	
1050						
1051						
1052				.SBTTL	THIS IS THE START OF THE RKXX/RK06 BOOT STRAP (DISK DUMMY) ;COMMAND REGISTER ADDRESS IS 177400	
1053						
1054						
1055	173260	010061	000010	RK06:	MOV R0,10(R1)	;LOAD DRIVE NUMBER INTO DRIVE SELECT REG.
1056	173264	012711	000003		MOV #3,(R1)	;LOAD PACK ACKNOWLEDGE FUNCTION
1057	173270	000740			BR TU10A	

M02

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 23
DQM9AA.P11 13-APR-77 11:11

THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RMP04)

1058
1059
1060
1061
1062
1063
1064

173272 110061 000010
173276 112311
173300 012761 014000 000032
173306 000470

.SBTTL THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RMP04)
;COMMAND REGISTER ADDRESS IS 176700

RP04: MOVB R0,10(R1) ;SELECT UNIT NUMBER TO BOOT FROM
MOVB (R3)+,(R1) ;ISSUE READ-IN PRESET COMMAND
MOV #14000,32(R1) ;SET FMT22 & ECC INHIBIT BITS
BR CMNSRH ;GO JOIN THE COMMON RH70 CODE

N02

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 24
 DQM9AA.P11 13-APR-77 11:11 THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RWP04)

```

1065
1066
1067      .SBTTL THIS IS THE MEMORY SIZING CODE
1068      ;ENTER WITH R0=RETURN ADDRESS
1069      ;EXIT WITH R5=LAST MEMORY ADDRESS
1070
1071 173310 012705 160000      SIZE:  MOV      #160000,R5      ;SETUP MEMORY CHECK LIMIT (28K)
1072 173314 005037 000006      CLR      #6          ;CLEAR LOC. 6 (TIMEOUT VEC.+2)
1073 173320 012737 173326 000004      MOV      #15,2#4      ;SETUP TIMEOUT VECTOR
1074 173326 012706 000776      1S:    MOV      #775,SP      ;SETUP STACK POINTER
1075 173332 005745      TST     -(R5)         ;FIND LAST MEM. LOC.
1076 173334 010007      MOV     R0,PC         ;RETURN
1077
1078
1079      .SBTTL THIS IS THE START OF THE RH11/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM, TWU16)
1080      ;COMMAND REGISTER ADDRESS IS 172440
1081
1082 173336 010061 000032      TU16:  MOV     R0,32(R1)      ;LOAD UNIT NUMBER INTO SLAVE SELECT REG.
1083 173342 052361 000032      BIS     (R3)+,32(R1)   ;MERGE IN FORMAT AND DENSITY BITS
1084 173346 032761 010000 000012      1S:    BIT     #MOL,12(R1) ;IS THE MEDIUM ON LINE?
1085 173354 001774      BEQ     1$           ;WAIT FOR BIT 12 OF DRIVE STATUS REG
1086 173356 112311      MOVB   (R3)+,(R1)     ;ISSUE REWIND COMMAND
1087 173360 105761 000012      2S:    TSTB   12(R1)     ;IS DRIVE READY BIT SET YET?
1088 173364 100375      BPL    2$           ;WAIT FOR DRIVE READY BIT
1089 173366 112311      MOVB   (R3)+,(R1)     ;ISSUE DRIVE CLEAR COMMAND
1090 173370 105761 000012      3S:    TSTB   12(R1)     ;IS DRIVE READY BIT SET?
1091 173374 100375      BPL    3$           ;WAIT UNTIL BIT 07 IS SET
1092 173376 012761 177777 000006      MOV     #-1,6(R1)     ;SET SKIP COUNT TO 1 RECORD
1093 173404 112311      MOVB   (R3)+,(R1)     ;ISSUE SPACE FORWARD COMMAND
1094 173406 105761 000012      4S:    TSTB   12(R1)     ;HAS THE DRIVE FINISHED THE SPACE?
1095 173412 100375      BPL    4$           ;WAIT UNTIL BIT 07 IS SET
1096 173414 000425      BR     CHNSRH        ;GO JOIN COMMON RH70 CODE
1097
1098      .SBTTL THIS IS THE START OF THE PC11 BOOTSTRAP (HIGH SPEED PAPER TAPE READER)
1099      ;THE STATUS REGISTER ADDRESS IS 177550
1100
1101 173416 012700 173424      PC11:  MOV     #15,R0        ;SAVE RETURN PC
1102 173422 000732      BR     SIZE          ;GO SIZE MEMORY
1103
1104      1S:    MOV     R1,(R5)      ;RETURN WITH R5=LAST ADDR.
1105 173426 142705 000024      BICB   #24,R5        ;MASK FOR SPECIAL ADDRESS
1106 173432 010515      MOV     R5,(R5)      ;STORE OWN ADDRESS IN POINTER
1107 173434 011503      2S:    MOV     (R5),R3    ;GET BYTE POINTER
1108 173436 005211      INC    (R1)          ;ENABLE TAPE READER
1109 173440 105711      3S:    TSTB   (R1)        ;TEST DONE BIT
1110 173442 100376      BPL    3$           ;WAIT UNTIL READY
1111 173444 116113 000002      MOVB   2(R1),(R3)    ;STORE DATA AT BYTE POINTER
1112 173450 005215      INC    (R5)          ;BUMP POINTER
1113 173452 122703 000375      CMPB   #375,R3       ;STORED JUMP OFFSET?
1114 173456 001366      BNE    2$           ;BRANCH IF NOT YET
1115 173460 105223      INCB   (R3)+         ;YES, ALL DONE
1116 173462 000143      JMP    -(R3)        ;GO EXECUTE AS BRANCH
1117
1118
1119      .SBTTL THIS IS THE START OF THE RH11/R504 BOOT STRAP (FIXED HEAD DISK, RWS04)
1120      ;COMMAND REGISTER ADDRESS IS 172040

```

B03

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 25
DQM9AA.P11 13-APR-77 11:11

THIS IS THE START OF THE RM11/R504 BOOT STRAP (FIXED HEAD DISK, RWS04)

1121
1122
1123

173464 110061 000010

R504: MOV8 R0,10(R1) ;LOAD THE DRIVE NUMBER TO BOOT FROM

MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 26
 CMNSRA.P11 13-APR-77 11:11

THIS IS THE START OF THE COMMON RH-70 CODE

```

1124 .SBTTL THIS IS THE START OF THE COMMON RH-70 CODE
1125
1126 173470 016161 000016 000016 CMNSRH: MOV 16(R1),16(R1) ;TURN OFF ANY ACTIVE ATTENTION FLAGS
1127 173476 000643 CSWH1: -BR CMNSGC ;BRANCH TO COMMON READ CODE
1128
1129
1130 .SBTTL THIS IS THE START OF THE RX11/RXD1 BOOT STRAP (FLOPPY DISK)
1131 ;COMMAND REGISTER ADDRESS IS 177170
1132
1133 173500 052705 000040 RXD1: BIS #40,R5 ;ADD 'DONE' BIT TO 'ERROR' AND 'TR' BITS
1134 173504 005700 TST R0 ;TEST UNIT NUMBER
1135 173506 001401 BEQ 1$ ;BRANCH IF UNIT 0 WAS SELECTED
1136 173510 005723 TST (R3)+ ;ADD 2 TO FUNCTION CODE POINTER
1137 173512 130511 1$: BITB R5,(R1) ;TEST FOR 'TR' AND 'DONE' BITS
1138 173514 001776 BEQ 1$ ;WAIT UNTIL ONE IS SET
1139 173516 112311 MOVB (R3)+,(R1) ;LOAD READ COMMAND FOR PROPER DRIVE
1140 173520 012702 000002 MOV #2,R2 ;LOAD LOOP COUNT INTO R2
1141 173524 105711 2$: TSTB (R1) ;TEST FOR THE 'TR' BIT
1142 173526 100376 BPL 2$ ;WAIT UNTIL IT IS SET
1143 173530 112761 000001 000002 MOVB #001,2(R1) ;LOAD TRACK ADDRESS THEN SECTOR NUMBER
1144 173536 077206 SOB R2,2$ ;LOOP BACK TO LOAD SECTOR NUMBER
1145 173540 030511 3$: BIT R5,(R1) ;TEST FOR 'ERROR', 'TR', AND 'DONE' BITS
1146 173542 001776 BEQ 3$ ;WAIT FOR ONE OF THE BITS
1147 173544 100615 BMI AGAIN ;BRANCH TO RETRY BOOTSTRAP IF 'ERROR' BIT SET
1148 173546 111311 MOVB (R3),(R1) ;LOAD EMPTY BUFFER COMMAND FOR PROPER DRIVE
1149 173550 130511 4$: BITB R5,(R1) ;TEST FOR 'TR' OR 'DONE' BITS
1150 173552 001776 BEQ 4$ ;WAIT FOR ONE OF THE BITS
1151 173554 100003 BPL CHK240 ;BRANCH TO CHECK ADDRESS ZERO IF 'DONE' BIT
1152 173556 116122 000002 MOVB 2(R1),(R2)+ ;STORE DATA IN MEMORY (R2 GOES FROM 000 TO 177)
1153 173562 000772 BR 4$ ;GO GET NEXT BYTE
1154 173564 022737 000240 000000 CHK240: CMP #240,2#0 ;CHECK THE FIRST ADDRESS BOOTED
1155 173572 001202 BNE AGAIN ;BRANCH TO RETRY IF NOT A 'NOP'
1156 173574 005007 CLR PC ;START SECONDARY BOOT AT ADDRESS ZERO
1157
1158 .SBTTL THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)
1159 ;COMMAND REGISTER ADDRESS IS 177404
1160
1161 173576 072227 000005 RK05: ASH #5,R2 ;LEFT SHIFT UNIT NUMBER 5 PLACES
1162 173602 010261 000006 MOV R2,6(R1) ;LOAD UNIT NUMBER INTO DEVICE
1163 173606 000733 BR CSWH1 ;BRANCH TO COMMON READ CODE
1164

```

.MAIN. MACY11 27(1006) 25-APR-77 06:26 PAGE 27
 DDM99A.P11 13-APR-77 11:11

THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-0)

			.SBTTL FUNCTION CODES FOR THE ALL OF THE DEVICES		
1165					
1166					
1167					
1168	173610	060017	TU10S:	.WORD 060017	;REWIND SELECTED DRIVE AND SET 800 BPI
1169	173612	011		.BYTE 011	;SPACE FORWARD COMMAND FOR TU10
1170	173613	003		.BYTE 003	;READ COMMAND FOR TU10
1171					;PACK ACKNOWLEDGE FOR RK06
1172	173614		RK06S:		
1173	173614	021	RP04S:	.BYTE 021	;READ-IN PRESET FOR RP04; READ FOR RK06
1174	173615	071	RS04S:	.BYTE 071	;READ COMMAND FOR RP04 & RS04
1175					
1176	173616	004003	TU56S:	.WORD 004003	;SEARCH FOR BLOCK 0, REVERSE DIRECTION
1177	173620		RK05S:		
1178	173620	005	RP03S:	.BYTE 005	;READ COMMAND FOR TU56, RK05, RP03
1179					
1180	173621	077		.BYTE 077	;THIS IS A FILLER-NON-ZERO BYTE
1181					;TO DISTINGUISH FROM THE (BYTE FOLLOWING
1182					;THE READ FORWARD COMMAND) IN TU16
1183					
1184	173622	001300	TU16S:	.WORD 1300	;FORMAT BITS FOR TU16, 800 BPI, NRZI
1185	173624	007		.BYTE 007	;REWIND SELECTED DRIVE
1186	173625	011		.BYTE 011	;DRIVE CLEAR COMMAND
1187	173626	031		.BYTE 031	;SPACE FORWARD
1188	173627	071		.BYTE 071	;READ FORWARD
1189	173630	001000		.WORD 1000	;FRAME COUNT ERROR
1190					
1191				.EVEN	;INSURE WORD BOUNDARY
1192	173632	007	RX01S:	.BYTE 007	;READ SECTOR COMMAND FOR DRIVE ZERO
1193	173633	003		.BYTE 003	;EMPTY BUFFER COMMAND FOR DRIVE ZERO
1194	173634	027		.BYTE 027	;READ SECTOR COMMAND FOR DRIVE ONE
1195	173635	023		.BYTE 023	;EMPTY BUFFER COMMAND FOR DRIVE ONE
1196					

E03

.MAIN. MACY11 27(1006) 25-APR-77 08:26 PAGE 28
 DQM9AA.P11 13-APR-77 11:11

FUNCTION CODES FOR THE ALL OF THE DEVICES

```

1197
1198
1199
1200 173636 172522
1201 173640 177342
1202 173642 177404
1203 173644 176714
1204 173646 177440
1205 173650 172440
1206 173652 176700
1207 173654 172040
1208 173656 177170
1209 173660 177550
1210
1211
1212
1213 173662 173610
1214 173664 173616
1215 173666 173620
1216 173670 173620
1217 173672 173614
1218 173674 173622
1219 173676 173614
1220 173700 173615
1221 173702 173632
1222
1223
1224
1225 173704 173144
1226 173706 173124
1227 173710 173576
1228 173712 173204
1229 173714 173260
1230 173716 173336
1231 173720 173272
1232 173722 173464
1233 173724 173500
1234 173726 173416
1235 173730 000000
1236 173732 000000
1237 000001
  
```

.SBTTL COMMAND AND STATUS REGISTER ADDRESS TABLE

```

CSRPTR: .WORD 172522      ; THIS IS THE C.S.R. ADDRESS FOR TU10
        .WORD 177342      ; THIS IS THE C.S.R. ADDRESS FOR THE TU56
        .WORD 177404      ; THIS IS THE C.S.R. ADDRESS FOR THE RK05
        .WORD 176714      ; THIS IS THE C.S.R. ADDRESS FOR THE RPO3
        .WORD 177440      ; THIS IS THE C.S.R. ADDRESS FOR THE RK06
        .WORD 172440      ; THIS IS THE C.S.R. ADDRESS FOR THE RH11/TU16
        .WORD 176700      ; THIS IS THE C.S.R. ADDRESS FOR THE RH11/RPO4
        .WORD 172040      ; THIS IS THE C.S.R. ADDRESS FOR THE RH11/RSO4
        .WORD 177170      ; THIS IS THE C.S.R. ADDRESS FOR RX11/RX01
        .WORD 177550      ; THIS IS THE C.S.R. ADDRESS FOR THE PC11
  
```

.SBTTL FUNCTION POINTER TABLE

```

CMDPTR: .WORD TU10$      ; POINTER TO FUNCTION TABLE FOR THE TU10
        .WORD TU56$      ; POINTER TO FUNCTION TABLE FOR THE TU56
        .WORD RK05$      ; POINTER TO FUNCTION TABLE FOR THE RK05
        .WORD RPO3$      ; POINTER TO FUNCTION TABLE FOR THE RPO3
        .WORD RK06$      ; POINTER TO FUNCTION TABLE FOR THE RK06
        .WORD TU16$      ; POINTER TO FUNCTION TABLE FOR RH11/TU16
        .WORD RPO4$      ; POINTER TO FUNCTION TABLE FOR THE RH70/RPO4 OR RH11/RPO
        .WORD RSO4$      ; POINTER TO FUNCTION TABLE FOR THE RH70/RSO4 OR RH11/RPO
        .WORD RX01$      ; POINTER TO FUNCTION TABLE FOR THE RX01
  
```

.SBTTL STARTING ADDRESS TABLE

```

ADDRS:  .WORD TU10      ; STARTING ADDRESS FOR THE TH11/TU10
        .WORD TU56      ; STARTING ADDRESS FOR THE TC11/TU56
        .WORD RK05      ; STARTING ADDRESS FOR THE RK11/RK05
        .WORD RPO3      ; STARTING ADDRESS FOR THE RP11/RPO3
        .WORD RK06      ; STARTING ADDRESS FOR THE RK06
        .WORD TU16      ; STARTING ADDRESS FOR THE RH70/TU16 (800 BPI NRZI)
        .WORD RPO4      ; STARTING ADDRESS FOR THE RH70/RPO4 OR RH11/RPO4
        .WORD RSO4      ; STARTING ADDRESS FOR THE RH70/RSO4 OR RH11/RSO4
        .WORD RX01      ; STARTING ADDRESS FOR THE RX11/RX01
        .WORD PC11      ; STARTING ADDRESS FOR THE PC11
        .WORD 0          ; RESERVED
        .WORD 0          ; RESERVED
        .END
  
```


COMMEN	328#	788	914												
ENDCOM	328#	798	932												
MSG1	343#	345													
MSG10	483#	485													
MSG11	502#	504													
MSG12	525#	527													
MSG13	548#	550													
MSG14	567#	569													
MSG15	592#	594													
MSG16	618#	620													
MSG17	645#	647													
MSG2	358#	360													
MSG20	676#	678													
MSG21	699#	701													
MSG22	737#	739													
MSG23	800#	802													
MSG24	851#	853													
MSG3	375#	377													
MSG4	397#	399													
MSG5	418#	420													
MSG6	438#	440													
MSG7	456#	458													
NXTTST	328#	343	358	375	397	418	438	456	483	502	525	548	567	592	618
	645	676	699	737	800	851									
SKIP	328#	355	372	394	415	435	453	480	499	522	545	564	589	615	642
	673	696													
STARS	328#	343	350	358	365	375	387	397	409	418	429	438	449	456	469
	483	495	502	514	525	538	548	560	567	580	592	605	618	630	645
	659	676	688	699	709	737	750	800	820	851	869				
SSHXT	328#	343	358	375	397	418	438	456	483	502	525	548	567	592	618
	645	676	699	737	800	851									
SSSKIP	328#	355	372	394	415	435	453	480	499	522	545	564	589	615	642
	673	696													

. ABS. 173734 000

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

DSKZ:DOM9AA.SEG/SOL/CRF=DOM9AA.P11
RUN-TIME: 2 3 .2 SECONDS
RUN-TIME RATIO: 43/5=7.3
CORE USED: 8K (15 PAGES)