CONTROL DATA®
CYBER 70 COMPUTER SYSTEM
7030 EXTENDED CORE STORAGE

DESCRIPTION AND PROGRAMMING
REFERENCE MANUAL VOLUME 3

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PREFACE

The CONTROL DATA © CYBER 70 series reference manuals are published in a series of volumes. This is Volume 3 of the series.

This volume contains information about the ECS (Extended Core Storage) system. Volume 1, Pub. No. 60347000 for MODEL 72, 60347200 for MODEL 73, and 60347400 for MODEL 74, contains system descriptions and general programming information. Volume 2, Pub. No. 60347300, contains detailed descriptions of the central processor and the peripheral processor instructions.

The publications listed are available through the nearest Control Data Corporation sales office.

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INTRODUCTION

The CONTROL DATA® Extended Core Storage System (ECS) is an optional supplementary rapid access storage system for use with CONTROL DATA® CYBER 70 Series Computer Systems. It consists of a storage element, a controller and an interface unit.

The ECS is a word organized storage system with transfer rates up to one 60-bit word every 100 nsec (10 MHZ). It is available in sizes from 125,952 60-bit words to 2,015,232 60-bit words.

A complete ECS system requires storage elements, an ECS controller, and an interface unit. Figure 5-1 shows a typical system configuration.

The storage elements are mounted in cabinets similar in appearance to the CYBER 70 Series Computer Systems. Each cabinet has a capacity of four banks of memory so systems with 1 bank, 2 banks, or 4 banks are mounted in a single cabinet. Systems with 8 banks includes two cabinets and systems with 16 banks includes four cabinets. Cabinets are commonly referred to as "bays."

Timing discussed in this manual is necessarily general in nature, because the exact configuration of a system must be taken into account to determine precise timing parameters.

STORAGE ELEMENT CHARACTERISTICS

- 125,952 60-bit words per bank
- 1-, 2-, 4-, 8, or 16 bank configurations (maximum size is 2,015,232 60 bit-words)
- Organized in logically independent banks of 488-bits (eight 60 bit words plus a parity bit for each) with multiphasing of banks
- Reserve memory to minimize downtime
- Cycle time of 3.2 μsec per bank (read/write time for a 488-bit word)
- Self contained maintenance hardware for off-line check-out
- Access to, or modification of, a single 60-bit word in ECS.

MODEL 72-1Z/73-1Z/74-1Z

ECS SYSTEM (OPTIONAL)

CPU

CENTRAL MEMORY

ECS COUPLER

ECS CONTROLLER

ECS BANKS

PERIPHERAL PROCESSORS

DISTRIBUTIVE DATA PATH (DDP)

MODEL 72-2Z/73-2Z/74-2Z

ECS SYSTEM (OPTIONAL)

CPU 1

CENTRAL MEMORY

ECS COUPLER

ECS CONTROLLER

ECS BANKS

CPU 0

DISTRIBUTIVE DATA PATH (DDP)

PERIPHERAL PROCESSORS
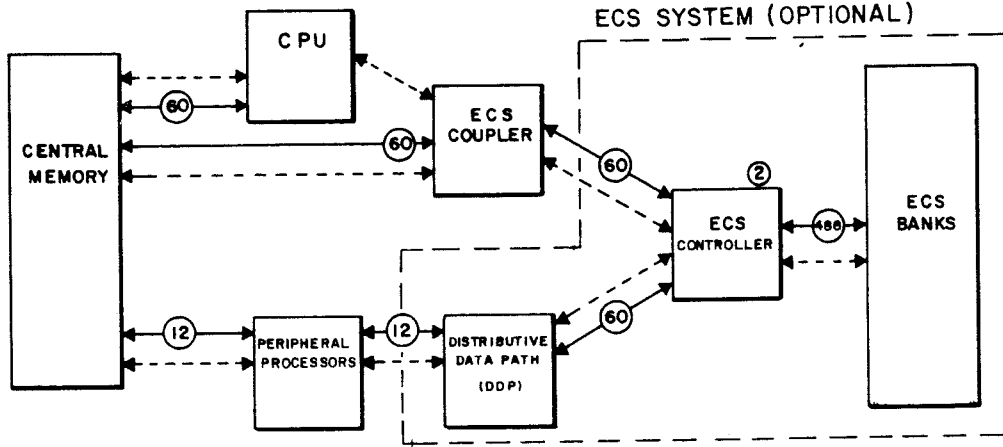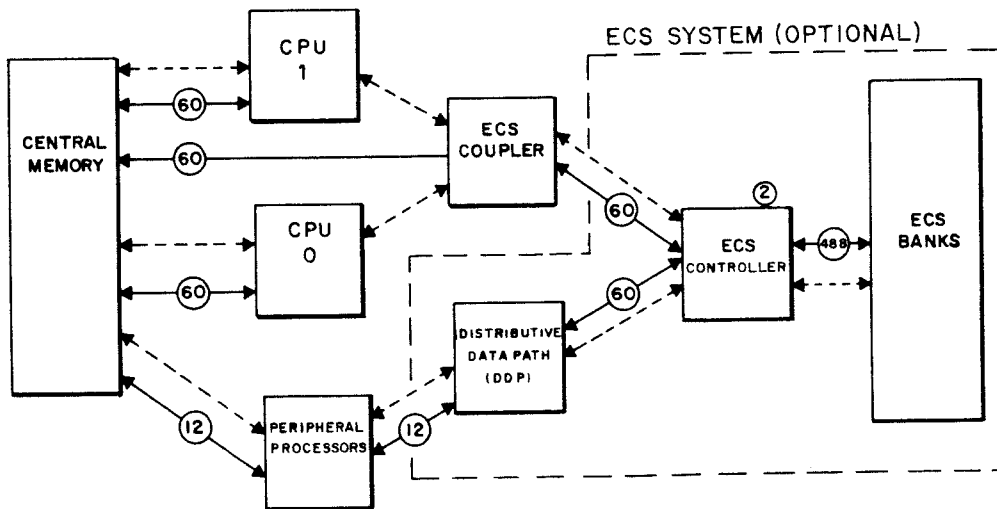
NOTES: 1. ◄----► CONTROL

◄─○─► DATA; SHOWING NO. OF BITS WIDTH.

② THE ECS CONTROLLER CAN ACCOMODATE A TOTAL OF FOUR COUPLERS OR DDP'S OR ANY COMBINATION THEREOF.

Figure 5-1. System Configuration Diagram

ECS CONTROLLER CHARACTERISTICS

- Four access channels; for communicating with up to four interface units. These access channels are standardized to allow any CYBER 70 interface unit to be attached to any channel.

- Scanning mechanism; services all channels equally and sequentially. Scanning occurs after each record of eight 60-bit words.

- Assembly/disassembly of ECS words (488-bits) into 60-bit words plus parity bits.

- Parity bit generation on write operations; parity checking on read operations.

- Hardware degradation that allows the use of half of the system in case of an ECS failure. (Applicable to systems with 250K words or more.)

- Communications register (Flag register); for computer to computer communications without ECS memory references.

INTERFACE UNIT CHARACTERISTICS

Two interface units are currently available for a CYBER 70 system; the Distributive Data Path (DDP) which allows a PPU to communicate with ECS and the Coupler which allows a CPU to Communicate with ECS.

Distributive Data Path (part of ECS system option)

- Allows any PPU in the system to communicate with ECS.

- Provides assembly/disassembly of 60-bit words to 12-bit words.

- Provides block or single record (8 60-bit words) transfer.

- Provides one PPU channel to ECS; expandable to four channels.

Coupler (part of standard mainframe)

- Provides block transfers between ECS and Central Memory initiated by a single instruction

- Provides bounds protection and relocation capabilities in ECS.

- Provides access by either CPU (Twin CPU's systems only)

- Provides PPU access to Central Memory during block transfers.

FUNCTIONAL DESCRIPTION

STORAGE ELEMENTS

EXTENDED CORE STORAGE ORGANIZATION

The ECS unit provides up to two million directly addressable 60-bit words of storage. Eight 60-bit words are organized into a 488-bit ECS data word (Figure 5-2). A parity bit is attached to each 60-bit word in the controller on an ECS Write. Although all transfers are basically eight 60-bit words, any number of words may be transferred.
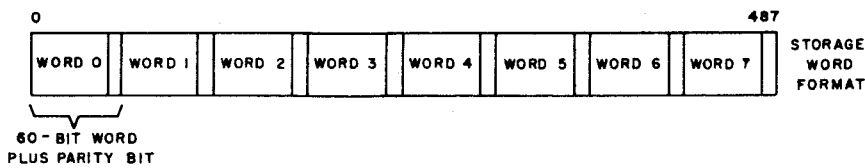
Figure 5-2. ECS Word Format

ECS is organized into banks of 125,952 60-bit words. The minimum ECS is a single bank of 125,952 60-bit words. Four banks provide a capacity of 503,808 60-bit words. Sixteen banks provide the maximum ECS capacity of 2,015,232 60-bit words. ECS is available in 1-, 2-, 4-, 8-, or 16-bank configurations.

An assembly/disassembly network in ECS assembles eight 60-bit words (plus eight parity bits) into a 488-bit word for Write operations. On Read operations, this network disassembles eight 60-bit words and their associated parity bits from the 488-bit word read from ECS. Each bank has an assembly/disassembly network.

Each bank has a read/write cycle time of 3.2 μsec per 488-bit word selected. This storage cycle time is diagrammed in Figure 5-3.
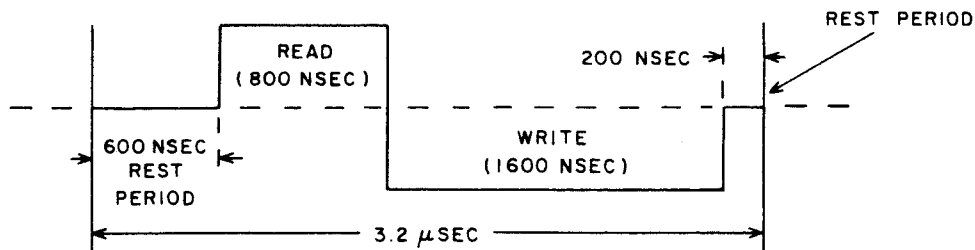
Figure 5-3. ECS Read/Write Cycle

Each ECS bank has 5K of reserve memory locations to minimize down-time. This ensures contiguously addressable memory even though a bank may develop some bad locations. The 5K of reserve memory is usable in 1K increments. To exchange one reserve increment with 1K of memory requires only the interchanging of two wires.

ECS has maintenance hardware that enables it to run independently of the controller. In a two bank configuration either bank can be run in maintenance mode. This feature, coupled with the 50% hardware degradation in the controller allows one bank to be retained in the system and the other bank to be run in maintenance mode off line. The four bank configuration does not have this combined capability. While it can be degraded 50%, that half that is not in the system cannot use the maintenance hardware while the system is using the other half. Four banks of an eight bank configuration and eight banks of a sixteen bank configuration can be removed from the system and run in maintenance mode.

ECS can modify one 60-bit word in an ECS 480 (plus parity) -bit word without affecting the remaining bits in the ECS word.

EXTENDED CORE STORAGE ADDRESSING

The address format varies with the ECS configuration (Figure 5-4). Addresses are phased so that consecutive addresses go to consecutive banks. The lowest 3 bits of any address are used to disassemble the 488-bit ECS word into 60-bit data words (and their associated parity bits). On a system of 250K or more (two or more banks), the next bits will select the bank. Up to 4 bits are provided to select 16 banks. The next 14 bits select one 488-bit word in the selected bank. The remaining bits are not used for addressing purposes but serve other functions. They are used to check for illegal addresses or they can be used to perform Flag register operations.

If the illegal address bits (Table 5-1) are set, they will cause an error exit as discussed under Error Action in the appropriate Interface Unit.

```
           23        17 16                      3 2    0
 I BANK        |         |                        |    |        125 K
              (7)              (6)                 (1)

           23        18 17                    4 3 2    0
 2 BANKS      |         |                      | |  |          250 K
              (7)              (6)              (2)(1)

           23        19 18                   5 4 3 2   0
 I BAY (4 BANKS) |       |                    |  | |  |        500 K
              (7)              (6)              (3)  (1)

           23        20 19                  6 5 4 3 2  0
 2 BAYS ( 8 BANKS) |     |                   | |  | |  |       1000 K
              (7)              (6)            (4)(3)  (1)

           23     21 20                    7 6 5 4 3 2 0
 4 BAYS (16 BANKS) |    |                    | |  | |  |       2000 K
              (7)              (6)            (5)(3)  (1)
```
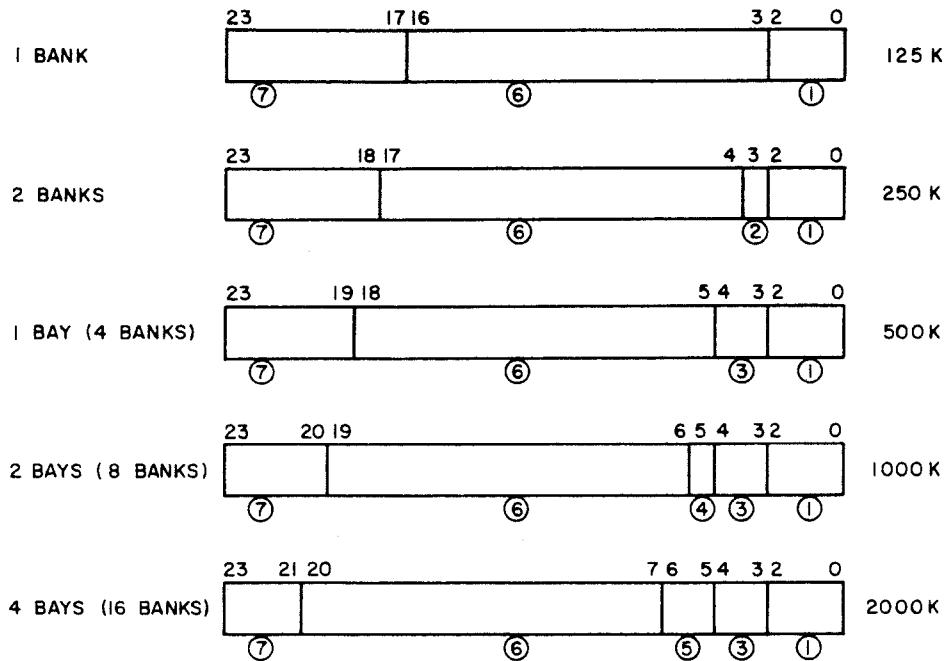
NOTES:

① 60 BIT WORD COUNT BITS
② SELECT I OF 2 BANKS
③ SELECT I OF 4 BANKS
④ SELECT I OF 2 BAYS
⑤ SELECT I OF 4 BAYS
⑥ SELECT I 488-BIT WORD IN ABANK
⑦ NOT USED FOR ADDRESSING

Figure 5-4. ECS Address Formats

TABLE 5-1. ILLEGAL ADDRESS BITS

Configuration	Bit Number
125K	17
200K	18
500K	19
1000K	20
2000K	21

TRANSFER TIMING

To achieve the maximum transfer rate, four banks (500K) of ECS must be performing back to back memory references with banks staggered 800 nsec apart. This gives four ECS records every 3.2 μsec; that is, 32 60-bit words every 3.2 μsec or one word per 100 nsec. The coupler must request memory every 800 nsec and furthermore must be phasing its addresses. ECS configurations larger than 500K do not increase this maximum transfer rate.

If ECS has two banks (250K), the controller will allow the first two requests but a third request will encounter a busy ECS bank. This request must wait until a bank becomes free. This gives an effective transfer rate of two ECS records per 3.2 μsec or one word every 200 nsec. The data words are transferred in a pattern of one word every 100 nsec for 1600 nsec, wait 1600 nsec, transfer another 16 words, and so on.

If ECS has one bank (125K), the controller will allow the second request only after the first memory cycle is complete. This gives an effective transfer rate of one ECS record per 3.2 μsec, or one word every 400 nsec. The data words are transferred in a pattern of eight words every 100 nsec for 800 nsec, wait 2400 nsec, transfer another eight words, and so on.

EXTENDED CORE STORAGE CONTROLLER

CONTROLLER OPERATION

The ECS Controller provides four bi-directional access channels to read or write 60-bit data words, a scanning mechanism to service the requests of these channels, a parity generator and checker, and the associated control elements necessary to time these operations. The controller also contains an 18-bit Flag register that may be used for communication by the attached Interface Units.

SCANNER AND ACCESS CHANNELS

Bi-directional access channels on the controller provide the paths for data and control signals between ECS and the Interface Unit. To permit access to ECS by other systems, a total of four access channels are provided. Data trunks in the access channels are 60 bits wide.

Data transfer (for block transfers) is accomplished in groups of eight words or less called records. Note that a record is actually one ECS word and therefore one record is obtained per memory cycle. Single 60-bit word transfers can also be effected. While one record is being transferred, the controller scans the other access channels for memory requests. If another channel is requesting access to ECS, that channel is serviced. If other channels are transferring data, each channel is serviced on a record basis. Thus, there may be time gaps between records on a given access channel.

The controller has the responsibility for timing the ECS banks. These banks are started into their memory cycle by the controller which must space the cycles so that data from one bank does not conflict with another. The controller also prevents two Interface Units from requesting the same bank simultaneously by holding the latter request until the first has been satisfied. The ECS controller performs much the same function for ECS that Central Memory control does for Central Memory. The controller has registers to store the information that is received with each request so that no request is lost. The controller can process four requests concurrently.

PARITY GENERATOR/CHECKER

For each 60-bit word to be stored in ECS, a parity bit is generated and stored along with that word (odd parity). Parity is checked on each 60-bit word as the storage word is disassembled after a Read operation.

CHANNEL SIGNAL FLOW

The Interface Unit transmits a Request signal, a Read/Write signal and a 24-bit address. If the operation is a write it will also send the 60 data bits at the same time as the other signals. Once the Request is received the controller will respond with an Accept signal. If, however, ECS is not available or the address sent is too large for the configured system, an Abort is returned shortly after the Accept signal. Response to the Abort is dictated by the Interface Unit.

In a read operation a parity error may occur during a data transfer. A Parity Error signal is then transmitted to the Interface Unit. The response to a Parity error is dictated by the Interface Unit.

The Abort and Accept signals have different meanings when a Flag Function is performed (See Flag Register Operation).

FLAG REGISTER

The Controller has an 18-bit Flag register to allow programs to provide information about the current or previous operations. One of its uses could be analogous to a reserved status word being maintained in ECS but available at far greater speed, since ECS references are not made. The register cannot be read directly; instead, an Interface Unit must interrogate it and/or write into it.

FLAG REGISTER SELECTION

The Flag register is selected by performing an ECS read or write operation with bit 23 set in the ECS address*. The operation is the same for either a read or write operation and is not affected by the Fifty Percent Capacity Reduction.

The address is sent to the controller as is any other ECS address. Since bit 23 is set, the controller recognizes this as a Flag register operation. It then translates bits 22 and 21 to see what function is to be performed.

The controller responds to a Flag register function by sending either an abort or an accept back to the Interface Unit.

For a Flag register operation the ECS address is considered to have three parts (Figure 5-5).

```
FUNCTION                    FLAG
  CODE                      WORD

  ┌──────┬──────┬──────────────────────────────┐
  │  N   │//////│                              │
  └──────┴──────┴──────────────────────────────┘
  23    2120   1817                             0
```
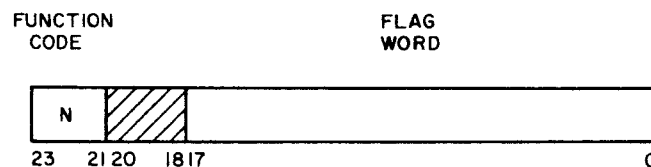
Figure 5-5.   ECS Address Format for Flag Register Operation

1.   Function Code (N) is bits 21-23.   Bit 23 is always set for a Flag register operation.

2.   Bits 18-20 are not used.

3.   The flag word is bits 0-17.   These bits are compared with or entered into the Flag register depending on the function specified by N.

---

*See appropriate Interface Unit for Flag Register Selection.

FLAG FUNCTION CODES

Four operations can be specified by bits 21 and 22.

N=4; Ready/Select

A bit by bit comparison is made between the contents of the Flag register and the flag word. If all the set bits in the flag word are cleared in the Flag register, a positive comparison has been made and all the set bits in flag word are entered into the Flag register. Note that the cleared bits in the flag word have no effect on the Flag register.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word = 101

This is a positive comparison so the Flag register is changed and an Accept is transmitted by the Controller to the Interface Unit.

Final contents of Flag register = 111

If a positive comparison is not made, the Flag register remains unchanged and an abort is transmitted to the Interface Unit.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word = 111

This is a negative comparison so the Flag register is unchanged.

Final contents of Flag register = 010

N=5; Selective Set

No comparison is made. All set bits in the flag word are set in the Flag register.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word = 100

Final contents of Flag register = 110

N=6; Status

This is the same as a Ready/Select code but the Flag register is not changed on a positive comparison. The comparison is made in the same manner and the exit conditions are the same.

N=7; Selective Clear

No comparison is made. All set bits in the flag word are cleared in the Flag register.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 110
flag word = 101
Final contents of Flag register = 010

FIFTY PERCENT CAPACITY REDUCTION

The system can be reduced to half of the configured capacity by a switch in the controller. This is done by left shifting some address bits by one position (Table 5-2). This means that one of the Bank selection bits in the controller address register is not used. This bit is set or cleared, depending on which half of the system is to be used. With the bit set, the upper half of the addresses are available; with the bit cleared, the lower half of the addresses are available. The selection is made by a second switch on the controller.

The capacity reduction is done per channel. It is therefore possible to degrade two channels and assign complementary halves of ECS to each channel. For example, in a 500K system, 250K could be assigned to channel 1 and the other 250K assigned to channel 2. The Flag register operations are not affected by the capacity reduction.

TABLE 5-2. ADDRESS SHIFTING

Configuration	Bits Shifted		Selection Bit
	FROM:	TO:	
250K	3-17	4-18	3
500K	4-18	5-19	4
1000K	5-19	6-20	5
2000K	6-20	7-21	6

Figure 5-6 shows a typical address shifted by the fifty percent capacity reduction.
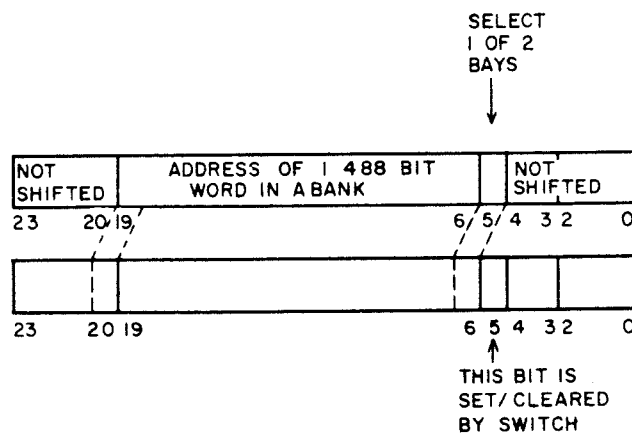
Figure 5-6. Example of Address Shifting for 1000K

CONTROLLER TRANSFER TIMING

The controller transfers a maximum of one ECS record (8 60-bit words) per request, and it services each channel sequentially.

All timing through the controller consists of:

1. The access time between the controller and the ECS bank, after the controller has accepted the request for data.

2. The delays between the servicing of concurrent requests. No interruption can occur during an eight word record.

For each request, the controller retains the address of the selected bank and the channel that originated the request. The controller contains four counters that sequence controller activity. One counter is assigned to each request which could come from separate channels or from one channel requesting successive memory references; that is, a block transfer. A further delay can occur when one Interface Unit requests a Write operation and that request is then followed immediately by a read request from a second Unit. Instead of waiting the normal 800 nsec between requests the second Unit waits 1600 nsec. Each counter is started when a request is sent to ECS and runs 200 nsec ahead of the read/write cycle counter in the bank. For normal transfers, each counter would start 800 nsec after the previous one; that is, when that counter equals 8. All conflicts in the controller delay the starting of the counter for the current request. The Interface Unit waits until the controller starts its counter. When a Flag register operation occurs, the counter is never started. The flow chart shows the access time for one request (Fig. 5-7).

60347100 C

RECEIVE ADDRESS, REQUEST AND READ/WRITE SIGNAL

IS THIS A FLAG REGISTER OPERATION?

ARE THERE ANY OTHER REQUESTS?

WAIT FOR PREVIOUS REQUESTS TO BE COMPLETED. MAXIMUM WAIT IS 3.2 μSEC PER REQUEST.

PERFORM FLAG OPERATION

TRANSMIT, ABORT OR ACCEPT TO INTERFACE UNIT DEPENDING ON FLAG RESULT.

STOP

IS THIS REQUEST FOR THE SAME BANK AS ANY OF THE PREVIOUS REQUESTS?

WAIT UNTIL BANK IS FREE. MAXIMUM WAIT IS 3.2 μSEC PER REQUEST FOR THAT BANK

WAS WAIT LESS THAN 1.6 μSEC?

COUNTER = 0

INFORM INTERFACE UNIT THAT REQUEST IS ACCEPTED. START COUNTER ASSIGNED TO THIS REQUEST.

A

1

IS THIS OPERATION A WRITE?

WAIT UNTIL PREVIOUS COUNTER ≥ 8. MAXIMUM WAIT IS 0.8 μSEC.

WAS REQUEST BEFORE THIS A READ?

WAIT UNTIL PREVIOUS COUNTER ≥ 16. MAXIMUM WAIT IS 1.6 μSEC.

A

IS THIS ECS ADDRESS AVAILABLE IN THE SYSTEM?

CONTROLLER CONTINUES TO RUN BUT DOES NOT REQUEST ECS. THEREFORE, ECS WILL NOT RESPOND.

COUNTER = 1

REQUEST ECS BANK

DID ECS RESPOND?

READ ALL ZEROES. COMPLETE DATA TRANSFER.

IS THIS A WRITE OPERATION?

TRANSMIT ABORT, TO INTERFACE UNIT.

STOP

IS THIS A WRITE OPERATION?

10 ≤ COUNTER ≤ 18

ALLOW 8 DATA WORDS TO ECS FROM INTERFACE UNIT

17 ≤ COUNTER ≤ 25

READ OPERATION: ALLOW 8 DATA WORDS FROM ECS TO INTERFACE UNIT.

COUNTER = 30

STOP

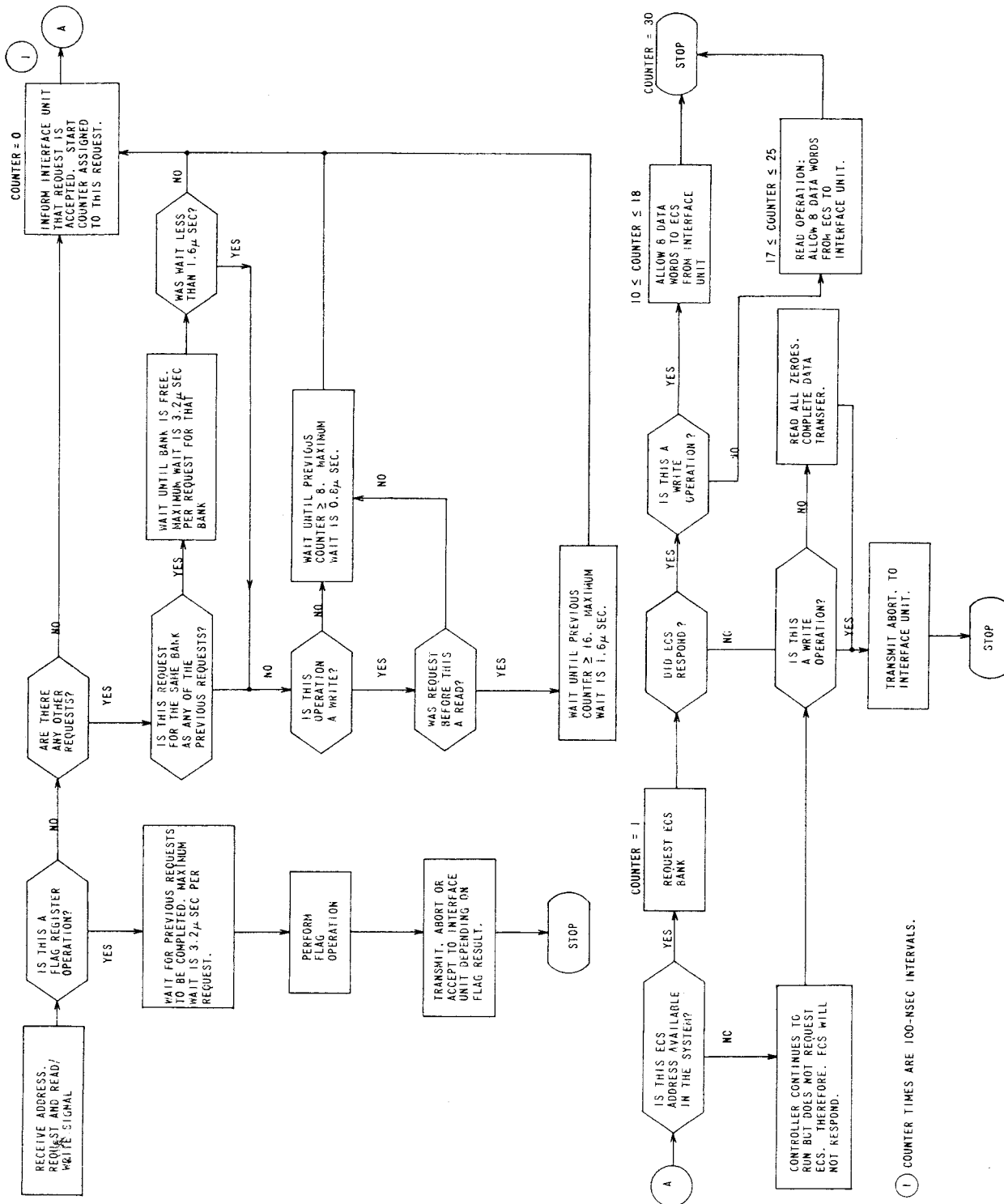① COUNTER TIMES ARE 100-NSEC INTERVALS.

Figure 5-7. Controller Access Timing

BLOCK TRANSFERS

When a CPU Interface Unit (Coupler) is attempting block transfers it must request the controller every 800 nsecs to sustain a rate of one 60-bit word every 100 nsec. If the controller is requested by another Interface Unit, the block transfer rate cannot be sustained. The transfer is interrupted by the length of time it takes to service that request. Note that two Couplers attempting block transfers would share the controller and therefore degrade the transfer rate to half of the maximum possible. To prevent this degradation, each requesting device should use the Flag Register to communicate to the other channels that a block transfer is underway. In using the flow chart to calculate transfer times, note that an uninterrupted block transfer incurs the access time only at the beginning of the transfer. Once the transfer is under way, a data word is available at every 100 nsec. (This is subject to the constraints of ECS memory size and Central Memory size as discussed in those sections).

SINGLE RECORD TRANSFERS

A PPU uses the Distributive Data Path as its Interface Unit. This unit is designed to accomplish single records transfers and cannot sustain block transfers greater than eight 60-bit words*. The flow chart, therefore, describes this type of transfer accurately.

FLAG REGISTER TIMING

Because of the inefficiency of allowing more than one Interface Unit to request ECS at the same time, the controller has a Flag register available which can be used by the software to coordinate the ECS transfers. The following discussion demonstrates the advantages of using the Flag register as a status register.

Assume that a transfer is underway; a second Interface Unit can perform a Flag register operation on a pre-defined bit which may inform it that ECS is being used. This will delay the actual data transfer by only 300 nsec minimum or by 3.5 μsec worst case. If a second and third Interface Unit are also requesting Flag register operations, the controller will perform them before returning to the data transfer. In this case, the second and third computers will add only 300 nsec each to the original delay of 3.5 μsec.

Assume that four 65K computers are using a 500K ECS System. Assume that each computer wishes to transfer 5000 data words from ECS; that is, a total of 20,000 words.

---

*The CPU Interface Unit has the capability to transfer a single record.

If all four are allowed to request ECS at the same time, the effective transfer rate as it appears to any one computer is one 60-bit word every 400 nsec, even though ECS is running at full speed. Since there is a total of 20,000 words to be transferred, the total transfer time for all four computers is 2 ms. This is the best case and ignores the conflicts due to requesting the same bank. In this example, bank conflicts could occur a significant percentage of the time; therefore, the calculated transfer time of 2 ms is less than the actual time required. Worst case transfer time is 400 nsec multiplied by 20,000 words or 8 ms.

Assume now that the transfers are sequential with one Unit transferring data and the other three performing Flag register operations to status ECS. Assume also that these Flag operations are done every 50 μsec; also, the Flag operations are not performed back to back but instead each one incurs an average penalty of 1.6 μsec. The operation then takes 300 nsec. This means that there is a total of 1.9 μsec penalty for each Flag operation.

Without an interruption the first Unit would take 500 μsec to transfer the data. However, each of the other Units would interrupt the transfer 10 times; a total of 30 in all. This would add 57 μsec (30 x 1.9 μsec) to the first 5000 word transfer, giving 557 μsec. Note that there will be only two Units doing Flag operations during the second 5000 words, one machine during the third 5000 words and none during the last 5000 words. Therefore, the total transfer time will be:

$$(500 + 57) + (500 + 38) + (500 + 19) + (500) \ \mu sec*$$

This gives a total of 2.114 ms. This is only slightly more than the best case time and a considerable improvement over the worst case time of 8 milliseconds. It should be noted that the systems performance is further enhanced because the first computer can start using its data only 557 μsec after starting a transfer. This is in marked contrast to the 2-ms delay when the Flag register is not used.

The Flag register can be used to advantage for improving the total transfer rate of the ECS system but it is particularly useful where priority transfers are necessary.

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*This ignores the initial access time.

INTERFACE UNITS

There are two Interface Units currently offered in the CYBER 70 computers. The Central Processor communicates with ECS through the Coupler. The Peripheral Processor communicates with ECS through the Distributive Data Path. Both types of units connect to one of the four available channels on the ECS controller.

ECS COUPLER

The coupler performs the following functions:

- Forms the initial ECS address and relays this address and the request and a Read or Write signal to the controller.

- Checks the ECS address to see if it is in bounds.

- Forms and checks the Central Memory address. This address is then sent to Central Memory.

- Receives the word count and compares the number of words transferred with the word count to ensure the transfer of the proper number of words.

- Increments the ECS address as each eight-word record is transferred.

- Generates an End of Transfer signal when the transfer is completed.

- Sends a Go signal to Central Memory for every word to be read from Central Memory. (Central Memory control increments the Central Memory address during the transfer.)

- Regulates data transfer rate for a 32K Central Memory which cannot sustain a transfer of one word every 100 nsec.

- Allows a Peripheral Processor to interrupt the ECS transfer each eight 60-bit words if necessary.

CPU/ECS COMMUNICATIONS INSTRUCTIONS

011   *Read Extended Core Storage*   *(30 Bits)*

fmi	j	K
59	51 50 48 47	30
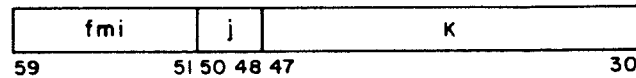
This instruction initiates a Read operation to transfer $[(Bj) + K]$ 60-bit words from ECS to Central Memory. The initial ECS address is $[(X0) + RA_{ECS}]$; the initial Central Memory address is $[(A0) + RA_{CM}]$.

012   *Write Extended Core Storage*   *(30 Bits)*

fmi	j	, K
59	51 50 48 47	30
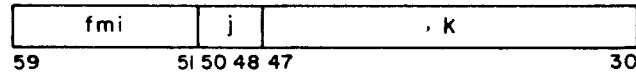
This instruction initiates a Write operation to transfer $[(Bj) + K]$ 60-bit words from Central Memory to ECS. The initial Central Memory address is $[(A0) + RA_{CM}]$; the initial ECS address is $[(X0) + RA_{ECS}]$.

Both instructions must be located in the upper-order position of the instruction word. Typical location of the ECS instructions in a program is shown in Figure 5-8. If an ECS instruction is not located in the upper-order position, the computer will exit to RA_{CM} regardless of the Exit Mode bits. This also occurs if an ECS instruction is attempted in a system that does not have ECS.
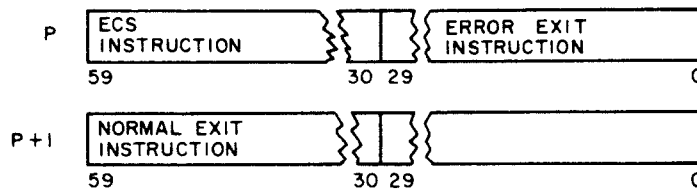

Figure 5-8. Instruction Locations

Either instruction in a system without ECS is illegal. For both instructions, provision is made to inform the Peripheral Processors that an ECS transfer is in progress. A 27, Read (P) Peripheral instruction can monitor the Central Processor Program Address register (P) by transferring its contents to the Peripheral Processor A register. Either ECS instruction forces bit 17 of the P register to appear set to a 27 instruction. However, the bit is not set in the P register.

ADDRESS FORMATION

The starting address in ECS is formed by taking the truncated lower-order 24 bits of operand register X0 and adding this quantity to RA_{ECS}. In the addition, both quantities are taken as positive with the upper-order 36 sign bits (zeros) extended. In the CYBER 72 and 73 the upper 3 bits of RA_{ECS} do not exist; that is, it is a 21-bit quantity.

RA_{ECS} is the Reference Address within ECS, and FL_{ECS} is the alotted Field Length within ECS. Both are 24-bit quantities contained in the Exchange Jump package. When the program specified by this package is being executed, these quantities are held in registers in the Central Processor. The lower-order 6 bits (0-5) of the RA_{ECS} and FL_{ECS} registers do not exist. Therefore, the lower-order 6 bits in either of these 24-bit quantities always appear as zeros.

The starting address in Central Memory is formed by a similar process; the contents of address register A0 are added to RA_{CM}. RA_{CM} is the Reference Address within Central Memory, and FL_{CM} is the allotted Field Length within Central Memory. Both are 18-bit quantities contained in the Exchange Jump package.

Note that adding the Reference Addresses to (A0) and (X0) is accomplished automatically when the Read or Write instructions are executed. The relative addresses in A0 and X0, however, must be placed there by the program prior to executing the ECS instructions.

An example of a typical Read ECS operation follows:

EXAMPLE: Assume that a program starting at an inbounds address contains a Read ECS (011) instruction. The instruction specifies the number of words to be transferred as (Bj) + K. Prior to execution of this instruction, it is assumed that the program loaded registers Bj, A0, and X0 with the control parameters. Because the program was initiated by executing an Exchange Jump, the Central Processor holds the Reference Addresses RA_{CM} and RA_{ECS} and the Field Lengths FL_{CM} and FL_{ECS} as part of the Exchange Jump package.

It is desired, in this example, to transfer a block of 300_8 60-bit words from ECS to Central Memory. The various control parameters (octal) are assumed to be as follows:

(Bj)	= 100	RA_{ECS}	= 26500
K	= 200	FL_{ECS}	= 1600
RA_{CM}	= 1400	(A0)	= 4600
FL_{CM}	= 5300	(X0)	= 603

A map of Central Memory and ECS would then appear as indicated in Figure 5-9.

A similar operation occurs for the Write ECS (012) instruction.

For both Read and Write operations, the parameters held with the Central Processor which control the block transfer (namely Bj, X0, A0, RA_{CM}, RA_{ECS}, FL_{CM}, and FL_{ECS}) do not vary during the transfer. Therefore, an Exchange Jump occuring during a transfer may be initiated. However, when the transfer program is again resumed, the transfer is started with the original parameters, and not from the addresses used just before the interruption in the program.
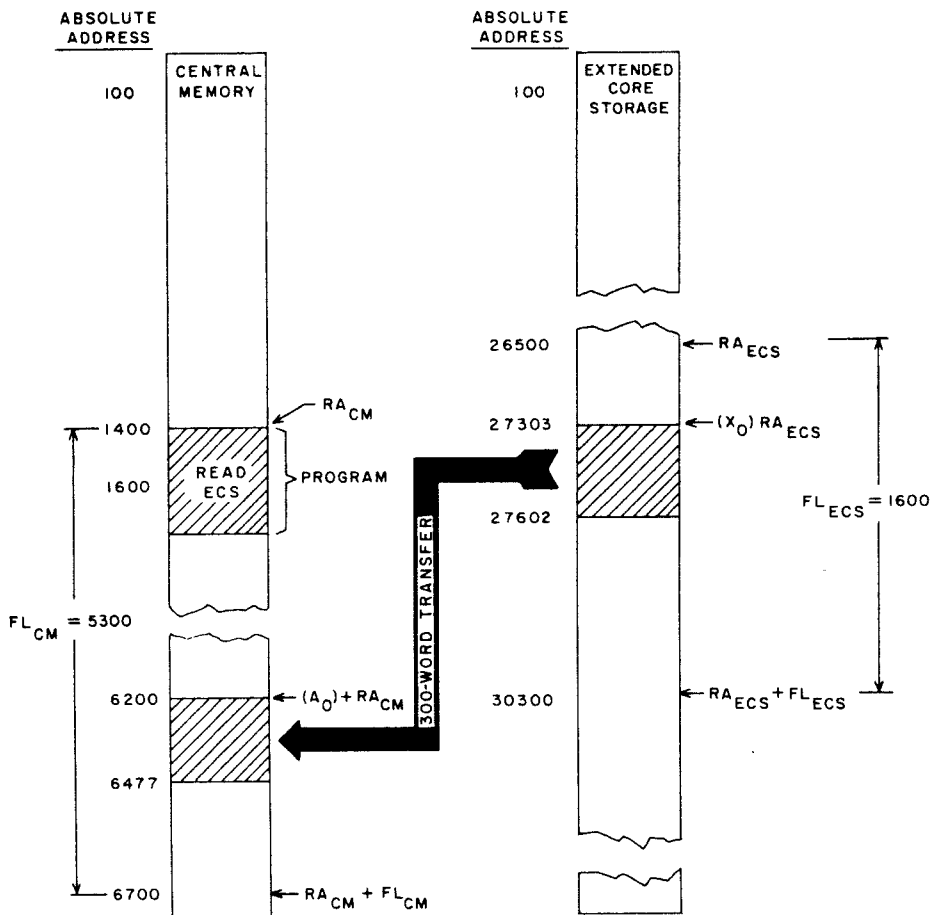

Figure 5-9. Memory Map (Read ECS Example)

ADDRESS RANGE FAULTS

Four address range fault conditions can arise when executing the Extended Core Storage Communication instructions:

- Word count fault

- Central Memory address out of range

- Extended Core Storage address out of range

- Last 60-bit word (word 7) in FL_{ECS} is referenced

    1. Word Count

        If, in forming the word count $[(Bj) + K]$, the result is negative, an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at $(P) + 1$ with no data transfer .

    2. Central Memory Address

        Central Memory address out of range is checked by comparing FL_{CM} with the sum $[(A0) + (Bj) + K]$. FL_{CM} must be greater than this sum or an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at $(P) + 1$ with no data transfer.

    3. Extended Core Storage Address

        Extended Core Storage address out of range is checked by comparing FL_{ECS} with the sum $[(X0) + (Bj) + K]$. In the comparison, FL_{ECS} is a 24-bit quantity with 36 upper-order bits of sign extended; X0 holds the 24-bit address quantity with 36 zeros occupying the upper-order bit positions. The result of this subtraction should always be negative; if positive, an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at $(P) + 1$ with no data transfer.

    4. Word 7 reference in FL_{ECS}

        If, after formation of the ECS address, the address format specifies a reference to word 7 in relative address FL_{ECS}, an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at $(P) + 1$ with no data transfer.

Note that address range checks are made on the entire block of both Extended Core Storage and Central Memory addresses before the transfer (Read or Write) is begun. If any address in the block to be transferred is out of range, either in Central Memory or Extended Core Storeage, no data is transferred, regardless of whether or not the Address Out of Range bit is set in the Exit Mode register.

ERROR ACTION

An error exit is an exit to the lower-order 30 bits of the instruction word containing the ECS Read or Write instruction. These 30 bits should always hold a jump to an error routine.

Three error conditions cause an error exit:

1. Parity error(s) when reading ECS. If a parity error is detected, the entire block of data is transferred before the exit is taken.

2. The ECS bank from/to which data is to be transferred is not available because the bank is in Maintenance mode, or the bank has lost power. If either of these conditions exists on an attempted Read or Write, an immediate error exit is taken.

3. An attempt to reference a nonexistent address. On an attempted Write operation, no data transfer occurs and an immediate error exit is taken. If the attempted operation is a Read, and addresses are in range, zeros are transferred to Central Memory. This is a convenient high-speed method of clearing blocks of Central Memory.

EXCHANGE JUMP DURING ECS COMMUNICATION

If an Exchange Jump occurs while an Extended Core Storage transfer is in progress, the exchange waits until completion of a record. Action is then as follows:

1. If the record just completed is the last record of the block transfer, and the transfer was error-free, the Central Processor exits to (P) + 1. The Exchange Jump then takes place.

2. If the record just completed is the last record of the block transfer, and an error condition exists, the Central Processor exits to the lower instruction, executes it, and the Exchange Jump is performed.

3. If the record just completed does not complete the block transfer, the Exchange Jump occurs, and (P) are stored in the Exchange Jump package. A return Exchange Jump to this program begins execution with the ECS Read or Write instruction and restarts the transfer. Note that the transfer does not resume at the point at which it was truncated; rather, the entire transfer must be repeated.

PERIPHERAL PROCESSOR READ OR WRITE DURING ECS TRANSFERS

The Peripheral Processors can access Central Memory during an ECS transfer. The Central Memory address requested by the Peripheral Processor is held by the Coupler until the end of a record is reached (maximum delay is 1 μsec). The Coupler then stops all ECS action and allows the memory reference by the Peripheral Processor. When it is complete, Coupler action proceeds as before. There is no effect on the ECS transfer other than the delay of 1 μsec. Note that conflicts can be minimized by using the Access Priority capability (see Volume 1, System Description) and by monitoring the Central Processor P Register bit 17 which is set during an ECS transfer.

DISTRIBUTIVE DATA PATH

INTRODUCTION

The Distributive Data Path unit (DDP) provides the capability for any CYBER 70, Model 72, 73, or 74 PPU to communicate with Extended Core Storage. The DDP has one PPU port in the standard configuration, with two, three, and four PPU port configurations available (Figure 5-10). Each port accommodates one PPU channel.

DISTRIBUTIVE DATA PATH

NOTE: ◄ — — — ► CONTROL

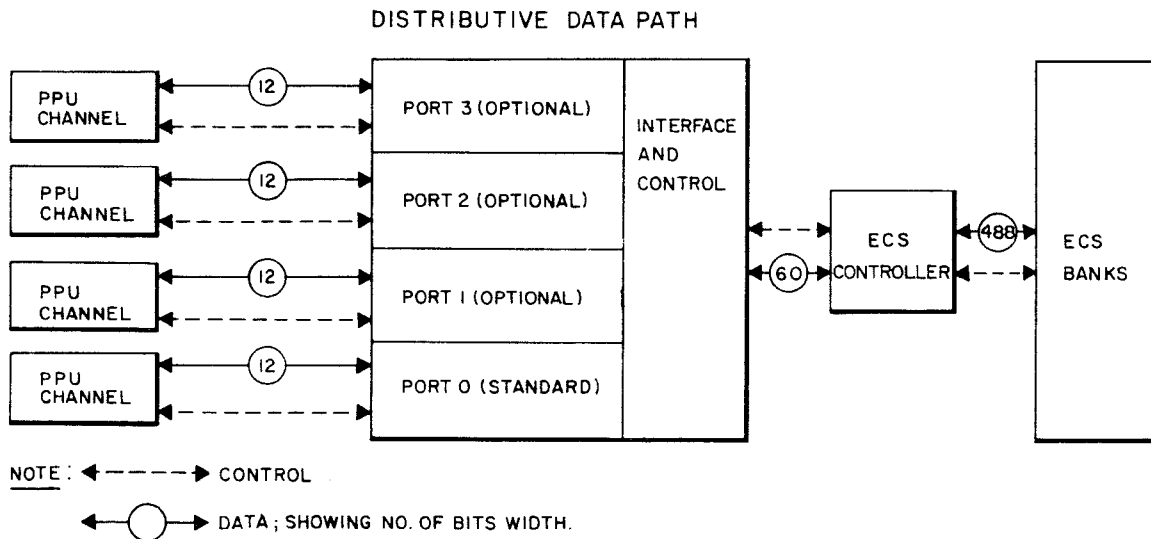◄—◯—► DATA ; SHOWING NO. OF BITS WIDTH.

Figure 5-10. DDP Configuration

The DDP communicates with the ECS Controller through one of the four, 60-bit controller accesses, and communicates with PPU's through 12-bit normal data channels. The DDP allows a PPU to do block transfers, or to modify a 480-bit ECS record by writing a single 60-bit word into the ECS record.

A DDP port consists of nine 60-bit buffer registers, a 24-bit Address/Flag Word register, and PPU channel interface and control logic. A port may operate in maintenance mode to perform diagnostics, or to transmit an ECS record containing a parity error to a PPU.

PROGRAMMING

Data Assembly

The DDP assembles (on a write operation) or disassembles (on a read operation) a full ECS record of 480 bits in eight of the buffer registers. The ninth buffer register accommodates 12-bit byte transfers between the PPU and the DDP port while the 480-bit ECS record is transferred between the DDP and the ECS Controller. The buffer registers hold 12-bit bytes as shown in Figure 5-11.

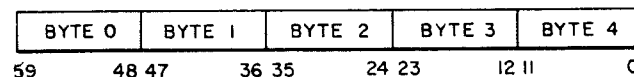| BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4
59 48	47 36	35 24	23 12	11 0

Figure 5-11. DDP Assembly of Bytes in a 60-bit Word

Function Codes

A DDP port performs functions according to a 12-bit function code and the upper three bits of a 24-bit address/flag word. The most significant octal digit (5) is the equipment select code for the DDP. Table 5-3 shows codes and upper address bit values for legal functions.

TABLE 5-3. DDP FUNCTION CODES AND UPPER ADDRESS BITS

Function	Code	Address Bit 23	Address Bit 22	Address Bit 21
Block Read ECS	5001	0	0	0
Block Write ECS	5002	0	0	0
Select Status	5004	0	0	0
Master Clear Port	5010	0	0	0
Read ECS, One Reference	5001	0	1	0
Select Maintenance Mode	5001	0	0	1
Function Flag Register	5001	1	X	X

5001 - Block Read ECS

This function causes the port to read data from ECS and direct the data to the PPU channel
to be read by the PPU. The port responds to a Block Read ECS function by disconnecting
the data channel. When the channel is activated by the PPU, the port accepts an output of
two 12-bit bytes from the PPU and loads them into the 24-bit Address Register. The port
then requests ECS and holds the data received for input to the PPU.

The first 12-bit byte received from the PPU is put into the upper portion of the Address
Register; the second 12 bits are put into the lower portion of the Address Register. The
Address Register now designates the address of the first 60-bit word to be made available
to the PPU. This address is presented to the controller along with a Request signal. As
data is received from the controller the Address Register is incremented once for each 60-bit
word. When data is received from ECS, it is presented to the PPU. When the PPU has
emptied the data buffer, a new ECS reference is made. Unless an error condition is
encountered, the port continues to present data to the PPU in this manner until the PPU
terminates the read operation by disconnecting the data channel.

Two error conditions cause the port to disconnect the data channel during a Block Read ECS
operation. They are:

    ECS Abort
    ECS Parity Error

If the port receives either of these two conditions from the controller, the port will disconnect
the data channel when it is Empty, rather than send a Full and the next byte of data. Thus,
in order to prevent a data channel hang-up when disconnecting via the PPU, the PPU must
look for a Full condition on the data channel before performing a disconnect.

NOTE

The PPU must not disconnect the data channel if it senses
the channel as being Empty, as the port may disconnect
before the PPU disconnect instruction can be carried out
causing the PPU to hang on that instruction.

When the data channel is disconnected by the port, the PPU must issue a Select Status (5004) function to determine the reason for the disconnect. In the case of Parity Error, the PPU may issue a Read function while in maintenance mode to input the data contained in the buffer registers. After a parity error, the PPU must issue a new Block Read ECS function or a Single Record Read function to read more data from ECS.

A typical instruction sequence to do a block ECS Read is:

Address	Instruction		Comments	
	FNC	5001	Send 5001 function to channel	
	ACN		Activate channel	
	OAM	XXXX	(A)=2, output two bytes on channel for ECS address.	
	IAM	XXXX	Input (A) bytes of data from channel	
	NJN		Check reason for exit from previous instruction. If (A)=0 then transfer is complete; if (A)≠0 then DDP disconnected channel. In the latter case the NJN instruction would cause a jump to an error checking routine.	
B	IJM	A	Jump to A if channel is inactive	Wait for channel to go from Active and Empty to Active and Full.
	EJM	B	Jump to B if channel is empty	
	DCN		Disconnect channel	
A	Continue			

Note that the time required for the channel to change from the Active and Empty state may vary from 0 to 50 microseconds. The Block Read ECS condition is cleared by a disconnect or a channel Master Clear.

5002 - Block Write ECS

This function causes the port to write data into ECS, from data sent to the port via the PPU. The port responds to an ECS Write function by disconnecting the data channel. When the PPU activates the channel, the port accepts a block output of data. The first two bytes of data received from the PPU are loaded into the 24-bit Address Register. Additional bytes received from the PPU are regarded as data to be sent to ECS.

The DDP places the first 12-bit byte into the upper portion of the Address Register, and the second byte into the lower portion of the Address Register. The Address Register now designates the address of the first 60-bit word to be written. The DDP presents this address to the ECS Controller along with a request signal after the buffer in the port is filled by the PPU or after a disconnect from the PPU. The Address Register is incremented as the buffer empties into ECS. Unless an error condition is encountered, data continues to be transferred. A disconnect from the PPU causes accumulated data to be written into ECS, but increments the Address Register only by the number of 60-bit words written into ECS. A disconnect also terminates the BlockWrite ECS condition. If the PPU disconnects with less than an integer multiple of 60-bit words assembled in the buffer registers, the port writes the partial 60-bit word into ECS with zeros in the missing byte(s).

A program sequence such as the following produces a partial ECS write with zero fill.

Instruction		Comments
FNC	5002	Send 5002 function to channel
ACN		Activate channel
LDC	20_{10}	Load A register with 20_{10} (18 bytes data 2 bytes address)
OAM		Output 20_{10} bytes on channel
DCN		Disconnect channel

When the channel is disconnected, the data in the buffers progresses to fill the buffer registers as shown in Figure 5-12.

Rank	0	1	2	3	4	5	6	7	8
	0	0	0	0	0	X	X	X	X
	0	0	0	0	0	X	X	X	X
	0	0	0	0	0	X	X	X	X
	0	0	0	0	0	0	X	X	X
	0	0	0	0	0	0	X	X	X

Where X=one byte of PPU data

Figure 5-12. DDP Buffer Register Contents on a Partial Write

An ECS reference is then made. Only four 60-bit words are written into ECS: 216 bits of data followed by 24 bits of zero fill. The remaining 240 bits of the ECS record are not altered. Note that this allows writing a single 60-bit word anywhere in the ECS record by sending an address and five, 12-bit bytes to the port. The lower three bits of the address specify the 60-bit word to be written in the 480-bit record specified by the upper address bits.

Only the Abort error condition is possible on ECS Write. When the controller returns an Abort signal during a PPU-port transfer, the port disconnects the I/O channel. This disconnect is sent to the I/O channel in the place of an Empty response to a Full signal from the data channel. The Inactive status on the channel causes an exit from the OAM instruction to a jump instruction. Before issuing a new read or write function, the PPU must issue a Select Status (5004) function to determine whether the write status bit has dropped, or whether the ECS Controller returned an Abort to the port after the PPU disconnected the channel.

A typical instruction sequence to do a Block Write ECS is:

Instruction		Comments
FNC	5002	Send 5002 function to channel
*OAM	XXXX	(A)=2; output two bytes on channel as ECS address
*OAM	XXXX	Output data
NJN		Check reason for exit from previous instruction. If (A)=0 then transfer is complete; if (A)≠0 then DDP disconnected channel. In the latter case, the NJN instruction would cause a jump to an error checking routine.

* A single OAM could be used.

Instruction	Comments
DCN	Disconnect channel
FNC	Read status until either an Abort or an Accept is detected. This requires from zero to 50 μsec, depending on ECS activity

The Block Write ECS condition is cleared out by a disconnect, a new function, or by a channel Master Clear.

5004 - Select Status

This function makes the status of the port available for PPU input after the channel is activated by the PPU. The port responds to this function by disconnecting the channel. The PPU then activates the channel and performs an input.

Status bits are assigned to indicate the following: (Bits 4 through 11 are not used)

        Bit 0   ECS Abort
        Bit 1   ECS Accept
        Bit 2   ECS Parity Error
        Bit 3   ECS Write Selected

Bit 0 - ECS Abort: This status bit is cleared upon a new request to ECS, a Select Status or Master Clear Port function, or a channel Master Clear.

Bit 1 - ECS Accept: This status bit is cleared upon a new request to ECS, a Select Status or Master Clear Port function, or a channel Master Clear.

Bit 2 - ECS Parity Error: This status bit indicates that a 60-bit word from ECS was found to have a parity error. This bit is cleared upon a Select Status or Master Clear Port function, or a channel Master Clear.

Bit 3 - ECS Write Selected: The status bit indicates that the port is busy with an ECS Write. When the write terminates, the status bit clears.

5010 - Master Clear Port

This function performs a Master Clear on the port logic.

5001 - With Address Bit 22 Set, Read ECS, One Reference

This function is identical to Block Read ECS except that only one reference is made to ECS.

5001 - With Address Bit 21 Set, Select Maintenance Mode

This function blocks the port associated with that channel from requesting ECS. This allows data to be put into the port buffer from the PPU, and then to be read back again for hardware maintenance purposes.

A PPU may input an ECS record containing a parity error by selecting maintenance mode and performing a Read function. The port returns only the record in its buffer registers. The PPU will hang if more data is requested than the buffer contains.

A Read or Write function with address bit 21 clear brings a port out of maintenance mode and allows it to function normally.

5001 - With Address Bit 23 Set, Function Flag Register

This function is used to do a Flag Register operation. The contents of the Flag Register in the ECS Controller cannot be read directly, but may be interrogated and/or changed. When address bit 23 is set, the controller treats the address as a Flag Function word, and no ECS reference is made.

The port responds to the 5001 function code by disconnecting the I/O channel. The PPU then activates the channel, and sends the Flag word out as two 12-bit bytes. The port places the first byte in the upper part of the Address Register, and the second byte in the lower part of the Address Register. When the port sends the contents of the Address Register to the controller, the controller monitors the upper three bits to determine which Flag Register Function to perform.

ECS Controller responses to Flag Function operations are described on page 5-9 under FLAG REGISTER.

5020 - Clear Maintenance Mode

This function brings the port associated with that channel out of maintenance mode and allows it to function normally. This function is provided for hardware maintenance purposes. The port disconnects the I/O channel in reply to this function.

5030 - Clear DDP Port

This function performs a Master Clear on the logic associated with one port.