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DEFINITIONS

GENERAL DEFINITIONS

COMPUTER- IN THE FOLLOWING DEFINITIONS, WE SHALL USE THE TERM "COMPUTER", MEANING "THE PHYSICAL UNIT, HARDWARE", ONLY.

COMPUTER PROGRAM- A COMPLETE AND SEQUENCED GROUP OF INSTRUCTIONS, NECESSARY TO SOLVE A PROBLEM BY COMPUTER. REFERRED TO AS A "PROGRAM".

B1500 DEFINITIONS

S-SOURCE PROGRAM- A COMPUTER PROGRAM, CONSISTING OF A SET OF INSTRUCTIONS, FROM WHICH A TRANSLATOR (GENERATOR, COMPILER, OR ASSEMBLER) GENERATES AN S-OBJECT PROGRAM.

S-OBJECT PROGRAM- A COMPUTER PROGRAM, CONSISTING OF A SET OF INSTRUCTIONS. THE INSTRUCTIONS ARE MADE ENTIRELY OF CHARACTERS, CAPABLE OF REPRESENTING THE "PLUS-MINUS" LOGIC OF A COMPUTER WITHOUT TRANSLATION, USUALLY THE BINARY NUMBERS 0 AND 1.

PRE-B1500 PROCEDURE- IN THE FIELD, AN APPLICATIONS PROGRAMMER WOULD CODE AN S-SOURCE PROGRAM, A SEQUENCED GROUP OF INSTRUCTIONS WRITTEN IN SOME PRE-DEFINED LANGUAGE (FORTRAN, COBOL, ETC.), TO SOLVE A SPECIFIC PROBLEM. BY MEANS OF THE APPROPRIATE TRANSLATOR AN S-OBJECT PROGRAM WOULD BE GENERATED. THE S-OBJECT PROGRAM, WOULD THEN BE DIRECTLY INTERPRETED AND USED BY THE COMPUTER (HARDWARE).

M- ACRONYM FOR MICRO.

M-SOURCE PROGRAM- A COMPUTER PROGRAM, CONSISTING OF A SET OF M-INSTRUCTIONS, FROM WHICH THE MIL ASSEMBLER GENERATES AN M-OBJECT PROGRAM.

B1500 DEFINITIONS 00000570

M-OBJECT PROGRAM- A COMPUTER PROGRAM, CONSISTING OF A SET OF INSTRUCTIONS. THE INSTRUCTIONS ARE MADE ENTIRELY OF THE BINARY NUMBERS 0 AND 1. THE M-OBJECT PROGRAM IS CAPABLE OF BEING USED DIRECTLY, WITHOUT TRANSLATION, BY THE B1500 COMPUTER (HARDWARE). 00000585 00000585 00000590 00000595 00000610

B1500 PROCEDURE- WITH THE B1500 COMPUTER AN ADDITIONAL LEVEL OF PROGRAMMING HAS BEEN INTRODUCED, THE "M-LEVEL". THE TASK OF ALL M-PROGRAMS IS TO INTERPRET S-OBJECT PROGRAMS, THUS PLACING PREVIOUS HARDWARE TASKS IN THE HANDS OF THE SYSTEMS PROGRAMMER. WITH THE B1500, AN APPLICATIONS PROGRAMMER WOULD CODE AN S-SOURCE PROGRAM; BY MEANS OF THE APPROPRIATE TRANSLATOR AN S-OBJECT PROGRAM WOULD BE GENERATED, AND THEN INTERPRETED BY THE APPROPRIATE "M-OBJECT PROGRAMS". THUS THE "M-LEVEL" ACTS AS A LINK BETWEEN S-OBJECT PROGRAMS AND THE COMPUTER HARDWARE. 00000615 00000615 00000620 00000625 00000630 00000635 00000635 00000640 00000645 00000650 00000660

M-SOURCE INSTRUCTION- AN M-OPERATOR, KEYWORDS, OPERAND OR OPERANDS, AND CONSTANTS ARRANGED IN A PRE-DEFINED PATTERN. 00000665 00000665 00000675

M-OBJECT INSTRUCTION- A PRE-DEFINED PATTERN OF BINARY NUMBERS 0 AND 1, DIRECTLY USED BY B1500 HARDWARE WITHOUT TRANSLATION. USUALLY GENERATED BY THE MIL ASSEMBLER FROM M-SOURCE INSTRUCTIONS. 00000680 00000685 00000685 00000700

M-OPERATOR- THE ACTION WORDS OR VERBS OF AN M-INSTRUCTION. 00000710

KEYWORDS- PREPOSITIONS (FROM, TO, BY, WITH) USED FOR CLARIFICATION IN M-SOURCE INSTRUCTIONS. 00000710 00000725

OPERAND- THAT PORTION OF AN INSTRUCTION THAT IS ACTED UPON BY THE M-OPERATORS. REGISTERS, SCRATCHPADS, A-STACK, M-MEMORY. 00000730 00000730 00000740

ALPHABETICAL LIST OF REGISTERS

NAME	LENGTH (BITS)	NOTE	
A	20	MICRO-MEMORY ADDRESS	00000780
BICN	4	BIT CONDITIONS	00000785
BR	24	BASE REGISTER	00000790
C	24	INTERRUPTS, FUNCTION BOX INFO.	00000795
CA	4	-HIGH SUBFIELD OF C	00000800
CB	4	- SUBFIELD OF C	00000805
CC	4	- SUBFIELD OF C	00000810
CD	4	- SUBFIELD OF C	00000815
CMPX	24	RESULT: COMPLEMENT OF X	00000820
CMPY	24	RESULT: COMPLEMENT OF Y	00000825
CP	8	- SUBFIELD OF C	00000830
DIFF	24	RESULT: X MINUS Y	00000835
FA	24	S-MEMORY ADDRESS	00000840
FB	24	S-MEMORY UNIT AND LENGTH	00000845
FL	20	S-MEMORY LENGTH	00000850
FLB	4	-HIGH SUBFIELD OF FL	00000855
FLC	4	- SUBFIELD OF FL	00000860
FLD	4	- SUBFIELD OF FL	00000865
FLE	4	- SUBFIELD OF FL	00000870
FLF	4	-LOW SUBFIELD OF FL	00000875
FLCN	4	FL CONDITIONS	00000880
FU	4	S-MEMORY UNIT	00000885
INCN	4	INTERRUPT CONDITIONS	00000890
L	24	NO SPECIAL USES	00000895
LA	4	-HIGH SUBFIELD OF L	00000900
LB	4	- SUBFIELD OF L	00000905
LC	4	- SUBFIELD OF L	00000910
LD	4	- SUBFIELD OF L	00000915
LE	4	- SUBFIELD OF L	00000920
LF	4	-LOW SUBFIELD OF L	00000925

ALPHABETICAL LIST OF REGISTERS

NAME	LENGTH (BITS)	NOTE	
----	------	----	00000945
			00000950
			00000955
			00000960
LR	24	LIMIT REGISTER	00000965
M	16	CONTAINS CURRENT MICRO-INSTRUCTION	00000970
MC	4	-HIGH SUBFIELD OF M	00000975
MD	4	- SUBFIELD OF M	00000980
ME	4	- SUBFIELD OF M	00000985
MF	4	-LOW SUBFIELD OF M	00000990
MSKX	24	RESULT: MASKED X	00000995
MSKY	24	RESULT: MASKED Y	00001000
SUM	24	RESULT: X + Y	00001005
T	24	ROTATE, SHIFT, EXTRACT BITS, ETC.	00001010
TAS	24	TOP OF ASTACK	00001015
TA	4	-HIGH SUBFIELD OF T	00001020
TB	4	- SUBFIELD OF T	00001025
TC	4	- SUBFIELD OF T	00001030
TD	4	- SUBFIELD OF T	00001035
TE	4	- SUBFIELD OF T	00001040
TF	4	- SUBFIELD OF T	00001045
X	24	INPUT TO FUNCTION BOX	00001050
XANY	24	RESULT: X AND Y	00001055
XEOY	24	RESULT: X EXCLUSIVE OR Y	00001060
XORY	24	RESULT: X OR Y	00001065
XYCN	4	XY CONDITIONS	00001070
XYST	4	XY STATUS	00001075
Y	24	INPUT TO FUNCTION BOX	00001080

SCRATCHPAD WORDS

THE M-PROCESSOR MAKES USE OF THE SCRATCH PAD FOR TEMPORARY STORAGE OF ACTIVE REGISTERS. THE SCRATCH PAD WORDS MAY BE ADDRESSED AS 16 FORTY-EIGHT BIT WORDS OR 32 TWENTY-FOUR BIT WORDS.

PAD-WORDS - 24 BITS EACH

S0A	S4A	S8A	S12A
S0B	S4B	S8B	S12B
S1A	S5A	S9A	S13A
S1B	S5B	S9B	S13B
S2A	S6A	S10A	S14A
S2B	S6B	S10B	S14B
S3A	S7A	S11A	S15A
S3B	S7B	S11B	S15B

DOUBLE PAD-WORDS - 48 BITS EACH

(SI=SIA AND SIB CONCATENATED)

S0	S4	S8	S12
S1	S5	S9	S13
S2	S6	S10	S14
S3	S7	S11	S15

SPECIAL TERMS

TERM	BITS	NOTE	
----	----	----	00001235
			00001240
			00001245
F	48	FA AND FB CONCATENATED	00001250
XY	48	X AND Y CONCATENATED	00001255
SO	48	SOA AND SOB, DOUBLE SCRATCHPAD WORD	00001260
CP	8	CYF,CPU,CPL COLLECTIVELY	00001265
CYF	1	CARRY FLIP-FLOP, PART OF CP	00001270
CPU	2	INDICATES UNIT, PART OF CP	00001275
CPL	5	LENGTH OF X AND Y, PART OF CP	00001280
FU	4	INDICATES UNIT SIZE	00001285
SU	4	UNIT, PART OF SOB CORR. TO FU IN FB	00001290
CYL	4	CARRY LEVEL	00001295
CYD	1	CARRY DIFFERENCE	00001297
FL	20	S-MEMORY ACCESS LENGTH	00001300
SFL	20	PART OF SOB CORRESPONDING TO FL IN FB	00001305

ORGANIZATION OF FIELDS AND SUBFIELDS

FIELD	SUBFIELDS	00001325
		00001330
		00001335
C	CA CB CC CD CP	00001340
F	FA FB	00001345
FB	FU FL	00001350
FL	FLB FLC FLD FLE FLF	00001355
L	LA LB LC LD LE LF	00001360
M	MC MD ME MF	00001365
T	TA TB TC TD TE TF	00001370

MICRO-INSTRUCTION CONTROLS 00001390

A 00001400
M 00001405
TAS 00001410

S-MEMORY CONTROLS 00001420

BR 00001430
LR 00001435
FA 00001440
CP 00001445

INTERRUPT CONTROLS 00001455

CA 00001465
CB 00001470
CC 00001475
CD 00001480

REGISTER GROUP AND SELECT

	SELECT 0	SELECT 1	SELECT 2	SELECT 3	
	------ -	------ -	------ -	------ -	00001500
					00001505
GROUP 0	TA	FU	X	SUM	00001510
GROUP 1	TB	FLB	Y	CMPX	00001515
GROUP 2	TC	FLC	T	CMPY	00001520
GROUP 3	TD	FLD	L	XANY	00001525
GROUP 4	TE	FLE	A	XEQY	00001530
GROUP 5	TF	FLF	M	MSKX	00001535
GROUP 6	CA	BICN	BR	MSKY	00001540
GROUP 7	CB	FLCN	LR	XORY	00001545
GROUP 8	LA	MC	FA	DIFF	00001550
GROUP 9	LB	MD	FB		00001555
GROUP 10	LC	ME	FL		00001560
GROUP 11	LD	MF	TAS		00001565
GROUP 12	LE	XYCN	CP		00001570
GROUP 13	LF	XYST			00001575
GROUP 14	CC	INCN			00001580
GROUP 15	CD				00001585

VARIABLES

```
A                                                                   00001605
BR                                                                  00001610
CA CB CC CD CP                                                      00001615
FA                                                                  00001620
FB                                                                  00001625
FL                                                                  00001630
FLB FLC FLD FLE FLF                                                 00001635
FU                                                                  00001640
L                                                                   00001645
LA LB LC LD LE LF                                                   00001650
LR                                                                  00001655
M                                                                   00001660
MC MD ME MF                                                         00001665
T                                                                   00001670
TA TB TC TD TE TF                                                   00001675
X                                                                   00001680
Y                                                                   00001685
```

RESERVED WORDS

=	≠	>	≥	<	≤	00001705
(	)	*	A	ALL	ALL CLEAR	00001710
AND	ANY	ASTACK	BIAS	BICN	BITS	00001715
BR	BY	C	CA	CALL	CARRY	00001720
CB	CC	CD	CLEAR	CMPX	CMPY	00001725
COUNT	CP	CPL	CPU	CYL	DEC	00001730
DIFF	DOWN	EOR	EQL	EXIT	DIFFERENCE	00001735
EXTRACT	F	FA	FALSE	FB	FL	00001740
FLB	FLC	FLD	FLE	FLF	FROM	00001745
GO	INC	INCN	INTO	JUMP	L	00001750
LA	LABEL	LB	LC	LD	LE	00001755
LEFT	LF	LIT	LOAD	LR	LSBX	00001760
LSBY	M	MC	MD	ME	MF	00001765
MOVE	MSBX	CYD	MSKX	MSKY	NORMALIZE	00001770
OR	OVERLAY	PORT	READ	REVERSE	RIGHT	00001775
ROTATE	S	S0	S0A	S0B	S1	00001780
S1A	S1B	S2	S2A	S2B	S3	00001785
S3A	S3B	S4	S4A	S4B	S5	00001790
S5A	S5B	S6	S6A	S6B	S7	00001795
S7A	S7B	S8	S8A	S8B	S9	00001800
S9A	S9B	S10	S10A	S10B	S11	00001805
S11A	S11B	S12	S12A	S12B	S13	00001810
S13A	S13B	S14	S14A	S14B	S15	00001815
S15A	S15B	SET	SFL	SHIFT	SKIP	00001820
STORE	SUM	SUMMARY	SWAP	T	TA	00001825
TAS	TB	TC	TD	TE	TEST	00001830
TF	TO	TRUE	UNIT	UP	WHEN	00001835
WITH	WRITE	X	XANY	XCH	XEOY	00001840
XORY	XY	XYCN	XYST	Y	IF	00001845
FU	CYF	SU				00001850

ACTIVE REGISTERS

X-Y REGISTERS

THE X AND Y REGISTERS ARE EACH 24 BITS WIDE AND ARE USED AS THE BUFFERS INTO THE X-Y FUNCTION BOX. ALL FUNCTIONS ARE PERFORMED UNDER CONTROL OF THE C REGISTER WHICH CONTAINS THE LENGTH OF OPERATION, THE TYPE OF UNIT, AND LEAST SIGNIFICANT CARRY INPUT. IN ADDITION THE X AND Y REGISTERS ARE CAPABLE OF BEING SHIFTED OR ROTATED AND MAY RECIEVE OR TRANSMIT DATA TO THE MAIN MEMORY SYSTEM.

F REGISTER

THE F REGISTER IS DIVIDED INTO FA AND FB, EACH 24 BITS WIDE. THE FA PORTION IS USED TO ADDRESS MAIN MEMORY. FB IS FURTHER DIVIDED INTO FU, 4 BITS INDICATING UNIT SIZE, AND FL, 20 BITS GENERALLY USED TO INDICATE LENGTH OF FIELDS IN MAIN MEMORY. FL IS FURTHER SUBDIVIDED INTO FLB, FLC, FLD, FLE, AND FLF, EACH BEING 4 BITS LONG.

L REGISTER

THE L REGISTER IS 24 BITS WIDE AND SUBDIVIDED INTO LA, LB, LC, LD, LE, AND LF, EACH 4 BITS IN LENGTH. L AND ITS SUBDIVISIONS ARE GENERALLY USED TO HOLD TEMPORARILY THE CONTENTS OF OTHER M-PROCESSOR REGISTERS. NO SPECIAL FUNCTIONS ASSOCIATED WITH L.

T REGISTER

THE T REGISTER IS A 24 BIT TRANSFORMATION REGISTER USED EXTENSIVELY FOR INTERPRETATION OF OPERATORS. IT IS SUBDIVIDED INTO TA, TB, TC, TD, TE, TF, EACH OF 4 BITS. T HAS STRONG SHIFT AND EXTRACT LOGICS ASSOCIATED WITH IT AND IS THE PRINCIPAL FORMATTING REGISTER OF THE M-PROCESSOR. THE REGISTER ALSO HAS THE CAPABILITY OF RECIEVING OR TRANSMITTING DATA WITH MAIN MEMORY.

M REGISTER

THE M REGISTER IS A 16 BIT REGISTER WHICH HOLDS THE MICRO- OPERATOR. AS SUCH, IT IS THE MACHINE INSTRUCTION REGISTER. IT IS FURTHER DIVIDED INTO MC, MD, ME, AND MF, EACH OF 4 BITS.

BR AND LR REGISTERS

THE BR AND LR REGISTERS ARE EACH 24 BITS WIDE AND USED TO HOLD THE BASE AND LIMIT ADDRESS OF THE ACTIVE PROCESS WORK SPACE. THE HARDWARE USES THESE REGISTERS TO DETERMINE IF ADDRESSES IN THE FA REGISTER ARE WITHIN THE BASE/LIMIT BOUNDRIES OF MAIN MEMORY.

A REGISTER

THE A REGISTER IS A 20 BIT ADDRESS REGISTER USED TO FETCH M INSTRUCTIONS TO THE M REGISTER FOR EXECUTIONS. AUTOMATIC INCREMENTATION IS PROVIDED.

C REGISTER

THE C REGISTER IS A 24 BIT CONTROL REGISTER FOR THE PROCESSOR CONTAINING THE LENGTH AND TYPE OF MEMORY OPERAND, CARRY INPUT, INTERRUPT CONDITIONS AND INTERRUPT MASK. IT IS FURTHER SUBDIVIDED INTO CA, CB, CC, CD EACH 4 BITS, AND CP, 8 BITS. CA AND CB (8 BITS) REPRESENT THE M-PROCESSOR INTERRUPT MASK. CC AND CD (8 BITS) REPRESENT THE M-PROCESSOR INTERRUPT REGISTER. CP (8 BITS) CONTAINS FUNCTION BOX CONTROLS; CYF (0 BIT OF CP), CPU (1 AND 2 BITS OF CP), AND CPL (3,4,5,6,7 BITS OF CP). CYF NOTIFIES THE FUNCTION BOX THAT A PREVIOUS UNIT CARRY MUST BE ADDED TO ITS SUMMARY RESULTS. CPL NOTIFIES THE FUNCTION BOX OF THE LENGTH IN BITS OF THE ITEMS IN X AND Y. CPU NOTIFIES THE FUNCTION BOX OF THE TYPE OF UNITS CONTAINED IN X AND Y; 00 = BINARY, 01 = 4 BIT DECIMAL, 10 = 6 BIT DECIMAL, AND 11 = 8 BIT DECIMAL.

RESULT REGISTERS

XORY	XANY	XEOY
CMPX	CMPY	MSKX
MSKY	SUM	DIFF

EACH OF THE NINE RESULT REGISTERS ARE 24 BITS IN LENGTH. THEY ARE PRODUCED IMMEDIATELY AND AUTOMATICALLY FROM X AND Y. THEY CANNOT BE CHANGED EXCEPT BY CHANGING THE INPUTS TO THE FUNCTION BOX, X OR Y. THE RESULT REGISTERS MAY NOT BE THE RECIEVING FIELDS IN A "MOVE" OR ANY INSTRUCTION.

XORY

"OR" X INCLUSIVELY WITH Y. THIS IS A 24 BIT COMPARE. CORRESPONDING PAIRS OF BITS ARE TREATED INDEPENDENTLY.

XANY

"AND" X WITH Y. THIS IS THE LOGICAL PRODUCT OF X AND Y. CORRESPONDING PAIRS OF BITS ARE TREATED INDEPENDENTLY. THE "AND" FUNCTION IS PERFORMED ON ALL 24 BITS OF X AND Y.

XEOY

"OR" X EXCLUSIVELY WITH Y, MEANING THAT THE SUM OF X, Y, AND XEOY IS MODULO 2. THIS IS A 24 BIT COMPARE, WITH CORRESPONDING PAIRS OF BITS BEING TREATED INDEPENDENTLY.

CMPX

ONES COMPLEMENT OF X. A 24 BIT COMPLEMENT, WITH CORRESPONDING BIT PAIRS BEING TREATED INDEPENDENTLY.

CMPY

ONES COMPLEMENT OF Y. 24 BIT COMPLEMENT, AND CORRESPONDING PAIRS OF BITS ARE TREATED INDEPENDENTLY.

RESULT REGISTERS

MSKX 00002450

"MASKED X". CORRESPONDING BIT PAIRS ARE INDEPENDENT, AND MASK IS LEFT TRUNCATED. LENGTH OF MASK IS CONTROLLED BY CPL. 00002465 00002475

MSKY 00002475

"MASKED Y". CORRESPONDING BIT PAIRS ARE TREATED INDEPENDENTLY, AND THE MASK IS LEFT TRUNCATED. LENGTH OF THE MASK IS CONTROLLED BY CPL. 00002490 00002505

SUM 00002505

"SUM". THE DECIMAL OR BINARY ADDITION (DETERMINED BY CPU) OF X AND Y. CORRESPONDING PAIRS OF BITS ARE GROUPED BY CPU. GROUPING MAY BE BINARY, DECIMAL FOUR BIT, SIX BIT, OR EIGHT BIT. LENGTH IS CONTROLLED BY CPL. IF "CYF", THE CARRY FLIP-FLOP, IS ON, THEN SUM WILL BE ONE LARGER. IF SUM IS LARGER THAN THE SIZE SPECIFIED BY CP, THEN "CYL" WILL BE ON (=1). 00002520 00002525 00002530 00002535 00002540 00002550

DIFF 00002550

"X MINUS Y". Y SUBTRACTED FROM X, EITHER DECIMAL OR BINARY SUBTRACTION, ACCORDING TO CPU. CORRESPONDING PAIRS OF BITS ARE GROUPED BY CPU. LENGTH IS CONTROLLED BY CPL. IF THE DIFFERENCE IS NEGATIVE, THAT IS IF X IS LESS THAN Y, THEN XMY WILL BE IN TWOS COMPLEMENT FORM OR TENS COMPLEMENT FORM DEPENDING UPON THE MODE,EITHER BINARY OR DECIMAL. IF "CYF" IS ON (=1) THEN XMY WILL BE ONE LESS. 00002565 00002570 00002575 00002580 00002585 00002600

CONDITION REGISTERS

BICN FLCN INCN XYCN XYST

THERE ARE FIVE CONDITION REGISTERS, EACH CONTAINING FOUR BITS. THE BITS ARE IDENTIFIED FROM LEFT TO RIGHT AND ARE ASSIGNED THE POSITION NUMBERS 0-3. BICN DESCRIBES "BIT CONDITIONS" AND MAY INDICATE PRESENCE OR ABSENCE OF HI OR LO ORDER BITS OF X AND Y. XYCN DESCRIBES "XY CONDITIONS", THAT IS X>Y, X<Y, X=Y, AND OVERFLOW AT SUMMING X AND Y. FLCN DESCRIBES "FL CONDITIONS", THAT IS RELATIONS BETWEEN FL AND THE FIRST LOCATION IN SCRATCHPAD (SFL). INCN DESCRIBES INTERRUPT CONDITIONS. XYST DESCRIBES "XY STATUS", X=0, Y=0, XY=0.

REGISTER	BIT 0	BIT 1	BIT 2	BIT 3
BICN	CYL	CYD		LSUY
FLCN	FL≠0	FL<SFL	FL>SFL	FL=SFL
INCN	LOCKOUT	INTERRUPT	HI-PRI	BUF-HUNG
XYCN	X>Y	X<Y	X=Y	MSBX
XYST	X≠0	Y≠0	XY≠0	LSUX

NOTE: "MSBX"=MOST SIGNIFICANT BIT OF X, ON (=1) MEANS THE MOST SIGNIFICANT BIT (AS DEFINED BY CPL) OF X IS 1 FOR BINARY OR FOR DECIMAL.

"LSUX"=LEAST SIGNIFICANT UNIT OF X ≠ 0 (DEPENDING ON CPU, CPL)

"LSUY"=LEAST SIGNIFICANT UNIT OF Y ≠ 0 (DEPENDING ON CPU, CPL)

"CYL" =CARRY LEVEL, TRUE (SET TO 1) WHEN SUM OF X AND Y, LIMITED BY CPL, OVERFLOWS.

"CYD" =CARRY DIFFERENCE FLIP-FLOP, SET TO ONE WHEN X IS LESS THAN Y, THAT IS A UNIT CARRY WAS NEEDED FOR DIFFERENCE.

CLASSIFICATION OF M-OPERATORS

ACCESS CLASS	MODIFY CLASS	CONTROL CLASS	BRANCH CLASS
MOVE	SET	COUNT	GO TO
LOAD	AND	CARRY	SKIP WHEN
STORE	OR	BIAS	IF--GO TO
XCH	EOR		CALL
READ	CLEAR		EXIT
WRITE	ROTATE		JUMP TO
OVLY	SHIFT		
SWAP	INC		
LIT	DEC		
	NORMALIZE		
EXTRACT			

PSEUDOS
DEFINE
DUMP
SPACE
TRACE

```
                [UNIT]                                                          00002875
FORMAT:     BIAS BY [REGISTER-1] [AND REG-2] [AND REG-3] [TEST]                 00002885


DESCRIPTION:                                                                    00002895

     SETS CP TO A VALUE CALCULATED FROM THE OPERANDS.                           00002915

     IF  ONLY  REGISTER-1 IS USED IT MUST BE F OR S.  IF ONLY REGISTER-1        00002920
AND  REGISTER-2  ARE  USED  THEY MAY NOT BE S AND CP, I.E., ONE OF THEM         00002925
MUST BE F.                                                                      00002935

     REGISTER  REFERS  TO  F,  S,  OR  CP.   IDENTICAL  INSTRUCTIONS ARE       00002940
PRODUCED IF THE POSITIONS OF ANY TWO OR THREE REGISTERS ARE INTERCHANGED         00002945
WITHIN THE INSTRUCTION.                                                         00002955

     CPU  IS SET TO 1, 2, 3, OR 0 DEPENDING ON WHETHER FU IS 4, 6, 8, OR        00002960
SOME  OTHER  VALUE, 0-15.  THIS IS DONE FOR ALL TEN VARIATIONS OF "BIAS"        00002965
EXCEPT "BIAS BY S", WHICH SETS CPU FROM SU INSTEAD OF FROM FU.                  00002980

     "BIAS BY ...."  SETS  CPL  EQUAL TO THE VALUE OF THE SMALLER OF 24         00002985
AND THE SPECIFIED OPERANDS.  "BIAS BY UNIT" SETS CPL EQUAL TO FU.               00002995

     "BIAS BY S AND F AND CP" IS NOT ALLOWED.                                   00003005

     IF  "TEST"  IS  USED,  THE ABOVE ACTIONS ARE PERFORMED AND THE NEXT        00003010
MICRO-INSTRUCTION  IS  SKIPPED  IF  CPL  HAS NOT BEEN SET TO ZERO AS THE        00003015
RESULT  OF  THE  ABOVE ACTIONS.  TEST MAY BE USED WITH ALL VARIATIONS OF        00003020
"BIAS".                                                                         00003030


EXAMPLE:      "BIAS BY S" OR "BIAS BY F"                                        00003030

     THIS  WILL  SET  CPL  EQUAL  TO  THE  SMALLER  OF  24 AND SFL OR FL        00003045
RESPECTIVELY.   CPU  IS  SET  DEPENDING  ON  THE  VALUE  OF  SU  OR  FU        00003050
RESPECTIVELY.                                                                   00003052
```

BIAS

TIME: ONE CLOCK; TEST OPTION WITH A SKIP: TWO CLOCKS

00003052

CALL

FORMAT: CALL LABEL=1 00003070

DESCRIPTION: 00003080

DOES A STACK PUSH. 00003100

SAVES THE ADDRESS OF THE NEXT M=INSTRUCTION IN THE A=STACK (TAS), 00003105
THEN BRANCHES TO LABEL=1 IN THE M=PROGRAM. 00003115

THE "EXIT" INSTRUCTION CAUSES RETURN. 00003117

TIME: TWO CLOCKS 00003117

```
                [0]                                                          00003135
                [1]                                                          00003145
FORMAT:     CARRY [SUM]                                                      00003155
                [DIFFERENCE]                                                 00003165


DESCRIPTION:                                                                 00003175

     SETS THE CARRY FLIP-FLOP (CYF) TO EITHER 0 (ZERO) OR 1 (ONE).           00003195

     CARRY 0 OR CARRY 1 SETS CYF TO 0 OR 1 RESPECTIVELY.                     00003205

     CARRY SUM SETS CYF TO THE VALUE OF CYL.                                 00003215

     CARRY  DIFFERENCE SETS CYF TO THE VALUE OF CYD: 1 IF X IS LESS THAN     00003215
Y;  0  IF  X  IS  GREATER  THAN  Y.   IF  X=Y, CYF IS UNCHANGED BY CARRY     00003220
DIFFERENCE.                                                                  00003222

TIME: ONE CLOCK                                                              00003222
```

CLEAR

FORMAT: CLEAR [REGISTER-1] [REGISTER-2] [REGISTER-N]

DESCRIPTION:

SETS THE SPECIFIED REGISTERS TO ZERO.

ALL REGISTERS TO BE CLEARED IN ONE OPERATION, MUST BE ENTIRELY FROM GROUP "A" OR GROUP "B", BUT MUST NOT BE MIXED.

GROUP A	GROUP B
FL	ASTACK (STACK POINTER RESET)
FA	SO (CLEARS ALL 48 BITS)
FU	
L	BR LR-LR SET TO MAIN MEMORY SIZE
T	
X	
Y	

TIME: ONE CLOCK

COUNT

```
                [FA]        [UP]      [CPL]                                  00003345
FORMAT:     COUNT [FL]      [DOWN] BY [LITERAL-1]                            00003355
                [FA AND FL]                                                  00003365
```

DESCRIPTION: 00003375

INCREMENTS OR DECREMENTS THE DESIGNATED REGISTER BY THE AMOUNT OF THE LITERAL OR CPL. IF THE VALUE OF THE LITERAL IS ZERO, CPL IS USED. 00003390 00003405

WHEN "FA AND FL" IS USED, THE DIRECTION UP OR DOWN APPLIES TO FA ONLY, AND FL COUNTS DOWN. 00003410 00003420

IF FA IS COUNTED DOWN, IT MAY GO THROUGH ZERO (I.E., IF FA=0 AND IS COUNTED DOWN BY ONE, IT IS SET TO ALL ONES). IF FL IS COUNTED DOWN, IT WILL NOT BECOME LESS THAN ZERO. 00003420 00003425 00003435

LITERAL-1 IS 5 BITS, VALUE 0 TO 31. 00003445

EXAMPLE: INSTRUCTION= COUNT FA AND FL UP BY 10 00003445

	REGISTER FA	REGISTER FL
	00003455	00003460
INITIAL	09A7FB	00008
RESULT	09A805	00000

FA IS COUNTED UP BY DECIMAL 10, HEXADECIMAL A, WHILE FL IS COUNTED DOWN 8 TO ITS MINIMUM VALUE. 00003485 00003487

TIME: ONE CLOCK 00003487

EXIT

FORMAT: EXIT 00003505

DESCRIPTION: 00003515

ALLOWS RETURN TO THE CALLING PROGRAM BY CAUSING THE ASSEMBLER TO GENERATE A "MOVE TAS TO A" OPERATION. 00003530 00003540

THE TOP OF THE A-STACK (TAS) WILL BE MOVED TO A, WHICH IS USED BY THE HARDWARE LOGIC AS THE ADDRESS OF THE NEXT INSTRUCTION TO BE FETCHED. A STACK "POP" IS DONE AUTOMATICALLY BY THE HARDWARE, AFTER THE MOVE. 00003545 00003550 00003565

THEREFORE, "MOVE TAS TO A" MAY BE USED INSTEAD OF "EXIT" WITH THE SAME RESULT. 00003570 00003572

TIME: TWO CLOCKS 00003572

FORMAT: EXTRACT [INTEGER-1] BITS FROM T(INTEGER-2) TO [REGISTER-1] 00003590

DESCRIPTION: 00003600

ISOLATES THE SPECIFIED BITS FROM T AND MOVES THEM TO REGISTER-1. 00003620

ANY NUMBER OF BITS MAY BE MOVED FROM 1 THROUGH 24. THESE MAY BE 00003625
TAKEN FROM ANY BITS OF T. INTEGER-1, THE NUMBER OF BITS TO BE 00003630
EXTRACTED, MAY BE FROM 0-24. IF IT IS ZERO, NO OPERATION IS PERFORMED. 00003635
INTEGER-2 INDICATES THE LEFT-MOST BIT TO BE MOVED AND MAY BE FROM 0 TO 00003640
23. 00003650

THE SELECTED BITS ARE RIGHT JUSTIFIED IN THE RECEIVING FIELD, AND 00003655
LEFT ZEROES ARE INSERTED IF THE NUMBER OF BITS MOVED IS LESS THAN THE 00003660
LENGTH OF THE RECEIVING REGISTER. 00003670

SPACES BEFORE AND AFTER THE PARENTHESES ARE OPTIONAL, PARENTHESES 00003675
ARE REQUIRED. 00003685

REGISTER-1 MAY BE T, X, Y, OR L. T REMAINS UNCHANGED, UNLESS IT IS 00003690
SPECIFIED AS THE DESTINATION REGISTER. 00003700

EXAMPLE: INSTRUCTION- EXTRACT 4 BITS FROM T(20) TO L 00003700

	REGISTER T	REGISTER L	
	-------- -	-------- -	00003715
INITIAL	0138E4	1E39FC	00003720
RESULT	0138E4	000004	00003725

T REMAINS UNCHANGED, WHILE THE FOUR EXTRACTED BITS FROM T ARE 00003740
PLACED IN L. THE BITS ARE RIGHT JUSTIFIED AND LEADING ZEROES ADDED. 00003747

TIME: ONE CLOCK 00003747

GO TO

FORMAT: GO TO LABEL-1 00003765

DESCRIPTION: 00003775

CAUSES A BRANCH TO THE ABSOLUTE ADDRESS SPECIFIED BY LABEL-1. 00003790
LABEL-1 MUST BE AT AN ADDRESS EQUAL TO OR LESS THAN 8191 OR (HEXADECIMAL 00003792
1FFF). 00003794

TIME: TWO CLOCKS 00003794

JUMP TO

FORMAT: JUMP TO LABEL-1 00003810

DESCRIPTION: 00003820

CAUSES TRANSFER OF CONTROL TO THE DESIGNATED LOCATION. THE ADDRESS 00003835
OF LABEL-1 IS LIMITED TO A RELATIVE DISPLACEMENT OF PLUS OR MINUS 127. 00003842

TIME: TWO CLOCKS 00003842

```
                [REGISTER-1 (LITERAL-1)] [TRUE]                                  00003860
FORMAT:     IF [CONDITION-1]             [FALSE] GO TO [LABEL-1]                 00003870
```

DESCRIPTION: 00003880

TESTS THE BIT DESIGNATED BY LITERAL-1 WITHIN THE SPECIFIED REGISTER AND BRANCHES TO LABEL-1 IF THE CONDITION IS MET. 00003895 00003905

THE CONDITION-1 OPTION IMPLIES A TEST OF THE SPECIFIED CONDITION. CONDITIONS ARE LIMITED ONLY BY WHAT IS AVAILABLE IN THE CONDITION REGISTERS. EACH PART OF THE CONDITION MUST BE ENCLOSED BY BLANKS, IE. "IF FL > SFL GO TO +LABEL" 00003910 00003915 00003917 00003925

LITERAL-1 MUST BE INTEGER 0 TO 3 AND ENCLOSED IN PARENTHESES. ALL REGISTERS USED WITH THE "IF" OPERATOR CONTAIN FOUR BITS. THE BITS ARE REFERRED TO FROM LEFT TO RIGHT AND ASSIGNED POSITION NUMBERS OF 0 TO 3 (BIT 0 IS THEREFORE THE 8 OR MOST SIGNIFICANT BIT OF REGISTER-1). 00003930 00003935 00003940 00003950

LABEL-1 MUST NOT BE MORE THAN 15 INSTRUCTIONS AWAY, HIGHER OR LOWER. 00003965

TRUE MEANS IF THE DESIGNATED BIT IS ON (=1) THEN BRANCH. FALSE MEANS IF THE DESIGNATED BIT IS OFF (=0) THEN BRANCH. OMISSION OF TRUE AND FALSE MEANS TRUE. 00003970 00003975 00003985

REGISTER-1 MAY BE: 00003995

TA	LA	CA	FU	MC	BICN
TB	LB	CB	FLB	MD	FLCN
TC	LC	CC	FLC	ME	INCN
TD	LD	CD	FLD	MF	XYCN
TE	LE		FLE		XYST
TF	LF		FLF		

00003995 00004000 00004005 00004010 00004015 00004020

IF

EXAMPLE: INSTRUCTION= IF TA(2) TRUE GO TO LABL7 00004040

REGISTER TA	BRANCH	
B0101	NO	00004060
B1101	NO	00004065
B0111	YES	00004070
B0011	YES	00004075

IN CASES THREE AND FOUR THE BRANCH TO "LABL7" WOULD BE TAKEN SINCE 00004090
BIT POSITION TWO OF TA IS ON. 00004092

TIME: IF THE BRANCH IS TAKEN TWO CLOCKS, OTHERWISE ONE CLOCK 00004092

FORMAT: LIT [LITERAL-1] TO [REGISTER-1]

DESCRIPTION:

MOVES AN 8 OR 24 BIT LITERAL TO A REGISTER.

REGISTER-1 MUST BE A SELECT-2 REGISTER:

X	FA	FL
Y	FB	A
L	T	M
TAS	CP	
BR	LR	

IF LITERAL-1 IS NOT GREATER THAN DECIMAL 255 (BINARY B11111111 OR HEXADECIMAL HFF) THEN A ONE WORD M-STRING INSTRUCTION IS PRODUCED BY THE ASSEMBLER. OTHERWISE LITERAL-1 MAY BE AS LARGE AS DECIMAL 16777215 (BINARY B111111111111111111111111 OR HEXADECIMAL HFFFFFF).AND THE ASSEMBLER PRODUCES A TWO WORD M-STRING INSTRUCTION WITH THE LOW ORDER 16 BITS OF THE LITERAL IN THE SECOND WORD.

LEFT TRUNCATION OCCURS IF THE DESTINATION REGISTER IS SHORTER THAN 8 OR 24 BITS RESPECTIVELY.

TIME: 8 BIT LITERAL ONE CLOCK, 24 BIT LITERAL THREE CLOCKS

FORMAT: LOAD F FROM [DOUBLE-PAD-WORD-1] 00004225

DESCRIPTION: 00004235

MOVES A PAIR OF SCRATCHPAD WORDS (48 BITS TOTAL) TO F. THE 00004250
SCRATCHPAD IS UNCHANGED. 00004260

DOUBLE-PAD-WORDS: 00004270

S0	S4	S8	S12
S1	S5	S9	S13
S2	S6	S10	S14
S3	S7	S11	S15

00004270
00004275
00004280
00004285

TIME: ONE CLOCK 00004295

FORMAT: MOVE [REGISTER-1] TO [SCRATCHPAD-WORD-1] 00004435
[REGISTER-1] 00004445

FORMAT: MOVE [SCRATCHPAD-WORD-1] TO [REGISTER-1] 00004455

DESCRIPTION: 00004465

THE SOURCE FIELD IS UNCHANGED. 00004485

MOVES TO UNEQUAL LENGTH WILL JUSTIFY RIGHT AND FILL WITH LEADING 00004490
ZEROES OR TRUNCATE FROM THE LEFT. 00004500

ONLY ONE OF THE FIELDS MAY BE IN SCRATCHPAD AND THE OTHER MUST BE A 00004505
REGISTER NAME. A RESULT REGISTER, OR A CONDITION REGISTER, MAY NOT BE 00004510
THE RECEIVING FIELD OF A MOVE. IF M IS USED AS THE SOURCE REGISTER THE 00004512
DESTINATION REGISTER IS SET TO ZERO. 00004520

"MOVE TAS TO...." CAUSES AUTOMATICALLY A STACK "POP" AFTER THE 00004525
MOVE. "MOVE....TO TAS" CAUSES AUTOMATICALLY A STACK "PUSH" BEFORE THE 00004530
MOVE. 00004540

EXAMPLE: MOVE X TO S7B 00004540

	REGISTER X	SCRATCHPAD-WORD S7B	
	00004550		
	00004555		
INITIAL	39FED0	333E05	00004560
RESULT	39FED0	39FED0	00004565

THE CONTENTS OF REGISTER X HAVE BEEN MOVED TO THE SCRATCHPAD-WORD 00004580
S7B, X REMAINS UNCHANGED. 00004582

TIME: ONE CLOCK 00004582

FORMAT: NORMALIZE 00004600

DESCRIPTION: 00004610

SHIFTS XY (X CONCATENATE Y) LEFT WHILE COUNTING FL DOWN, ANY NUMBER 00004625
OF BITS, UNTIL FL=0, OR UNTIL THE MOST SIGNIFICANT BIT OF X (DETERMINED 00004630
BY CPL)=1. 00004632

TIME: ONE CLOCK PER BIT SHIFTED, MINIMUM ONE CLOCK 00004632

OVERLAY

FORMAT: OVERLAY 00004650

DESCRIPTION: 00004660

OVERLAY M-STRING MEMORY FROM S-MEMORY. DETAILS TO COME LATER. 00004680

```
                                        [T]                                    00004690
                                        [X] [INC] [FA]                         00004700
FORMAT:    READ [LITERAL-1 BITS] [REVERSE] TO [Y] [DEC] [FL]                   00004710
                                        [L]       [FA AND FL]                  00004720
```

DESCRIPTION: 00004730

INITIATES A MAIN MEMORY READ CYCLE TO THE SPECIFIED REGISTER (T,X, 00004745
Y,L). FA MUST HAVE BEEN SET TO THE APPROPRIATE S-MEMORY ADDRESS 00004750
PREVIOUSLY. 00004760

LITERAL-1, THE NUMBER OF BITS TO READ AND THE NUMBER TO INC OR DEC, 00004765
IS OPTIONAL. LITERAL-1 MUST BE AN INTEGER 0 TO 24. IF LITERAL-1 IS 00004770
OMITTED OR IF IT EQUALS ZERO, THEN CPL INDICATES THE NUMBER OF BITS. 00004775
READ "CPL BITS" IS NOT PERMITTED. 00004785

IF THE NUMBER OF BITS TO READ IS ZERO, THE DESTINATION REGISTER 00004790
WILL BE SET TO ALL ZEROES, OTHERWISE THE SELECTED BITS ARE RIGHT 00004795
JUSTIFIED IN THE DESTINATION REGISTER, AND LEFT ZEROES ARE INSERTED IF 00004800
THE NUMBER OF BITS READ IS LESS THAN THE LENGTH OF THE DESTINATION 00004805
REGISTER. 00004815

REVERSE (OPTIONAL), DETERMINES THE BITS TO BE READ FROM S-MEMORY. 00004820
REVERSE IMPLIES THE POINTER IS SET AT THE LAST BIT TO BE READ. IF 00004825
REVERSE IS OMITTED THE POINTER IS SET AT THE FIRST BIT TO BE READ. READ 00004830
OCCURS FROM LEFT TO RIGHT. 00004840

INCREMENTING OR DECREMENTING OCCURS FOLLOWING THE READ AND IS 00004845
OPTIONAL. FOR DETAILS SEE THE "COUNT" VERB. 00004847

TIME: FIVE CLOCKS 00004847

ROTATE OR SHIFT T LEFT

```
          [SHIFT]    RIGHT   [LITERAL-1 BITS]                                  00004865
FORMAT:   [ROTATE] T LEFT BY [CPL]           [TO REGISTER-1]                   00004875


DESCRIPTION:                                                                   00004885

     ROTATES OR SHIFTS T LEFT, AND PLACES THE RESULT IN EITHER T OR            00004900
DESTINATION REGISTER-1.  ZERO FILL ON THE RIGHT OCCURS WITH SHIFT.              00004915

     LITERAL-1 HAS A VALUE OF 0 THRU 23.  WHEN LITERAL-1=0 OR WHEN "CPL"       00004920
IS USED, A SHIFT OR ROTATE BY THE VALUE OF CPL WILL OCCUR.                     00004935

     IF THE "TO REGISTER-1" OPTION IS USED, THE ROTATED OR SHIFTED             00004940
RESULT WILL BE PLACED IN REGISTER-1, AND T IS UNCHANGED.  OTHERWISE THE        00004945
RESULT IS PLACED IN T.                                                         00004947

     ROTATE T RIGHT IS CONVERTED BY THE ASSEMBLER TO THE PROPER LEFT           00004948
ROTATE TO ACCOMPLISH THE SAME THING,  SHIFT RIGHT IS NOT ALLOWED               00004950

TIME: ONE CLOCK                                                                00004950
```

ROTATE OR SHIFT

```
          [SHIFT]  [X]  [LEFT]     [UNIT]                              00004965
FORMAT:   [ROTATE] [Y]  [RIGHT] BY [LITERAL-1]                         00004975
                   [XY]                                                00004985
```

DESCRIPTION:

ROTATES OR SHIFTS (X, Y, OR XY) A SPECIFIED NUMBER OF BITS TO THE RIGHT OR LEFT. ZERO FILL OCCURS WITH SHIFT.

WHEN "UNIT" IS USED, THE OPERAND IS ROTATED OR SHIFTED BY 1, 4, 6, OR 8 BITS ACCORDING TO THE VALUE OF CPU (TYPE OF UNITS CONTAINED IN X AND Y MAY BE DETERMINED BY CPU, EITHER BINARY, 4 BIT, 6 BIT OR 8 BIT DECIMAL). FOR XY (X CONCATENATE Y) LITERAL-1 MAY BE 0-47. FOR X AND Y LITERAL-1 MAY BE 0-23.

TIME: ONE CLOCK

```
                    [ALL] [CLEAR]                                          00005060
                [REGISTER-1] [ANY]        [LITERAL-1]                      00005070
                    [EQL]                                                  00005080
FORMAT:    SKIP WHEN                                [FALSE]                00005090
                [CONDITION-1]                                              00005100
```

DESCRIPTION: 00005110

SKIPS ONE M-INSTRUCTION IF THE DESIGNATED CONDITION IS SATISFIED. 00005130

LITERAL-1 IS A 4 BIT MASK. IT MAY BE DECIMAL, BINARY OR HEXADECIMAL. 00005135 00005145

"ALL" MEANS THAT ALL BITS IN REGISTER-1 CORRESPONDING TO ONE BITS IN MASK MUST BE ONE. "ANY" IS TRUE IF AT LEAST ONE BIT IN REGISTER-1 CORRESPONDING TO A ONE BIT IN MASK IS ONE. "EQL" MEANS THAT ALL REGISTER-1 BITS MUST EQUAL CORRESPONDING BITS IN MASK, OR REGISTER-1 MUST EQUAL THE MASK. 00005150 00005155 00005160 00005165 00005175

"CLEAR", OPTIONAL AND USED ONLY WITH "ALL", CAUSES THE MASKED BITS OF THE REGISTER TO BE SET TO ZEROES AFTER TESTING THE "ALL" CONDITION. ALL OF THE BITS ARE NOT CLEARED; ONLY BITS TESTED ARE CLEARED. IF "ALL CLEAR" IS USED, THE CLEAR ALWAYS OCCURS WHETHER THE SKIP IS TAKEN OR NOT. IF "ALL" IS USED WITH A MASK OF 0000 THE RESULT IS ALWAYS TRUE. IF "ANY" IS USED WITH A MASK OF 0000 THE RESULT IS ALWAYS FALSE. 00005180 00005185 00005190 00005195 00005205 00005215

FALSE IS OPTIONAL AND CAUSES A SKIP WHEN THE WHOLE CONDITION IS FALSE. 00005220 00005230

SKIP

REGISTER-1 MAY BE:

FU	TA	LA	CA	MC	BICN
FLB	TB	LB	CB	MD	FLCN
FLC	TC	LC	CC	ME	INCN
FLD	TD	LD	CD	MF	XYCN
FLE	TE	LE			XYST
FLF	TF	LF			

TIME: TWO CLOCKS ON THE SKIP; ONE CLOCK OTHERWISE

STORE

FORMAT: STORE F INTO DOUBLE PAD-WORD-1 00005295

DESCRIPTION: 00005305

MOVES F (48 BITS) INTO A PAIR OF SCRATCHPAD WORDS. F IS UNCHANGED. 00005330

DOUBLEPAD WORDS: 00005340

S0	S4	S8	S12	00005340
S1	S5	S9	S13	00005345
S2	S6	S10	S14	00005350
S3	S7	S11	S15	00005355

TIME: ONE CLOCK 00005357

FORMAT: SWAP [LITERAL-1] BITS [REVERSE] WITH [REGISTER-1] 00005375

DESCRIPTION: 00005385

SWAPS THE SPECIFIED NUMBER OF BITS BETWEEN S-MEMORY AND REGISTER-1. 00005400
REGISTER-1 MAY BE T, X, Y, L. 00005410

FA MUST HAVE BEEN SET TO THE S-MEMORY ADDRESS PREVIOUSLY. 00005420

LITERAL-1 MUST BE AN INTEGER 0 THROUGH 24. IT DETERMINES THE 00005425
NUMBER OF BITS TO SWAP BETWEEN S-MEMORY AND REGISTER-1. IF THE VALUE OF 00005430
LITERAL-1 IS ZERO, CPL IS USED. 00005440

THE REVERSE OPTION IS USED TO ESTABLISH THE BEGINNING BIT IN S- 00005445
MEMORY. IF LESS THAN 24 BITS ARE SWAPED, THE LEADING BITS OF THE 00005450
REGISTER WILL BE ZERO. 00005452

TIME: SEVEN CLOCKS 00005452

```
                                        [T]                                  00005470
                                        [X] [INC] [FA]                       00005480
FORMAT:    WRITE [LITERAL-1 BITS] [REVERSE] FROM [Y] [DEC] [FL]              00005490
                                        [L]       [FA AND FL]                00005500
```

DESCRIPTION: 00005510

INITIATES A MAIN MEMORY WRITE CYCLE FROM THE SPECIFIED REGISTER (T, X, Y, L). FA MUST HAVE BEEN SET TO THE APPROPRIATE S-MEMORY ADDRESS PREVIOUSLY. 00005525 00005530 00005540

LITERAL-1, THE NUMBER OF BITS TO WRITE AND THE NUMBER TO INC OR DEC, IS OPTIONAL. LITERAL-1 MUST BE INTEGER, 0 THROUGH 24. IF LITERAL-1 IS OMITTED OR IF IT EQUALS ZERO, THEN CPL INDICATES THE NUMBER OF BITS. 00005545 00005550 00005555

WRITE "CPL BITS" IS NOT PERMITTED. 00005565

THE WRITE BITS ARE REMOVED FROM T, X, Y, OR L FROM RIGHT TO LEFT. THE REVERSE OPTION DETERMINES THE LOCATION IN WHICH THE BITS ARE PLACED IN S-MEMORY WITH RESPECT TO FA. 00005570 00005575 00005585

INCREMENTING OR DECREMENTING OCCURS FOLLOWING THE READ AND IS OPTIONAL. FOR DETAILS SEE THE "COUNT" VERB. 00005590 00005592

TIME: SEVEN CLOCKS 00005592

XCH

FORMAT: XCH [DOUBLE-WORD-1] F [DOUBLE-WORD-2] 00005610

DESCRIPTION: 00005620

MOVES F TO DOUBLE-SCRATCHPAD-WORD-2; THEN DOUBLE-SCRATCHPAD-WORD-1 00005635
IS MOVED TO F. THE TWO WORDS MAY BE THE SAME. 00005645

THE DOUBLE-SCRATCHPAD-WORDS: 00005655

	S0	S4	S8	S12	00005655
	S1	S5	S9	S13	00005660
	S2	S6	S10	S14	00005665
	S3	S7	S11	S15	00005670

TIME: ONE CLOCK 00005672

LOGICAL M-OPERATORS

```
          [SET]
          [AND]                [BY]
FORMAT:   [OR]  [REGISTER-1] [WITH] [LITERAL-1] [TEST]
          [EOR]                [TO]
          [INC]
          [DEC]
```

DESCRIPTION:

PERFORMS THE SPECIFIED OPERATION REPLACING REGISTER-1 WITH THE RESULT.

"SET" MEANS SET EQUAL TO LITERAL-1. "INC" AND "DEC" MEANS ADD OR SUBTRACT LITERAL-1 TO OR FROM REGISTER-1. "AND", "OR", AND "EOR" MEAN TO FIND THE AND, OR, OR EXCLUSIVE OR, TREATING EACH PAIR OF CORRESPONDING BITS IN THE MASK (LITERAL-1) AND THE REGISTER INDEPENDENTLY.

THE TRUTH TABLES:

AND	OR	EOR
0 0 = 0	0 0 = 0	0 0 = 0
0 1 = 0	0 1 = 1	0 1 = 1
1 0 = 0	1 0 = 1	1 0 = 1
1 1 = 1	1 1 = 1	1 1 = 0

REGISTER-1 MAY BE:

LA	TA	CA	FU	MC
LB	TB	CB	FLB	MD
LC	TC	CC	FLC	ME
LD	TD	CD	FLD	MF
LE	TE		FLE	
LF	TF		FLF	

LITERAL-1 MUST BE INTEGER, 0 THROUGH 15. 00005910

IF THE "TEST" OPTION IS USED, THE ABOVE ACTIONS ARE PERFORMED AND 00005915
THE NEXT MICRO-INSTRUCTION IS EXECUTED UNLESS THERE HAS BEEN AN 00005920
UNDERFLOW OR OVERFLOW, INWHICH CASE THE NEXT M INSTRUCTION IS SKIPPED. 00005924
"TEST" MAY BE USED WITH THE INC AND DEC OPTIONS ONLY. 00005926

TIME: ONE CLOCK; WITH THE TEST OPTIONS AND A SKIP: TWO CLOCKS 00005926

PSEUDO INSTRUCTIONS

DEFINE DUMP SPACE TRACE

DEFINE - USED TO ASSIGN VARIABLE NAMES TO SCRATCHPAD AREAS.
  FORMAT: DEFINE [VARIABLE NAME] = [SINGLE OR DOUBLE PADWORD]
DUMP - USED TO DUMP S OR M MEMORY.
  [S]
  FORMAT: DUMP [M] MEMORY
SPACE - USED TO SPACE ASSEMBLER LISTING TO TOP OF NEXT PAGE
  FORMAT: SPACE
TRACE - USED TO CAUSE SIMULATOR TRACE TO SWITCH ON-OFF.
  FORMAT: TRACE [OFF]
  NOTE: TRACE CAUSES TRACE ON; TRACE OFF CAUSES TRACE OFF.
NOTE: ALL PSEUDO INSTRUCTIONS MUST BEGIN IN COLUMN 6 OR ABOVE.

THIS IS THE LAST PAGE OF THE MANUAL