LESSON 2

MAGNETISM

ELECTRICITY AND MAGNETISM:

In treating such phenomena as the flow of electricity, a general law (Ohm's Law) is used, in which the magnitude of the effect is given as the ratio of a driving force divided by an opposition factor dependent upon the properties of the medium in which the action takes place.

$$\text{Current} = \frac{\text{Electromotive Force}}{\text{Resistance}}$$

In treating magnetism, it is convenient for purposes of calculation, to regard the region in which a magnetized state exists as the seat of a magnetic flow. The magnetic lines of induction are the closed circuits along which the flow takes place. Materials are then classified as good or bad magnetic conductors according to the ease with which they are magnetized.

Magnetic Flux is analogous to flow of current in electricity. The unit of magnetic flux is the maxwell - one magnetic line of induction.

Magnetic Induction is defined as the total flux per unit area and is, therefore, the flux density the unit of which is the Gauss.

$$\text{Gausses} = \frac{\text{Maxwells}}{\text{Sq. Centimeters}}$$

Magnetomotive Force may be regarded as the cause of magnetic flux. The unit of magnetomotive force is the Gilbert.

Reluctance is the resistance a body offers to being magnetized and depends upon the constants of the circuit similar to resistance in the electrical circuit. It is directly proportional to the length and inversely proportional to the area and the permeability of the medium. Unit of reluctance is the Oersted.

THUS $\phi = \frac{4\ NI}{\frac{L}{UA}}$

WHERE ϕ = Total Flux
N = Total No. of turns
L = Mean length of magnetic lines
U = Permeability
A = Area of cross section

The equation of the "Law of the Magnetic Circuit":

Magnetic Flux = $\frac{\text{Magnetomotive Force}}{\text{Reluctance}}$

Another similarity between magnetics and electrical circuits is seen in the stated "Law of the Magnetic Circuit":

If, in a magnetic circuit, the flux is one maxwell when the magnetomotive force is one Gilbert, the reluctance is one Oersted.

Magnetizing Curve

If a piece of unmagnetized iron is placed in a field which may be varied at will, it is found, starting at H = 0 and gradually increasing it, that the induction B increases slowly at first, remaining nearly proportional to the field, then increases rapidly after a certain interval of H, after which a further increase produces only relatively small changes in B. This curve showing values of induction for diffrent magnetizing fields is called the "Magnetizing Curve" and is represented by OB in figure one.

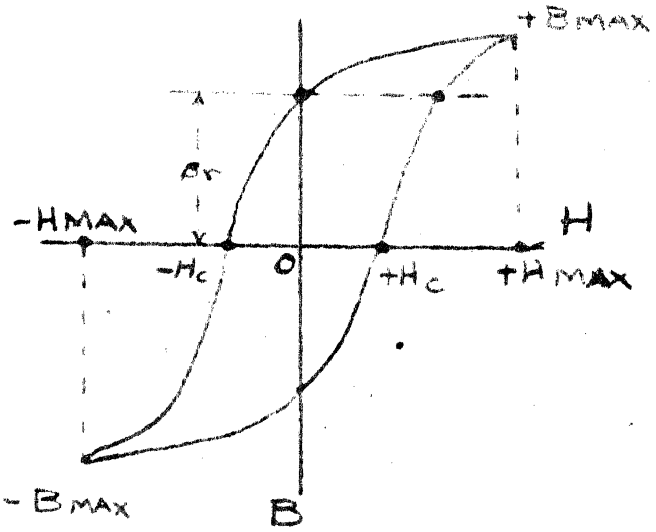


FIGURE 1

The three parts of the curve are accounted for by assuming that, in the unmagnetized condition, the magnetic axis of the molecular magnets are distributed entirely at random. Under the action of a weak magnetic field, these molecular magnets are all sprung to a slight extent from their initial positions, giving a resultant component in the direction of the applied field, amount of differmation being proportional to the field. With increase in H, some of these magnetic circuits are broken up and new alignments are formed. As each local circuit breaks, becoming part of a chain, neighboring groups become unstable, break and form other chains, thus giving a sort of spontaneous magnetization. As the condition is approached where all local groups have broken and molecules placed in complete alignment, saturation is set to have been reached, and further increases in field H produce only small changes in induction.

Hysteresis Loop

If after the induction has been carried to the point marked +B max. on figure one, the magnetizing field is gradually decreased, the induction does not attract the magnetization curve, but takes on values, for a given field, greater than thoes for the magnetization curve; and when H has been reduced to zero, an amount of induction indicated by Br still persists. If a reverse field is applied, the induction rapidly falls, and when a certain value, - Hc, has been reached, the resultant induction is zero. A further negative increase in field to -H max. gives a reverse value of induction -B max. equal in magnitude to +B max. With an increase in H to its original positive value "+H max.", B assumes values shown by lower curve of figure one, symmetrical with respect to the origin of the upper curve.

This tendency of any material to persist in a given magnetic state is known as "Hysteresis", and the corresponding curve as the Hysteresis Curve. Br is called the retentivity, and Hc, the coercive field. The area of the hysteresis loop is a measure of the energy consumed by molecular friction in each cubic centimeter of material carried once through a magnetic cycle. This loss is due to the fact that, as the current in the magnetizing coil is changed, producing changes of flux in the ring, a counter EMF is induced, against which the magnetizing current must flow. The electrical energy which thus disappears is the energy consumed by hysteresis and reappears in the form of heat within the ring.

The area of the loop divided by 4 gives the energy lost per cycle per cubic centimeter of material. The shape of the loop varies with the quality of the iron.

	Retentivity	Coercive Force
Hard steels	High	High
Soft steels	High	Low
Swedish iron	Low	Low

For a given material, the area of this loop depends on the limits of induction.

LESSON 3

BIMAG CHARACTERISTICS

INTRODUCTION: The principle circuit component of INTERLOCK Model IV is the Bistable Ferromagnetic Core herein called BIMAG. The principal advantages of the Bimag component are its rectangular hysterisis loop, physical size and low power consumption.

PHYSICAL PROPERTIES: Bimag cores are normally toroidal in shape, with a diameter between 90 mils and one-half inch, and may be in either of two forms:

1. Metallic tape cores, which consist of strips of metallic tape wrapped around a bobbin which is usually made of ceramic.
2. Ferrite cores, made from a fine powder of magnetic materials that are pressed into core shapes.

MAGNETIC PROPERTIES: -

A. Magnetic Circuits - Hysteresis Loop

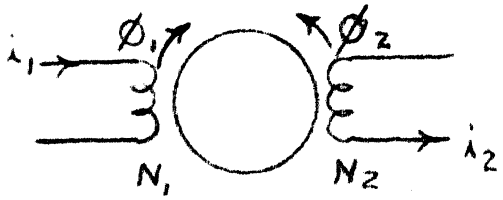


Figure 1

Where: i - Current
N - No. Turns
ϕ - Flux Generated

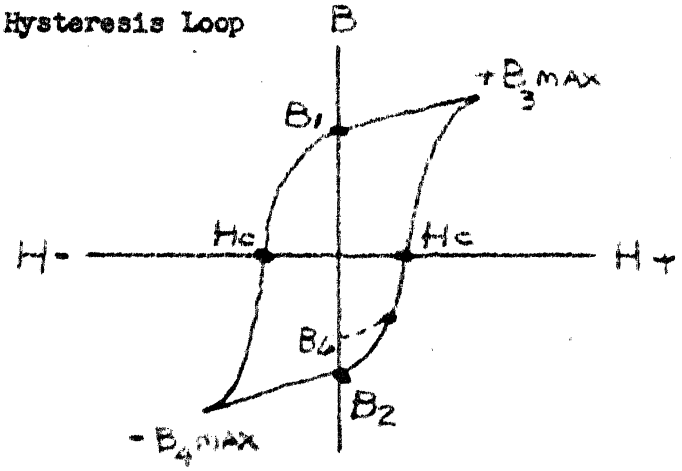


Figure 2

Where: H - Amp. Turns (NI)
B - Flux/Unit Area
B/ - ONE State
B— - ZERO State

When a current I_1 flows through winding N_1, a flux ϕ is generated. A plot of I_1 vs. ϕ_1 will result in the hysteresis loop shown in

Figure 2. A more general graph is obtained if the axis of the hysteresis loop is changed from ϕ to B, ($B = \phi/A$) and I to H, ($H = NI$), generally referred to as the B-H curve, where B is flux density and H is the magnetizing force.

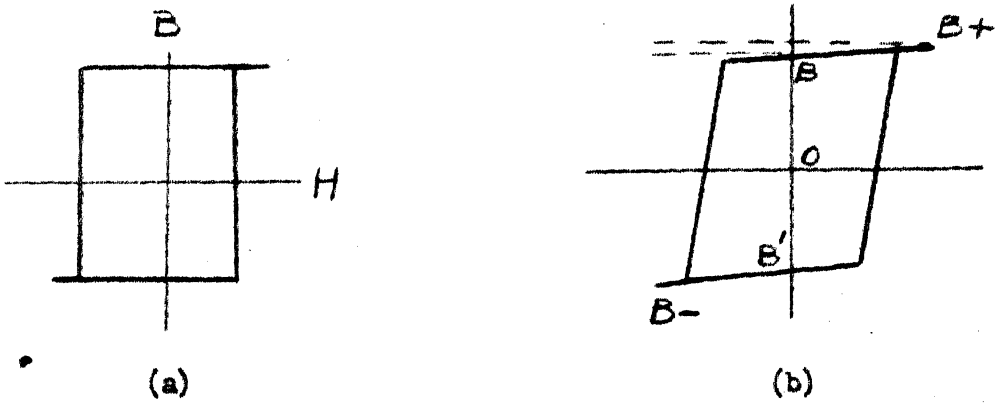
The points B_1 and B_2 are the points of residual magnetism. If the current was increased from ZERO to a value that caused saturation of the core, and then was reduced to zero, the state of flux in the core would be at one of these points. Assume the core is in the B_2 state. Positive current will cause the state of the core to change from B_2 to B_3, provided the current saturates the core with flux. If then the current is reduced to zero, the state of the core will be at point B_1. Passing from point B_2 to B_3, to B_1 is called COMPLETE SWITCHING of the magnetic core. By definition, the state of the core, when at point B_1, is called the ONE state; when at point B_2, it is called the ZERO state.

Reference is again made to Figure 2. Assume the core is in the ZERO state (at point B_2). If I is varied in the positive direction from zero to some small value and then returned to zero, the core will return to the ZERO state. But there is some point at which after increasing I in positive direction and then reduced to zero, the core will not return to the ZERO state, but will return to a point between B_1 and B_2, indicated by B_6. The point on the B-H curve at which the core will not return to this ZERO state for some value of I, is termed the THRESHOLD POINT. The passing from point B_2 to B_6 is called PARTIAL SWITCHING of the magnetic core. Since the hysteresis loop is symmetrical, the same statements are true of negative values of I (with the core in the ONE state).

If the core is at point B_2 (the ZERO state) and a negative magnetizing force is applied, the core will be driven into saturation to point B_4 and will return to B_2 when the magnetizing force is returned to ZERO. Flux is generated in going from B_2 to B_4. This is termed core NOISE.

B. Magnetic Core as a Bistable Device.

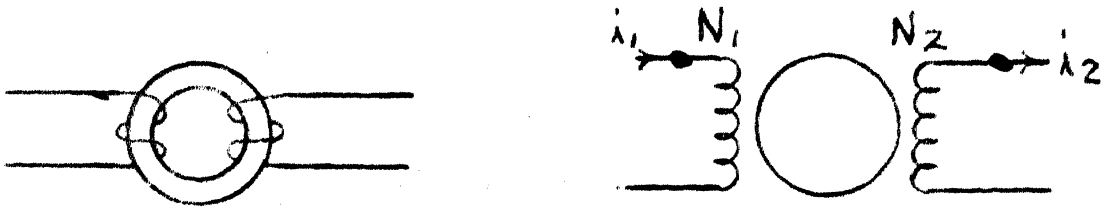
The hysteresis loop, most desirable for a core to operate as a good bistable device, is the rectangular loop shown in Figure 3a. The hysteresis loop for a Bimag core approaches this rectangular shape as shown in Figure 3b. The Square Hysteresis Loop gives maximum voltage storage. Therefore a low OB $\not-$ / OB max ratio most desirable. The Ideal ratio being 1:1.



(a) (b)

FIGURE 3

C. Magnetic Core Schematic Symbols.



(a) (b)

FIGURE 4

The core and windings of Figure 4a may be represented by the schematic drawing of Figure 4b. The dot notations are used to indicate LIKE POLARITY of the windings. The dot notation has the following properties:

(1) A conventional current entering the NON-DOT terminal will switch the core from the ZERO state to the ONE state.

(2) A conventional current entering the DOT terminal will switch the core from the ONE state to the ZERO state.

(3) Switching the core from the ZERO state to the ONE state generates a flux that will induce voltages in all other windings of the same core which will cause a current to flow into the dot terminal of these windings.

ie: CURRENT OUT OF THE DOT IS CURRENT INTO THE DOT.

(4) Switching the core from the ONE state to the ZERO state generates a flux that will induce voltages in other windings of the same core which will cause a current to flow out of the dot terminal of these windings.

ie: CURRENT INTO THE DOT IS CURRENT OUT OF THE DOT.

LESSON 4

TRANSFER LOOPS

SINGLE DIODE TRANSFER LOOP

The purpose of this circuit is to transfer the ONE state from core T-1 to core T-2. Figure 5 shows the schematic diagram of a single diode loop circuit.

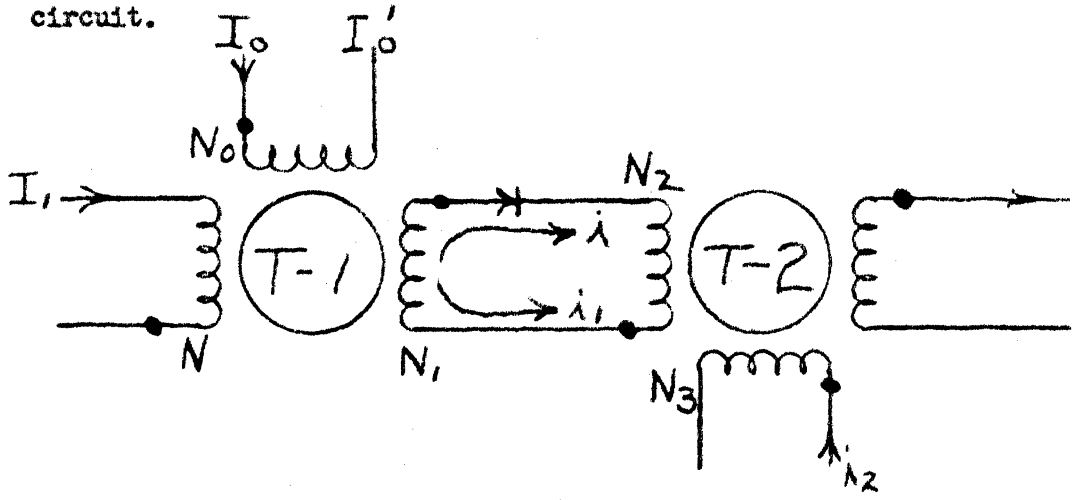


FIGURE 1 - SINGLE DIODE TRANSFER LOOP

LOGIC - Core T-1 is in the ONE state. (Figure 1)

Core T-2 is in the ZERO state.

LOGICAL OPERATION

Current I_o enters the dot terminal of winding No. This current switches core T-1 from the ONE state to the ZERO state and causes a transfer current i in N_1, which is a forward current for the diode. Current i enters the non-dot terminal of winding N_2 and switches core T-2 from the ZERO state to the ONE state. Thus the ONE that was in core T-1 is transferred to core T-2. This is called Unconditional Transfer of information, since the information in core T-1 is always transferred to core T-2 when the circuit is operated as explained.

The purpose of the diode is to prevent the loss of information stored in T-2 by a current I_o' flowing in winding N_o that is opposite to current I_o.

Other than this use the diode only uses up voltage required to drive N_2.

LOGIC - Core T-1 is in the ZERO state. (Figure 1)

Core T-2 is in the ONE state.

Current I_1 flows into the non-dot terminal of N.

LOGICAL OPERATION

Current I_1 would switch T-1 to the ONE state, producing a current i_1 that flows into the dot winding of N_2, switching T-2 to the ZERO state, except for the high back resistance of the crystal diode. This resistance limits current i_1 to a value well below the threshold current for winding N_2, thus keeping T-2 in the ONE state.

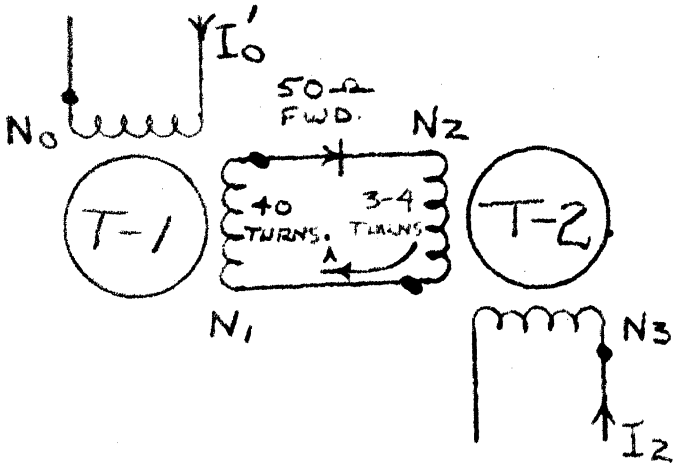


FIGURE 2 - SINGLE DIODE TRANSFER LOOP

LOGIC - Core T-1 is in the ZERO state. (Figure 2)

Core T-2 is in the ONE state.

Current i_2 flows in winding N_3.

LOGICAL OPERATION

Current i_2 switches core T-2 to the ZERO state. In sensing the core in the manner a transfer current is produced in N_2 in the same direction as i. This current i being in the correct direction so as to cause the diode to conduct would

seem to be the proper current to switch core T-1 to the ONE state and thus transfer the ONE from T-2 to T-1. This however, would be transferring in reverse as well as forward and this is not the desire of this type of circuit. Therefore, the output winding of a core, N_1 in this case, is wound with many turns (approximately 40 turns) and the input winding of a core, N_1 in this case, is wound with few turns (approximately 4 turns).

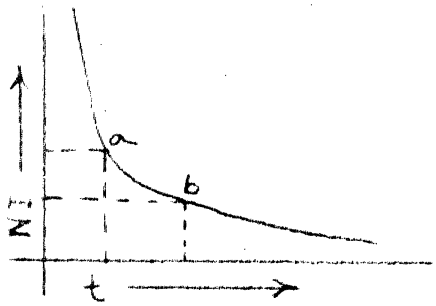
This accomplishes two things, the main of which is to prohibit the before mentioned condition, as follows:

(1) Since the turns ratio of N_2/N_1 is small, the impedance ratio of Z_1/Z_2 is large and the current induced in winding N_2 due to current I_2 is small, thus the current flow (i) in N_1 will not completely switch T-1. T-1 will be partially switched from the ZERO state, and this partial switching is referred to as NOISE (Refer to Lesson 1 - Magnetic Properties of Bimags).

(2) Since few turns are used, more switching current is required to provide the proper NI (ampere turns) to switch T-2. This is allowed for in design.

NOTE: SWITCHING

T-2 must be completely switched before T-1 has completed switching. However, after T-2 has been switched the current requirement presented to T-1 by T-2 no longer exists. The load on T-1 is thus removed and only the very low DC resistance of N_2 is seen. This will draw more than T-2's share of driver current thus taking switching current away from T-1. Due to the NI to Switching-Time relationship (FIGURE 3) TAILOUT will result. (Less Ampere Turns - More Switching Time required). The circuit is thus designed to allow for the extra tie to complete the switching of T-1 .



a - normal load
b - tailout condition

FIGURE 3 - SWITCHING

BIASED DIODE TRANSFER LOOP

The purpose of this circuit is to transfer information from core T-1 to core T-2 only when current i_2 flows. This is called Conditional Transfer, of information. FIGURE 4 shows the schematic diagram of a Biased Diode Transfer Loop, sometimes called a Split Winding Transfer Loop.

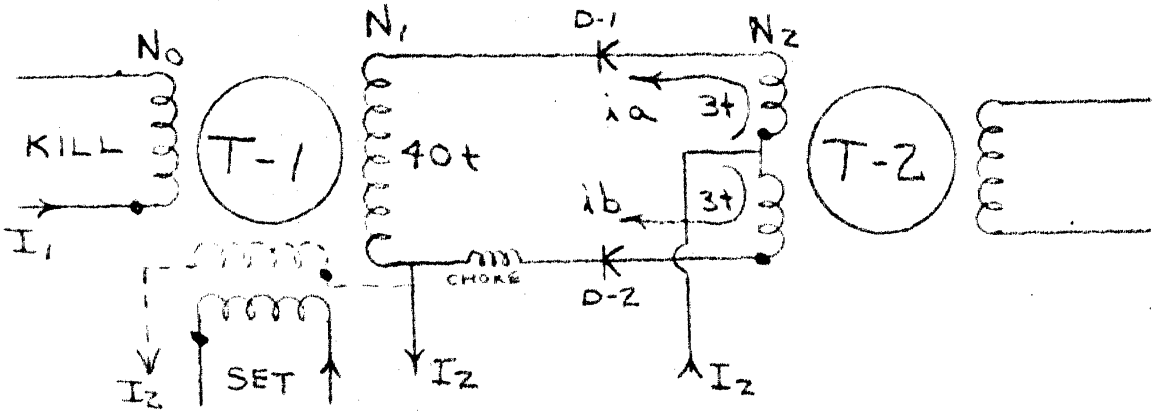


FIGURE 4 - BIASED DIODE OR SPLIT WINDING TRANSFER LOOP

LOGIC - Core T-1 is in the ZERO state. (FIGURE 4)

Core T-2 is in the ZERO state.

Current I_2 flows into N_2 center-tap.

LOGICAL OPERATION

Current I_2 divides into i_a and i_b. The impedance path to i_a and to i_b is equal, thus the currents are equal. (The impedance of N_1 in the path of i_a is balanced by a choke place in the path of i_b equal to N_1.) Note that current i_a flowing into the dot winding of N_1 will see a low impedance since core T-1 is in the ZERO state. Thus core T-2 will remain in the ZERO state since the flux generated by equal and opposite currents, will cancel in core T-2.

LOGIC - Core T-1 is in the ONE state. (FIGURE 4)

Core T-2 is in the ZERO state.

Current I_2 flows into N_2 center-tap.

LOGICAL OPERATION

Current i_a flowing into the dot terminal winding of N_1 will now see a high impedance since it will switch the state of the core T-1. Due to this higher impedance in the leg i_a is flowing in i_a will be smaller than i_b. Current i_b will then override the effect of i_a and switch core T-2 to the ONE state while i_a is switching T-1 to the ZERO state. Thus the transfer of information from core T-1 to core T-2.

If a current i_1 should flow into the dot terminal of winding N_0 as shown in FIGURE 4 a current would be induced in winding N_1 which would flow out of the dot, but the back resistance of diode 1 would limit the current flow to well below the threshold value. Note that core T-1 will be switched to the ZERO state by i_1 but core T-2 will not be switched, thus no transfer of information and a conditional transfer circuit is accomplished.

The advantage of the Biased Diode Transfer Loop is the ability to be CLEARED without Bit Transfer. It is used however, at times due to noise problems where a Single Diode Loop could be used but would give trouble due to erroneous read-outs by the noise pulses.

LESSON 5

LOGICAL SYMBOLS

BASIC RULES -- The representation of BIMAG circuits is based on the following rules:

1) In a logical diagram all cores and drivers are represented.

2) A magnetic core is represented by a circle.

3) The winding or windings around a magnetic core belonging to the same transfer loop are represented by a single straight line limited to the circle.

4) An input winding is indicated by an arrow pointed toward the circle and touching the circle. A binary digit at the end of the input line within the circle indicates the state to which the magnetic core is brought by this input. If the input is a d.c. input, the arrow is replaced by a blocked-in triangle.

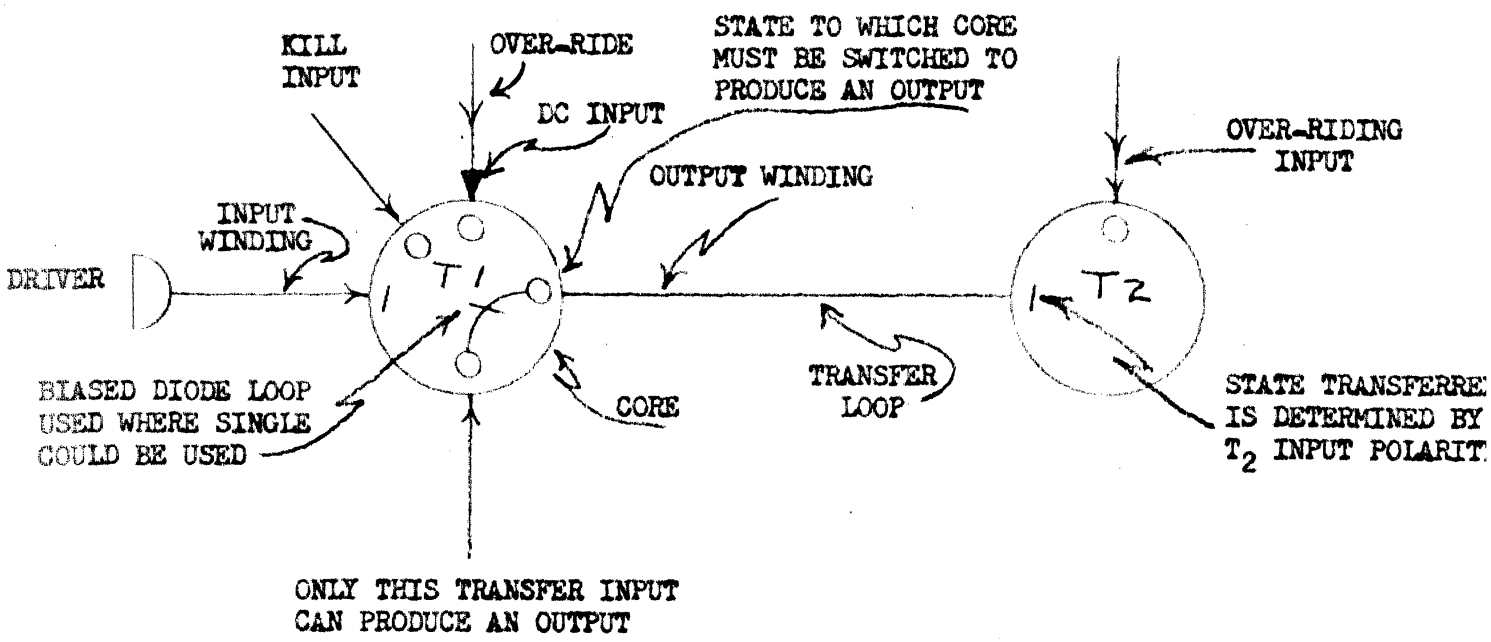
5) An output winding is indicated by a line touching the circle with the arrow pointed away from the circle. A binary digit within the circle at the beginning of the output line, indicates the transfer state to which the magnetic core must be brought, (from the other state) to produce this output.

NOTES

1) An input which brings the magnetic core into the transfer state, is called a transfer input.

2) The transfer state of a magnetic core may be ZERO for some outputs, and ONE for some other outputs.

6) If there is no special indication, any output may be produced by any transfer input when the core is switched from the non-transfer state to the transfer state. If an output may be produced by only one of several inputs, it must be connected by a connecting bar inside the circle to the transfer input able to produce it.

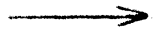


7) A driver is represented by a large D with an arrow touching it to indicate the input, and a straight line leaving it, to indicate the output.

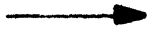
8) Basic timing pulses are represented by the letter t, a subscript indicating the time of occurence.

9) An arrow on a line indicates the direction of the logical flow along this line.

BASIC LOGICAL SYMBOLS FOR MAGNETIC CORES



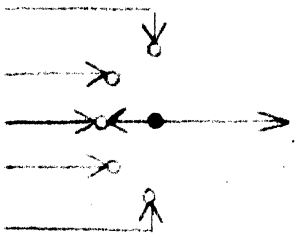
Pulse (from driver or core).



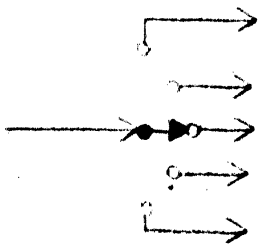
Direct Current.

Pulse over-ride.

D. C. over-ride.

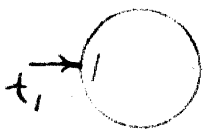


Logical switch for selection of one of several input sources.

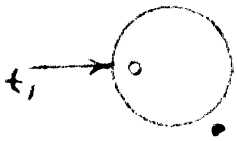


Logical switch for selection of one of several output destinations.

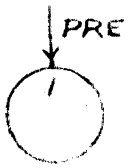
A square core.



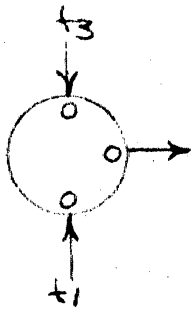
A core switched to the ONE state at Time t_1.



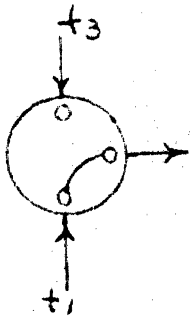
A core switched to the ZERO state at Time t_1.



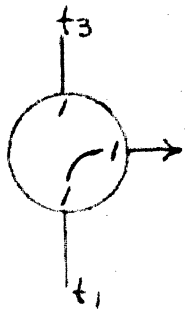
Preset of core into ONE state. This refers to initial setting. Where the symbol is not used, preset is understood to be ZERO.



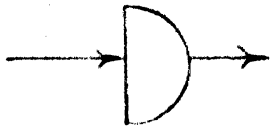
A core producing transfer if switched from the ONE to the ZERO state at times t_1 or t_3. This is unconditional transfer.



A core producing transfer as above except only at time t_1. This is conditional transfer. (t_3 puts core into ZERO state without producing transfer.)



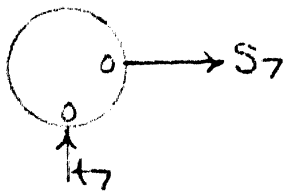
A core producing conditional transfer at time t_1 when switched from the ZERO to the ONE state.



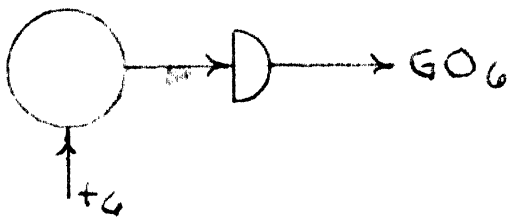
Current Driver.

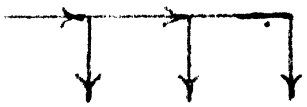
NOMENCLATURE

Lower case t for basic clock drivers. Upper case symbols for all other core pulses or drivers. Subscripts indicate the time that a pulse or driver occurs with respect to the basic clock drivers. For example, a sampling pulse occuring at time t_7 may be called S_7:

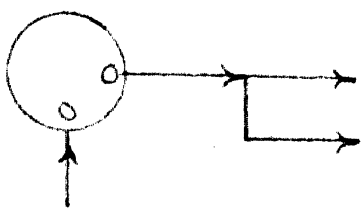


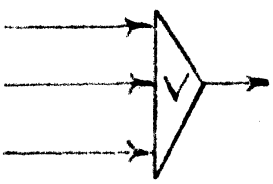
Or a driver which fires at time t_6 which is used to generate output may be called GO_6:



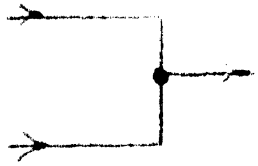


Pulse goes to more than one place (arrows at each point of divergence). For example, a core with double output:

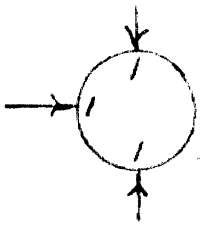




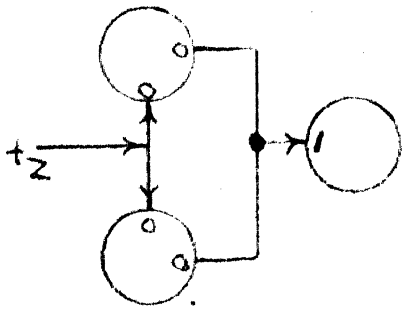
Inclusive - or - several pulses go to one winding (Triangle at point of convergence.)



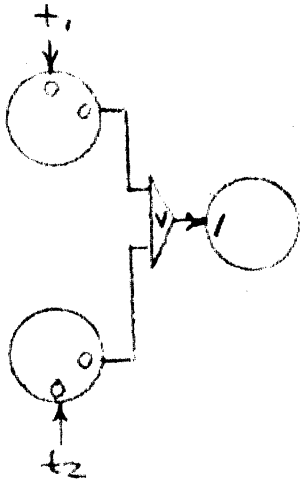
Inclusive - or - several pulses to one winding at the same time. (Dot at point of convergence.)



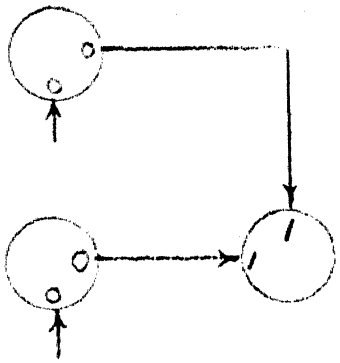
Inclusive - or - several input windings which put core into the ONE state.



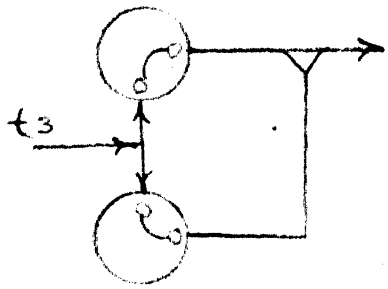
EXAMPLES: OF INCLUSIVE OR:
Two cores producing transfer if either or both are switched from ONE to ZERO at t_2. (OR circuit). Both cores must be read out at same time.



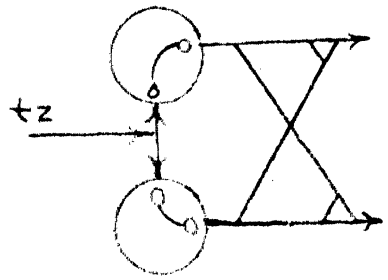
Same as above with both cores read out at different times. Designs are identical and one input winding is used.



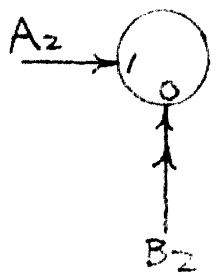
Two inputs of different designs ORed on separate windings.



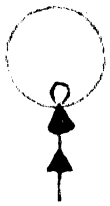
Top core transfer inhibited by bottom core. Action occurs at t_3.



Double inhibit (exclusive-or). Action occurs at t_2.



Conditional input A at t_2 overridden by conditional input B at t_2. The double arrow indicates greater strength.



Current clamp. Core held powerfully in ZERO state for long period of time. This symbol indicates that the core cannot possibly switch while clamp exists.

LESSON 7

LOGICAL REPRESENTATION

The following circuit diagrams and logical schematics illustrate the basic rules.

1. Transfer Loop--A single diode transfer loop is shown in Fig. 1.
   A split winding transfer loop is shown in Fig. 2.
2. Fig. 3 shows a circuit in which an output may be produced by any of the transfer inputs a, b or c. Note, that a connecting bar is not used.

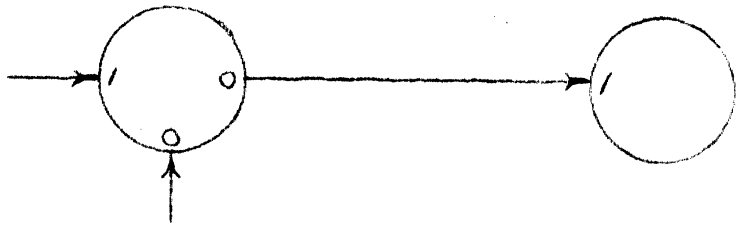


FIGURE 1 SINGLE DIODE LOOP

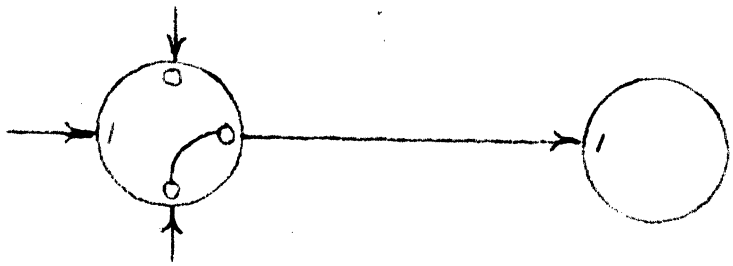


FIGURE 2 SPLIT WINDING LOOP

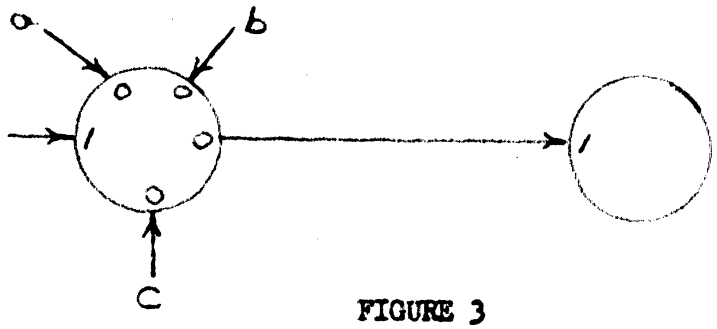


FIGURE 3

MAGNETIC SHIFT REGISTER

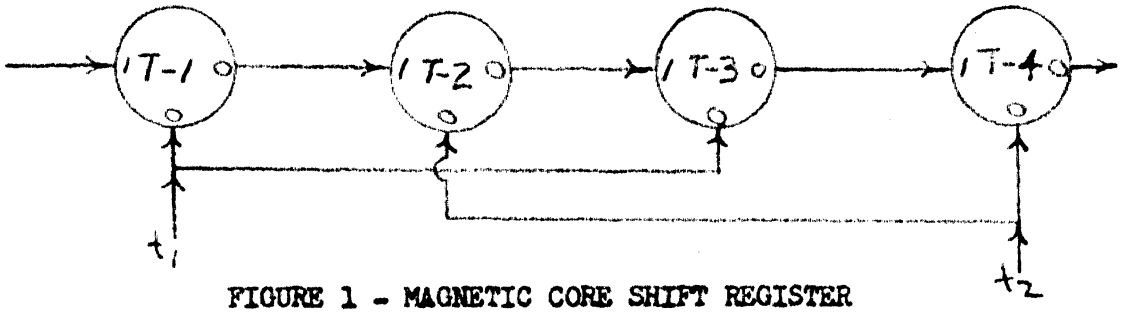


FIGURE 1 - MAGNETIC CORE SHIFT REGISTER

LOGIC - T-1 is set to the ONE state. (FIGURE 1)

All other cores are in the ZERO state.

LOGICAL OPERATION

At t_1 core T-1 is read to the ZERO state giving an output which sets T-2 to the ONE state, thus the ONE bit of information is transferred. At t_2 the ONE is transferred to T-3 with t_2 having no effect on T-4 as it is in the ZERO state already. At the next t_1 core T-1 is unaffected, but the ONE in T-3 is transferred to T-4. Thus the ONE that began in core T-1 has shifted down the register until its present position in T-4.

MAGNETIC COUNTER

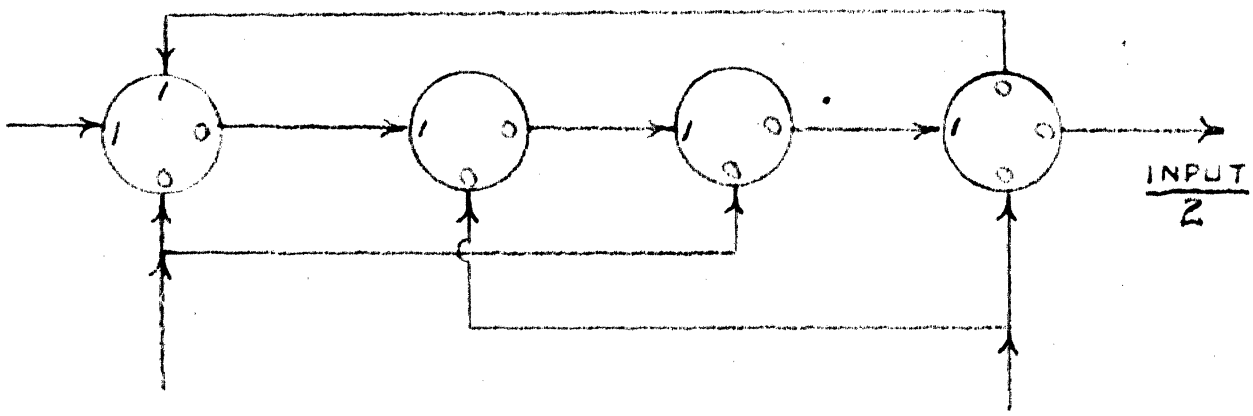


FIGURE 2 - MOD 2 MAGNETIC COUNTER

LOGIC - T-1 is set to the ONE state. (FIGURE 2)

All other cores are in the ZERO state.

LOGICAL OPERATION

The counter is the same in operation as the Magnetic Shift Register except that the output of T-4 is fed back to T-1 thus resetting T-1 at the same time an output is obtained from T-4. This makes a complete and continuous loop not requiring any external resetting until all cores have been cleared for a new initial start-up. Operating in this manner every other t_2 will give an output thus dividing the input pulsed by two. This is called a Mod 2 counter. A Mod 3 counter would have the same hook-up but using six cores to give an input to output division of three, thus a pattern may be seen in this for the arrangement of cores for specific counter divisions.

CYCLE DISTRIBUTOR

This is a Magnetic Counter with more than one output. Such would be the case if another output was taken off core T-3 in FIGURE 2.

IDLER

The odd cores of a counter are called IDLERS as it is only used for bit transfer. Thus two cores are required for one BIT transfer.

The use of one driver for each core eliminates the idler cores as in FIGURE 3.

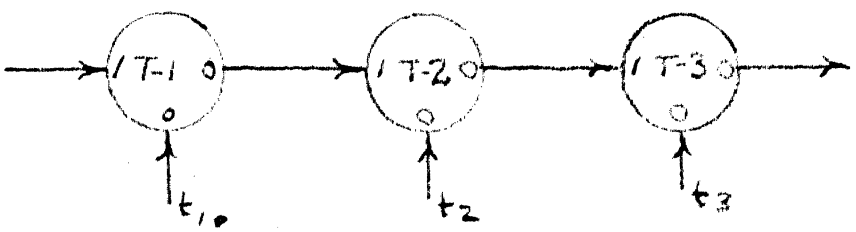


FIGURE 3 - SHIFTER REGISTER WITHOUT IDLER CORES

COMBINATION OF LOGICAL OUTPUTS

INCLUSIVE OR

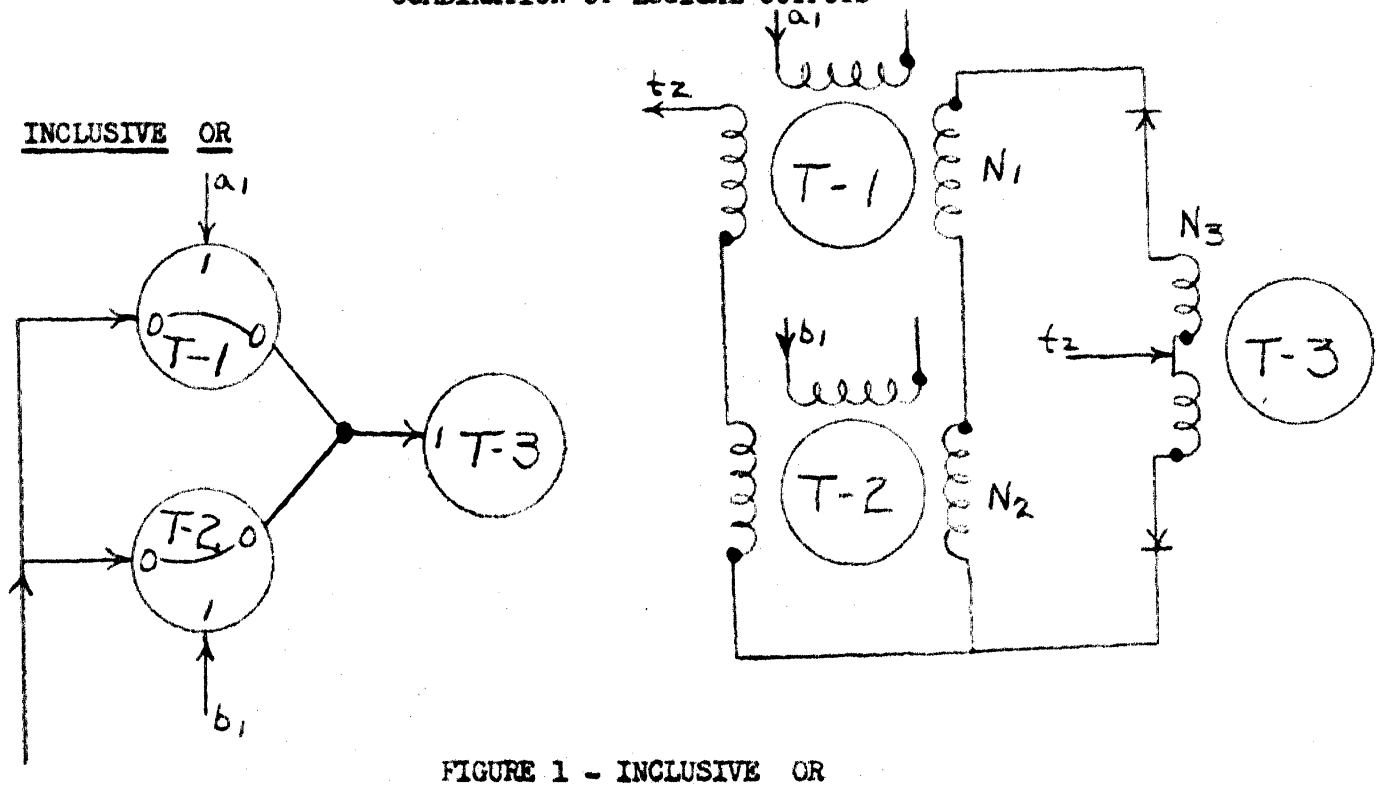


FIGURE 1 - INCLUSIVE OR

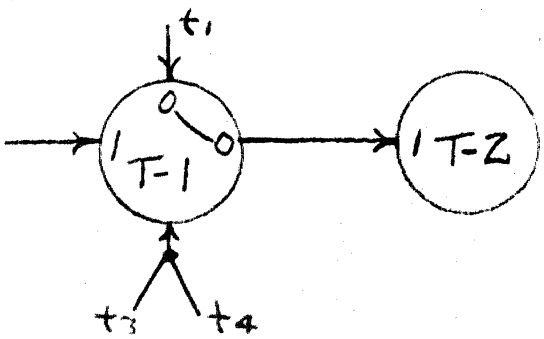
LOGIC - Cores T-1, T-2 & T-3 in the ZERO state. (FIGURE 1)

At t_1 time, no transfer input occurs.

LOGICAL OPERATION

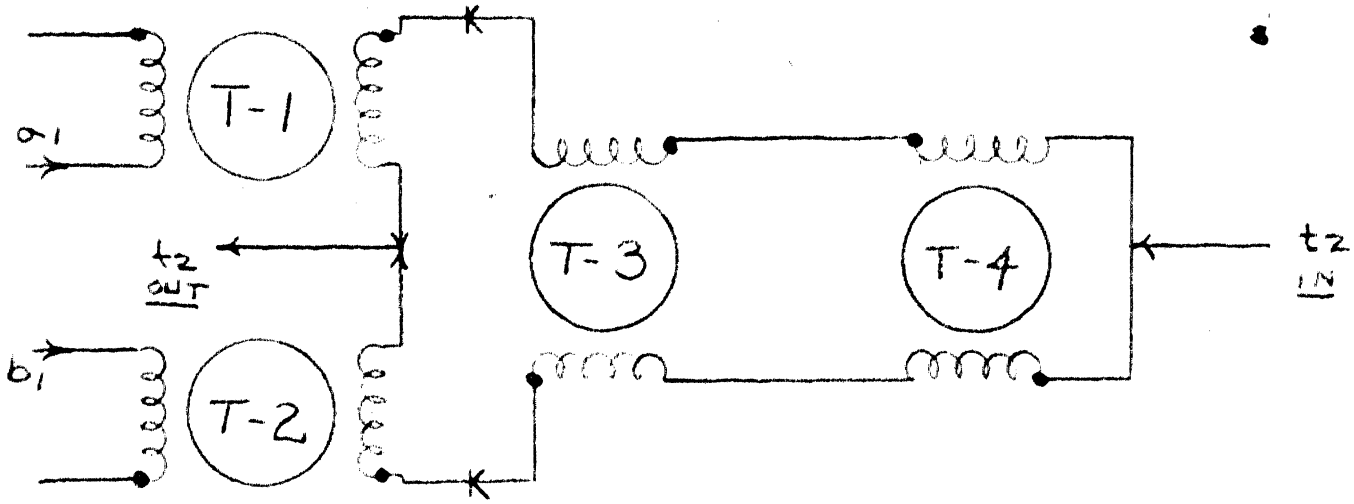
Transfer current t_2 will split evenly and T-3 will remain in the ZERO state. Next, consider at t_1 time transfer input a or b or both occur. Transfer current t_2 will divide, and switch T-1 and/or T-2, thus causing an unbalance in loop Z, with the larger portion of the current entering the non-dot terminal of winding N_3. This will switch T-3 to the ONE state, while T-1 and/or T-2 are being switched to the ZERO state.

JOINT DENIAL -



After T-1 is set to the ONE state a t_1 input will transfer the ONE to T-2 unless t_3 or t_4 or both occur first which would kill the ONE in T-1.

EXCLUSIVE OR



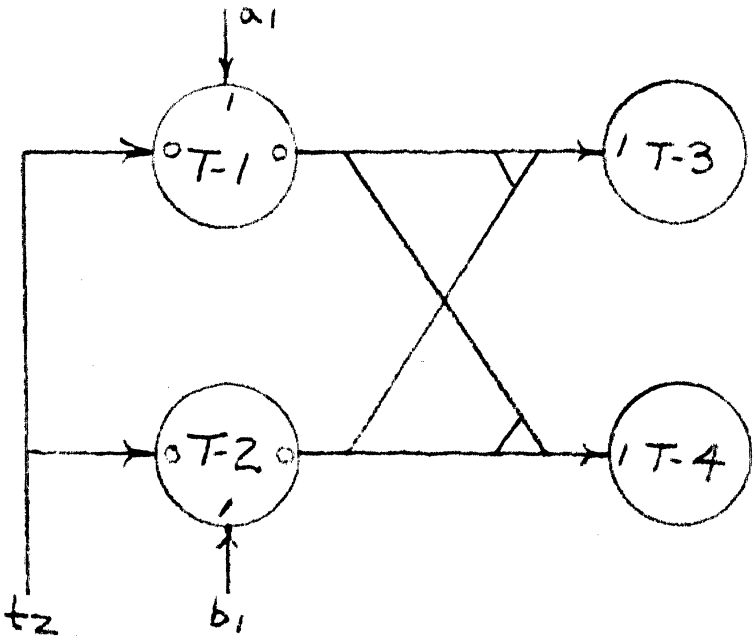


FIGURE 2 - EXCLUSIVE OR

LOGIC - Cores T-1, T-2, T-3 & T-4 are in the ZERO state. (FIGURE 2)

LOGICAL OPERATION

Inputs a_1 and b_1 switch T-1 and T-2 respectively to the ONE state. Current t_2 will split evenly since the impedance paths are equal. If only a_1 exists, the unbalanced current will switch T-3 to the ONE state. If b_1 exists, T-4 will be

switched to the ONE state. Thus an output is obtained for a_1 or b_1 input, but not if both inputs are present or if both inputs are absent.

INHIBIT

FIGURE 3 shows the schematic and logical diagram of an INHIBIT circuit. The INHIBIT output is connected by a triangle to the output it inhibits. There is a transfer of information if an output from T-1 exists logically and if an output from T-2 does not exist logically.

The inhibiting output may have as its sole function the inhibiting of another output, or may perform a transfer action on another receiving core depending upon the type of circuit.

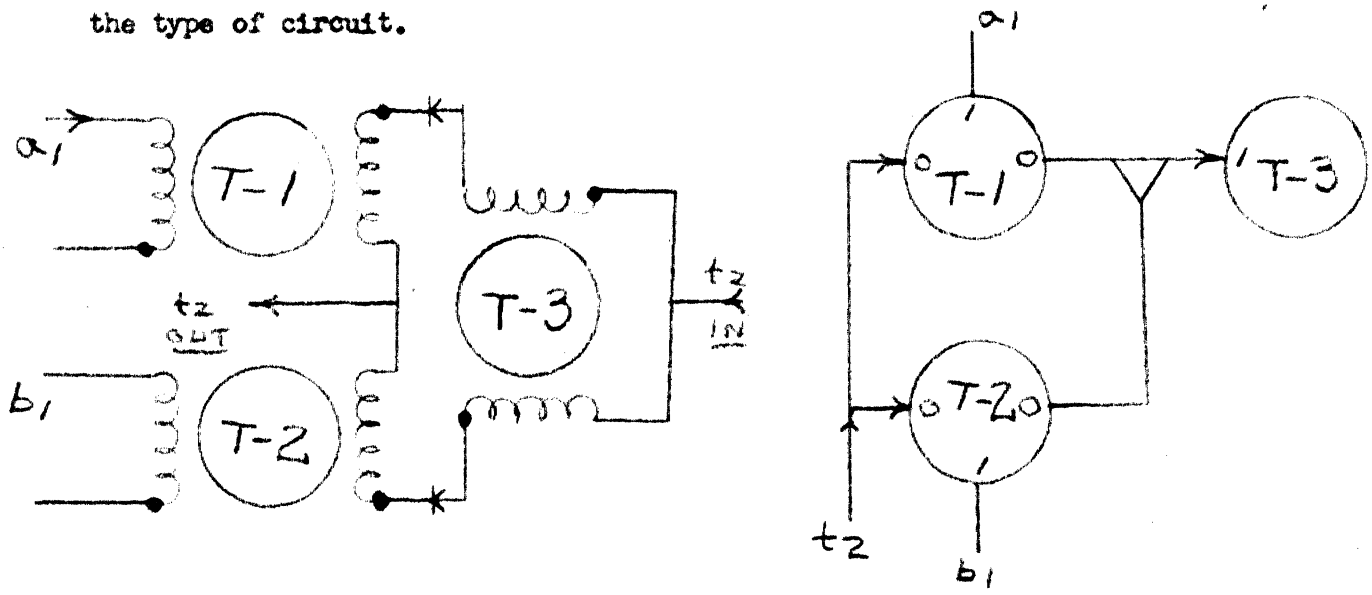


FIGURE 3 - INHIBIT

LOGIC - Core T-3 is in the ZERO state. (FIGURE 3)

Transfer inputs a_1 and b_1 set cores T-1 and T-2 to ONE state respectively.

LOGICAL OPERATION

Current t_2 will split evenly since the impedance paths are equal, leaving T-3 in the ZERO state. If transfer input a_1 exists however, and b_1 does not, then the impedance path thru the dot winding of T-3 and T-1 is greater than the path thru the non-dot winding of T-3. The greater current, therefore flows thru the lower impedance paths thus switching T-3 to the ONE state, thus completing a conditional transfer for this circuit.

LESSON 9

TRUTH TABLES

To analyze the logic of a circuit involving the output windings of several cores, it is convenient to consider the notion of logical output of a core: When a core is switched from the non-transfer state to the transfer state, the transfer input is always assumed to produce a logical output. The various logical outputs of the different cores are mixed, and the existence or absence of a physical output depends upon the logical mixing. This is illustrated in Fig. 4.

LOGICAL OPERATIONS

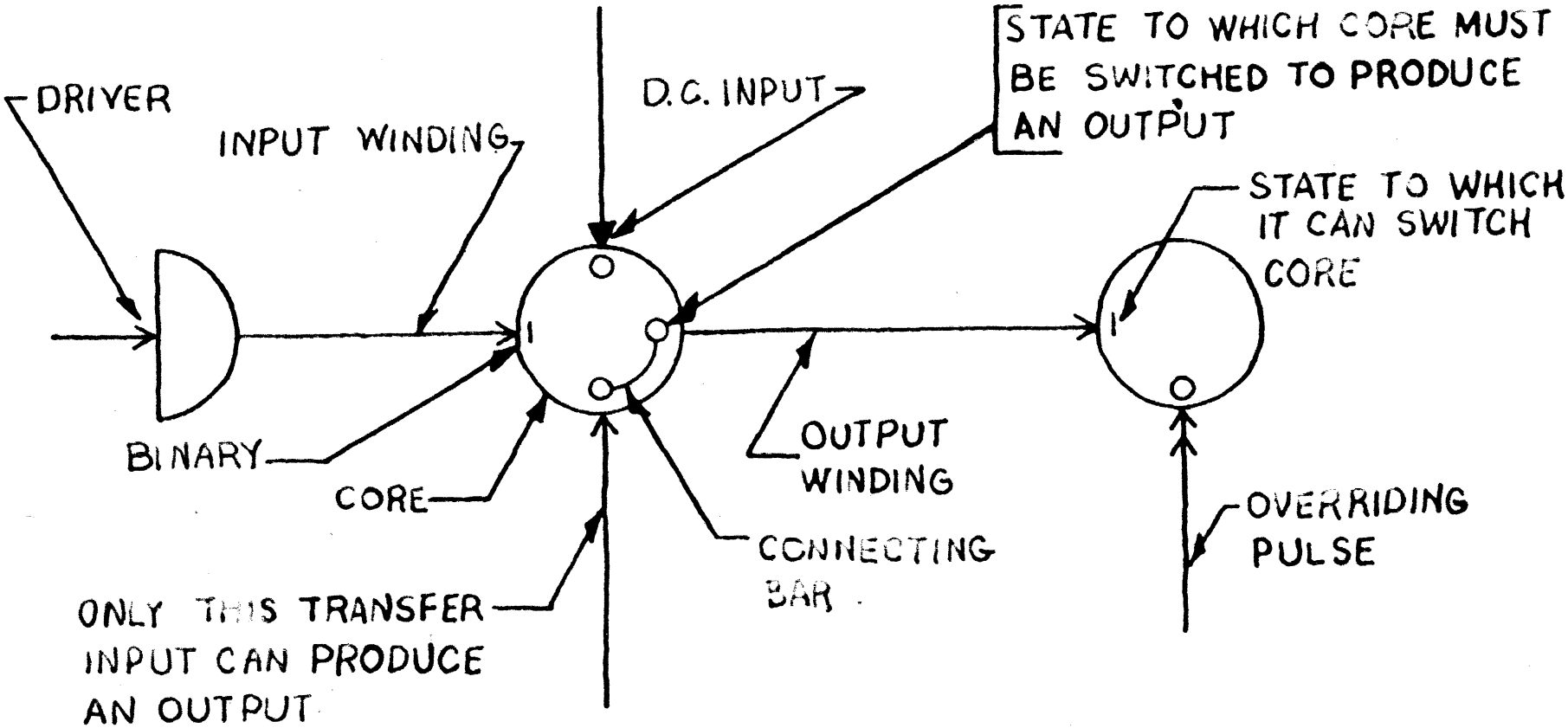
All logical operations can be expressed in terms of INCLUSIVE OR, AND, and INHIBIT functions. These are summarized in the following truth table:

TABLE I

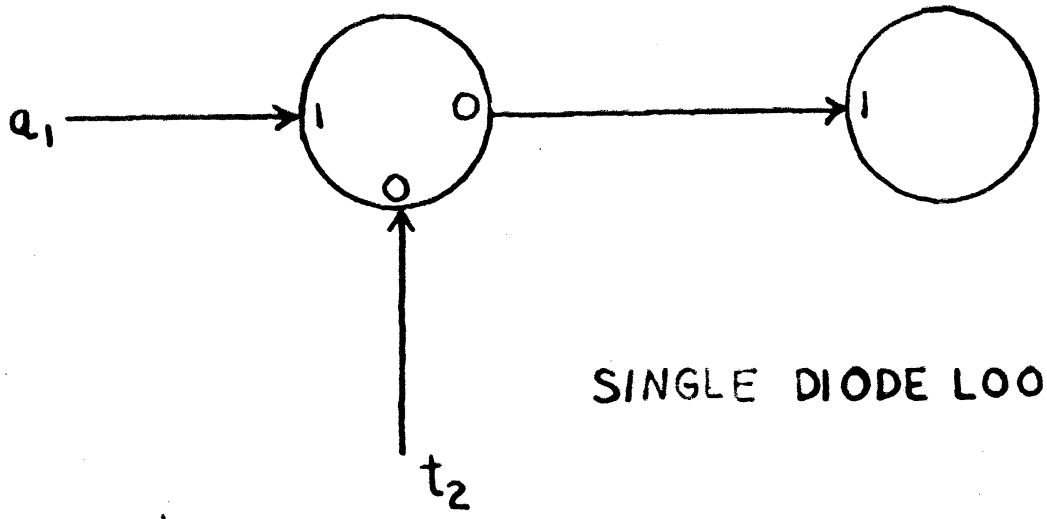
INPUTS		OUTPUTS					
a	b	INCLUSIVE OR a, b or both	EXCLUSIVE OR a or b not ab	INHIBIT a only	AND both	JOINT DENIAL neither a, b nor both	MATERIAL EQUIVALENCE
0	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	1	0	0	1	0	1

Symbols to represent these functions have been established and are described below.

INCLUSIVE OR---The two logical outputs are joined at a function marked by a small dot. (see Fig. 4)


DRIVER
INPUT WINDING
D.C. INPUT
STATE TO WHICH CORE MUST BE SWITCHED TO PRODUCE AN OUTPUT
STATE TO WHICH IT CAN SWITCH CORE
BINARY
CORE
ONLY THIS TRANSFER INPUT CAN PRODUCE AN OUTPUT
CONNECTING BAR
OUTPUT WINDING
OVERRIDING PULSE

LOGICAL REPRESENTATION



SINGLE DIODE LOOP

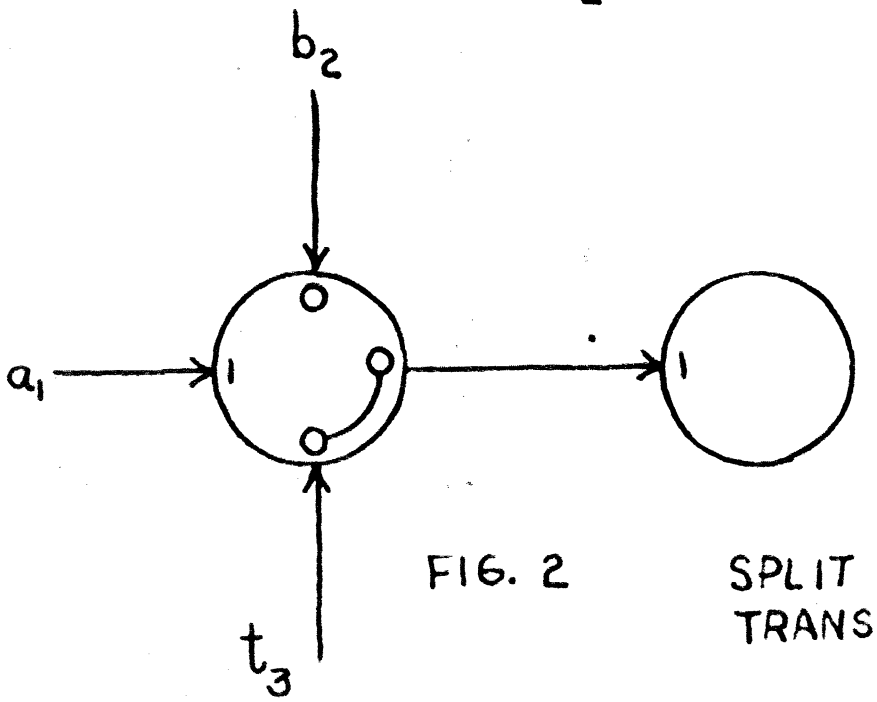
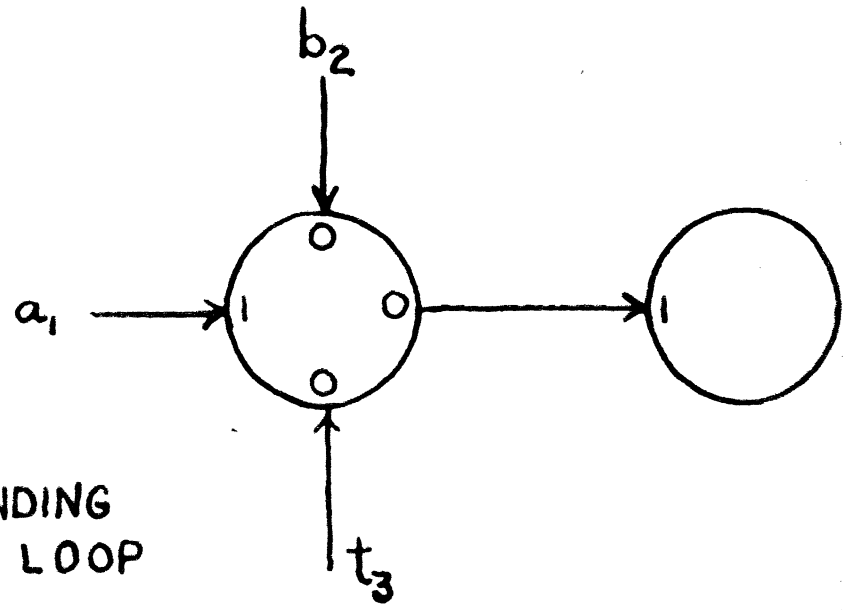


FIG. 2



SPLIT WINDING TRANSFER LOOP

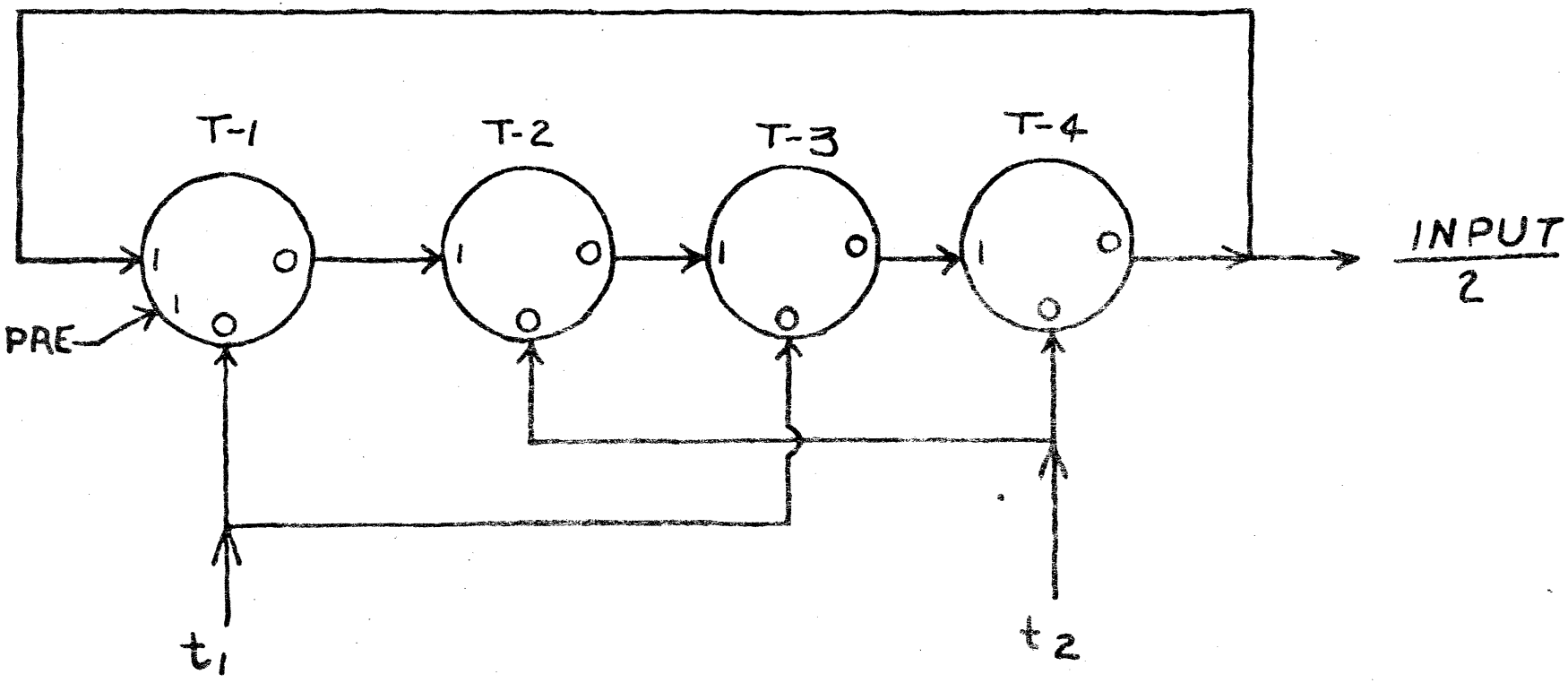
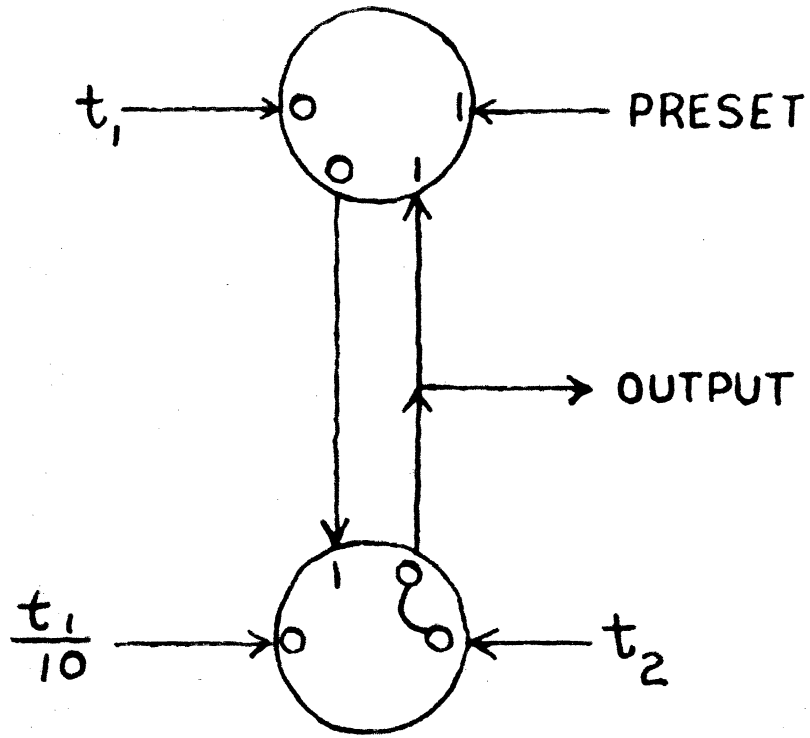


FIG. 2 COUNTER



PING PONG

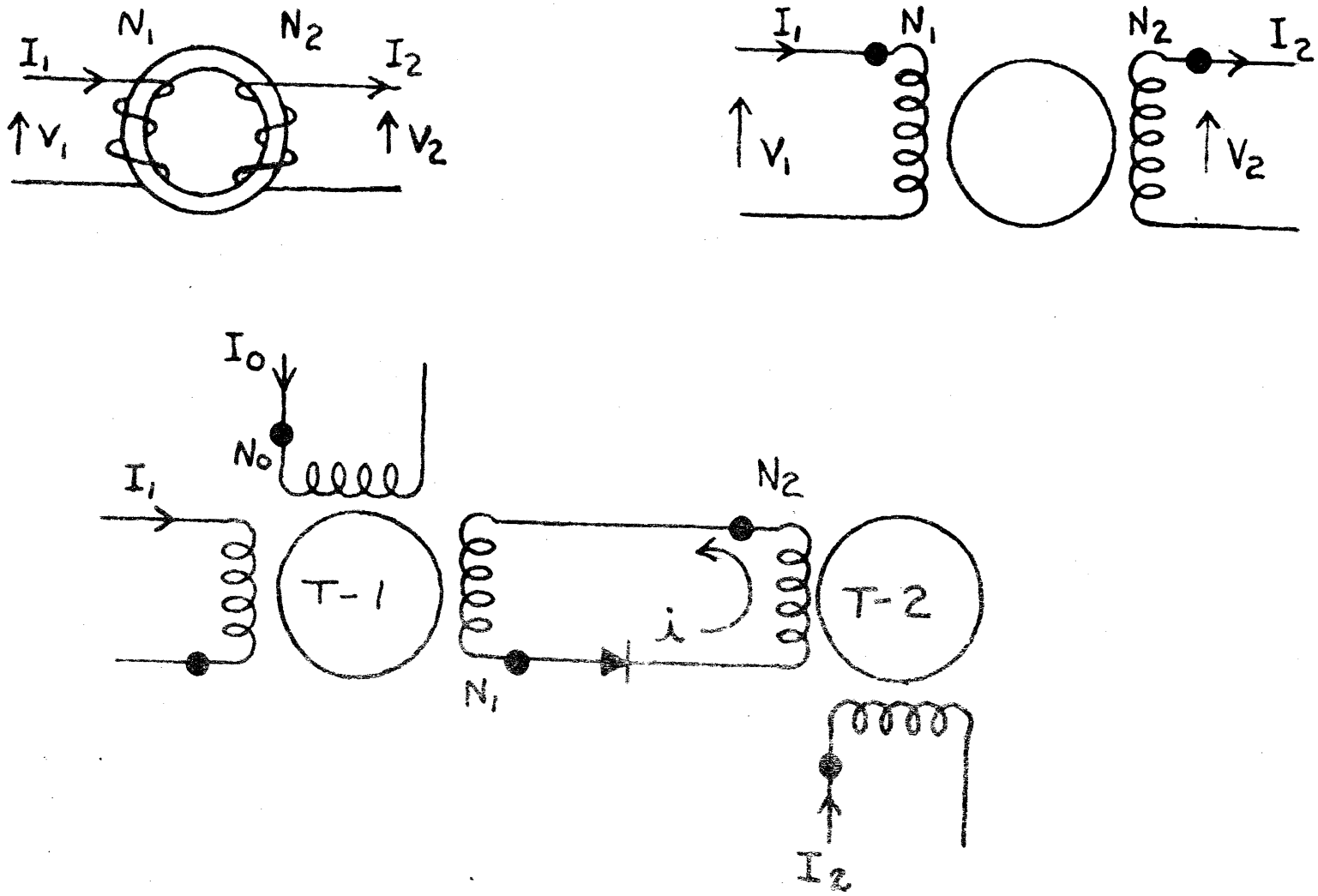


FIG. 1 SINGLE DIODE TRANSFER LOOP

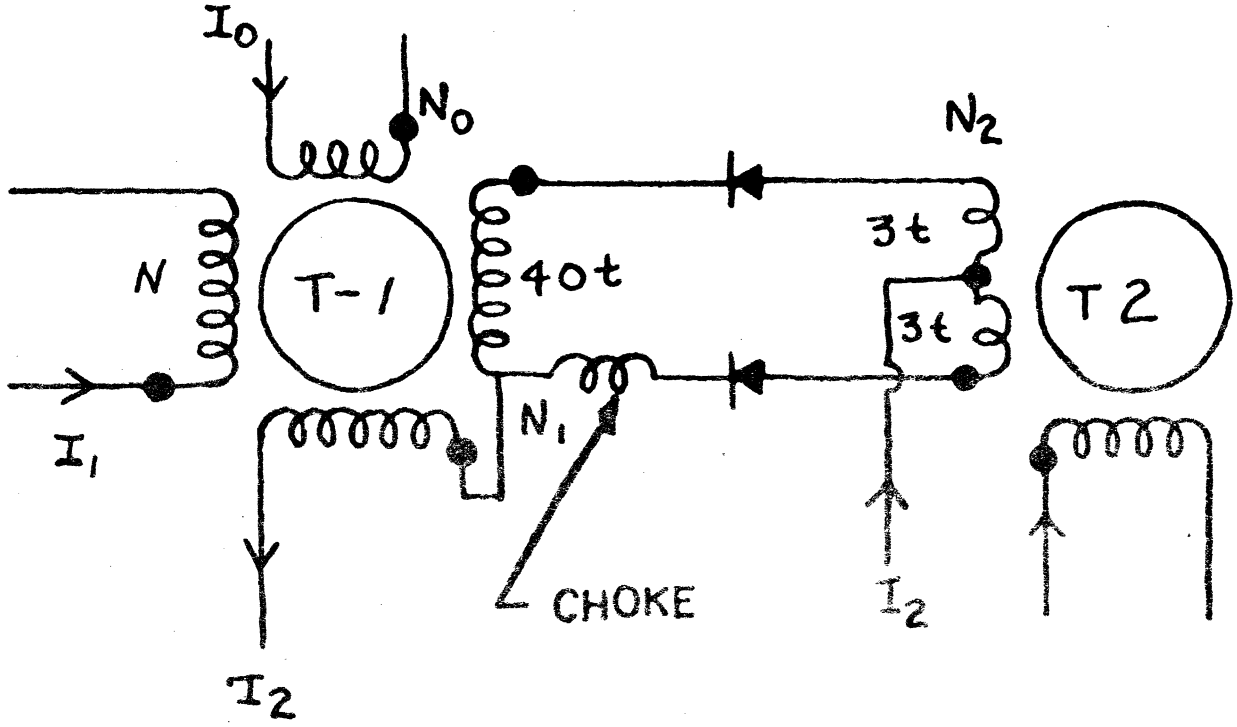
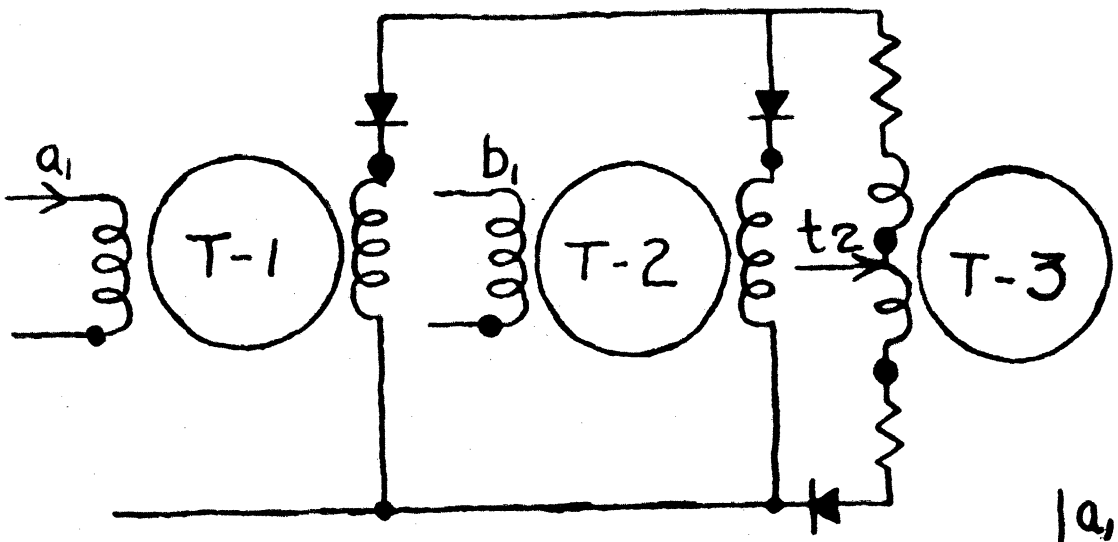
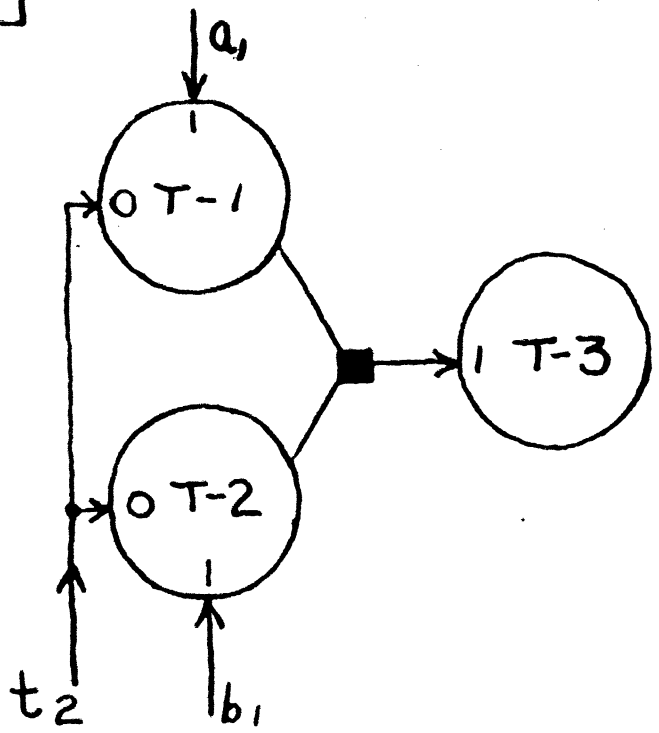


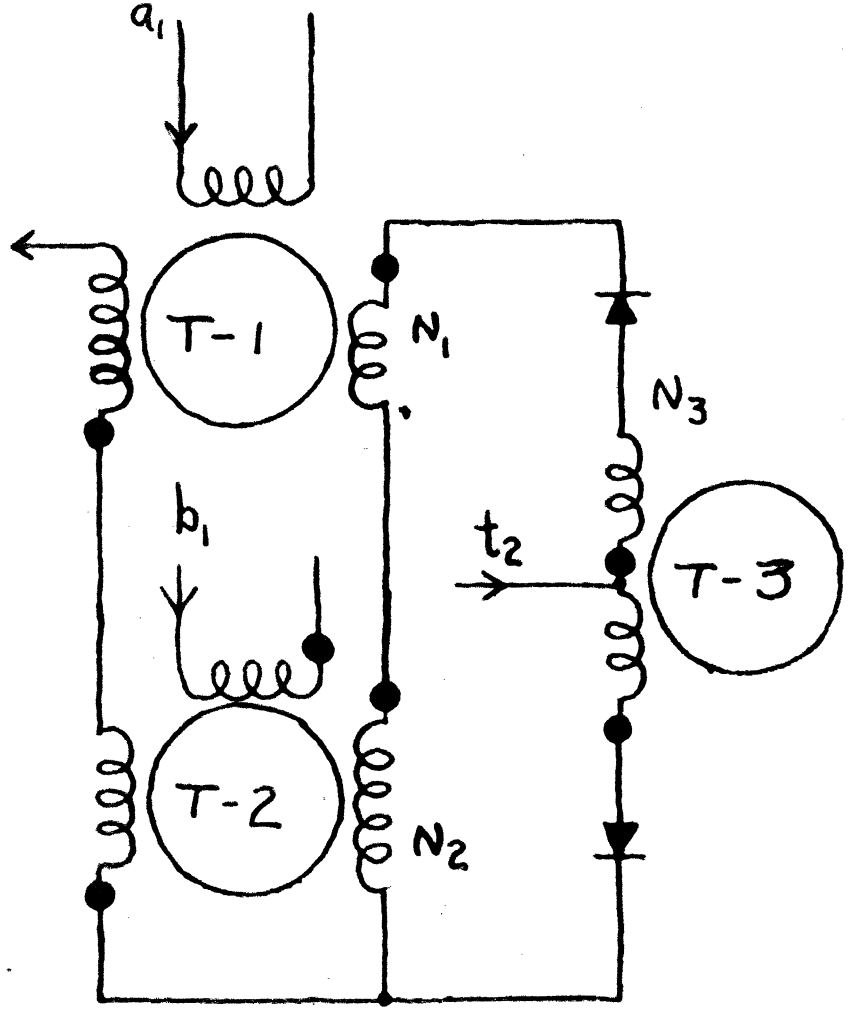
FIG. 4 SPLIT WINDING TRANSFER LOOP

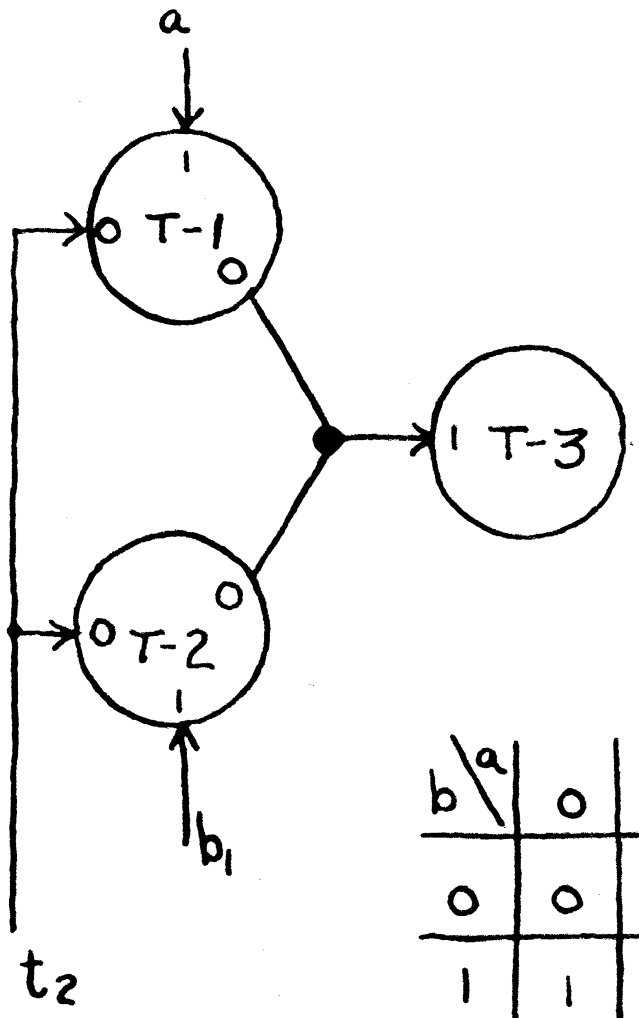
b \ a	0	1
0	0	0
1	0	1





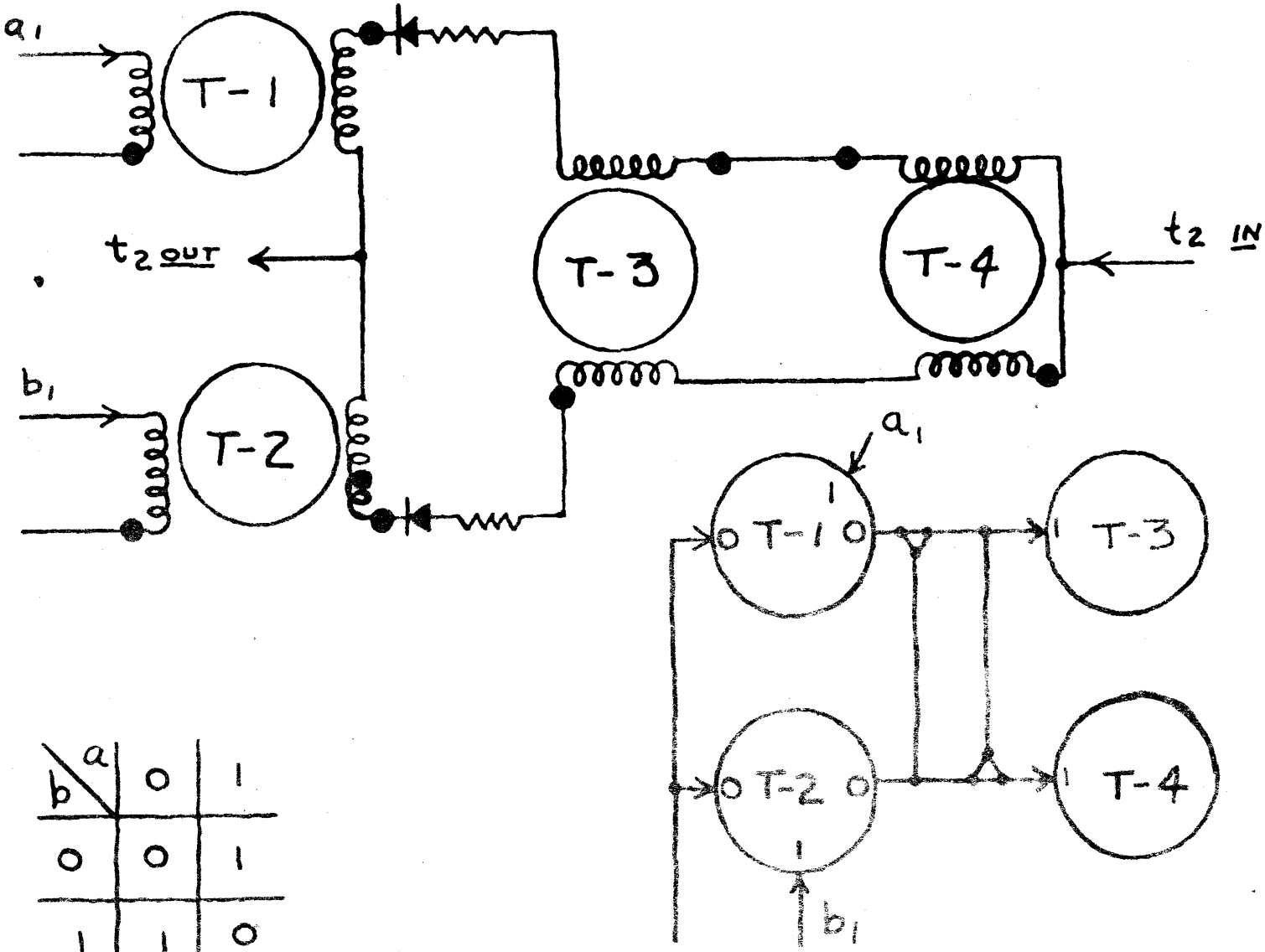
AND





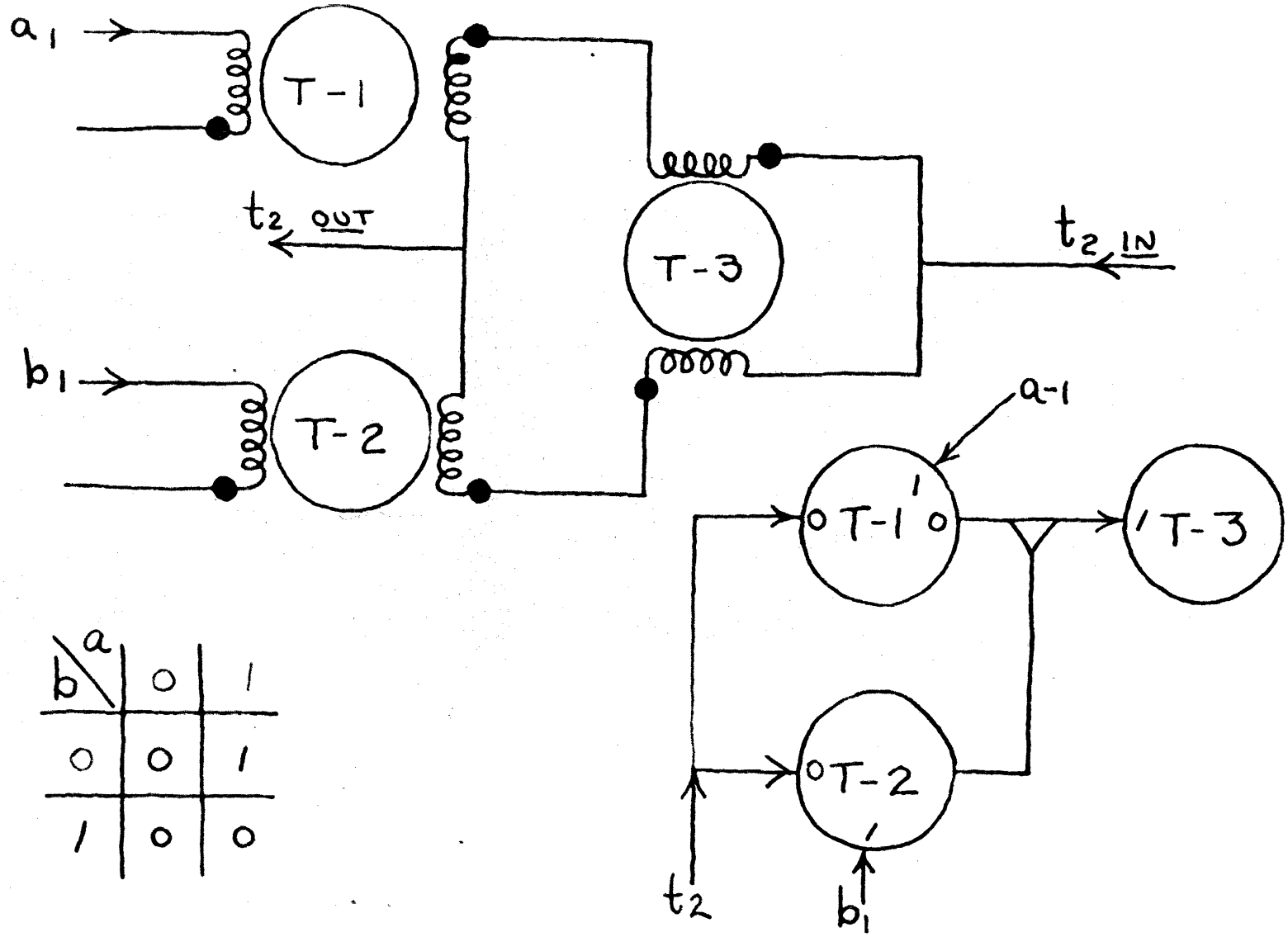
b \ a	0	1
0	0	1
1	1	1

FIG. 1 INCLUSIVE OR



b \ a	0	1
0	0	1
1	1	0

FIG. 2 EXCLUSIVE OR



b \ a	0	1
0	0	1
1	0	0

FIG. 3 - INHIBIT