

The AES-80 Microprocessor



A Fourth dimension in data acquisition processing and communication



There used to be three

There were three ways to design a digital data product or system, that is, until the AES-80 Microprocessor.

1) The traditional approach required dedicated hardware — a time consuming exercise involving long lead times for prototyping. Just when you have your product developed a customer with different requirements sends you back to redesign and modify. Often you end up with a proliferation of products, none with enough volume for reasonable manufacturing costs. Why build hardware if a make/buy analysis favours the AES-80 over your own design?

2) A recent approach uses a controller for logical functions. Typically, controllers have limitations: they are slow — with a limited instruction set and inadequate input/output capability. If you have not found a suitable controller, why not look at our Microprocessor?

3) In more complex applications, a minicomputer is a frequent choice for your dedicated processing application - often a case of overkill (and overexpenditure). A mini is a general purpose digital computer and its capabilities are not required in many applications. Furthermore minicomputer instructions do not always result in an optimum approach to a given problem and input/output is relatively complex. Finally, when you add up the cost for a minicomputer plus memory plus interface options, you have a pretty expensive item. Until the AES-80, however, you had no viable alternatives. Why buy a mini when a micro will do?

Go fourth

with the AES-80 Microprocessor, a byte oriented processor at a fraction of the cost of a mini. It is designed for the OEM or sophisticated user in dedicated processing applications. The AES-80 is part of a family of Modular System Units (MSU's) designed for data acquisition, processing and communication. Serial I/O, analog I/O, communication, control, and special purpose modules are designed for "daisy chaining" with the microprocessor MSU to satisfy specific applications.

Why the AES-80?

Using the AES-80, your design cycle is reduced to writing a software program and debugging it on our easy-to-use Program Development and Control Console. We then convert this program to a permanent Read Only Memory (ROM) and supply the completed microprocessor with memory and input/output MSU's ready for installation. Alternatively, our Programming Service is available for the software phase.

You eliminate that costly design and prototyping cycle and get to your market while others are still in the design phase. In short, the AES-80 can make you money.

The AES-80 features exceptionally fast processing-240 nanoseconds full cycle time with bipolar memory. The instruction set of 92 micro-instructions allows great flexibility for solving application problems efficiently. The input/output capability is exceptional with the serial I/O bus capable of a transfer rate of over 100,000 (8-bit) characters per second to or from the microprocessor. Parallel I/O peripherals share the high speed parallel bus with the data memory and communicate at internal processor speeds.

Naturally there is the cost element. Using the AES-80 optimizes the tradeoff between hardware and software: the microprocessor is extremely competitive with standard hardware design and when you compare our prices to those of a minicomputer, well, there is no contest. If the AES-80 will do the job then it will definitely save dollars and that's the name of the game, isn't it?

Features

- 240 nanosecond full cycle time with bipolar memories.
- serial transfer up to 100,000 8-bit characters/second.
- high speed parallel I/O.
- capability of intermixing memory types in both data and instruction memories (bipolar, MOS, ROM, etc.).
- add-on I/O capability with standard MSU's.
- direct accessing to 1K of data memory and 2K of instruction memory.
- easy to use Program Development and Control Console, which supports a teletype or high speed tape reader. No other computing facilities required.
- expandable to 4K ROM and 4K RAM with additional memory accessible on an indirect basis.
- comprehensive set of 92 micro instructions.
- complete software support includes a cross assembler, minicomputer emulator, a self assembler and standard system development routines.
- multiprocessor configuration facilitated with relinquish bus command.

Applications

- 1 OEM
- 2 End user 3 - Research
- 3 Research
- bread boards
- data communication
- process control
- terminals
- machine tool control
- remote concentration
- educational systems
- custom designs
- CRT controllers
- processing
- peripheral control
- switching
- front end preprocessing
- instrument systems
- automated testing
- airline reservations
- point of sale concentration
- simulators
- medical systems
- contour plotting
- spectrum analysers
- batch terminals
- sequence controllers
- line concentrators
- monitors
- lane counters

- Cut your design time
- Eliminate bread boards
- Tradeoff software and hardware optimally
- Replace minicomputers in dedicated processing applications
- Reduce engineering in custom designs

Architecture

The AES microprocessor is a bus organized machine designed around a data transfer concept. An 8-bit three-state processor bus is used as the main highway for data traffic between registers and the data memory. The source and destination of data travelling along the processor bus is under complete microprogram control. The basic microprocessor elements are shown in the block diagram.

Memory

A data memory word is 8 bits chosen for its applicability in data communications. To reduce memory costs a 12-bit instruction word is used, a length which is extremely efficient yet allows single word literal instructions.

Commands from the read-only instruction memory control all aspects of the microprocessor operation and are executed in a single machine clock cycle. The 12-bit data from the ROM output bus is fed to an instruction decoder, the output of which determines the logic functions to be performed within the processor during the machine cycle. The ROM data bus also goes to the inputs of various registers within the microprocessor so that, depending upon the particular instruction decoded, literal data can be outputted directy from ROM.

Data is both read out of and written into data memory via the high speed 8-bit three-state processor bus.

Intermixing

A unique feature of the AES-80 microprocessor is the ability to intermix types of memories in both Data and Instruction Memories. Memory modules of 256 words each (8-bit data memory or 12-bit instruction memory) of many types may be intermixed.

- Bipolar ROM or RAM
- MOS ROM or RAM
- Core RAM
- Capacitive ROMSpecial purpose memories

Memory module selection depends on your requirements for processing speed, power failure protection, and program length. Depending on your volume requirements memories are chosen to minimize set up and unit costs. Intermixing provides flexibility for the solution of many application problems.

Arithmetic Logic Unit (ALU)

The arithmetic logic unit operates on two 8-bit variables the processor bus and its own output buffer accumulator. The ALU is capable of performing up to 16 logic operations on its two input variables and a variety of arithmetic operations, the most important being add and subtract. The mode of the ALU is selected by the ALU command register which is set by executing a single ALU literal instruction.

Registers-

P-Register: The 12-bit P (Program Counter) register indicates the address of the next instruction to be fetched out of instruction memory.

A-Register: The 12-bit A (Data Memory Address) register holds the address of the data memory cell being read from or written into.

LA-Register: The 8-bit LA (ALU Command) register is similar to the L-Register in that an 8 bit literal from ROM is loaded into it during an ALU literal instruction. The output of the LA-Register selects the operating mode of the ALU. B-Register: The 8-bit (ALU Output Buffer) register is the ALU accumulator in which all results of the arithmetic and logical operations are stored.

U-Register: The U (Universal) register is an 8-bit parallel in, parallel out, serial in or serial out register. It is primarily used as the serial I/O buffer register.

Push Down Stack

The AES microprocessor has an automatic push down stack for routine linkage. With this feature subroutines are written with a minimum of instruction time overhead.

Input/Output

The AES microprocessor serial I/O interface provides the necessary timing and control to communicate with both low and high speed peripheral devices. This I/O bus is used to transfer 8-bit serial characters at rates up to one character every 9.12 microseconds. When a start I/O instruction is executed, the clocking and transfer of I/O data then becomes automatic, with the microprocessor free to execute other instructions during the I/O interval. In addition to the serial I/O, a high speed parallel I/O capability is available. This is normally used as a means of providing fast hardware processor options such as multiply/divide or sine/cosine, etc. This bus is also used as a means of accessing a large data base such as a disc or magnetic tape unit where maximum data throughput is necessary.

The AES-80 MICROPROCESSOR

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Physical Configuration

The basic microprocessor MSU consists of a wire wrap mother board with nine connectors for insertable printed circuit boards. The microprocessor boards consist of 3 logic cards, one ROM card, and one RAM card. Four additional connector slots are available on the mother board. The first of these is reserved for an interface board for communication with the Program Development and Control Console used for program development and checkout. One position is reserved for serial input/output control which comes in two versions - equipped with threestate inputs and outputs or differential line drivers and receivers. This card increases the load capability on the I/O bus. The remaining two slots may be filled by two parallel I/O interface cards or one interface card and one parallel I/O buffer expander.

MSU back planes contain three standard connectors — a differential serial I/O connector and 2 parallel I/O connectors. MSU's may be "daisy chained" at distances up to 1000 feet.

OEM Configurations

The AES-80 is available in packages specifically designed to the mechanical requirements of an OEM user.



Microprocessor Modular System Unit (MSU)



MSU backplane with timing and control cards

Loddns

Program Development and Control Console (PDCC)

and tape loading. including controls for program listing controls for program development, of indicators, displays, switches, and the P.D.C.C. contains a complete set paper tape reader. The front panel of sole, an ASR teletype, or a punched It via the switch registers on the conalterable by loading instructions into ROM. Its contents, however, are memory simulates the permanent speed random access bipolar P.D.C.C. Within the P.D.C.C. a high cessor and also connected to the Only Memory slot of the microprointertace card is inserted in the Read face card for the P.D.C.C. A second without ROM but including the interdevelopment is a microprocessor configuration used for program an external microprocessor. The a ROM or for passively monitoring bugging prior to the "burning in" of either program preparation and de-Control Console is available for A unique Program Development and

When used to monitor a microprocessor installed in a larger system, the P.D.C.C. is primarily a passive display; active control is limited to halt, reset, single step and set command address. The microprogram is limited to fixed instruction in ROM unless read/ write memory is interunless read/ write memory is intermixed in the Instruction Memory.

A configuration of the P.D.C.C. which provides a convenient packaging arrangement for program development is one in which the microprocessor



tacture of the permanent ROM.

ities are required.

words of ROM permitting easy manu-

a truth table for every block of 256

I able generator is used to generate

language. No other computer facil-

program development in assembler

This configuration permits complete

with a 4K x 16-bit external memory.

ment and Control Chassis equipped

execution on the Program Develop-

A self assembler is available for

Once a program is debugged a Truth

Program Development and Control Console (PDCC)

cards themselves are inserted in the P.D.C.C. The combined console is ideal for software development or for prototyping.

Software

ters with 4K of memory. one of the more popular minicompuassembler version is designed for core and a Fortran compiler; the executed on any computer with 8K of nostics. The Fortran version can be comprehensive listing, and diagobject program on paper tape, a tape, or disc. Output consists of an paper tape, punched card, magnetic bler language. Input can be from Itself written in Fortran II or assemlanguage. This cross assembler is programming the AES-80 in symbolic software development which allows A cross assembler is available for

AES-80 Specifications

Characteristics

- general purpose, 8 bit, byte oriented, programmable digital microprocessor
- serial I/O up to 1 character every 9.12 microseconds
- parallel I/O on data memory bus at internal processor speeds.
- physically and functionally expandable with Modular System Units

Memory

- 8 bit data memory, 12 bit instruction memory
- either memory available with 1 to 16 256 word modules intermixed from the following types:
 - 1 Bipolar read/write 240 nsec cycle time
 - 2 Random Access read/write Core — 1 microsecond cycle time
 - 3 MOS random access read/ write memory—2 microsecond cycle time
 - 4 Bipolar Read Only Memory 240 nsec cycle time
 - 5 Capacitive Read Only Memory — 240 nsec cycle time
 - 6 Special purpose
 - 7 Other

Serial I/O

- 8 address lines, 1 read/write line, 1 load strobe line, 3 I/O clock lines.
- 1 flag status line, 1 interrupt flag,
- 1 IAK line, 1 serial data line, and
- 1 power on pulse line.
- automatic I/O of 8 bit data stream
- serial I/O can address 256 devices

Parallel I/O

12 address line, 8 I/O data lines, 1 write strobe, 1 read enable, 1 interrupt flag, 1 device ready flag, 1 interrupt line and 1 power on pulse line.

Instruction Set

ALU mode instructions	20
Data bus instructions	4
RAM address instructions	3
Accumulator instructions	4
Register instructions	6
Branch instructions	23
I/O instructions	16
Other instructions	16
TOTAL	92

Environment

0 to 70° C

Dimensions

- MSU backplane 5.25 x 8.5 inches
 Insertable
- PC boards 7.5 x 7.5 inches • PDCC 19" W x 8.75 H x 17" D

Power

9 amps maximum at 5 VDC for complete microprocessor with 1K x 8 Bipolar RAM and 1K x 12 Bipolar ROM.



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