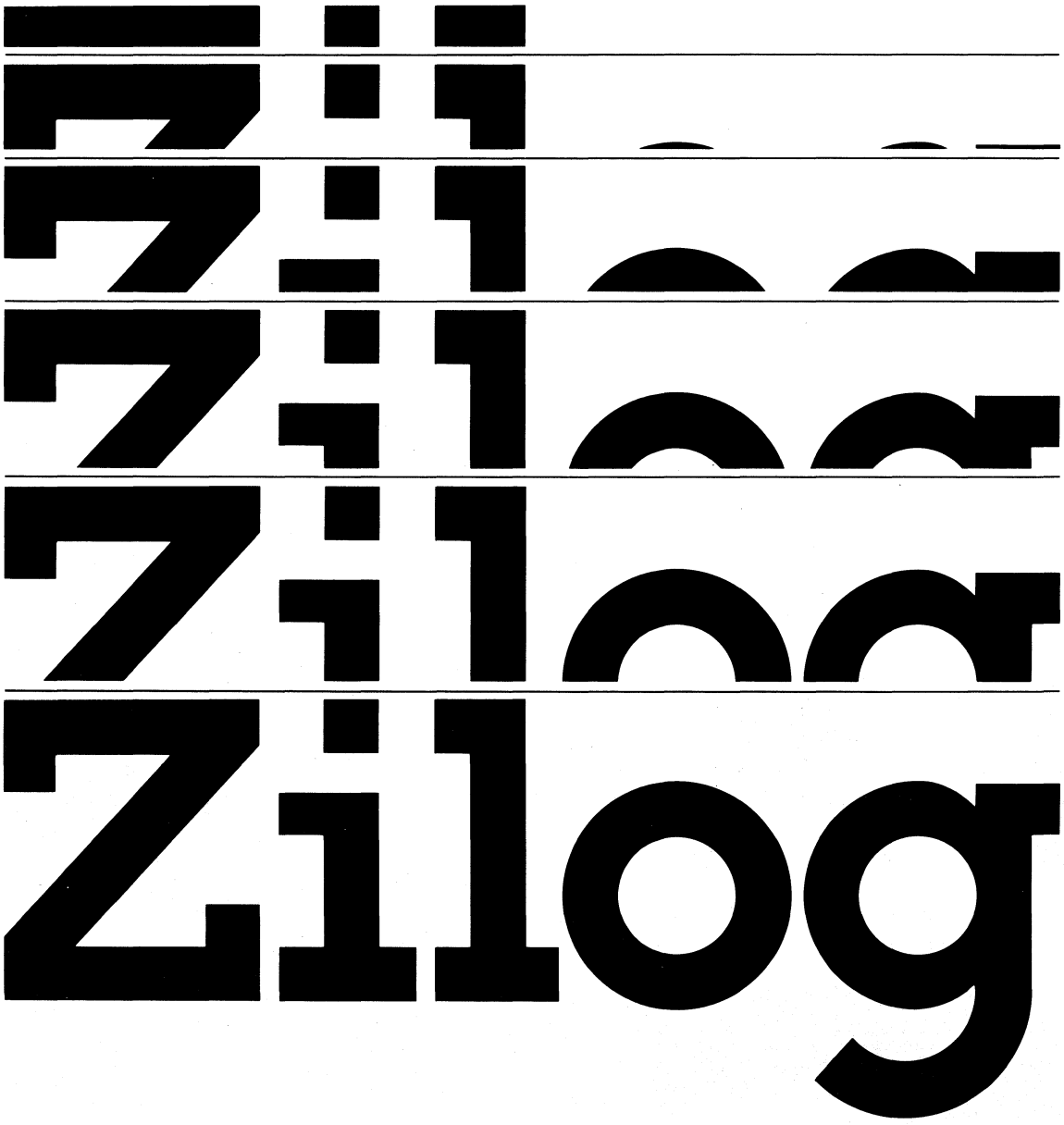
Z8® MCU Test Mode

Zilog

Application Note

June 1982



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This application note is intended for use by those with either a Z8601 or a Z8611 Microcomputer device. It is assumed that the reader is familiar with both the Z8 and its assembly language, as described in the following documents:

- Z8 Technical Manual (Reset Section) (03-3047-02)
- Z8 Family Z8601, Z8602, Z8603 Product Spec (00-2037-A0)
- Z8 Family Z8611, Z8612, Z8613 Product Spec (00-2038-A0)
- Z8 PLZ/ASM Assembly Language Programming Manual (03-3023-02)

This note briefly discusses the operation of Test Mode, which is a special mode of operation that facilitates testing of both Z8 devices that incorporate an internal program ROM (Z8601, Z8611). There are two problems associated with testing a Z8 with an internal program ROM; the solutions are presented below.

The first problem is: how can the device be tested with standard microprocessor automatic test equipment? To solve this problem, Test Mode causes the Z8 to fetch instructions from Port 1 while it is in the external Address/Data bus mode, instead of fetching instructions from the internal Program ROM. Diagnostic test routines are then forced onto this external bus from the test equipment in the same manner as with microprocessor testing.

The second problem is: since the Test Mode requires that Port 1 operate only in the Address/Data bus mode, how are the other Port 1 modes of operation tested? To solve this problem, an on-chip Test ROM is provided for execution while in Test Mode. The program in the Test ROM checks the other modes of Port 1: input, output, with handshake control, and without handshake control.

Figure 1 compares normal and Test Mode operations in the Z8. (In both normal and Test Mode, program execution begins at address $00C_H$.)

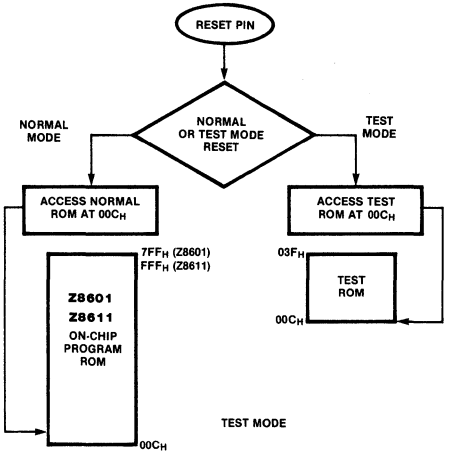
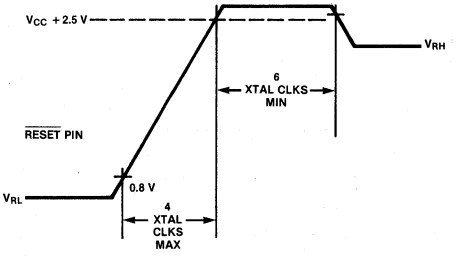


Figure 1. Comparison of Normal and Test Modes

Test Mode can be entered immediately after reset by driving the $\overline{\text{RESET}}$ input (pin 6) to a voltage of V_{CC} + 2.5 V. (See the Reset section of the Z8 Technical Manual for a description of the Reset procedure.) Figure 2 shows the voltage waveform needed for Test Mode. After entering Test Mode, instructions are fetched from the internal Test ROM, which is programmed with Port 1 diagnostic routines. The Z8 stays in Test Mode until a normal reset occurs.



Note the maximum ramp for application of +7.5 VDC to $\overline{\text{RESET}}$ pin. After a minimum of 6 XTAL CLK cycles, the $\overline{\text{RESET}}$ voltage can be relaxed to VRH.

Figure 2. Test Mode Wave Form

The program listing in the ROM is included at the end of this document. Program Listing A (Internal Test ROM Program) is mask programmed into the internal Test ROM of the Z8601. Program Listing B (External Test Program) is an example of a program that could be executed while in Test Mode. It was written as a compliment to the internal Test ROM program, to check the Port input and output functions. To test the other functions of the Z8, the user must execute other programs developed for testing.

The interrupt vectors in the Z8601 Test ROM point to the locations in external memory %800, %803, %806, %809, %80C, %80F. The interrupt vectors in the Z8611 Test ROM point to the locations in external memory %1000, %1003, %1006, %1009, %100C, %100F. This allows the external program to have a 2- or 3-byte jump instruction to each interrupt service routine.

Programs that are run in Test Mode can use an LDE instruction for accessing the Test ROM. The LDC instruction can be used for accessing the program ROM.

Program Listing A. Internal Test ROM Program

```
Z8ASM      4.0
LOC     OBJ CODE     STMT SOURCE STATEMENT

                       1                ! Z8 TEST ROM ROUTINE FOR VERIFYING !
                       2                ! PORT 1 I/O, WITH AND WITHOUT H.S. !
                       3
                       4
                       5 TESTROM MODULE
                       6
                       7
                       8 $SECTION PROGRAM
                       9 $ABS 0
                      10    INTERNAL
P 0000 0800   0803     11         RUPT_VECTOR ARRAY [6 WORD]:=
P 0004 0806   0809
P 0008 080C   080F
                      12         [%800 %803 %806 %809 %80C %80F]
                      13 $SDEFAULT
                      14
                      15
                      16 INTERNAL
                      17 TEST
P 000C                18 PROCEDURE ENTRY $ABS %00C
                      19
P 000C E6  F8  96     20         LD P01M #%96     ! P1&P0=EXT MEM,STK=IN,NORMAL !
P 000F 8D  0812       21         JP EXT           ! JUMP TO EXTERNAL TEST CODE !
P 0012 99  F8         22 START1: LD P01M R9       ! START OF P1 I/O TEST !
P 0014 A9  F7         23         LD P3M R10       ! SET H.S.& P2 PU ACTIVE !
P 0016 48  E3         24         LD R4 %E3        ! TEST RDY=1,DAV=1 !
P 0018 F3  DE         25         LD @R13 R14      ! WRITE PORT !
P 001A 61  ED         26         COM @R13         ! WRITE PORT !
P 001C 58  E3         27         LD R5 %E3        ! TEST RDY=0,DAV=1 !
P 001E E3  6B         28         LD R6 @R11       ! READ PORT & STUFF DATA !
P 0020 E3  7B         29         LD R7 @R11       ! DITTO !
P 0022 88  E3         30         LD R8 %E3        ! TEST RDY=1,DAV=1 !
P 0024 C9  F8         31         LD P01M R12      ! CONFIGURE FOR EXT !
P 0026 8D  0831       32         JP VERIFY1       ! JUMP TO VERIFY ROUTINE !
                      33
```

Program Listing A. Internal Test ROM Program (continued)

```
P 0029 B9  F7          34 START2: LD P3M R11      ! START TEST NO H.S. !
P 002B 99  F8          35         LD P01M R9      ! SET P1 TO INPUT !
P 002D 1E              36         INC R1          ! READ & WRITE P1 AS INPUT !
P 002E F9  F8          37         LD P01M R15     ! SET P1 TO OUTPUT !
P 0030 1E              38         INC R1          ! READ & WRITE PI AS OUTPUT !
P 0031 98  E1          39         LD R9 %E1       ! SAVE RESULTS IN R9 !
P 0033 C9  F8          40         LD P01M R12     ! P1&P0=EXT,STK IN,NORMAL !
P 0035 8D  086D        41         JP VERIFY2      ! JUMP TO VERIFY #2 ROUTINE !
P 0038                 42 END TEST
```

Program Listing B. External Test Program

```
                       47 INTERNAL
                       48 SETUP
P 0800                 49 PROCEDURE ENTRY $ABS %800
                       50
P 0800 8D  0800        51 VECT1:  JP VECT1
P 0803 8D  0803        52 VECT2:  JP VECT2
P 0806 8D  0806        53 VECT3:  JP VECT3
P 0809 8D  0809        54 VECT4:  JP VECT4
P 080C 8D  080C        55 VECT5:  JP VECT5
P 080F 8D  080F        56 VECT6:  JP VECT6
                       57
P 0812 8F              58 EXT:    DI
P 0813 31  00          59         SRP #%00
P 0815 2C  FF          60         LD R2 #%FF      ! INITIALIZE P2 !
P 0817 3C  FF          61         LD R3 #%FF      ! DITTO !
P 0819 E6  F6  FF      62         LD P2M #%FF     ! SET P2 TO INPUT !
P 081C 4C  88          63         LD R4 #%88      ! SET P2<>P1 MUX,P3 GRP B MUX !
                       64                         ! ALSO DUMMY ADDRS HIGH BYTE !
P 081E 5C  00          65         LD R5 #%00      ! DUMMY ADDRS LOW BYTE !
P 0820 9C  86          66         LD R9 #%86      ! P1 OUTPUT MODE VALUE !
P 0822 AC  39          67         LD R10 #%39     ! R10 SETS H.S.MODE & P2 PULLUPS
P 0824 BC  02          68         LD R11 #%02     ! R11 POINTS TO P2 FOR PASS1 !
P 0826 CC  96          69         LD R12 #%96     ! R12 SETS P01M TO EXT MEM,ETC.
P 0828 DC  01          70         LD R13 #%01     ! R13 POINTS TO P1 FOR PASS1 !
P 082A FC  86          71         LD R15 #%86     ! SAME AS R9 !
P 082C EC  AA          72         LD R14 #%AA     ! DATA LOADED TO TEST PORT !
P 082E E6  10  10      73         LD %10 #%10     ! RDY/DAV RESULT PASS 1 !
P 0831 E6  11  40      74         LD %11 #%40     ! DITTO !
P 0834 8D  0012        75         JP START1       ! END SETUP--JUMP TO TEST START
P 0837                 76 END SETUP
                       77
                       78
                       79 INTERNAL
                       80 VERIFY
P 0831                 81 PROCEDURE ENTRY $ABS %831
                       82
                       83
P 0831 DC  02          84 VERIFY1:LD R13 #%02     ! R13 POINTS TO P2 FOR PASS2 !
P 0833 BC  01          85         LD R11 #%01     ! R11 POINTS TO P1 FOR PASS 2 !
P 0835 E6  F6  00      86         LD P2M #%00     ! SETS P2 FOR OUTPUT !
P 0838 66  E4  50      87         TCM R4 #%50     ! FROM HERE TO THERE WE VERIFY !
                       88                         ! TEST RESULTS FOR I/O WITH H.S.
                       89                         ! BOTH PASS 1&2 !
```

Program Listing B. External Test Program (continued)

```
P 083B ED  0880      90          JP NZ FAIL
P 083E 64  10  E5    91          TCM R5 %10
P 0841 ED  0880      92          JP NZ FAIL
P 0844 74  11  E5    93          TM R5 %11
P 0847 ED  0880      94          JP NZ FAIL
P 084A A6  E6  AA    95          CP R6 #%AA
P 084D ED  0880      96          JP NZ FAIL
P 0850 A6  E7  55    97          CP R7 #%55
P 0853 ED  0880      98          JP NZ FAIL
P 0856 66  E8  50    99          TCM R8 #%50
P 0859 ED  0880     100          JP NZ FAIL
P 085C A6  E9  86   101          CP R9 #%86       ! IS THIS PASS1? !
P 085F E6  10  40   102          LD %10 #%40      ! RDY/DAV RESULT PASS 2 !
P 0862 E6  11  10   103          LD %11 #%10      ! DITTO !
P 0865 9C  8E       104          LD R9 #%8E       ! P1 IS GOING TO BE AN OUTPUT !
P 0867 6D  0012     105          JP EQ START1     ! PASS1 SUCCESSFUL--TRY PASS2 !
P 086A 8D  0029     106          JP START2        ! PASS2 SUCCESSFUL--TEST NO H.S.
P 086D A6  E9  57   107 VERIFY2:CP R9 #%57       ! CHECK RESULT OF I/O NO H.S.TES
                    108
P 0870 6D  0890     109          JP EQ PASS
P 0873              110 END VERIFY
                    111
                    112
                    113 INTERNAL
                    114 TPASS
P 0890              115 PROCEDURE ENTRY $ABS %890
                    116
  0890 8B  FE       117 PASS:JR PASS
                    118
  0892              119 END TPASS
                    120
                    121
                    122
                    123 INTERNAL
                    124 TFAIL
  0880              125 PROCEDURE ENTRY $ABS %880
                    126
                    127
  0880 8B  FE       128 FAIL:JR FAIL
                    129
  0882              130 END TFAIL
                    131
                    132 END TESTROM

  Assembly complete
```

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