WD90C56 T-52-33-49

Video Local Bus Interface

(VLBI) Device

WESTERN DIGITAL

T-52-33-49

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1.0 INTRODUCTION

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1.1 DOCUMENT SCOPE

This document describes the WD90C56, a single chip VLBI, Video Local Bus Interface.

In this document, the term VLBI (Video Local Bus Interface) is used as a term when referring to the WD90C56.

1.2 REFERENCE DOCUMENTS

The following reference documents may be of help:

- WD90C30 Data Sheet
- WD90C31 Data Sheet
- WD90C56 Product Bulletin

1.3 FEATURES

- 160 pin PQFP
- High speed local bus interface to VGA controllers
- Minimal local bus capacitive loading - typically ≥ 10 pF
- Designed to work with current integrated cache controllers (ISA, MC, and EISA bus controllers)
- Designed to work with stand-alone cache controllers
- Supports 386SX, 386DX, and 486 microprocessors
- Supports 20, 25 and 33 MHz 486 CPU operation
- Supports 20, 25, and 33 MHz 386SX/DX operation
- Supports WD90C30, WD90C31 and future 32-bit data bus VGA chips
- One level 32-bit write buffer
- Laptop Mode - supports future Western Digital laptop VGAs
- Supports Dual RAMDACs (one on the local bus and one on the AT bus)
- Supports dual display modes (VGA and Monochrome AT card)
- VGA MEMCLK can be synchronous or asynchronous to the CPU for optimized bandwidth
- RAMDAC low and high time for IOWs 9 and 18 clocks - programmable
- RAMDAC high time for IORs 9 and 18 clocks - programmable
- $\overline{\text{VIOW}}$s, $\overline{\text{VIOR}}$s have two to five programmable clocks (low and high time)
- $\overline{\text{VMWR}}$, $\overline{\text{VMRD}}$ have two to five clocks separately programmable low and high

1.4 GENERAL DESCRIPTION

The WD90C56 is a 160-pin device that can significantly improve VGA performance in high end PC systems. The VGA chip is directly interfaced to the 486/386 or 386SX local bus through the VLBI interface chip to achieve high-performance VGA subsystems.

2.0 ARCHITECTURE

2.1 FUNCTIONAL DESCRIPTION

The VLBI chip monitors the CPU ADS for detecting CPU accesses to the VGA chip. If the chip detects a VGA cycle, it generates a $\overline{\text{VLBICS}}$ signal to block the core logic from generating any cycles on the system bus (AT, MC, EISA, or other bus). The VGA chip, WD90C31, uses a 16-bit multiplexed AD0:15 data address bus. The VLBI chip drives the address on AD0:15, for a read cycle and turns the AD0:15 into input mode. For IO cycles the number of wait states can be programmed into the VLBI chip. The VGA does not assert VGARDY for I/O cycles. For memory cycles to the VGA, it looks at VGARDY and extends the cycles until VGARDY is sampled high. A typical cycles on the VGA side is shown at the bottom of the page.

For a Read cycle, the VLBI stops driving the address on AD0:15 after meeting a hold time to the read command ($\overline{\text{VIOR}}$/$\overline{\text{VMRD}}$). For a Write cycle, the write data is driven onto AD0:15 after negation of the address. Similar to the read commands, the data is transferred on AD0:15 and sampled into the VGA chip at the rising edge of either $\overline{\text{VMWR}}$ or $\overline{\text{VIOW}}$. For different speeds the wait states can be programmed into the VLBI chip.

The VLBI chip can interface with CPU speeds from 16 MHz 386SX to 33 MHz 386 and 486 processors. The wait states for IO access can be programmed while memory access to the VGA depends on VGARDY from the VGA as well as the chosen (programmable) parameters for command high and low durations. For 16-bit access to IO ports in VGA, the VLBI knows which ports are 8-bits and which are 16-bits and handles the byte swapping function for 8-bit ports. The VLBI chip can tell the difference between a Laptop and Desktop bus and places the data/address on the appropriate VD or AD bus.

2.2 VGA RAMDAC COLOR PALETTE SHADOWING

The RAMDAC is also interfaced to the Local Bus through the VLBI, via lines [AD7:0] and [LA18:16]. For compatibility with 8514/A, XGA, and others, the Dual RAMDAC mode can be invoked by setting Bit 7 of 2DF7. The write cycles to the RAMDAC registers generate both local VLBI cycles and system cycles by NOT generating $\overline{\text{VLBICS}}$ and the VLBI chip does not generate $\overline{\text{READY}}$ but waits for the core logic to run a write cycle on the system bus and then completes the cycle when a ready from the core logic is received. For read cycles, $\overline{\text{VLBICS}}$ is always generated and data is read through the VLBI interface. This guarantees that any plug-in card in the system bus can still

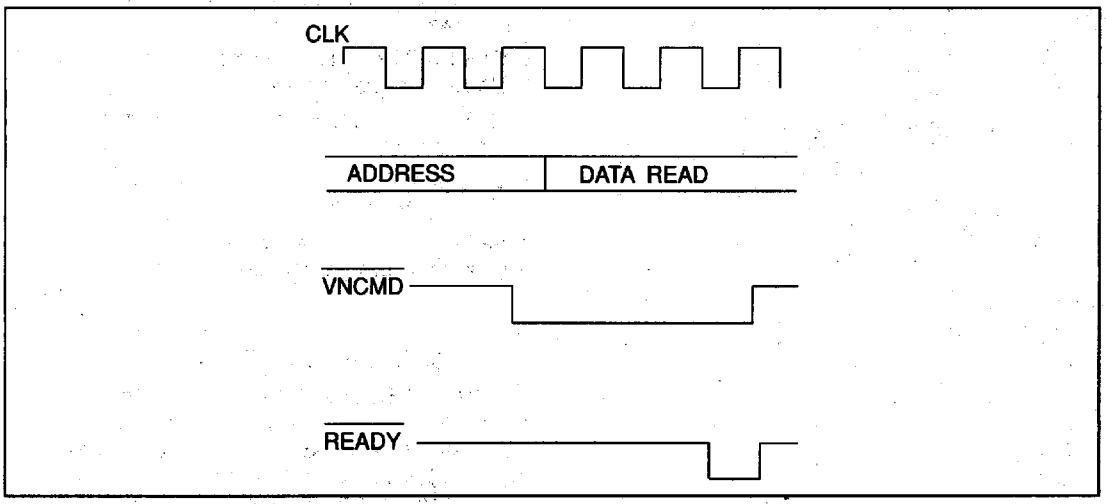

FIGURE 2-1. TYPICAL 16-BIT VGA READ CYCLE

Note: The VGA commands: $\overline{\text{VIOR}}$, $\overline{\text{VIOW}}$, $\overline{\text{VMRD}}$, and $\overline{\text{VMWR}}$ are collectively called $\overline{\text{VNCMD}}$.

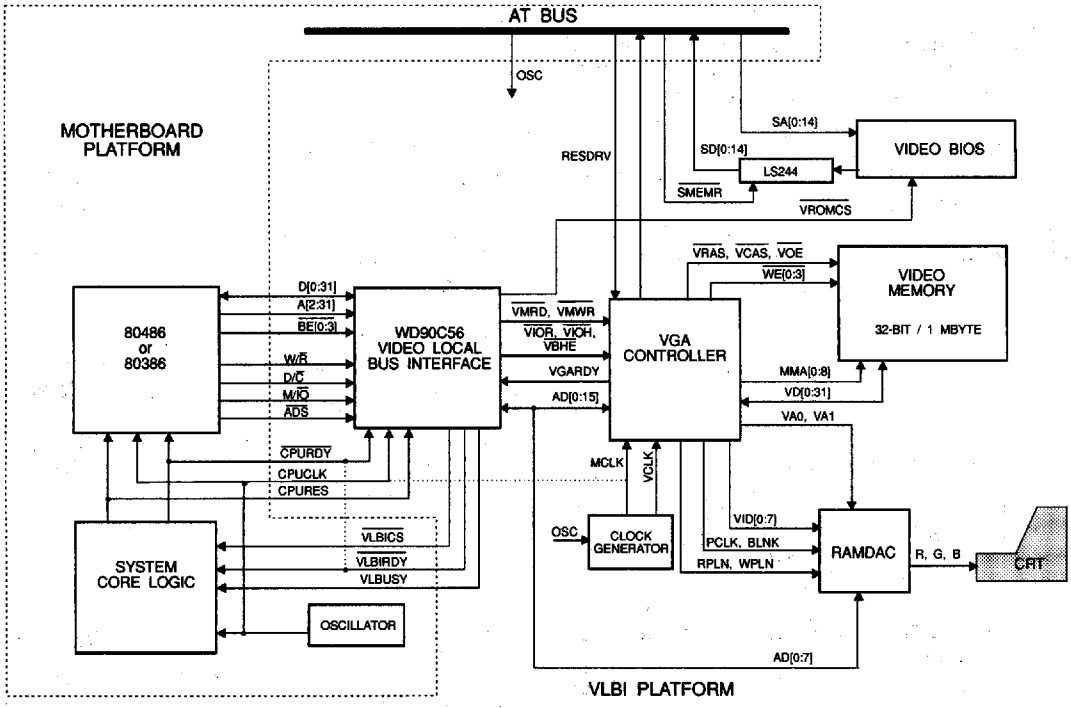

FIGURE 2-2. VLBI SYSTEM BLOCK DIAGRAM

see all writes to the RAMDAC and capture the data for emulation modes.

In systems where the AT bus contains write buffers the VLBUSY signal from the VLBI is used to delay the system READY signal being returned to the CPU by the write buffer logic. The READY is gated by the VLBUSY to avoid coherency problems.

2.3 VGA WRITE BUFFER

There is one level of 32-bit write buffer. This is the default. For 486 applications with multiple Bus Masters, there may be overruns due to insufficient time. This can be caused by a read from a CPU to the VGA when the write buffer is full. This is avoided by asserting the BOFF signal if there is a Hold request to the 486 thus making the 486 retract its last cycle. This option is disabled by setting bit 2 of 2DF6. The default is the BOFF signal asserted when the buffer is full and there is a Hold request.

2.4 VLBI DATA TRANSFER MODE

2.4.1 Direct Transfer Mode

The Direct Transfer mode can be invoked on either 16-bit (default) or 32-bit VGA interfaces. The 16-bit transfers are exactly like the normal 16-bit transfers on an AT bus.

In 32-bit Direct Transfer mode, there are four byte enables provided to the VGA. They are in the form of AD0/BB0, VBHE/BBE1, AD1/BBE2 and VBE3/BBE3.

In either case the protocol is the same. The VNCMD signal is asserted after the address and then the VLBI waits for the VGA RDY signal from the VGA to terminate the current cycle. The procedure is repeated again for a new cycle.

The VLBI is designed to work with 16-bit and 32-bit VGAs. At power up the default is a 16-bit interface. The software changes modes by writing to registers. See Register Summary Table.

2.5 LAPTOP SUPPORT

The VLBI in conjunction with the WD7710/7910 fully supports Laptop features. It also supports the full range Laptop features when interfaced to the WD86C10.

There are three special features that are supported in the WD7600/7700 family. These are as follows:

- Suspend
- Processor Power-Down
- Stop clock

2.5.1 Suspend

In Suspend, the DC power is removed to all devices except the WD7600 core chip set. In this mode the VLBI's power is also removed. Prior to removal of power, the CPU interrogates the VLBI BUSY flag to ensure that the VLBI is idle before invoking suspend.

On resume, the power is restored to the VLBI along with the rest of the system. This routine is identical to the power up routine from a cold start.

For Laptop VGAs like the WD90C26, the Data (SD 15:0) will be on the AD bus and the address (SA 15:0) will be on the VD bus. This is determined at power up on interrogation of the LA20 pin.

2.5.2 Processor Power-Down and Clock Stop

In Processor Power-Down, the DC power is removed from only the processor and co-processor. The rest of the system is in quiescent mode, expending very little power. In this mode, the CPU interrogates a BUSY flag (Bit 0: @ address 2DF7) provided by the VLBI. If active, this means that the VLBI is still involved in a transfer with the VGA and that it is not ready to be put to sleep or suspended. If the BUSY flag is inactive, the VLBI is ready to be put to sleep and the CPU can do so by setting the Sleep flag in the VLBI. Once the sleep flag is set, the VLBI disables all processor interface inputs including the incoming clocks. At this stage, the VLBI awaits the assertion of the PROC PWRDN signal from the external logic. On receipt of the PROC PWRDN signal, the VLBI

drives the PD bus low to prevent it from floating during sleep.

On coming out of sleep, the VLBI is awakened by the negation of the PROC $\overline{\text{PWRDN}}$ signal followed by the processor interface input clocks and ultimately by the CPURES signal. At the end of this sequence, the VLBI is once again ready for more VGA transfers.

On Clock Stop, the procedure is similar except there is no assertion of the Sleep Flag or the PROC $\overline{\text{PWRDN}}$ signal. Instead, the CPU interface clock from either the WD76C10A or the WD7710 is reduced in frequency or stopped completely.

The reversal into the operating mode is completely transparent to the VLBI.

2.6 VLBI DUAL DISPLAY MODE

The VLBI supports a second display adapter card, which can be either a Monochrome card (MDA), a Color Graphic Card (CGA), or another Video Graphics Array card (VGA), while residing on the local bus.

There are two read/write bits (5,6) assigned at address 2DF4 which indicate whether there is a secondary display in the system. Since, the local VLBI/VGA and secondary card share the same addresses for several I/O writes, these accesses are passed to the VLBI/VGA as well as to the system bus. The VLBUSY signal is generated in all these accesses. The system designer is responsible for assigning two independent memory areas to the VLBI/VGA and the secondary display adapter, so that the individual display memories can be independently read and written.

The following table defines the various configurations:

I/O PORT	VLBICS-	VLBUSY
03D0-03DF	No, if bits 6,5=11. (System Bus CGA is enabled) Else, Yes	Yes, if bits 5,6=11 for IOWs. Else,No.
03B0-03BF	No, if bits 6,5=10 Else, Yes. System bus MDA enabled	Yes, if bits 6,5=10 for IOWs Else, No
03C0-03C2 03C4-03C5 23C0-23C7 03CA-03CF	Yes,always	No
46E8,56E8, 66E8, 76E8, 03C3, 0102	Yes for IOWs Yes for IORs	No for IOWs. No for IORs.
03C6-03C9 (for dual RAMDAC)	No for IOWs Yes for IORs	Yes for all IOW's. No for IORs

Notes:

1. I/O decode control register; R/W, @ I/O port: 2DF4 bits 5,6.

BIT5	BIT6	CGA	MDA	VLBI
0	0	Dis	Dis	En
0	1	Dis	En	En
1	0	Dis	Dis	En
1	1	En	Dis	En

Dis=disable
En=enable

2. VLBUSY signal should be used to disqualify the RDY signal from the core logic to prevent these write cycles from finishing prior to the VLBI finishing.

3. When $\overline{\text{VLBICS}}$ is not generated for the VGA I/O operation, the cycles are passed to the core logic. However, the VLBI still responds and lets the core logic terminate these cycles. Under no circumstances does the VLBI generate read cycles when the $\overline{\text{VLBICS}}$ signal is not generated.

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2.7 CONFIGURING THE VLBI

At power up, the latched upper two bit address lines LA19:18 are used as inputs. By lightly pulling up or down with resistors, the user is able to configure the VLBI to one of the following modes.

Alternatively, the user can configure the VLBI by making the BIOS setup these parameters and writing to the appropriate registers. See the Register Summary Table.

LA19	LA18	MODE
1	1	AT style
1	0	Reserved
0	1	Reserved
0	0	Reserved

The LA19 and LA18 lines are internally latched by $\overline{\text{RESET}}$ going high and the mode is configured and preserved. Shortly after $\overline{\text{RESET}}$ going high the LA19:18 lines are turned into permanent outputs.

Similarly, LA17 is used to either use the VMCLK or internal CPU CLK for the VGA interface logic.

LA7	VGA I/F CLK
1	VMCLK
0	CPU CLK

Similarly, LA16 is used to configure the pin $\overline{\text{RDYIN}}$ as input for terminating cycles by the VLBI or to ignore that input when terminating cycles.

LA16	NRDYIN
1	Default - ignore
0	Terminate on valid low

LA20	LAPTOP
1	Laptop mode
0	Desktop mode

The initial condition of the LA20 to LA16 line is reflected in a register which is readable by the CPU at the I/O port address 2DF5.

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REG ADDR PORT	BIT	DESCRIPTION
2DF5	7	LA21
2DF5	6	LA20
2DF5	5	LA19
2DF5	4	LA18
2DF5	3	LA17
2DF5	2	LA16
2DF5	1	VD22*
2DF5	0	Reserved

* Async RDY, hardware configurable -VD22

On power up, the VLBI interrogates the CPU config pin, to tell if it is in 386 or 486 mode. If the CPU config pin is low, the VLBI assumes 386 mode. If the CPU config is high, the VLBI assumes 486 mode. The CPU config pin has an internal pull up resistor.

Similarly the VMCLK config pin is interrogated at power up to determine whether an external source is driving it. In the absence of an external clock, the VLBI should be set up in synchronous mode.

To distinguish between 386SX and 386DX, the byte enable $\overline{BE3}$ is inspected. If $\overline{BE3}$ is high, then the CPU is assumed to be a 386SX.

CLK ARRANGEMENT (AFTER INITIALIZATION):				
CASE	CLK 2386	CLK 486	VMCLK	MODE
1	IN	NC	NC	386
2	IN	*	IN	386**
3	NC	IN	NC	486
4	NC	IN	IN	486**

*Either input or no connect (NC)
**Asynchronous

Notes:

Case 1: CLK2386 is divided by 2 and is used internally.

Case 2: This is asynchronous mode. VMCLK is a different frequency and the CLK486 can be either input or a no connect (NC).

Case 3: The 486 clock is the input to the CLK486 pin and is used internally.

Case 4: This is asynchronous mode. VMCLK is a different frequency and the CLK486 is an input.

Cases 1 and 3 can also function with a different clock (high frequency greater than or equal to 50 MHz) on the VGA MEMCLK. In these cases, the pin VD22 should either be pulled up at power up or Bit 1 of register 2DF5 should be set to a 1 by the software. Also Bit 1 of 2DF4 should be set to 1. See the Clock Scheme section.

2.7.1 Hardware Configuration

Most timing parameters are made programmable; however, their default values are preset by either pulling up or down VD bus pins with resistors. This arrangement eliminates using different BIOS PROMs for different CPU speeds, etc. These pre-settings can be overridden by writing software to the appropriate registers.

See Register Summary Table in the "Register Description" section.

PIN	REG	BITS	FUNCTION
VD16	2DF0	0	VIOW- H/L 2-5 clocks
VD17	2DF0	1	VIOW- H/L 5 clocks if pulled up
VD18	2DF0	2	VIOR- H/L 2-5 clocks
VD19	2DF0	3	VIOR- H/L 5 clocks if pulled up
VD20	2DF0	5	VLBI EN/DIS EN if pulled up
VD24	2DF1	0	VMRD- L
VD25	2DF1	1	VMRD- L 2-5 clocks
VD26	2DF1	2	VMRD- H 5 clocks if pulled up
VD27	2DF1	3	VMRD- H
VD28	2DF1	4	VMWR- L
VD29	2DF1	5	VMWR- L 2-5 clocks
VD30	2DF1	6	VMWR- H 5 clocks if pulled up
VD31	2DF1	7	VMWR- H

TABLE 2-1. HARDWARE REGISTERS

Note: It is preferred that the VLBI is disabled at power-up and later is enabled by the software. In this case, Pin VD20 should be pulled low with a resistor.

2.7.2 Software Configuration

In addition to configuring the VLBI by means of pull/down down resistors, there are several modes and parameters that can be invoked by software at power up. See Register Summary section for complete details.

MODE	REG	BITS	FUNCTION
16/32 Direct transfer	2DF4	0	L - 16 bit, H - 32 bit VGA Interface
Sync	2DF4	1	L - Async Mode Default
Future1	2DF4	2	L -Disabled Default
Future2	2DF4	3	L - Disabled Default
Laptop Sleep Mode		4	L - Disabled Default
*	2DF4	5:6	See below
End Pos/Neg	2DF0	6	0 Pos default
Start Pos/Neg	2DF0	7	0 Neg default

TABLE 2-2. CONFIGURE USING SOFTWARE REGISTERS

* 2DF4, Bits 5 and 6 are used as follows:

BIT6	BIT5	CGA	MDA	VLBI
0	0	Dis	Dis	En
0	1	Dis	Dis	En
1	0	Dis	En	En
1	1	En	Dis	En

Dis=disable
En=enable

At power-up all register bits are reset to zero.

MODE	REG	BITS	FUNCTION
$\overline{\text{READY}}$ Assertion	2DF6	1:0=00 01 10 11	2 wait states 1 wait states 0 wait states Reserved
BOFF#	2DF6	2	0 - Default $\overline{\text{BOFF}}$ asserted 1 - No assertion of $\overline{\text{BOFF}}$
BUSY	2DF7	0	VLBI BUSY - default 0 not busy.

TABLE 2-3. ADDITIONAL SOFTWARE REGISTERS TO CONFIGURE

2.8 PROGRAMMING THE VLBI CHIP

The VLBI chip shadows all necessary configuration programmable registers for the Western Digital VGA chip, so that the VLBI knows about all IO address space and all memory space occupied by the VGA chip. All writes to programmable configuration registers of the VGA chip are captured by the VLBI chip and are transparent to the software. These configurations include the start address of the VGA RAM and the size of the RAM, the type of CPU (16- or 32-bit), and other parameters.

The VLBI chip interprets the CPU Bus cycles for the VGA chip and converts the CPU address and Data Bus to a multiplexed 16-bit AD0:15 bus for the VGA chip. For the highest possible performance while accessing the VGA, the interface between the VGA chip and the CPU can be configured in synchronous or asynchronous mode. The asynchronous mode is suitable when the CPU is running at a low frequency. In this case the VLBI's VMCLK can be connected to the VGA's MEMCLK (at 45 MHz). This will increase the rate of data transfer between the VGA and the VLBI. However, the interface can be configured to synchronous mode as well, to increase performance at higher frequencies. In this case the VMCLK is left unconnected.

All three devices (CPU, VLBI, and VGA) **must** operate on one clock. This mode is known as the synchronous mode. See figure below.

For this mode, CLK486 **must** be connected to the VGA chip MEMCLK pin. It is necessary to use the same clock to the VGA interface in the VLBI and to MEMCLK in the VGA device. This assures that the VGA and VLBI are always synchronous. Similarly the CPU interface in the VLBI and the CPU use the same clock to maintain synchronous operation.

In synchronous mode, yet another configuration is possible, for this mode, CLK486 can be asynchronous to the VGA MEMCLK, although the VLBI is configured in synchronous mode. This is possible because the WD90C30 and WD90C31 sample the VGA commands from the VLBI with the VGA MEMCLK.

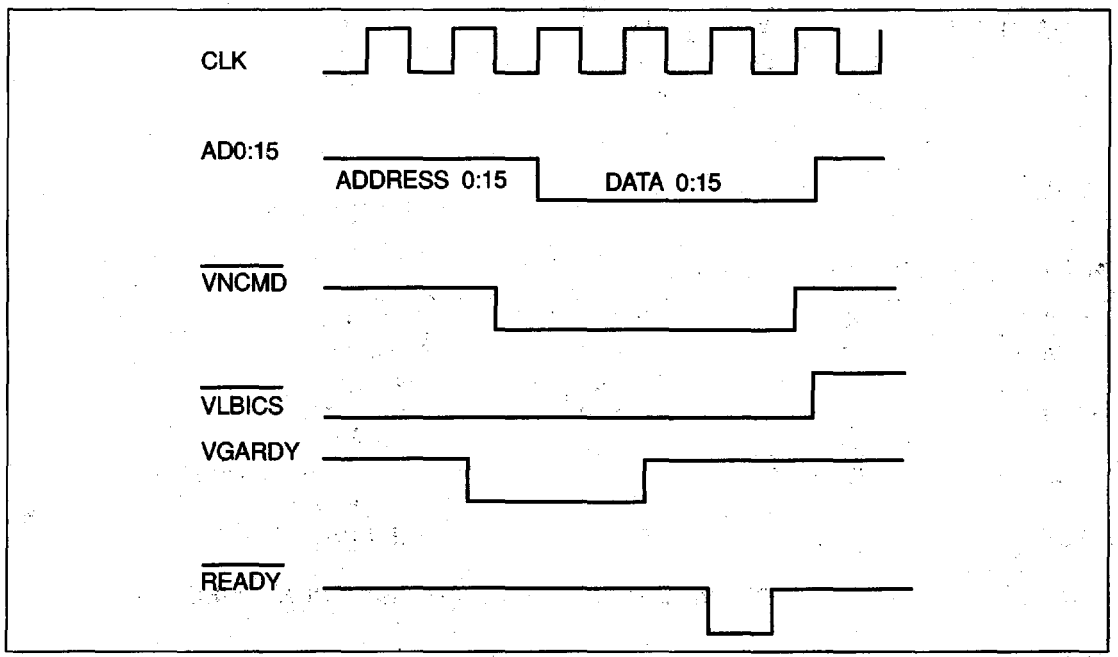

FIGURE 2-3. VLBI SYNCHRONOUS INTERFACE

For a Read cycle, the VLBI chip stops driving AD0:15 after generating VNCMD so that the VGA chip can drive the read data. The VNCMD is generated from the falling edge of CLK (programmable positive/negative start, and others. See timing diagram VLBI3). The VLBICS is valid after T1 but before the middle of T2 of CPUCLK. The VLBI chip stops driving the AD0:15 bus at the end of the CLK edge. If at the beginning of the next rising edge of the CLK and on every subsequent rising edge of the CLK, if the VGARDY is low, then the VNCMD is extended (for normal memory cycles only). When VGARDY is sampled high on the rising edge, the next CPUCLK is the last clock of the cycle. Therefore, the VLBI will drive READY low to complete the CPU Bus cycle. This mode is known as synchronous mode.

The VLBI is designed to accomodate various configurations brought upon by different CPU speeds and different VGA memory bandwidths.

For 32-bit mode access to the VGA, both the VLBI and the VGA chip (next generation) are put in 32-bit access mode. The VLBI chip drives the address on AD0:15 and LA16:21. For read modes, it takes data on AD0:15 and VD16:31 and drives the signal onto the CPU data bus.

For 32-bit write mode, the address is driven on AD0:15 and LA16:21. The 32-bit data is driven on AD0:15 and VD16:3. See the 32-bit VGA figure below.

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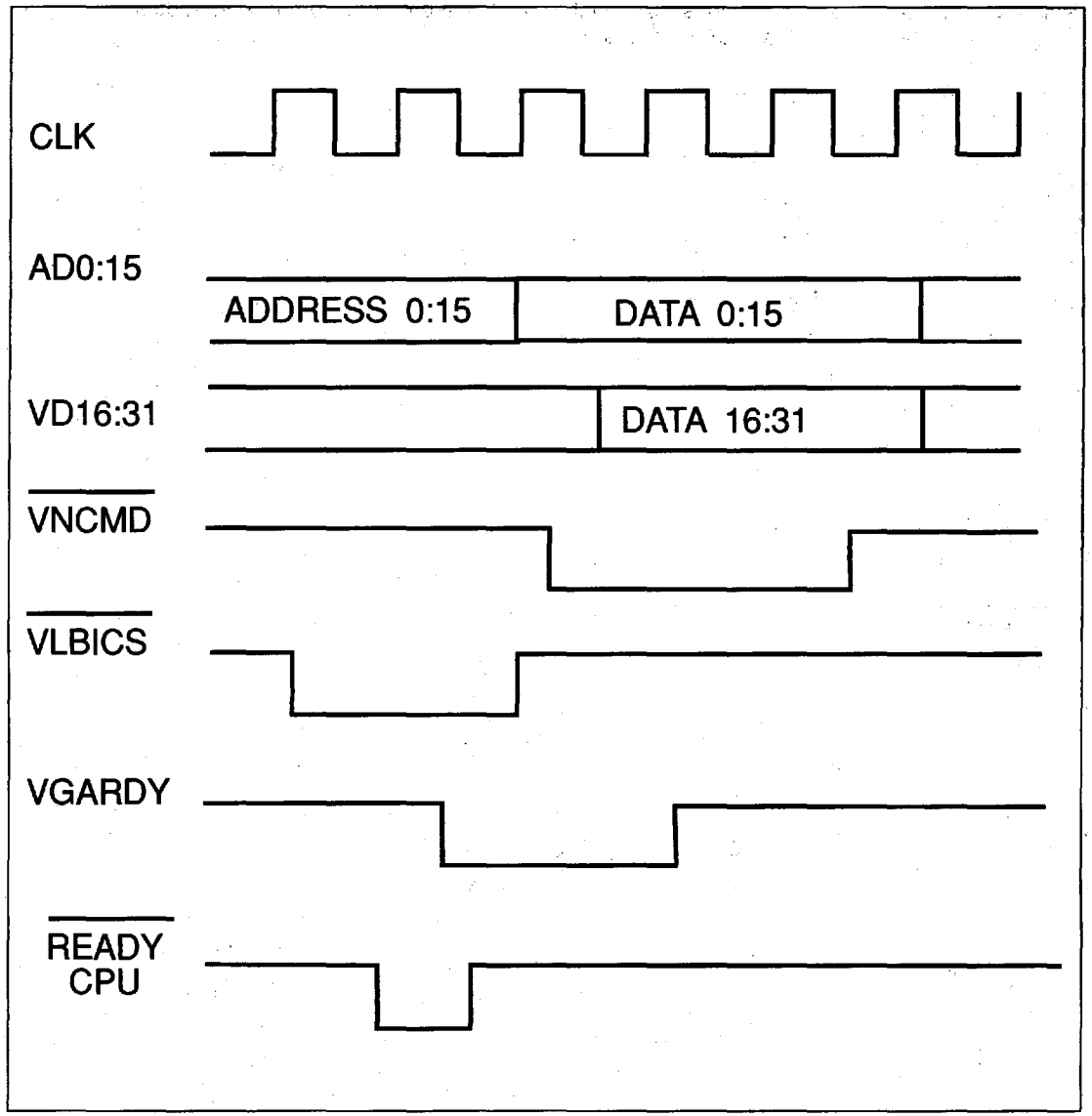

FIGURE 2-4. 32-BIT ACCESS TO VGA (WRITE CYCLE)

3.0 INTERFACES

3.1 VLBI INTERFACE FOR INTEGRATED CACHE CONTROLLER BASED SYSTEM

The VLBI chip is designed to interface with various CPU and cache and core logic chip sets to improve VGA performance in Intel 80x86 based high end PCs. The VLBI and the system core logic monitor the $\overline{ADS}$, PA2:31 and bus status information (M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$) from the CPU in the T1 cycle. The VLBI generates the $\overline{VLBICS}$ signal for all address references it is going to satisfy. The timing of the $\overline{VLBICS}$ is such that it can be sampled by the end of the T2 cycle. The $\overline{VLBICS}$ can be directly connected to the core chip sets.

3.2 VLBI INTERFACE WITH STAND-ALONE CACHE CONTROLLER BASED SYSTEMS

For a system which has a stand-alone cache controller, the VLBI chip is connected to $\overline{ADS}$ A2:31 and M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$ from the CPU. The VLBI chip monitors the CPU cycle and generates the $\overline{VLBICS}$ signal for access to its address space.The Cache controller generates $\overline{SADS}$ for non-cachable cycles which is suppressed by external PAL logic before going to the core logic chip set, so that the core logic chip set does not generate system bus cycles.

3.3 PROCESSOR INTERFACE

The VLBI supports both 386 and 486 processors. The 386 is only supported in non-pipeline mode and the same is true for the 386SX. In 486 mode, the clock that drives the 486 processor also drives the VLBI. In 386 mode, since the 386 runs on CLK2, the VLBI is required to run on CLK2 as well. The CPURES signal is taken in by the VLBI for synchronizing the CPU access. The VLBI is capable of supporting 386 and 486 designs up to 33 MHz.

3.4 CLOCK SCHEME

When the CPU, VLBI, and VGA are operated synchronously the CPU, VLBI, and VGA must run from the same clock source, that is the same frequency/phase. In the case of a 486 design, the clock used by all three can be the same (CLK486) and the VLBI's VMCLK is left unconnected. The CLK486 in the VLBI is an input. The CLK2386 is also an input and should be left unconnected in 486 mode. The CLK486 is sourced by an external source, by discrete logic, or in the case of Western Digital's AT design it is sourced by the WD76C10A family of devices. **Bit 1 of 2DF4 must be set to 1.**

In the case of a 386 design, CLK2386 comes from the same source that provides the CLK2 to the 386 CPU. However, CLK486 is left unconnected.

In other applications, the VLBI VMCLK will be an input and is connected to the VGA MEMCLK. An external clock source drives both VGA MEMCLK and VLBI VMCLK and this clock is treated as completely asynchronous to the CPU interface clock both in 386 as well as 486 modes.

On power up the VLBI assumes the asynchronous mode and can be changed to synchronous mode by software.

The VLBI VMCLK can be left unconnected and the VGA MEMCLK can have a higher frequency than the CPU. For example, CPUCLK=33 MHz; VGA MEMCLK=50 MHz. For maximum performance, set the internal VLBI logic to synchronous mode, i.e., Bit 1 of 2DF4=1. Also VD22 should either be pulled up at power-up or Bit 1 of 2DF5 should be set to 1.

4.0 SIGNAL DESCRIPTION

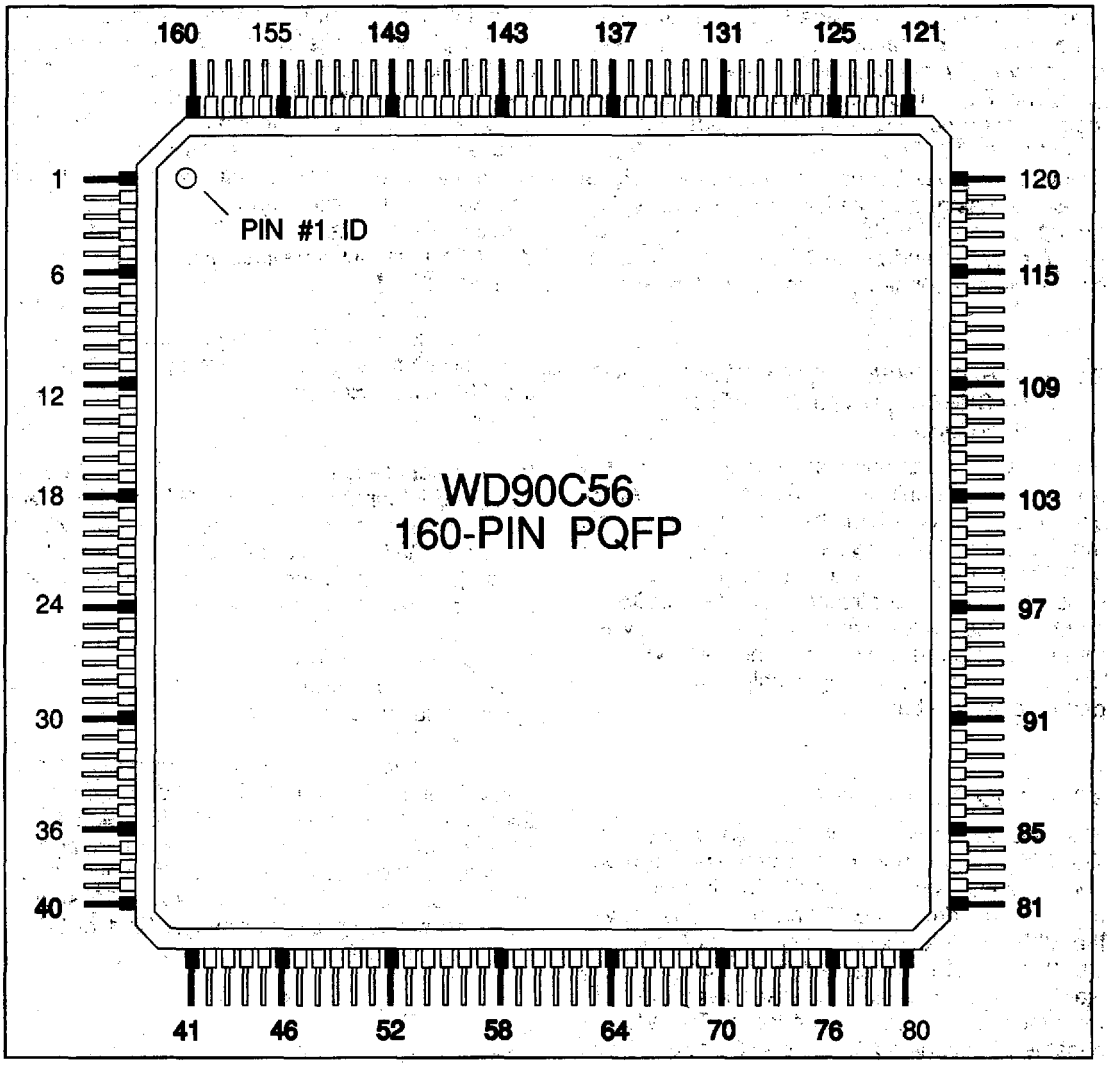

FIGURE 4-1. 160-PIN PACKAGE

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PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-GND	41-A14	81-GND	121-GND
2-CLK486	42-$\overline{ADS}$	82-VMCLK	122-AD14
3-A28	43-$\overline{BE0}$	83-VGARDY	123-AD13
4-A21	44-$\overline{BE1}$	84-$\overline{VIOR}$	124-AD12
5-A20	45-$\overline{BE2}$	85-$\overline{VIOW}$	125-AD11
6-$\overline{BOFF}$	46-$\overline{BE3}$	86-CPU config	126-AD10
7-A19	47-W/$\overline{R}$	87-$\overline{VBHE}$	127-AD9
8-A18	48-D/$\overline{C}$	88-RESRV9	128-GND
9-VCC	49-M/$\overline{IO}$	89-LA16/VA0	129-AD8
10-GND	50-GND	90-GND	130-RESRV4
11-PD6	51-A15	91-LA17/VA1	131-AD7
12-PD7	52-A16	92-LA18/VA2	132-AD6
13-PD8	53-A17	93-LA19	133-AD5
14-PD9	54-A7	94-RESRV7	134-AD4
15-PD10	55-A8	95-RESRV8	135-AD3
16-PD11	56-A9	96-$\overline{VMWR}$	136-VCC
17-PD12	57-A10	97-$\overline{VMRD}$	137-AD2
18-PD13	58-A11	98-LA20	138-AD1
19-GND	59-A12	99-LA21	139-GND
20-VCC	60-VCC	100-VCC	140-TEST
21-PD14	61-$\overline{VLBICS}$	101-VD31	141-AD0
22-PD15	62-A13	102-VD30	142-PD31
23-PD0	63-A6	103-VD29	143-PD30
24-PD1	64-A5	104-VD28	144-PD29
25-PD2	65-A4	105-VD27	145-PD28
26-PD3	66-A3	106-VD26	146-PD27
27-PD4	67-VLBUSY	107-VD25	147-PD26
28-PD5	68-A2	108-VD24	148-PD25
29-HREQ	69-$\overline{READY}$	109-AD15	149-PD24
30-GND	70-GND	110-GND	150-GND
31-PD16	71-A30	111-VD23	151-PD23
32-PD17	72-A31	112-VD22	152-PD22
33-PD18	73-CPURES	113-VD21	153-A23
34-PD19	74-VCC	114-VD20	154-A24
35-PD20	75-$\overline{RESET}$	115-VCC	155-A25
36-PD21	76-$\overline{RDYIN}$	116-VD19	156-A26
37-RESRV1	77-$\overline{PWRDWN}$	117-VD18	157-A27
38-RESRV5	78-$\overline{VBE3}$	118-VD17	158-RESRV2
39-RESRV6	79-$\overline{VBROM}$	119-VD16	159-CLK2386
40-A22	80-A29	120-VCC	160-VCC

TABLE 4-1. WD90C56 PIN ASSIGNMENTS

PIN	MNEMONIC	I/O	DESCRIPTION
			VLBI INTERFACE
68, 66-63, 59-54, 62,41 53-51, 8-7, 5-4, 40, 157-153, 3, 80, 72-71	A2:31	I	**CPU Address Bus** CPU Address Bus Input for decoding VGA address map decodes. Use only A2:23 for 386SX.
43-46	$\overline{BE0}$-$\overline{BE3}$	I	**Byte Enable 0 thru 3** Active low byte enable from the CPU or BLE, BHE, and A1 for the 386SX CPU. If the trailing edge of $\overline{RESET}$ BE3 is low, then a 16-bit SX CPU mode is assumed. If high, a 32-bit 386 or 486 mode is assumed.
42	$\overline{ADS}$	I	**CPU Address Strobe** From 386/486.
	PD0:31	I/O	**CPU Data Bus** CPU DATA BUS 32-bits. Uses only 16-bits in the case of 80386SX.
69	$\overline{READY}$	O	**Ready** The Ready signal of the CPU. The pin is driven high for 5 ns, then is left tristated and is driven low by the VLBI only if it is responding to a CPU cycle.
141, 138, 137, 135-131, 129, 127-122, 109	AD0:15 [AD0/$\overline{BBE0}$]	I/O	**Address and Data Bus** The 16-bit Multiplexed Address and Data Bus to the VGA chip WD90C30, and others. In 32-bit mode, AD0 and AD1 are the [AD1/$\overline{BBE2}$] output byte enable 0 and 2 to the VGA.
78	$\overline{VBE3}$	I/O	**Valid Byte Enable** Indicates to a 32-bit VGA a valid high byte in a 32-bit word. Active low.

TABLE 4-2. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
119-116, 114-111, 108-101	VD16:31	I/O	**High Data** The upper 16-bits of the data bus to the VGA. For VGA chips which have a 32-bit data interface, these pins carry the upper word and AD0:15 carry the lower word. They can carry either light pulldowns or pullups to configure various parameters at power on.
83	VGARDY	I	**VGA Ready** Active high ready signal from the VGA chip. For access to the VGA
87	$\overline{\text{VBHE}}$ [$\overline{\text{BBE1}}$]	O	**VGA Byte High Enable** Output during CPU access to the VGA. In 32-bit modes, this pin plays a double role because it indicates to the VGA a high byte for a low word.
97 96 84 85	$\overline{\text{VMRD}}$ $\overline{\text{VMWR}}$ $\overline{\text{VIOR}}$ $\overline{\text{VIOW}}$	O	Active low commands to the VGA chip. Their definitions are similar to the AT bus signals. The commands can be made to start and finish at rising or falling edges of the clock. These commands are collectively referred to as $\overline{\text{VNCMD}}$.
140	TEST	I	**Test** In conjunction with PD0, PD1, and NRESET, a positive edge on this input will pull the VLBI into various modes; i.e. tristate, I/0 map, and others.
61	$\overline{\text{VLBICS}}$	O	**VLBI Chip Select** Active low signal indicating that the current CPU cycle will be satisfied by the VLBI and the system logic chip set should ignore the cycle. This line is connected to the bidirectional signal AF32 of the Chips and Technology Peak chip set. Or it can be connected to the NLDS32 signal for WD86C10 based Western Digital designs. This line is driven only if the current cycle is to be serviced by the VLBI. Otherwise the line is tristated.
29	HLDREQ	I	**Hold Request** The output from the core logic chip set to the processor to indicate that the system bus request is received by either REFRESH, DMA, or a MASTER signal. The processor acknowledges by asserting HOLD ACKNOWLEDGE after relinquishing the bus.
2	CLK486	I	**Clock486** The input interface for the 486 CPU clock with a 486 CPU. In 386 this is a no connect (NC).
159	CLK2386	I	**Clock2386** The input interface for the 386DX or 386SX Mode. A clock on this pin assumes 386 mode (386 CPU clock).

TABLE 4-2. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
82	VMCLK	I	**VLBI VGA Clock** or left unconnected This is normally connected to VGA MEMCLK. If VGA MEMCLK is different from the 486CLK, the VLBI functions in asynchronous mode.
73	CPURES	I	**CPU Reset** The synchronous reset to the CPU used to generate internal CLK for maintaining phase of CLK2 in sync with 386DX, 386SX CPU.
75	$\overline{\text{RESET}}$	I	**Reset** Active low system reset (power on). Various parameters as well as the mode the VLBI assumes is preset on its trailing edge.
89, 91-93, 98-99	LA16:21	I/O	Upper 6-bits of the 22-bit address to the VGA chip. At power-up these bits are used as inputs to tell which mode (AT, etc.) should be selected. Pins LA18:16 contain the low order address A2:0 for the RAMDAC I/O cycles - these perform the same function as the AT bus SA2:0.
6	$\overline{\text{BOFF}}$	O	**BOFF** Connects directly to the 486 BOFF# pin. When active, it makes the 486 CPU retract its last cycle and enables the other masters to intervene and obtain the local bus, generated by a read cycle for the VGA when the write buffers are full and HLDREQ is active.
67	VLBUSY	O	**VLBI Busy** Output during RAMDAC or dual display I/O cycles, this signal is the result of the RAMDAC or dual display I/O decode. Once asserted it remains asserted until the cycle is captured by the VLBI. The VLBUSY signal is also generated for cycles that are common yet meant for CGAs or MDAs that reside on the system bus. Active high signal.
77	$\overline{\text{PWRDWN}}$	I	**Power Down** This signal is active low. When active it drives the PD bus low thus preventing the PD bus from floating during sleep.
79	$\overline{\text{VBROM}}$		**Video BIOS ROM** This pin provides the decode of the CPU address C0000-CFFFF to enable the video BIOS ROMs to be used with the VLBI. Active low.
76	$\overline{\text{RDYIN}}$	I	This pin is used for synchronizing with CPU cycles.
86	$\overline{\text{CPU config}}$	I	Processor select pin. High=486,low=386.

TABLE 4-2. SIGNAL DESCRIPTION (CONTINUED)

Note:
1. All clock inputs have internal pullups.

2. Address inputs PA2 to PA31 are not pulled up internally therefore, unused Address inputs in a 16-bit CPU environment should be externally terminated. This minimizes power dissipation in Laptop environment.

5.0 REGISTER DESCRIPTION

Some of the programmable register descriptions are included in Section 2, "Architecture." Additional register information is in Appendix A.

The VLBI has a lock mechanism to protect its registers from being accidentially tampered with by third party programs.

The address to unlock these is A875hex and the data is AChex. Once unlocked, the 2DF0hex series address can be accessed.

To lock data other than AChex is written to the address A875hex.

$\overline{\text{VLBICS}}$ is generated for all such accesses, exclusive of the address A875hex.

Once locked, any access requests to the 2DF0 series registers do not produce $\overline{\text{VLBICS}}$. Therefore, these access requests go to the AT bus.

The following table is a summary of the VLBI registers.

ADDRESS	DEFAULT VALUES	PROGRAM SIGNAL	DESCRIPTION
		LOCKED	
2DF0[0] 2DF0[1]	1 1	VD[16] VD[17]	Determines $\overline{\text{VIOW}}$ high/low duration (2 to 5 clk)
2DF0[2] 2DF0[3]	1 1	VD[18] VD[19]	Determines $\overline{\text{VIOR}}$ high/low duration (2 to 5 clk)
2DF0[4]	1	BIOS	Determines pulse width of RAMDAC VIOW command (0=9 clk; 1=18 clk) Also high time for $\overline{\text{VIOR}}$ during RAMDAC (0=9 clk; 1=18 clk)
2DF0[5]	1	VD[20]	VLBI enable control (0= disable)
2DF0[6] 2DF0[7]	1 1	BIOS BIOS	End VGA read cycle on pos/neg edge (1=pos) Start VGA read cycle on pos/neg edge (1=neg)
2DF1[0] 2DF1[1]	1 1	VD[24] VD[25]	Determines $\overline{\text{VMRD}}$ low duration (2 to 5 clk)
2DF1[2] 2DF1[3]	1 1	VD[26] VD[27]	Determines $\overline{\text{VMRD}}$ high duration (2 to 5 clk)
2DF1[4] 2DF1[5]	1 1	VD[28] VD[29]	Determines $\overline{\text{VMWR}}$ low duration (2 to 5 clk)
2DF1[6] 2DF1[7]	1 1	VD[30] VD[31]	Determines $\overline{\text{VMWR}}$ high duration (2 to 5 clk)
2DF2[7:0]	0x00	BIOS	Compares with A[31:24] to decode video memory
2DF3[7:4]	0x0	BIOS	Compares with A[23:20] to decode video memory
2DF3[3:0]	0xF	BIOS	Video memory decode enable 0000=decode A[31:24] 1000=decode A[31:23] 1100=decode A[31:22] 1110=decode A[31:21] 1111=decode A[31:20]
2DF4[0]	0	BIOS	VGA interface data width (0=16 bit)

TABLE 5-1. REGISTER SUMMARY

ADDRESS	DEFAULT VALUES	PROGRAM SIGNAL	DESCRIPTION
2DF4[1]	0	BIOS	CPU/VGA are async/sync clk (0=async)
2DF4[2]	0	BIOS	Reserved
2DF4[3]	0	BIOS	Reserved
2DF4[4]	0	BIOS	VLBI enters Sleep Mode (0=disable)
2DF4[6:5]	00	BIOS	Enable Dual Display CGA MDA 00= dis dis 10= dis en 01= dis dis 11= en dis
2DF4[7]	0	BIOS	Dual RAMDAC (0=disable=default)
2DF5[0]	0	---	Reserved
2DF5[1]	1	VD[22]	Async/sync VGARDY (1=async)
2DF5[2]	1	LA[16]	Terminate VLBI cycle when $\overline{\text{RDYIN}}$ low (1=terminate regardless of $\overline{\text{RDYIN}}$)
2DF5[3]	1	LA[17]	Use CPUCLK or VMCLK for VGA interface (1=use VMCLK)
2DF5[4] 2DF5[5]	1 1	LA[18] LA[19]	System interface selection 11=AT bus 10=reserved 01=reserved 00=reserved
2DF5[6]	1	LA[20]	Laptop/desktop mode select (1=laptop)
2DF5[7]	1	LA[21]	Reserved
2DF6[1:0]	00	BIOS	Number of wait states 00=2 wait states 01=1 wait state 10=0 wait state 11=invalid code
2DF6[2]	0	BIOS	Use $\overline{\text{BOFF}}$ (0=assert $\overline{\text{BOFF}}$)
2DF6[3]	0	BIOS	Reserved
2DF6[4] 2DF6[5]	0 0	BIOS BIOS	End VGA write cycle on pos/neg edge (0=pos) Start VGA write cycle on pos/neg edge (0=neg)
2DF7[0]	0	BIOS	VLBI ready to sleep (0=ready); Read only
VGA MIRROR			
03C4[4:0]	0x00	BIOS	Index to 03C5
03C5.11[1:0]	00	BIOS	8- or 16-bit I/O control
03CE[3:0]	0x0	BIOS	Index to 03CF
03CF.06[3:2]	00	BIOS	IBM VGA memory mapping
03CF.0A[2]	0	BIOS	16-bit memory cycle
03CF.0B[5:4]	00	BIOS	Control a [A19:0] decoding

TABLE 5-1. REGISTER SUMMARY (CONTINUED)

6.0 DC ELECTRICAL SPECIFICATIONS

6.1 MAXIMUM RATINGS

Maximum ratings; all voltages referenced to Vss.

Storage Temperature	0°C to 85°C
V_{CC}	5 volts ±5%

NOTE:
Stress above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to maximum rating conditions for extended periods may effect product reliability.

6.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows to the referenced pin.

Storage Temperature	0°C to 85°C
V_{CC}	5 volts ±5%

6.3 DC CHARACTERISTICS

F52-33-49

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	-0.3	0.8	V	All inputs except CLK2386, VMCLK
V_{IH}	Input High Voltage	2.2	V_{CC}+0.3	V	All inputs except CLK2386, VMCLK
V_{IL}	Input Low Voltage	-0.3	1.5	V	CLK2386, VMCLK
V_{IH}	Input High Voltage	3.7	V_{CC}+0.3	V	CLK2386, VMCLK
I_{LI}	Input Leakage Current	---	±10	µA	
V_{OL}	Output Low Voltage	---	0.45	V	
I_{OL}	Output Low Current	---	2.00	mA	LA(20:21), VD Bus
I_{OL}	Output Low Current	---	8.00	mA	PD Bus, AD Bus
I_{OL}	Output Low Current	---	24.00	mA	VLBUSY, $\overline{\text{READY}}$, $\overline{\text{VLBICS}}$*
I_{OL}	Output Low Current	---	8.00	mA	All other outputs
V_{OH}	Output High Voltage	---	2.4	V	
I_{OH}	Output High Current	---	2.0	mA	All outputs
I_{LO}	Output Leakage Current	---	±10	µA	
I_{CC}	Supply Current	---	100	mA	@ 25MHz
I_{CC}	Supply Current	---	130	mA	@ 33MHz
C_{IN}	Input Capacitance	---	15	pF	
C_{OUT}	Output Capacitance	---	15	pF	
C_{IN}	Clk Input Capacitance	---	15	pF	
C_{OUT}	Clk Output Capacitance	---	15	pF	
$C_{I/O}$	I/O Pin Capacitance	---	20	pF	

TABLE 6-1. DC CHARACTERISTICS

* $\overline{\text{VLBICS}}$ may require a strong pull-up resistor (470 ohm)

7.0 AC OPERATING CHARACTERISTICS

T-52-33-49

The following notes apply to all of the parameters presented in this section:

1. All units are in nanoseconds.

2. Temperature = 0°C to 70°C.

3. All timings are specified with the rising edge of CLK unless otherwise noted.

4. All timings are measured between 0.8 volts logic low and 2.2 volts logic high, unless otherwise noted.

7.1 TIMING FOR 33 MHZ CLOCK

SIGNAL	INPUT/OUTPUT	MIN	MAX	UNITS	CONDITIONS
AD Bus	AD Bus I/O at 30 pF	NA	NA		See Tables 7-6 and 7-7
LA Bus	LA Bus Output at 30 pF	NA	NA		
VD Bus	VD Bus I/O at 30 pF	NA	NA		
PD Bus	PD Bus I/O at 50 pF	4	14	ns	
$\overline{\text{VLBICS}}$	Output from $\overline{\text{NADS}}$ at 30 pF	---	20	ns	
*	Output at 30 pF	4	24	ns	
$\overline{\text{READY}}$	Output at 25 pF	13	16.5	ns	
VLBUSY (low)	Output at 30 pF	---	25	ns	from $\overline{\text{ADS}}$
VLBUSY (high)	Output at 30 pF	---	15	ns	from CLK
CLK 486	Input Frequency	---	33	MHz	
CLK2386	Input Frequency	---	66	MHz	
CLK2386	Rise/fall times	---	4	ns	CMOS
CLK486	Rise/fall times	---	3	ns	
CPURES	Setup time to CLK2386 @33MHz and @50 pF	7	---	ns	
CPURES	Hold time to CLK2386 @33MHz and @50 pF	2	---	ns	
**	Input setup time to CLK	11	---	ns	486/ref 486 clk
**	Input setup time to CLK	11	---	ns	386/ref 486 clk †
**	Input hold time to CLK	4	---	ns	486/ref 486 clk
**	Input hold time to CLK	4	---	ns	386/ref 486 clk †

TABLE 7-1. 33 MHZ CLOCK

* All other outputs: VBHE, $\overline{\text{VMRD}}$, $\overline{\text{VMWR}}$, $\overline{\text{VIOR}}$, $\overline{\text{VIOW}}$, and $\overline{\text{VBE3}}$

** CPU inputs: PA2:31, PD BUS, $\overline{\text{BE0}}$-$\overline{\text{BE3}}$/$\overline{\text{BLE}}$,$\overline{\text{BHE}}$,$\overline{\text{ADS}}$,M/$\overline{\text{IO}}$,D/$\overline{\text{C}}$ and W/$\overline{\text{R}}$

† Referenced to 486 clock or internal clock divided by two of clock2386, phase two

No.	PARAMETER	MIN	MAX	UNITS	CONDITIONS
1	Frequency	---	33	MHz	
2	Clock period	30	---	ns	
3	Clock high time	11	---	ns	0.8V
4	Clock low time	11	---	ns	0.8V
5	Clock fall time	---	3	ns	2V-0.8V
6	Clock rise time	---	3	ns	0.8V-2V

TABLE 7-2. 33 MHZ CLK486 SPECIFICATION

No.	PARAMETER	MIN	MAX	UNITS	CONDITIONS
1	Frequency	---	45	MHz	
2	Clock period	22.0	---	ns	
3	Clock high time	8.0	---	ns	2V
4	Clock low time	8.0	---	ns	0.8V
5	Clock fall time	---	3	ns	2V-0.8V
6	Clock rise time	---	3	ns	0.8V-2V

TABLE 7-3. 33 MHZ VMCLK INPUT (CMOS)

VMCLK ports is fabricated with CMOS buffers.

7.2 TIMING FOR 66 MHZ CLOCK

T-52-33-49

No.	PARAMETER	MIN	MAX	UNITS	CONDITIONS
1	Frequency	16	66	MHz	
2	Clock period	15	62.5	ns	
3	Clock high time	6.25	---	ns	2V
4	Clock low time	6.25	---	ns	2V
5	Clock high time	4.5	---	ns	3.7V
6	Clock low time	4.5	---	ns	0.8V
5	Clock fall time	---	4.0	ns	3.7V-0.8V
6	Clock rise time	---	4.0	ns	0.8V-3.7V

TABLE 7-4. 66 MHZ CLK2386 SPECIFICATION

7.3 VLBI CPU INTERFACE DIAGRAM

T-52-33-49

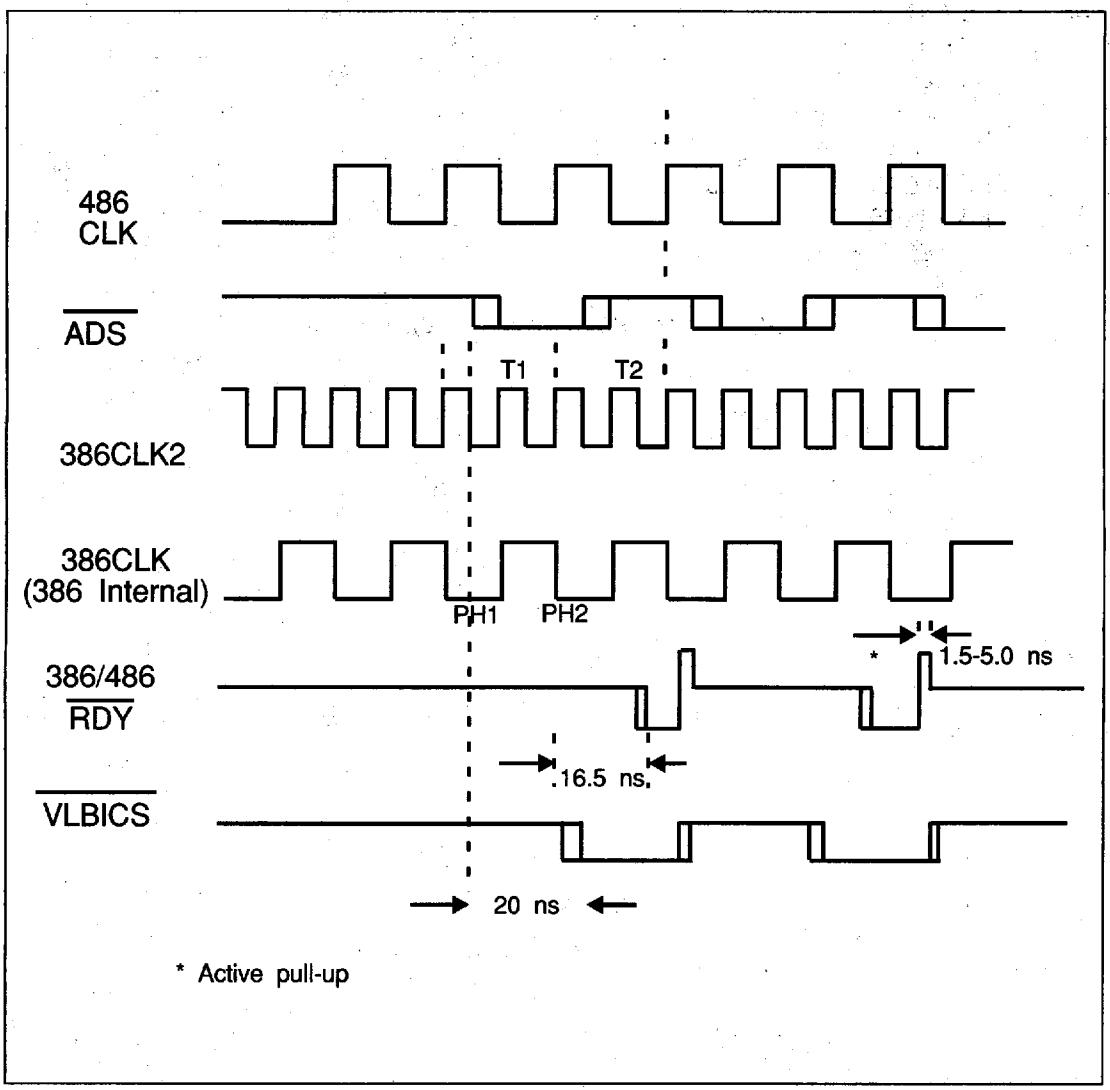

FIGURE 7-1. VLBI/CPU INTERFACE

T-52-33-49

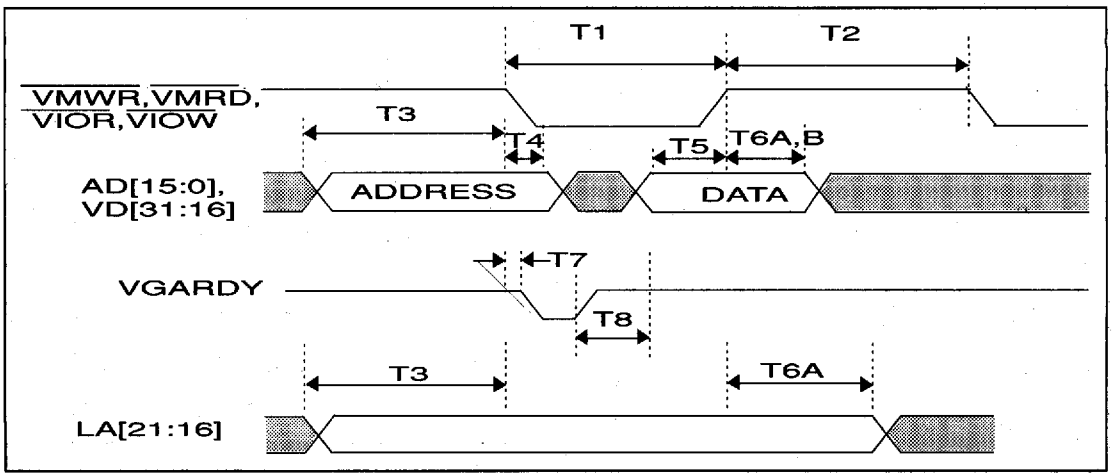

FIGURE 7-2. 33 MHZ COMMAND TIMING

No.	PARAMETER	MIN	MAX	UNITS
T1	CMD active low pulse width	1.5	5.5	VMCLK*
T2	CMD inactive high pulse width	1.5	5.5	VMCLK*
T3	Address set up to CMD active low	20	---	ns
T4	Address hold from CMD active low	10	---	ns
T5	Write data set up to CMD inactive high	20	---	ns
T6A	Write address/data hold from CMD inactive high	20	---	ns
T6B	Read data hold from CMD inactive high	10	25	ns
T7	RDY inactive from CMD low	---	15	ns
T8	Read data ready from RDY goes active high	---	10	ns

TABLE 7-5. 33 MHZ COMMAND

* The CMD pulse width is programmable. The 2 VMCLK CMD pulse width is defined for interfacing with the WD90C31 whose host interface and memory timing is generated by the VGA MEMCLK.

Note: VMCLK is equal to CPUCLK when Bit 1, 2DF4=1.

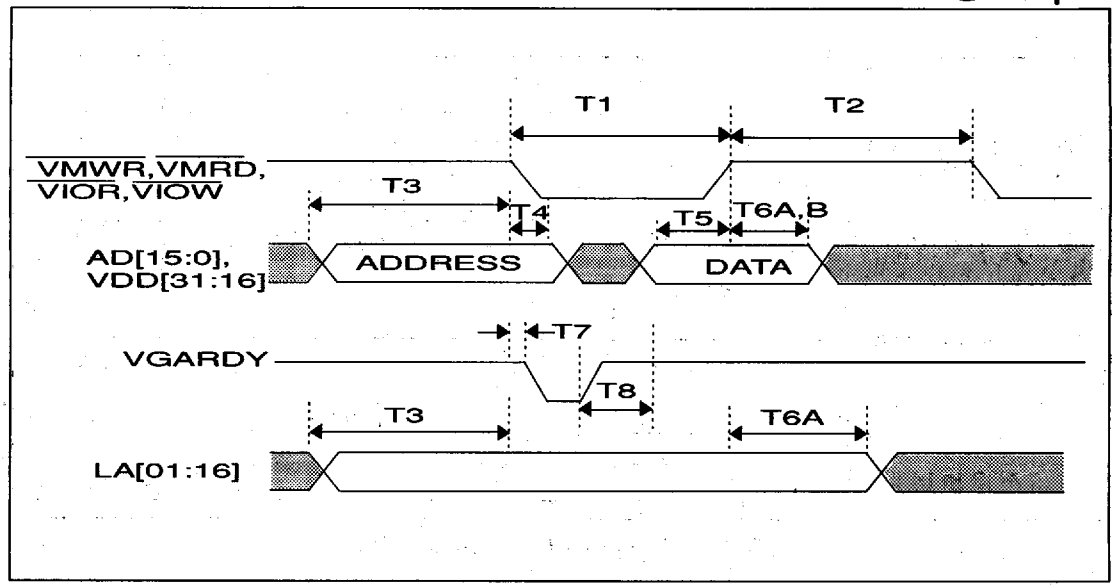

FIGURE 7-3. 45 MHZ COMMAND TIMING

No.	PARAMETER	MIN	MAX	UNITS
T1	CMD active low pulse width	1.5	5.5	VMCLK*
T2	CMD inactive high pulse width	1.5	5.5	VMCLK*
T3	Address set up to CMD active low	15	---	ns
T4	Address hold from CMD active low	7.5	---	ns
T5	Write data set up to CMD inactive high	15	---	ns
T6A	Write address/data hold from CMD inactive high	15	---	ns
T6B	Read data hold from CMD inactive high	10	25	ns
T7	RDY inactive from CMD low	---	15	ns
T8	Read data ready from RDY goes active high	---	10	ns

TABLE 7-6. 45 MHZ COMMAND

* The CMD pulse width is programmable. The 2 VMCLK CMD pulse width is defined for interfacing with the WD90C31 whose host interface and memory timing is generated by the VGA MEMCLK.

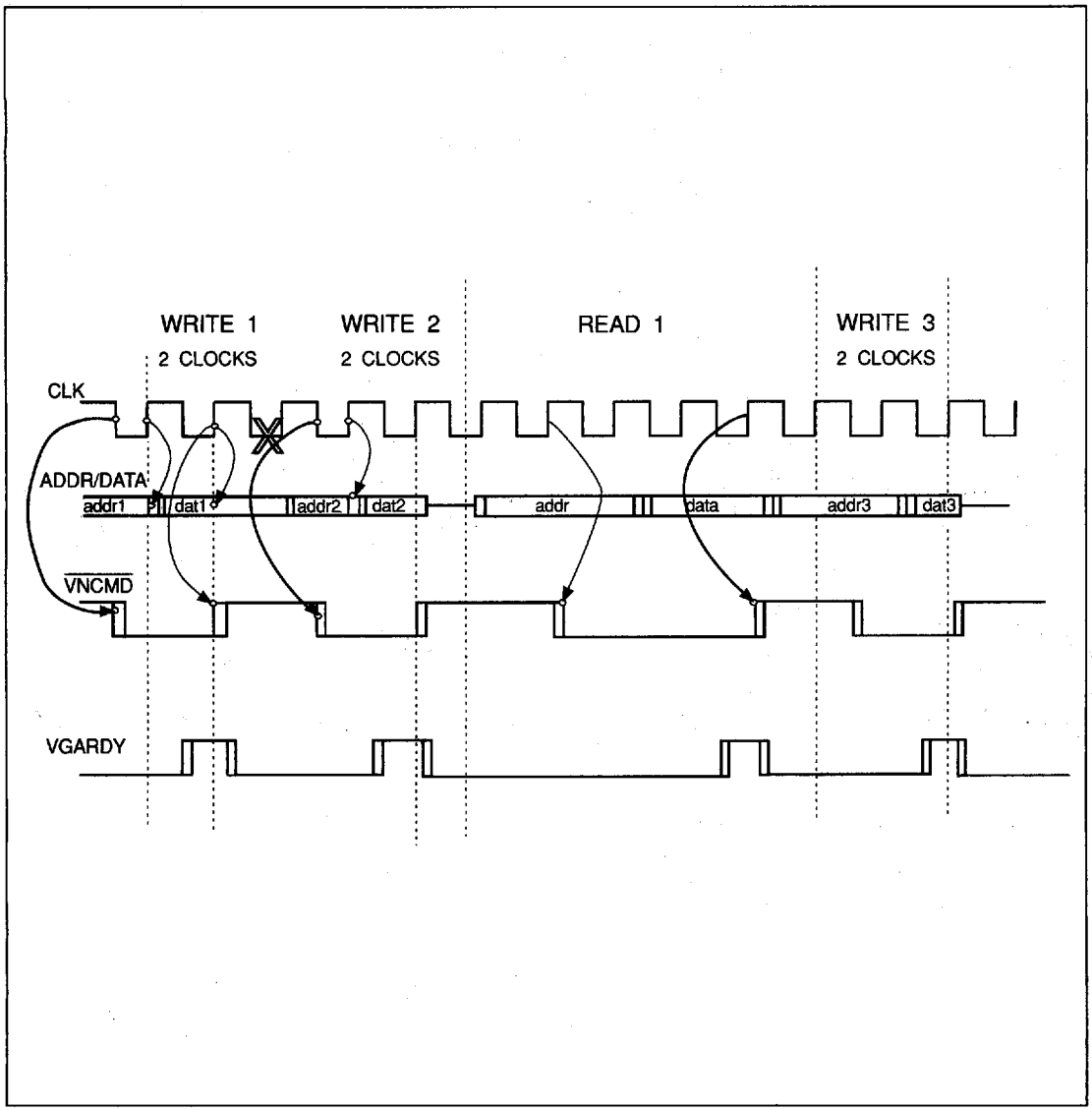

FIGURE 7-4. VLBI1 - DIRECT TRANSFER MODE

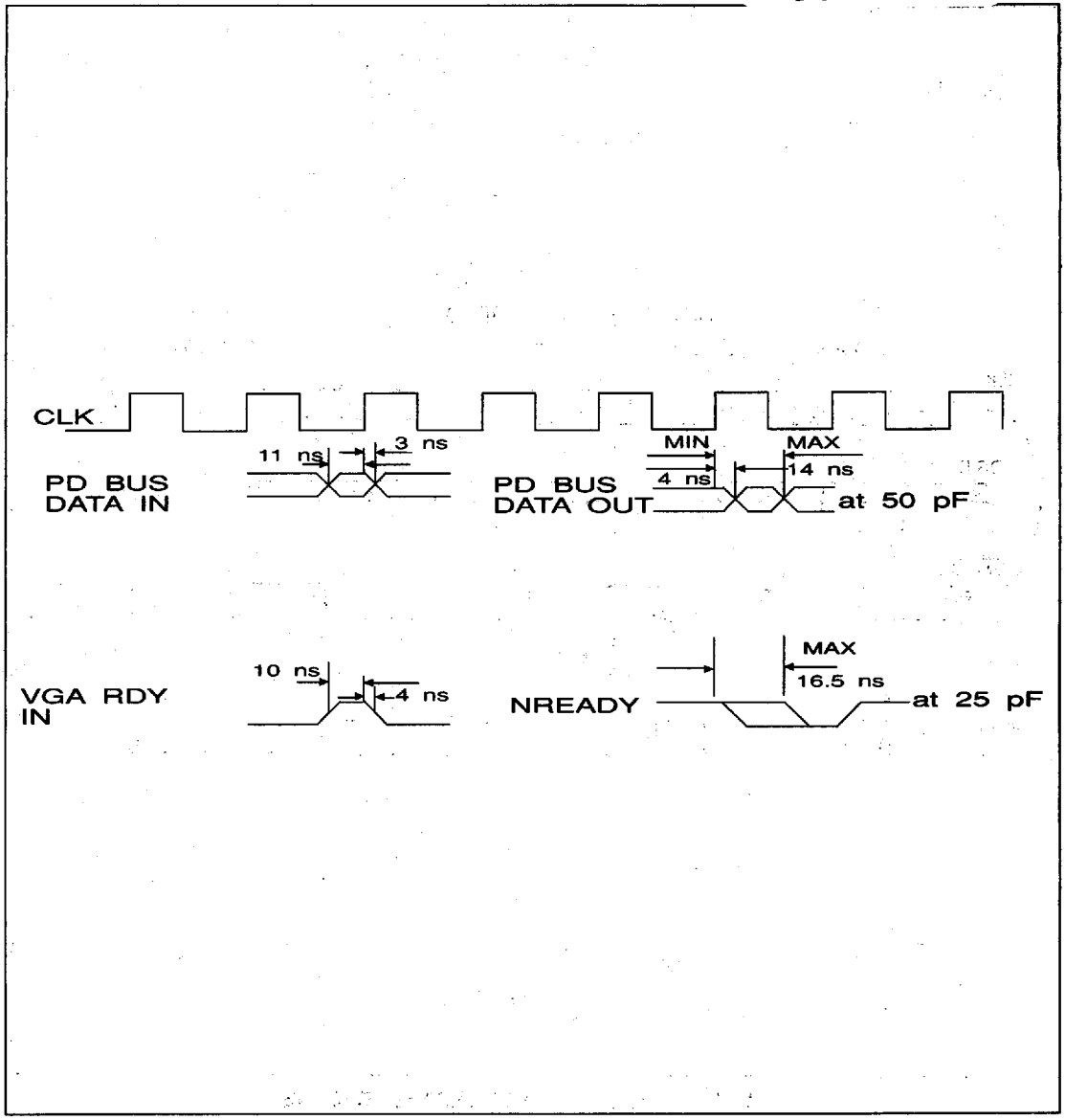

FIGURE 7-5. VLBI2

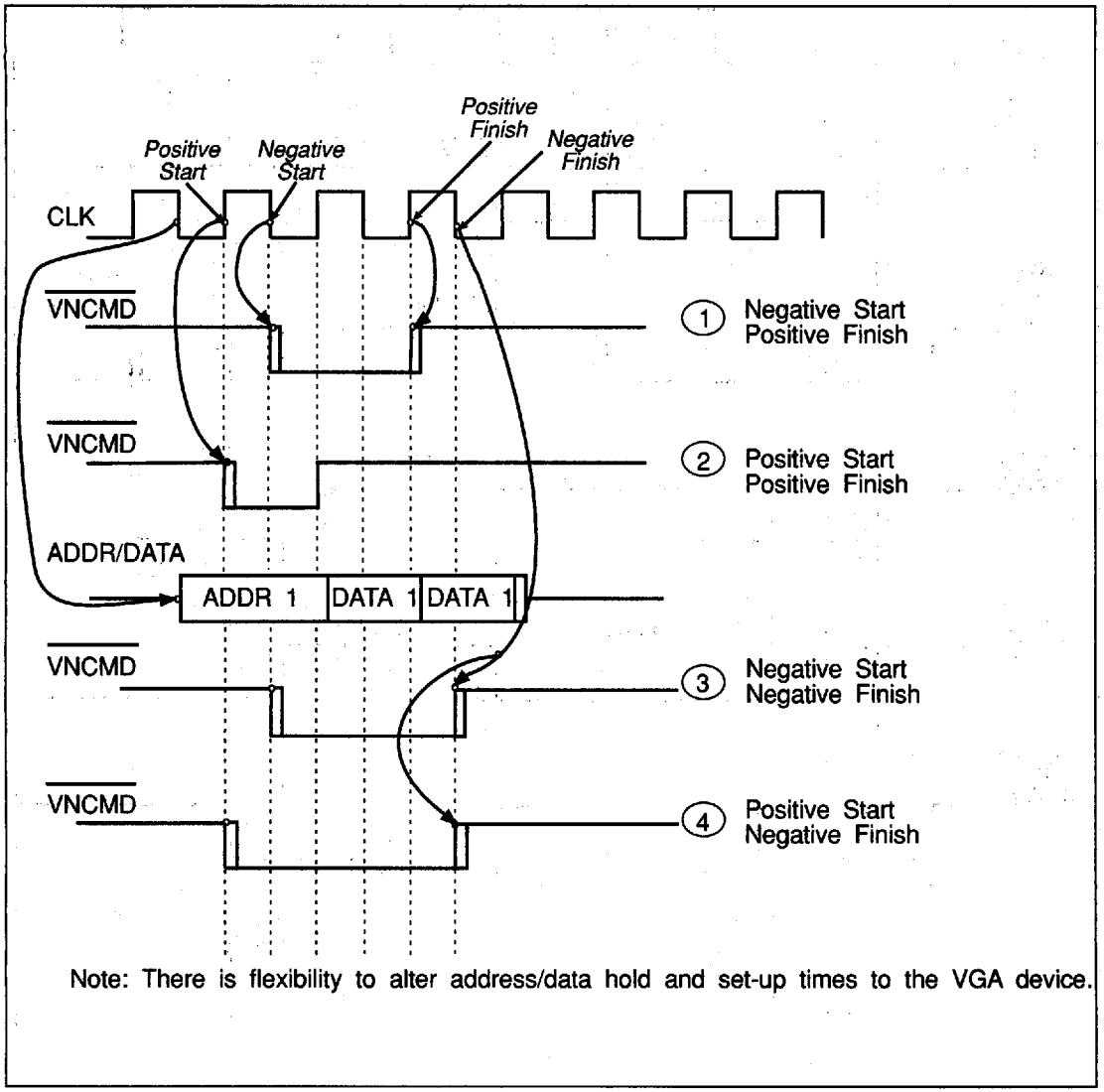

FIGURE 7-6. VLBI3

VLBI, $\overline{\text{VNCMD}}$ possible start, finish positions

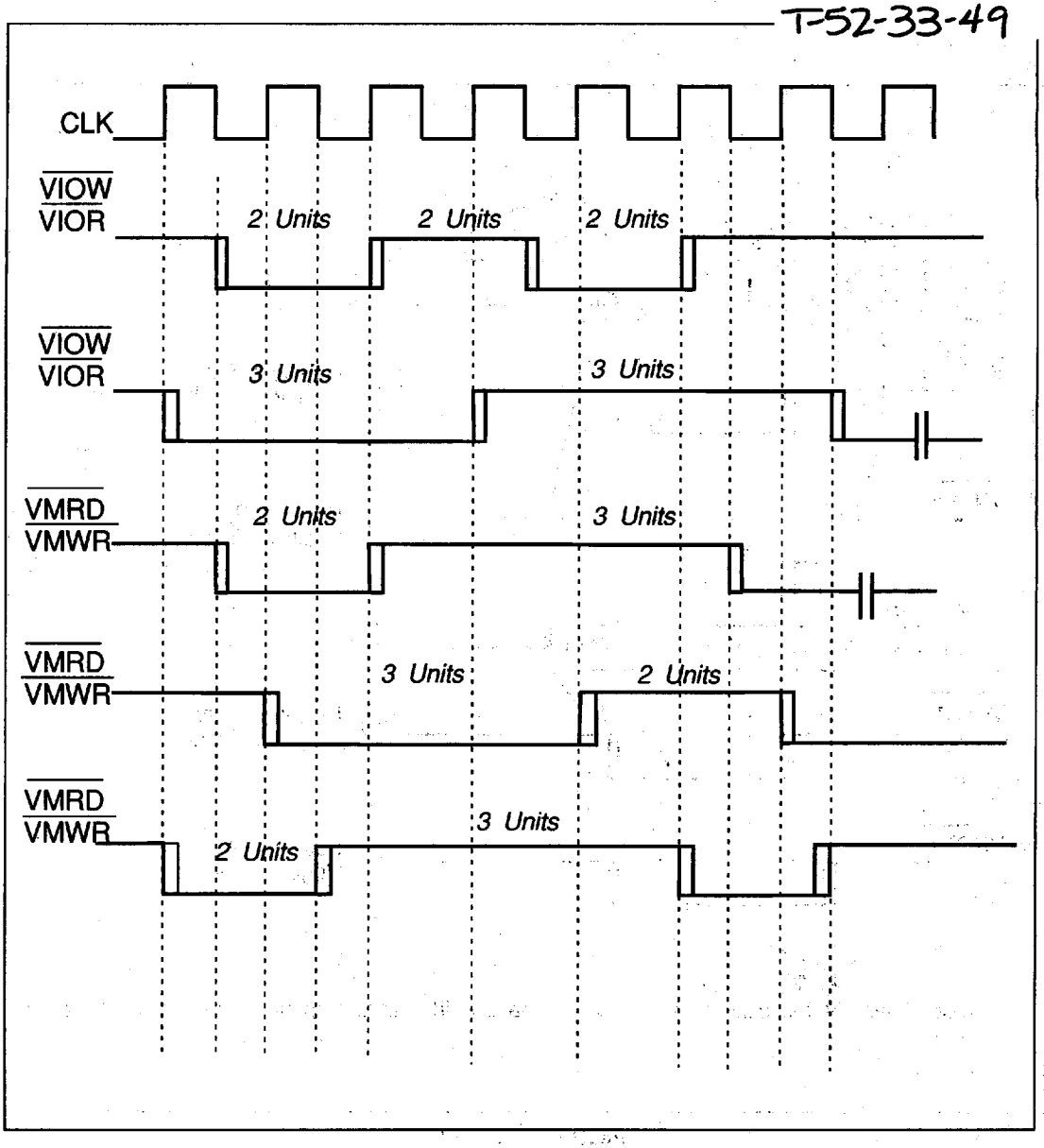

FIGURE 7-7. VLBI4

VLBI command timing configurations (as examples)

Note: $\overline{\text{VIOW}}$ and $\overline{\text{VIOR}}$ active and recovery times have the same lengths; whereas, $\overline{\text{VMRD}}$ and $\overline{\text{VMWR}}$ commands can have independent lengths.

8.0 PACKAGE DIMENSIONS

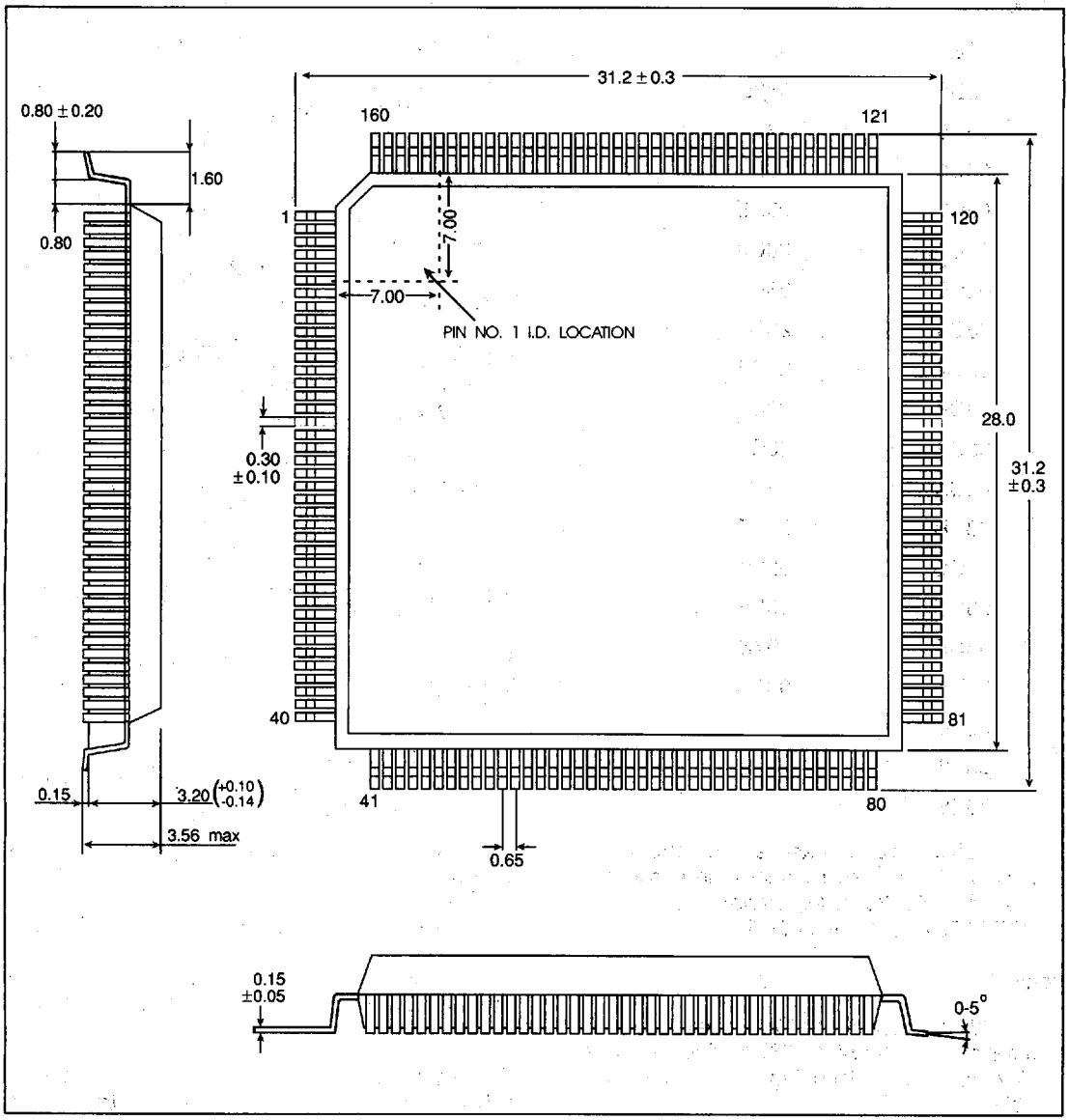

FIGURE 8-1. PACKAGE DIMENSIONS

A.0 VGA I/O AND MEMORY DECODE INFORMATION

T-52-33-49

A.1 VGA I/O DECODING

The following I/O spaces are decoded by the WD90C56.

03B9	03?4
03BF	03?5
03C0	03D9
03C1	03DC
03C2	03DE
03C4	23C0
03C5	23C1
03C6	23C2
03C7	23C3
03C8	23C4
03C9	23C5
03CA	23C6
03CB	23C7
03CC	03?8
03CE	03?A
03CF	03?B
46E8	03C3
56E8	
66E8	
76E8	

The $\overline{\text{VLIBCS}}$ signal is active when one of the I/O ports listed above is accessed *except for the RAMDAC I/O write port addresses 03C6,03C7,03C8, and 03C8.*

Notes:

1. The "?" is either "B" or "D." For example, 03?4 means either 03B4 or 03D4. The same principle applies to decoding 03?5, 03?8, 03?A, 03?B.

2. The following table shows data register pairs.

INDEX	DATA
3C4	3C5
3CE	3CF
3?4 (3D4 or 3B4)	3?5 (3D5 or 3B5)
3C0 (index and data)	*
23C0 (index and data)	**
	23C1
23C2 (index and data)	**
	23C3
23C4 (index and data)	**
	23C5
23C6 (index and data)	**
	23C7

* An internal toggle switch toggles between the Index and the Data Register

** Bits 7:4 are index and Bits 3:0 are data

3. Notation 3CF.06 Bit 4 means that Bit 4 of the register 3CF indexed by 3CE has a value of 06.

A.2 SIXTEEN-BIT I/O READ OR MEMORY ACCESS

The 16-bits of I/O read or write data apply to the following ports: 03CE; 03?4; 23C0; 23C2; 23C4; 23C6.

When 16-bits are written to the I/O port 03C4: the low byte contains the index value and the high byte contains data.

All other I/O ports except for those listed above are 8-bit I/O ports.

Sixteen-bits of I/O are enabled only if $\overline{\text{BHE}}$=0 and A0=0, and if 3C5.11 Bit 0=1 (for 3C0 port, both 3C5.11 Bit 0=1 and 3C5.11 Bit 1=1 is enabled.) Otherwise, VGA registers expect only the low byte of data.

The eight-bits of I/O are always on the low byte (AD[7:0] of the VLBI's output). The VLBI handles byte swapping.

VGA memory operation can be either 32-bits or 16-bits. The 16-bit operation is enabled only if 3CF.0A Bit 1=1.

The 16-bit memory operation follows the AT bus protocol as follows:

$\overline{BHE}$,A0 = 00: Word;

$\overline{BHE}$,A0 = 01: High byte;

$\overline{BHE}$,A0 = 10: Low byte;

$\overline{BHE}$,A0 = 11: Illegal.

A.3 VGA MEMORY DECODING

The VLBI decodes the CPU addresses A31 through A0 for the VGA memory mapping. The $\overline{VLIBCS}$ signal is active when the following memory address space is decoded.

A.3.1 CPU Address A19-A0 Decoding

3CF.0B Bits 5,4 = 00: IBM VGA Mapping and one of the following four cases:

3CF.06 Bits 3,2 = 00: decode A0000-BFFFF
3CF.06 Bits 3,2 = 01: decode A0000-AFFFF
3CF.06 Bits 3,2 = 10: decode B0000-B7FFF
3CF.06 Bits 3,2 = 11: decode B8000-BFFFF

A.3.1.1 Case1: 3CF.0B Bits 5,4 = 01

WD VGA Mapping, 256k bytes linear addressing.
3CF.06 Bits 3,2 = xx: decode 00000 - 3FFFF.

A.3.1.2 Case2: 3CF.0B Bits 5,4 = 10

WD VGA Mapping, 512k bytes linear addressing.
3CF.06 Bits 3,2 = xx: decode 00000 - 7FFFF.

A.3.1.3 Case3: 3CF.0B Bits 5,4 = 11

WD VGA Mapping, 1M byte linear addressing.
3CF.06 Bits 3,2 = xx: decode 00000 - FFFFF.

A.3.1.4 Case4: Decoding CPU Address A31-A20

Decoding of A31 through A20 is accomplished by matching signals A31 through A20 with the contents of the CPU Address A31 through A20 Mapping Registers, I/O address 2DF2 and 2DF3.

When decoding A31 through A20, there is an option to mask out A23 through A20 as described later in this section.

The VLBI indicates to the VGA by means of asserting either the $\overline{VMWR}$ or $\overline{VMRD}$ signal when A31 through A20 decoding results in a valid decode.

A.4 CMD PULSE WIDTH PROGRAMMING

All VLBI commands ($\overline{VMRD}$, $\overline{VMWR}$, $\overline{VIOR}$, and $\overline{VIOW}$) are made programmable for the positive/negative clock edge start as well as for different command lengths from two clock units to five clock units wide for $\overline{VMRD}$,$\overline{VMWR}$, $\overline{VIOR}$, and $\overline{VIOW}$. Also the trailing edges of commands are made programmable to end at either the positive or negative edge of the clock. See the System Timing Diagram-VLBI3.

The $\overline{VIOW}$ is a special case in that it can assume two different modes each of which can present two different pulse widths. One is the RAMDAC mode (I/O port address: 03C6, 03C7, 03C8 or 03C9) and the other mode includes the rest of the $\overline{VIOW}$s to the VGA. Therefore, it is possible, to have a long, low pulse width for the RAMDAC (as long as 1.0 µs [18 clocks @ 16 MHz] or 400 ns [18 clocks @ 45MHz]) and a low pulse for the rest that is two-clock units wide.

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A.4.1 $\overline{VIOW}$ Pulse Width Control for RAMDAC Operation

These cycles are passed to the system bus as well as to the VGA that resides on the local bus. During these cycles the VLBI has either a low pulse width of nine clocks or eighteen clocks (same for an inactive high period). An I/O write to the RAMDAC can be detected if the I/O ports 03C6, 03C7, 03C8 or 03C9 are accessed. An I/O write to the RAMDAC passes to the system bus ($\overline{VLIBCS}$ is inactive), which allows system slaves to write shadow the VGA RAMDAC registers. The inactive high time of $\overline{VIOR}$ is also programmable to be either nine clocks or eighteen clocks.

To obtain maximum performance, the command high duration, i.e, the inactive (high) time between two consecutive cycles of $\overline{VMRD}$ and $\overline{VMWR}$, is separately programmable in units of clock widths as well. These can be from two to five clock units. See timing, System Timing Diagrams - VLBI4.

The high pulse width and low pulse width can be independently controlled, i.e, the high can be two and the low can be five or visa versa. Any combination from two to five in one clock unit increments is possible. In order to avoid having different BIOS programs for inevitably different setups due to differing CPU speeds, the setup is made hardware-configurable using pullups and pulldowns on the pins of the VD bus. See Configuring the VLBI.

A.4.2 VGA Interface Timing for WD90C31 Only

See the VLBI Timing Diagrams section for the 33 MHz and 45 MHz CMD timing.

A.4.3 VLBI Write Shadow VGA Registers

The VLBI write shadows the following VGA registers to control address decoding.

ADDR	BITS	DECODE
03CF.06	3,2	IBM VGA memory mapping
03CF.0B	5,4	Controls CPU A19 through A0 memory address decoding.
03C5.11	1,0	8/16-bit I/O control
03CF.0A	2	16-bit memory cycle

A.4.4 VLBI and VGA Interface Control Registers

The VLBI specific Command Pulse Width Control Registers are controlled by I/O ports = 2DF0 through 2FD6.

These registers control the default pulse width in clock units for $\overline{\text{VIOR}}$, $\overline{\text{VIOW}}$, $\overline{\text{VMRD}}$ and $\overline{\text{VMWR}}$ command lines.

A.4.4.1 Register 2DF0

Bits 1,0
Pulse width control for $\overline{\text{VIOW}}$

0	0	Command low/high for 2 CLK
0	1	Command low/high for 3 CLKS
1	0	Command low/high for 4 CLKS
1	1	Command low/high for 5 CLKS

Bits 3, 2
Pulse width control for $\overline{\text{VIOR}}$ T-52-33-49

0	0	Command low/high for 2 CLK
0	1	Command low/high for 3CLKS
1	0	Command low/high for 4 CLKS
1	1	Command low/high for 5 CLKS

Bit 4:
Pulse width control for RAMDAC cycles $\overline{\text{VIOW}}$/$\overline{\text{VIOR}}$ (high only)

Bit 4 = 0, Command low for 9 CLKS.

Bit 4 = 1, Command low for 18 CLKS (Default).

Bit 5
VLBI enable control

Bit 5 = 0, VLBI disable

Bit 5 = 1, VLBI enable

Bits(7:6)
$\overline{\text{VIOR}}$/$\overline{\text{VMRD}}$ start/finish edge control

7	6	START	FINISH
0	0	Positive	Negative
0	1	Positive	Positive
1	0	Negative	Negative
1	1	Negative	Positive*

* default

A.4.4.2 Register 2DF1

Bits 1,0
Pulse width control for $\overline{\text{VMRD}}$

0	0	Command low for 2 CLK
0	1	Command low for 3 CLKS
1	0	Command low for 4 CLKS
1	1	Command low for 5 CLKS

Bits 3,2
Pulse width control for $\overline{\text{VMRD}}$

0	0	Command high for 2 CLK
0	1	Command high for 3 CLKS
1	0	Command high for 4 CLKS
1	1	Command high for 5 CLKS

Bits 5,4
Pulse width control for $\overline{VMWR}$

0	0	Command low for 2 CLK
0	1	Command low for 3 CLKS
1	0	Command low for 4 CLKS
1	1	Command low for 5 CLKS

Bits 7,6
Pulse width control for $\overline{VMWR}$

0	0	Command high for 2 CLK
0	1	Command high for 3 CLKS
1	0	Command high for 4 CLKS
1	1	Command high for 5 CLKS

Note:

The VLBI specific registers are designated as read and write by the CPU, unless specified otherwise.

A.4.4.3 CPU Address A31-A20 Mapping Register (I/O port = 2DF2 and 2DF3)

Bits 7:0 of I/O address 2DF2 and Bits 7:4 of I/O address 2DF3 (upper nibble) are used. The value programmed into this register is compared with the CPU address A31 through A20 as part of the CPU high address decoding by the VLBI.

A.4.4.4 Memory Access Decoding Control (I/O PORT = 2DF3 Lower Nibble)

Either $\overline{VMRD}$ or $\overline{VMWR}$ ENABLE MEMORY is active as the result of CPU address A31 through A20 decoding.

Bits 3 through 0 provide the following decoding control.

3	2	1	0	ENABLE MEMORY
0	0	0	0	ENABLE MEMORY is the result of decoding A31-A24 (A23-A20 are decoded by VGA). VGA has 16 Mbytes of memory space.
1	0	0	0	ENABLE MEMORY is the result of decoding A31-A23 (A22-A20 are decoded by VGA). VGA has 8 Mbytes of memory space.
1	1	0	0	ENABLE MEMORY is the result of decoding A31-A22 (A21-A20 are decoded by VGA). VGA has 4 Mbytes of memory space.
1	1	1	0	ENABLE MEMORY is the result of decoding A31-A21 (A20 is decoded by VGA). VGA has 2 Mbytes of memory space.
1	1	1	1	ENABLE MEMORY is the result of decoding A31-A20. VGA has 1 Mbytes of memory.
All other combinations are illegal.				

A.4.4.5 VIOW/VMWR Start/Finish Edge Control Register 2DF6

5	4	START	FINISH
0	0	Negative	Positive
0	1	Positive	Positive
1	0	Negative	Negative
1	1	Positive	Negative

B.0 VLBI INTERFACE IMPLEMENTATION TO WD90C30/WD90C31

The diagram below illustrated the VLBI interfaced to the WD90C30/WD90C31.

T-52-33-49

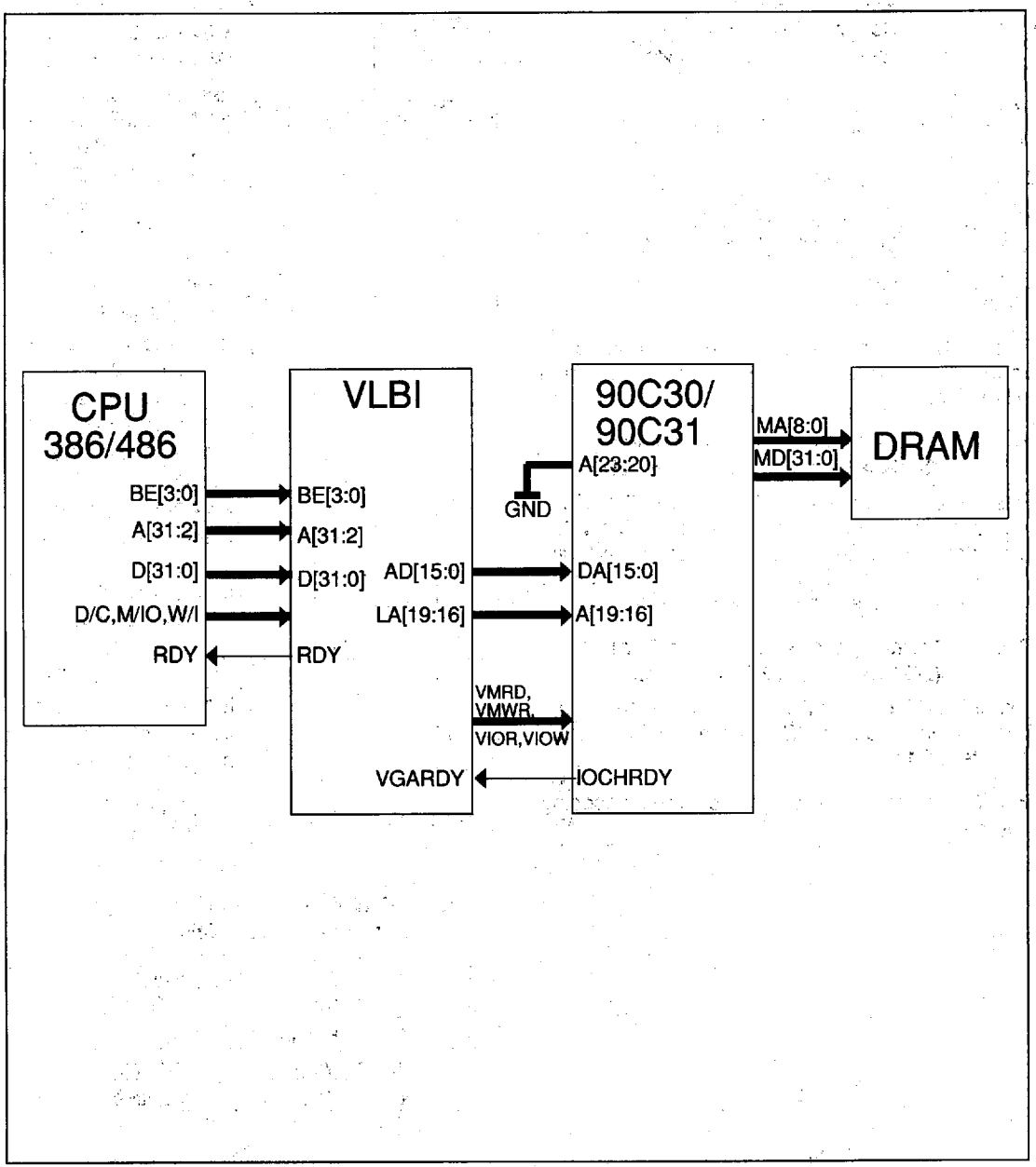

FIGURE B-1. VLBI INTERFACED TO WD90C30/WD90C31

C.0 TESTABILITY

The test methods incorporate both tristating the outputs and I/O mapping.

I/O mapping is invoked when $\overline{\text{RESET}}$ is high and the TEST pin is used as a clock to latch the two internal flip flops whose D inputs are PD0 and PD1. When the outputs are set to 1, the VLBI enters I/O mapping mode.

The I/O map with table approved by Western Digital Test Engineering division is shown below and on the following page.

INPUT	NAME	OUTPUT	NAME
55+57+51+53	A8,A10,A15,A17	39	RESRV6
54+56+58+52	A7,A9,A11,A16	38	RESRV5
42+44+46+48+40	$\overline{\text{ADS}}$,$\overline{\text{BE1}}$,$\overline{\text{BE3}}$,DC,A22	36	PD21
43+45+47+49	$\overline{\text{BE0}}$,$\overline{\text{BE2}}$,WR,MIO	35	PD20
41+37	A14,RESERV1	33	PD18
66+64+59+62	A3,A5,A12,A13	79	$\overline{\text{VBROM}}$
65+63+72	A4,A6,A31	78	$\overline{\text{VBE3}}$
80	A29	82	VMCLK*
83	VGARDY	88	RESRV9
73+76	CPURES,$\overline{\text{RDYIN}}$	84	$\overline{\text{VIOR}}$
68+71	A2,A30	85	$\overline{\text{VIOW}}$
2+4+8+159	CLK486,A21,A18, CLK2386	6	$\overline{\text{BOFF}}$
7+5+3	A19,A20,A28	158	RESRV2
149	PD24	141*119	AD0,VD16
95	RESRV8	138*118*99	AD1,VD17,LA21
148	PD25	137*117	AD2,VD18
130	RESRV4	135*116*98	AD3,VD19,LA20
147	PD26	134*114	AD4,VD20
95	RESRV8	133*113	AD5,VD21
146	PD27	132*112	AD6,VD22
94	RESRV7	131*111	AD7,VD23
145	PD28	129*108	AD8,VD24
130	RESRV4	127*107	AD9,VD25
144	PD29	126*106	AD10,VD26
94	RESRV7	125*105	AD11,VD27
143	PD30	124*104	AD12,VD28
86	RESRV3	123*103*92	AD13,VD29,LA18
142	PD31	122*102	AD14,VD30
95	RESRV8	109*101*91*93*97	AD15,VD31,LA17, LA19,$\overline{\text{VMRD}}$

TABLE C-1. VLBI PINSCAN TABLE

* only for I/O map

INPUT	NAME	OUTPUT	NAME
77	PWRDWN	87*89*96	VBHE,LA16,VMWR
153+155+157	A23,A25,A27	151	PD23
154+156	A24,A26	152	PD22
11+13+15+17	PD6,PD8,PD10,PD12	21	PD14
12+14+16+18	PD7,PD9,PD11,PD13	22	PD15
23+25+27+29	PD0,PD2,PD4,HREQ	32	PD17
24+26+28+31	PD1,PD3,PD5,PD16	34	PD19

TABLE C-1. VLBI PINSCAN TABLE (CONTINUED)

GND: 1,10,19,30,50,70,81,90,110,121,128,139,150
VCC: 9,20,60,74,100,115,120,136,160

Notes:

1. VD16 through VD31 are the duplicated output of AD0 through AD15 during the I/O scan.

2. The following signals are not I/O scanned: RESET, TEST, VLBICS, VLBUSY, READY.

3. The following table shows when the VLBI enters I/O mapping mode.

MODE	RESET	TEST	PD0	PD0
Functional	1	x	0	0
Tristate*	1	+clk	1	0
I/O Map	1	+clk	0	1
Fault Cover	1	+clk	1	1
Reset	0	x	0	0

* o/p

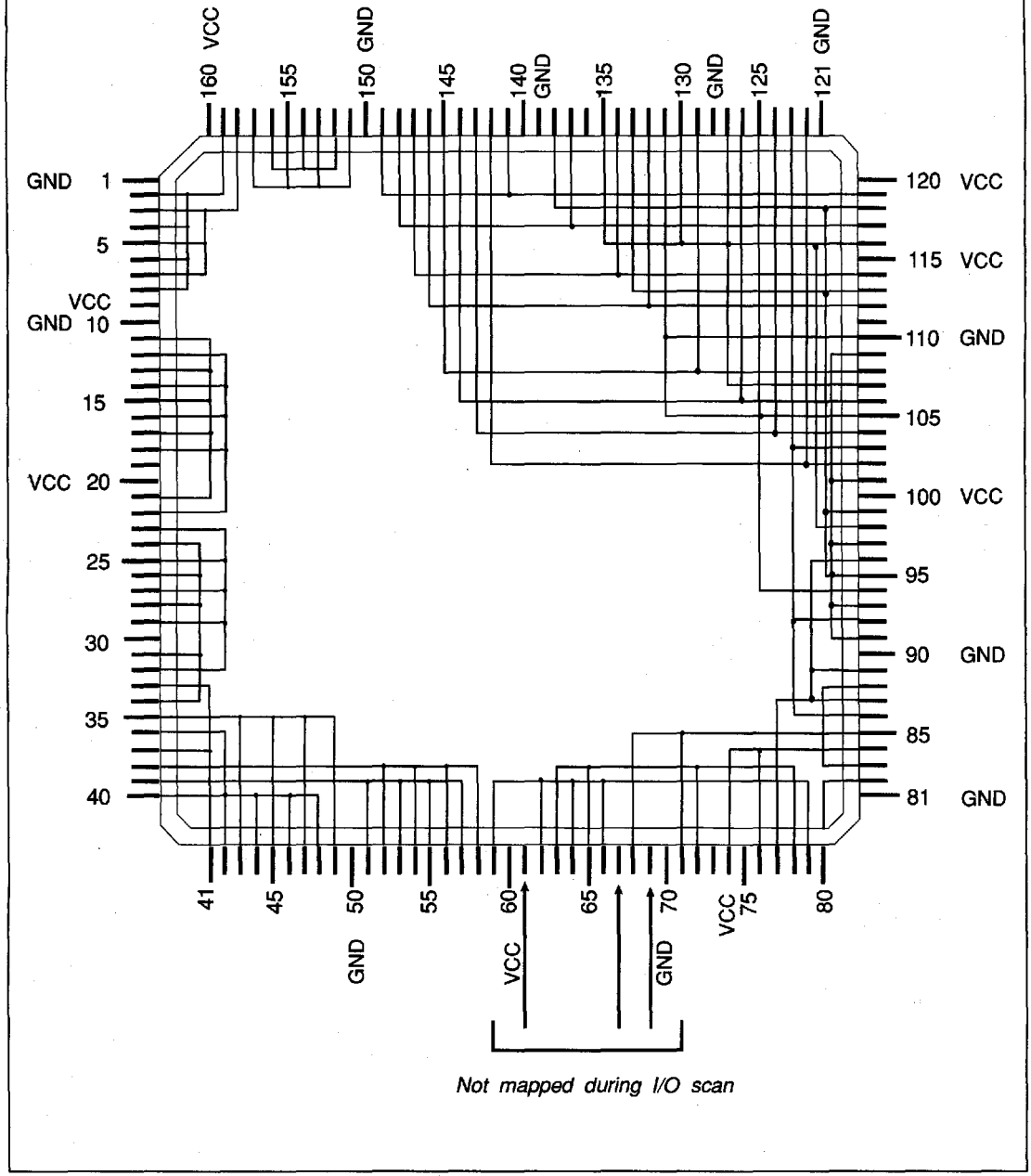

FIGURE C-1. WD90C56 PINSCAN I/O MAP