ADS10C00A

Winchester Disk

Controller

WESTERN DIGITAL

ADS10C00A DATA BOOK ADDENDUM

The following Data Book applies to both the ADS10C00 and the ADS10C00A versions.

Part Numbers:

STATUS	MODEL NUMBER	MANF. NUMBER	DESCRIPTION
Current	ADS10C00A JT 00 02	1000KB00JTL02	68-pin PLCC, released 6/90
Obsolete	ADS10C00 JT 00 02	1000PA00JTL02	68-pin PLCC

ADS10C00A Data Book Corrections

The following changes should be made to the existing ADS10C00:

Several pins are incorrectly labeled for the pinout drawing.

PIN#	WAS	CORRECTION
9	GN0	GND
8-1	D00-D07	DB0-DB7
63	WR20	NRZ0
59	R6	RG
58	W6	WG

List of Differences

There are no functional differences between the ADS10C00 and the ADS10C00A. Production process improvements were made to improve reliability.

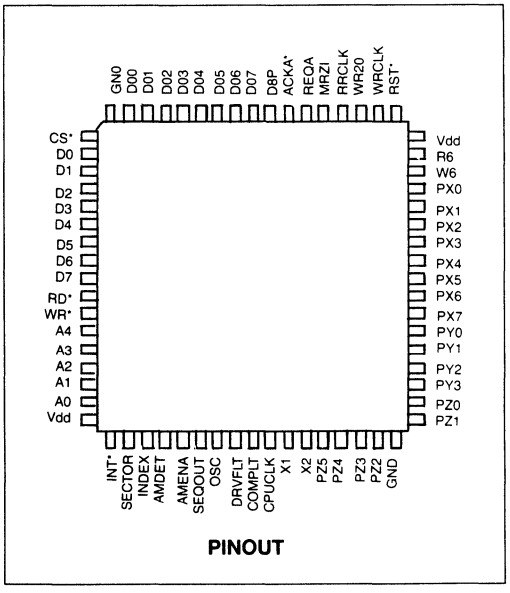
1. Change: Input buffers for the DB bus inputs were improved and signal routing optimized in order to improve DB bus setup and hold times with respect to CS and WR. The new input buffers have modified device sizes and decreased capacitance. These changes allow a greater margin in meeting the specified setup and hold times. No logic or specifications changes were involved.

2. Change: A potential race condition existed between a clock (CLK) and the inversion of that clock (CLKN). Previously both clocks were generated in parallel from a master clock; CLK through a buffer and CLKN through an inverting buffer. This was changed to CLK being generated serially from the CLKN signal by an inverting buffer. A minor routing/logic change was involved, no specification change.

ADS10C00 Winchester Disk Controller

FEATURES

- DISK INTERFACES AND FORMATS SUPPORTED INCLUDE ST412, ST412HP, ESDI, SMD, AND CPTICAL DISKS
- FULL MULTISECTOR OPERATION WITH FOUR BYTE ID AUTO-INCREMENT
- UP TO 24 MBITS/SECOND MAXIMUM TRANSFER RATE
- INTERNAL 48-BIT ECC, 32-BIT ECC, OR 16-BIT CRC-CCITT POLYNOMIAL, OR EXTERNAL USER DEFINED ECC
- INTERNAL SUPPORT FOR 4 TO 18 BIT ERROR CORRECTION SPANS
- UP TO 1:1 INTERLEAVE OPERATION
- FLEXIBLE ERROR RECOVERY, INCLUDING REDUNDANT ID AND SYNC FIELDS
- SECTOR SIZES TO 4096 BYTES, HARD OR SOFT SECTOR, LARGER SIZES POSSIBLE WITH SPECIAL TECHNIQUES
- BUILT IN CRYSTAL DRIVER FOR DATA RATE AND/OR CPU USE



PINOUT

- GENERIC CPU BUS INTERFACE WITH INTERRUPTS
- SEPARATE CPU AND DISK DATA BUSSES
- ASYNCHRONOUS DATA BUFFER INTERFACE WITH FULL 'THROUGH' PARITY
- ON THE FLY COMPARE AGAINST BUFFER DATA
- 20 I/O LINES FOR DISK DRIVE CONTROL
- 68 PIN PLCC PACKAGE

GENERAL DESCRIPTION

The ADS10C00 is a VLSI Winchester Disk Controller chip that provides the data handling and control for an intelligent Winchester disk controller. The ADS10C00 interfaces to nearly any serial disk interface, including ST412, ST412HP, ESDI, SMD, and many optical disk interfaces. The ADS10C00 provides great flexibility in format design, allowing for multiple ID fields, special sync requirements, special information fields, or almost any other special requirement. The ADS10C00 can provide all of the data, status, and control signals required by these interfaces.

The ADS10C00 requires only a buffer controller, such as the ADS60C40 buffer manager, a microprocessor, a data buffer memory, an optional data encoder and decoder, and drivers and receivers to make an intelligent disk controller. The ADS60C80 can be added to provide external Reed-Solomon ECC for optical disk formats.

The ADS10C00 performs all of the disk data serialization and deserialization, formatting, and error detection and correction tasks. The ADS10C00 also has data verify and compare capability, and generates and checks parity. The ADS10C00 can perform full track operations without CPU control through the use of a sector counter and auto-incrementing ID registers.

The ADS10C00 has a generic microprocessor bus interface that allows the ADS10C00 to be used with all popular 8-bit microprocessors. The ADS10C00 has interrupt capability, which means the microprocessor is freed from constant polling of the device. The ADS10C00 also has a built in crystal oscillator driver that can be used to generate data reference, buffer management, or microprocessor clocks. Two separate outputs are provided with internal programmable dividers. Both outputs have the extra drive voltage and current necessary for driving MOS microprocessor clock inputs.

The ADS10C00 has 20 lines dedicated to external I/O control lines that the microprocessor can use for drive and head select, seek command and status, and drive status. Eight lines are output only, six lines are input only, and four other lines can be individually programmed for input or output. Two other latch and hold input lines are tied to the interrupt logic and can be used to detect fault or attention conditions without constant polling.

The ADS10C00 provides error detection and correction support. The device can be programmed to use 16-bit CRC-CCITT, 32-bit ECC, or 48-bit ECC. The internal checksum register can be accessed by the microprocessor to aid in the correction of error bursts up to 18 bits. The ADS10C00 can also be programmed to use an external ECC generator and checker.

The highly programmable nature of the ADS10C00 allows the use of redundant ID and data sync fields within a single sector. This feature, along with the 48-bit ECC, gives the ADS10C00 a greater capability for recovering user data in a sector with 'grown' defects.

PIN DESCRIPTION

The following section describes the external signals available on the ADS10C00. Conventions are as follows:

I	indicates that a signal is an input to the ADS10C00.
O	indicates that a signal is an output from the ADS10C00.
I/O	indicates that a signal is bidirectional.
I,O	indicates that a signal can be input or output.

CPU INTERFACE

Name	Dir	Pin #	Description
A0-A4	I	25-21	CPU ADDRESS BUS. These signals are used to address internal ADS10C00 registers.
CPUCLK	O	36	CPU CLOCK OUTPUT. This is the OSC output (see below) divided by two or three, selected by an internal register. This output has extra drive for use with certain microprocessors.
$\overline{CS}$	I	10	CHIP SELECT. This active low signal enables the ADS10C00 bus interface logic.
D0-D7	I/O	11-18	CPU DATA I/O BUS. Used to transfer ADS10C00 control and status with the CPU.
$\overline{INT}$	O	27	CPU INTERRUPT.This active low, open drain, output is asserted whenever an enabled interrupt condition occurs on the ADS10C00.
OSC	O	33	OSCILLATOR OUTPUT. The 1x crystal oscillator output, optionally divided by two. This signal has the same drive capability as CPUCLK.
$\overline{RD}$	I	19	CPU READ STROBE. This active low signal enables data from the ADS10C00 on to the CPU data bus.
$\overline{RST}$	I	61	RESET. This active low signal resets all internal circuits that must be reset at power on. A complete list is given later in this document. The reset is latched and the condition must be cleared by the CPU.
$\overline{WR}$	I	20	CPU WRITE STROBE. This active low signal strobes data into the selected ADS10C00 register from the CPU data bus.
X1	I	37	CRYSTAL DRIVER INPUT. X1 can also be driven by an external clock.
X2	O	38	CRYSTAL DRIVER OUTPUT.

BUFFER INTERFACE

Name	Dir	Pin #	Description
$\overline{\text{ACKA}}$	I	67	BUFFER DATA ACKNOWLEDGE. This active low signal indicates to the ADS10C00 that data can now be transfered to or from the data buffer.
DB0-7	I/O	8-1	BUFFER MEMORY DATA BUS. This is an eight bit data bus that interfaces the ADS10C00 with the disk data buffer memory.
DBP	I/O	68	DATA BUS PARITY. This signal is used to generate and check parity with the disk data buffer memory.
REQA	O	66	BUFFER DATA REQUEST. This signal is asserted when the ADS10C00 has data to write to the data buffer, or needs data from the data buffer.

DISK DATA INTERFACE

Name	Dir	Pin #	Description
AMDET	I	30	ADDRESS MARK DETECTED. Used only in ST412 type interfaces that use missing clocks or other qualifiers to the sync bytes that mark the start of a field.
AMENA	O	31	ADDRESS MARK ENABLE. Used to write a missing clock sync byte (ST412) or soft sector mark (ESDI, SMD) on the media.
NRZI	I	65	NRZ READ DATA IN. Serial data input from the disk phase-locked loop. This signal is clocked in by the rising edge of RRCLK.
NRZO	O	63	NRZ WRITE DATA OUT. Serial data output. NRZO is valid on the rising edge of WRCLK.
RG	O	59	READ GATE. Active when reading from the disk drive. This signal is turned off for one byte time on an ID search error to reset external data decoders.
RRCLK	I	64	READ/REFERENCE CLOCK. This is the reference clock used to set the data rate for write, and is the recovered clock for read. The switching must be glitch free. NRZI is clocked into the ADS10C00 by the rising edge of this clock.
SEQOUT	O	32	SEQUENCER OUTPUT. This signal is a user definable output bit that is set up in the control byte of the sequencer control store (see below). This signal can be used to control an external ECC generator and checker, and is byte aligned with both read and write data.
WG	O	58	WRITE GATE. Active when writing to the disk drive.
WRCLK	O	62	WRITE CLOCK. This is output during write for drives that require it. NRZO data is valid on the rising edge of this clock.

DISK CONTROL INTERFACE

Name	Dir	Pin #	Description
COMPLT	I	35	COMPLETE. This signal is used to detect function complete conditions, such as seeks or status requests. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
DRVFLT	I	34	DRIVE FAULT. This signal is used to detect faults from the drive. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
INDEX	I	29	INDEX. This signal is used to indicate the start of a track. This signal is latched for CPU status and interrupt.
PX0-7	O	57-50	PORT X. This general purpose output port is intended for use as drive select and head select signals.
PY0-3	I,O	49-46	PORT Y. This general purpose port is intended for use as other control outputs or inputs. Each bit is selectable as input or output, but all bits are initialized to input when the ADS10C00 is reset.
PZ0-5	I	45,44, 42-39	PORT Z. This general purpose input port is used to receive drive status signals.
SECTOR	I	28	SECTOR MARK. This signal is used for marking sector start locations on the media. This can either be a hard sector mark, or a soft mark written on the media using AMENA (ESDI or SMD).

DEVICE POWER

Name	Dir	Pin #	Description
V_{dd}	I	26,60	+5 VOLTS DC.
V_{ss}	I	9,43	GROUND.

FUNCTIONAL DESCRIPTION

The ADS10C00 consists of the functional blocks shown in the block diagram, Figure 1. Vdd and Vss are applied to the device through two separate pins each to improve noise immunity. The top and right hand sides of the diagram show CPU interface features, the left hand side shows disk interface features, and the bottom shows buffer interface features. These blocks are discussed in the following paragraphs.

The PORT DECODE block generates the 32 write strobes and 23 read strobes used by the microprocessor to access the various internal control and status ports. These include the interrupt registers, external disk control ports, control store, control store control, configuration, ECC control, and ID registers.

The BUFFER CPU DATA block buffers the transfer of data between the microprocessor and the internal registers. The direction control is qualified by chip select ($\overline{CS}$) and read strobe ($\overline{RD}$).

The CPU CONFIGURATION PORTS are used to reset the ADS10C00, select checksum polynomials, set the address mark enable timing, set the buffer interface timing, and select the frequency of the clock outputs, OSC and CPUCLK.

The OSCILLATORS AND DIVIDERS block generates the clock outputs, OSC and CPUCLK, using an external crystal (or clock input) and dividers to select the frequency. Frequency selection is glitch free.

The INTERRUPT STATUS AND MASK registers are used to check and mask interrupts. The mask register does not affect the status register inputs. The interrupt sources include index and sector mark, drive fault and operation complete, and internal event status.

The EXTERNAL PORTS are used to generate control signals and read status with the disk drive. Eight bits are output, six are input, and four are individually programmable for either input or output.

The CONTROL STORE consists of 32 words of 28 bits that are used to program the format of the disk sector. The data source, field length, error handling and checksum selection, and control signals, like Read Gate and Write Gate, are controlled by the data stored here.

The CONTROL STORE CONTROL determines the next address in the control store to use, whether the next sequential address or a jump to another address. This block includes the sector counter used for multisector commands. This block also includes the BIT RING COUNTER, which determines the timing of data transfers in the ADS10C00.

The WAIT SEQUENCER handles searches for index, sector mark, address mark, and byte synchronization.

The ID WRITE REGISTERS are 8 eight bit registers that are used to set the ID write field for format, or the search field for read/update write. Four of the registers are counters that auto-increment during multisector commands. The other four registers do not increment, and are used for defect and flag information. The first byte of the four counters can be disabled for three byte ID fields.

The ID READ REGISTERS are used to read the last ID read from the media to aid in defect handling.

The CHECKSUM block sets the ECC/CRC polynomial, generates the checksums, and is also used to correct data errors.

The VALUE register holds immediate data from the control store when generating gaps, sync fields, and address mark bytes.

The SHIFT OUT register serializes internal or external (buffer) data for writing on the disk. The output is multiplexed with the output of the checksum register.

The SHIFT IN register deserializes the read data from the disk, clocked in by RRCLK. The data is also transfered to the checksum register for checking.

The COMPARE block is used to compare incoming read data with an internal or external data source. These include byte synchronization detection, ID field search, and buffer data compare.

The BUFFER INTERFACE handles the fetching and writing of data with the external data buffer. This includes parity generation and checking, and data handshake with the buffer controller.

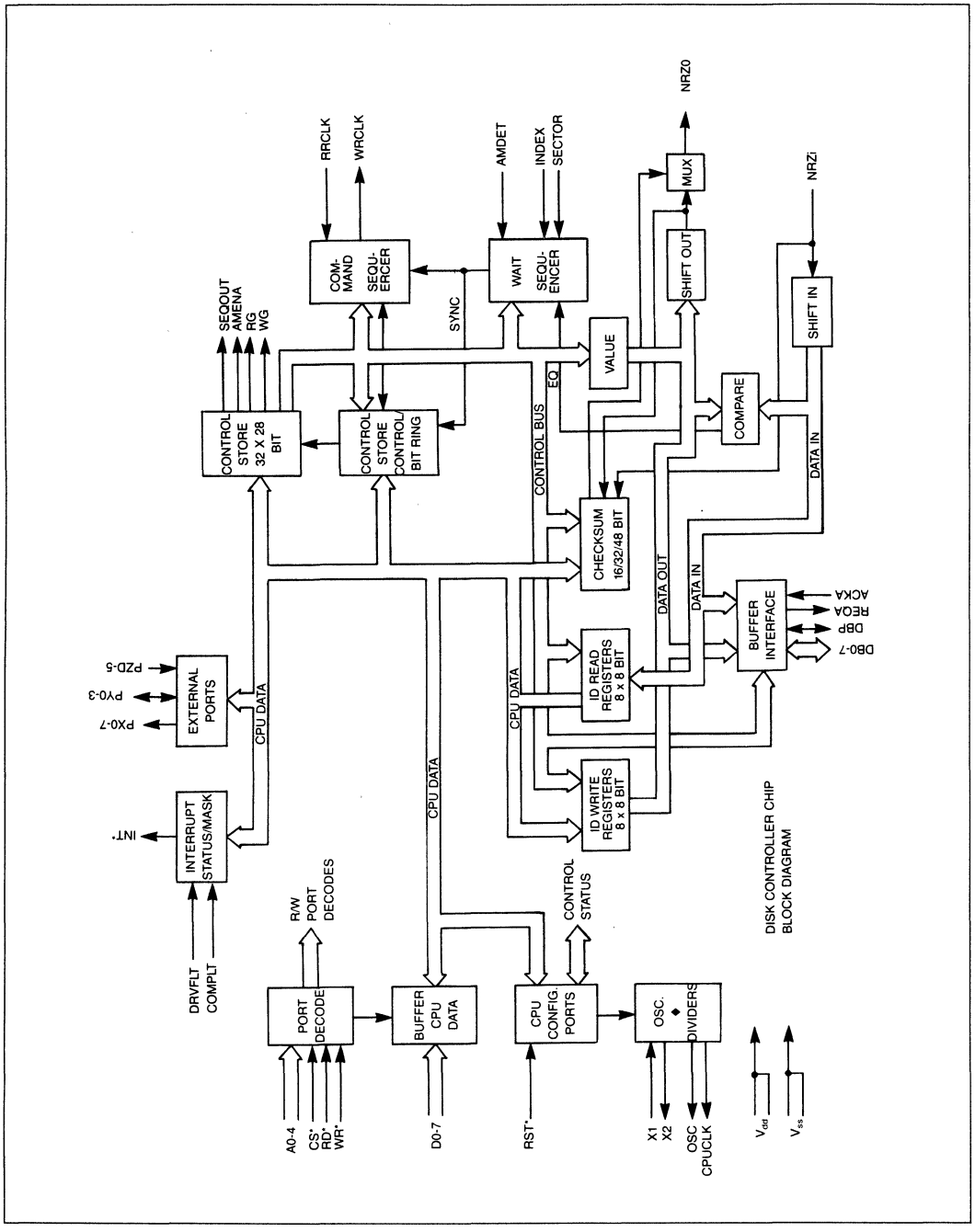


FIGURE 1. ADS10C00 BLOCK DIAGRAM

RESET CONDITIONS

The following list defines what is reset when $\overline{RST}$ is asserted on the ADS10C00, or the CPU sets the internal reset bit (SRST in SRESET register):

- SRST bit in SRESET is left set, and must be cleared by the CPU to take the ADS10C00 out of the reset state
- interrupts are disabled
- PY0-3 are set to input
- DB0-7,P are disabled
- OSC is set to X1/2
- CPUCLK is set to X1/6
- command sequencer stops
- The following CPU registers are reset to zero:
  - PORT X
  - PORT Y CONFIGURATION
  - ECC CONTROL (ECCSHT bit)
  - SECTOR COUNTER
  - INTERRUPT MASK REGISTER
  - SRESET REGISTER (except SRST)
- The following outputs are reset to zero:
  - PX0-7
  - SEQOUT
  - AMENA
  - RG
  - WG
  - NRZO
  - REQA
- The following error status bits are reset to zero:
  - IDERR
  - PTYERR

CRYSTAL OSCILLATOR APPLICATION

For applications that use the internal oscillator capability of the ADS10C00, a series resonant crystal must be used. This crystal must meet the following internal specifications:

C_S = 7 pf MAX

R_S = 30 ohms MAX

The oscillator also requires bypass capacitors, as shown in the following diagram:

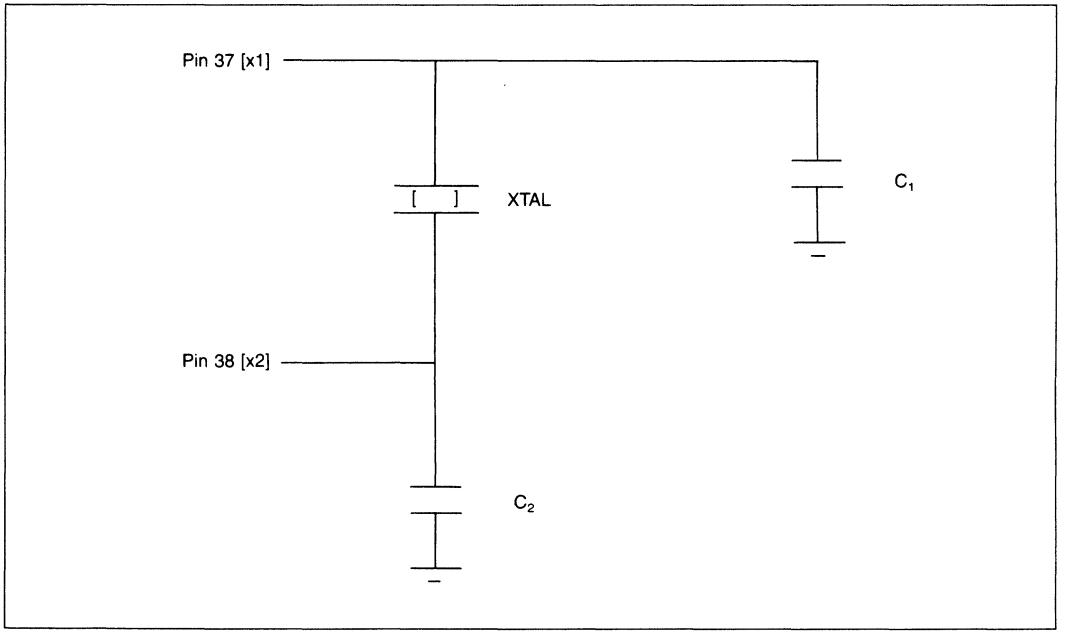


FIGURE 2. OSCILLATOR WITH CAPACITORS

The following table lists values for C_1 and C_2 for several typical crystal frequencies. The capacitor tolerances are +—10%. Values for intermediate frequencies (not listed in the table) may be extrapolated.

FREQ (MHz)	C_1 (pf)	C_2 (pf)
8	180	100
10	180	68
12	150	47
14	120	56
16	82	56
20	82	33
24	56	27
25	56	22
30	39	12
32	33	12

SPECIFICATIONS

NON-OPERATIONAL SPECIFICATIONS (absolute maximums)

	MIN	TYP	MAX	UNITS
Storage Temperature:	−65		150	Degrees C
Voltage on any pin with respect to V_{SS}:	−0.3		V_{DD} + 0.3	Volts
Voltage on V_{dd}, with respect to V_{SS}:			7.0	Volts

OPERATIONAL SPECIFICATIONS

	MIN	TYP	MAX	UNITS
Ambient Air Temperature:	0	25	70	Degrees C
V_{dd} Supply Voltage with respect to V_{SS}:	4.50	5.0	5.50	Volts
I_{CC} Supply Current: (X1 = 32MHz, RRCLK = 27MHz) (Full spec output loading)			100	Milliamps
Power Dissipation:			500	Milliwatts
Leakage Current on all input pins:			+/− 10	Microamps
Latch-Up Current:	+/− 40			Milliamps
Input Voltage			0.8	Volts
Logic 0 (V_{IL})				
Logic 1 (V_{IH})	2.0			Volts
X1 Drive Current (for TTL levels):			600	Microamps
Logic 0 (V_{IL} = 0.8)				
Logic 1 (V_{IH} = 2.0)			−600	Microamps

	MIN	TYP	MAX	UNITS
Output Voltages (all outputs except X2,CPUCLK,OSC,D0-D7) (*1)				
Logic 0 (V_{OL}) (I_{OL} = 2 mA)			0.40	Volts
Logic 1 (V_{OH}) (I_{OH} = −400 uA)	2.8			Volts
Output Voltages (CPUCLK and OSC only) (*1)				
Logic 0 (V_{OL}) (I_{OL} = 4 mA)			0.40	Volts
Logic 1 (V_{OH}) (I_{OH} = −800 uA)	V_{dd}-0.5			Volts
Output Voltages (D0-D7, $\overline{INT}$ Logic 0) (*1)				
Logic 0 (V_{OL}) (D0-D7, $\overline{INT}$) (I_{OL} = 6 mA)			0.40	Volts
Logic 1 (V_{OH}) (D0-D7) 2.8 (I_{OH} = −2.5 mA)				Volts
Input Capacitance (all inputs)			10	Picofarads
Output Capacitance Loading:				
All outputs except D0-D7, BMD0-BMD7, BMP, OSC, and CPUCLK			50	Picofarads
Outputs D0-D7, BMD0-BMD7, and BMP			100	Picofarads
Outputs OSC and CPUCLK			100	Picofarads
Input Static Discharge Protection (*2)			2000	Volts
Operating Humidity	20		95	Percent
X1 Input Operational Frequency:				
Using Crystal	8.0		32.0	MHz
TTL Source	---		25.0	MHz

NOTES:

(*1): Even under worst case AC transient switching conditions, V_{ol} = 0.4V shall not be exceeded on any output pin at any time.

(*2): This applies for both "human body" and "charged device" models.

TIMING SPECIFICATIONS

These timing relationships assume the maximum capacitive loading for both inputs and outputs, V_{DD} = 4.50 volts to 5.50 volts. Temp = 0 to 70 deg. C. All timing is measured between 0.8 volts logic low and 2.0 volts logic high, unless otherwise noted.

OSC AND CPUCLK TIMING

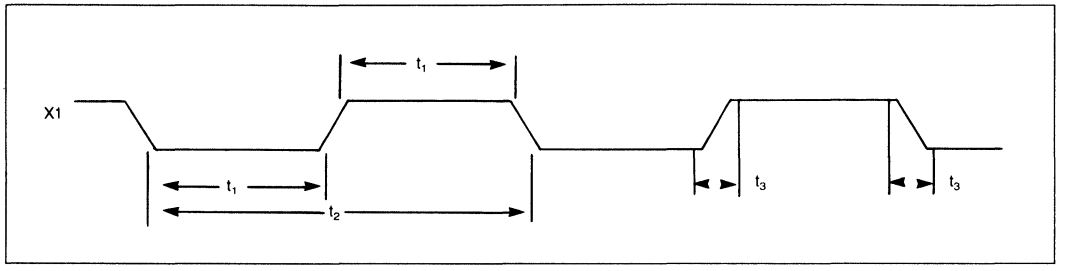


FIGURE 3. TTL SOURCE X1 CLOCK INPUT

The following table summarizes the relationship between the clock at X1 and the resultant outputs at OSC and CPUCLK. OSCDIV and CPUDIV are control bits in the RESET register that determine how the X1 clock is divided to produce OSC and CPUCLK. See the programming manual for more information.

OSCDIV	CLKDIV	OSC	CPUCLK
0	0	X1/2	X1/6
0	1	X1/2	X1/4
1	0	X1/1	X1/3
1	1	X1/1	X1/2

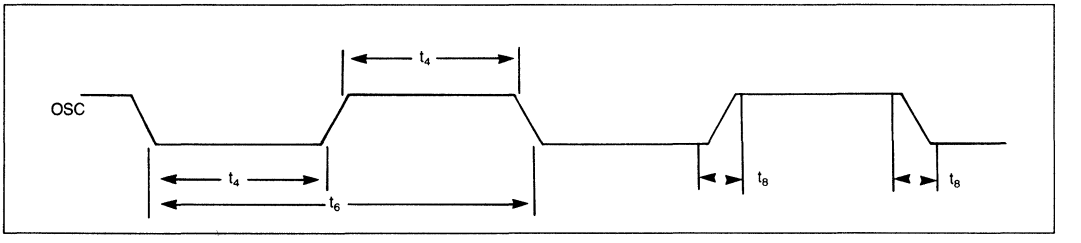


FIGURE 4. OSC OUTPUT

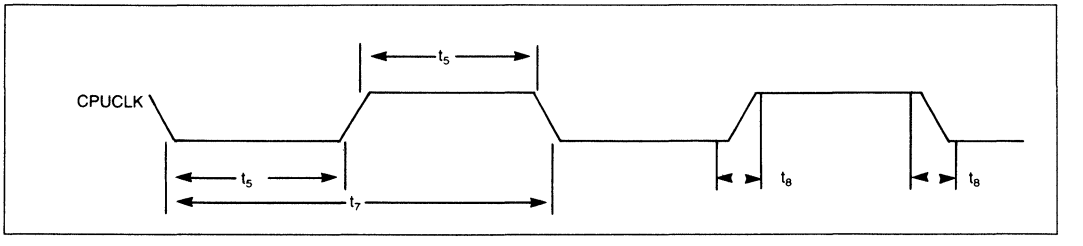


FIGURE 5. CPUCLK OUTPUT

CPU INTERFACE TIMING

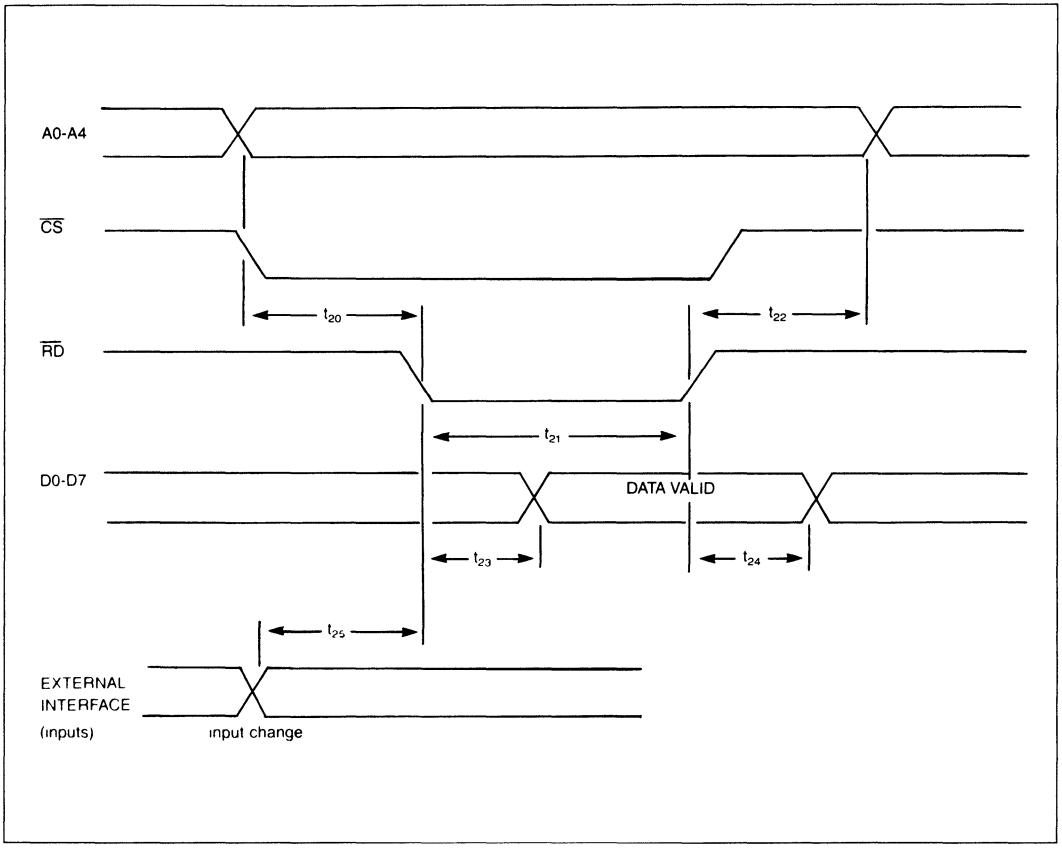


FIGURE 6. MICROPROCESSOR RD TIMING (RD CONTROLLED)

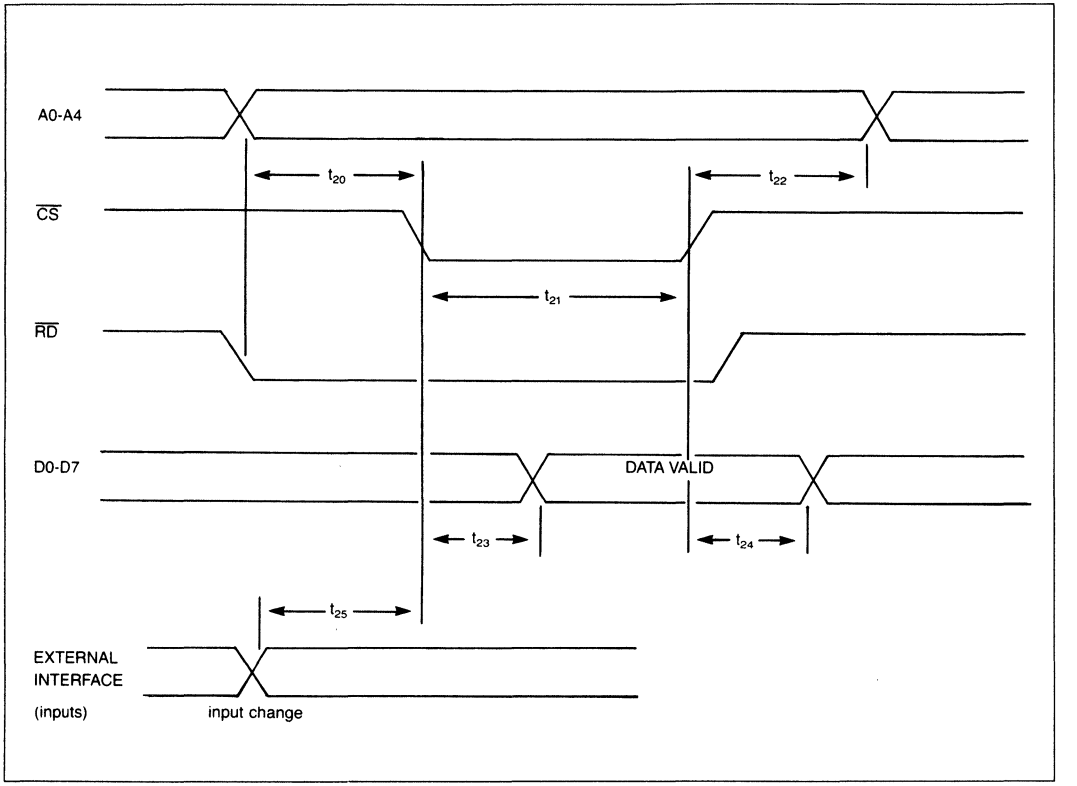


FIGURE 7. MICROPROCESSOR $\overline{RD}$ TIMING ($\overline{CS}$ CONTROLLED)

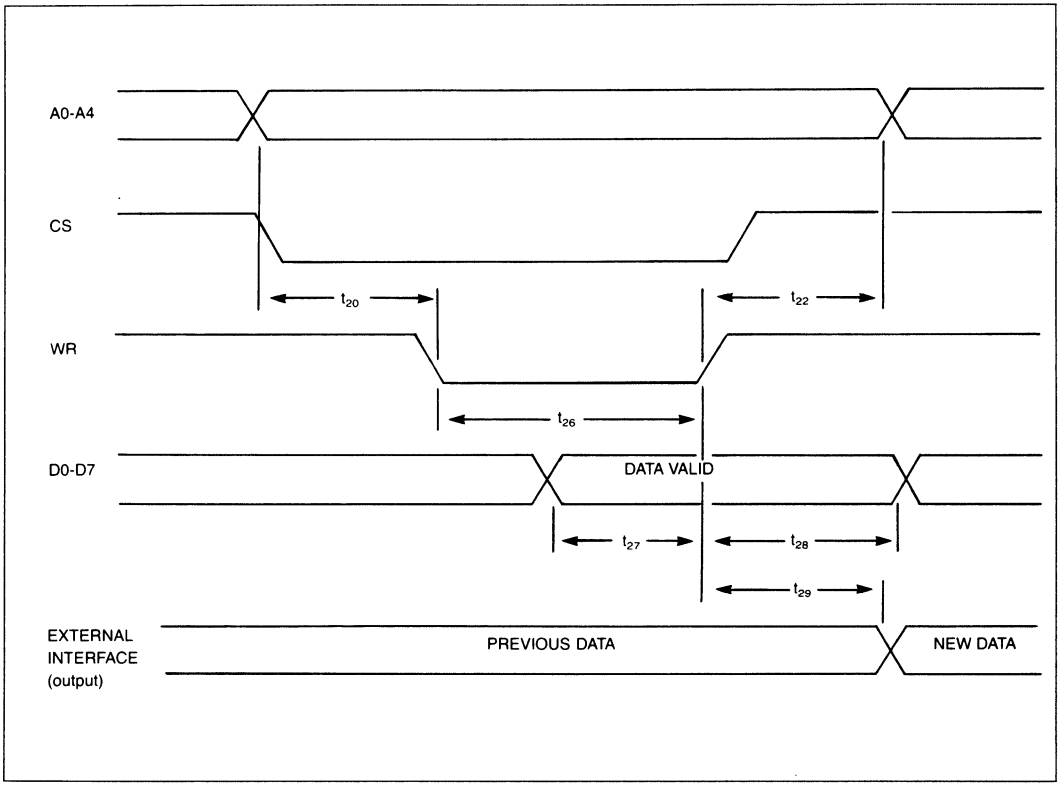


FIGURE 8. MICROPROCESSOR $\overline{WR}$ TIMING ($\overline{WR}$ CONTROLLED)

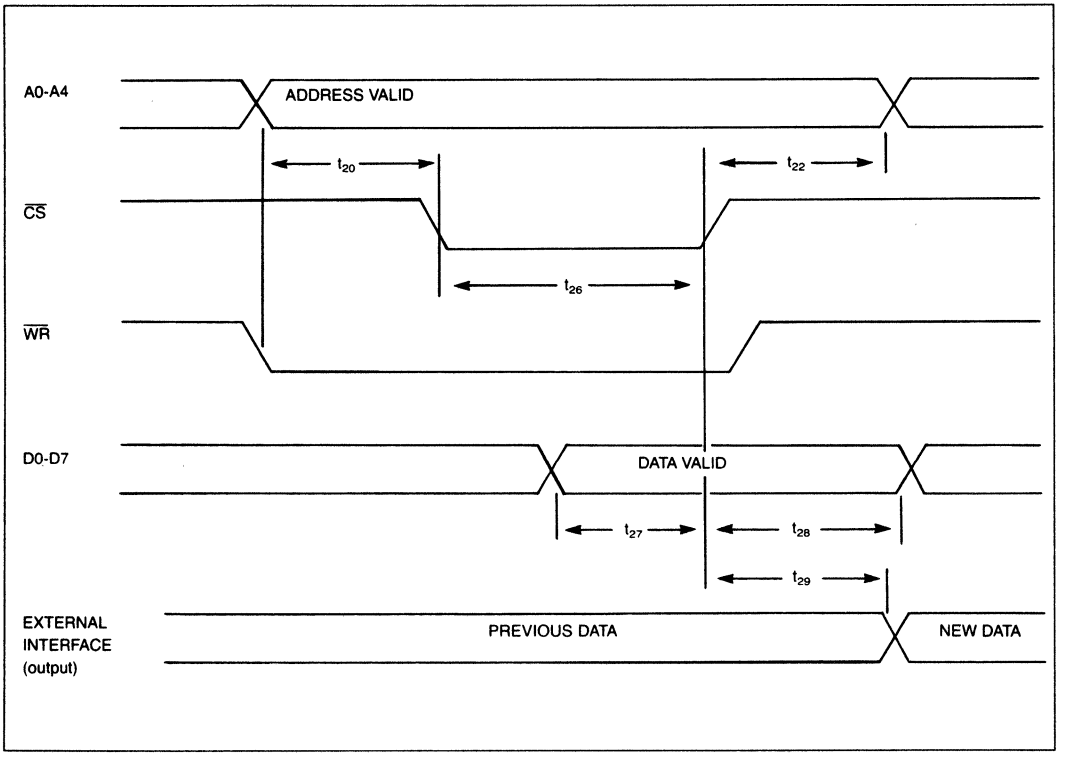


FIGURE 9. MICROPROCESSOR $\overline{WR}$ TIMING ($\overline{CS}$ CONTROLLED)

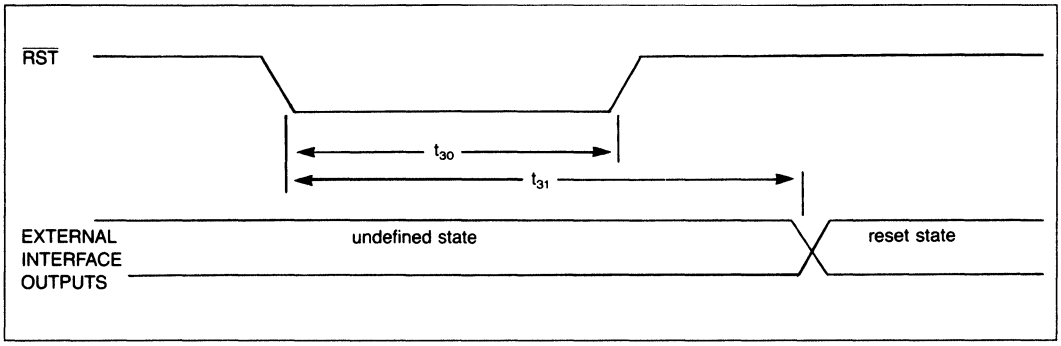


FIGURE 10. RESET TIMING

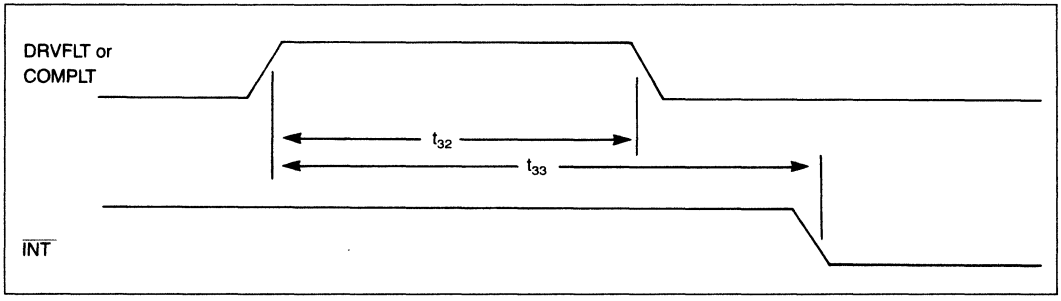


FIGURE 11. EXTERNALLY GENERATED INTERRUPT TIMING

BUFFER INTERFACE TIMING

(Data is coming out of the ADS10C00)
REQTIM = 1 in RESET register. (REQA true when internal data register is full.)

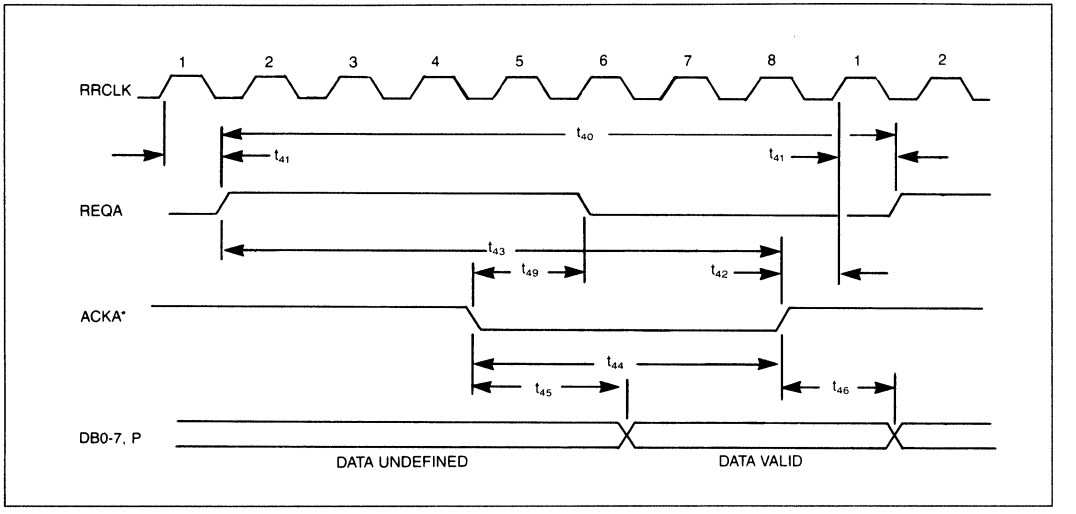


FIGURE 12. ASYNCHRONOUS MODE DATA BUS READ TIMING

REQTIM = 0 in RESET register. (REQA true one bit time before internal data register is full. Note that the cycles overlap by one bit time.)

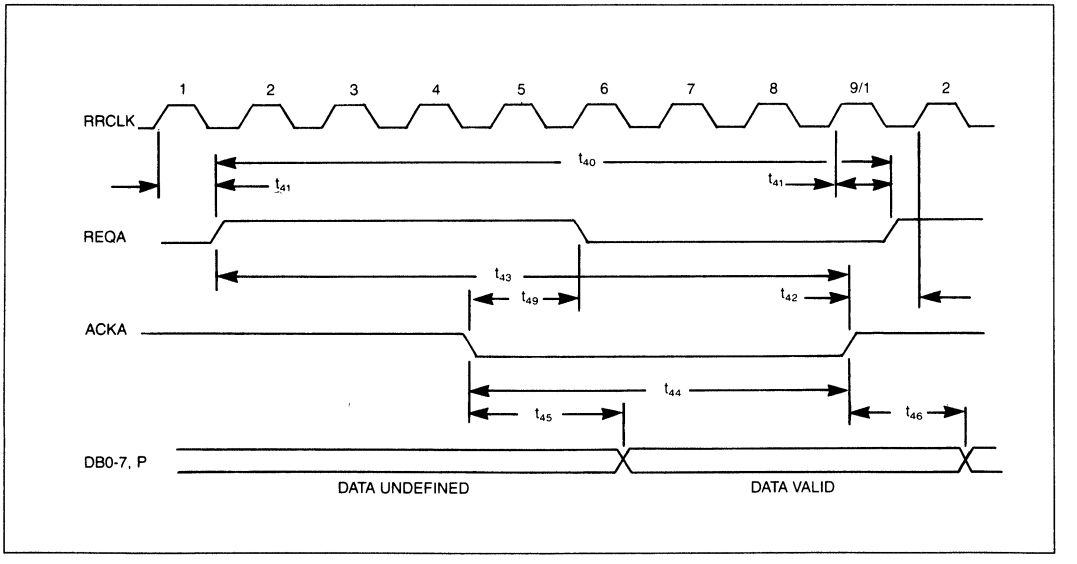


FIGURE 12A. ASYNCHRONOUS MODE DATA BUS READ TIMING

(Data is going into the ADS10C00)
REQTIM = 0 in RESET register. (REQA true when internal data register is empty.)

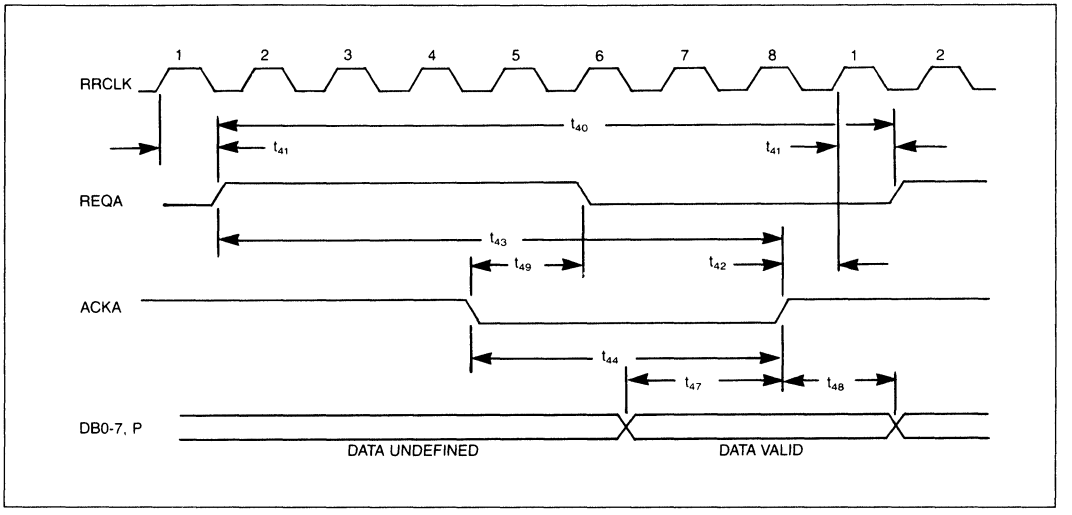


FIGURE 13. ASYNCHRONOUS MODE DATA BUS WRITE TIMING

REQTIM = 0 in RESET register. (REQA true one bit time before internal data register is empty. Note that the cycles overlap by one bit time.)

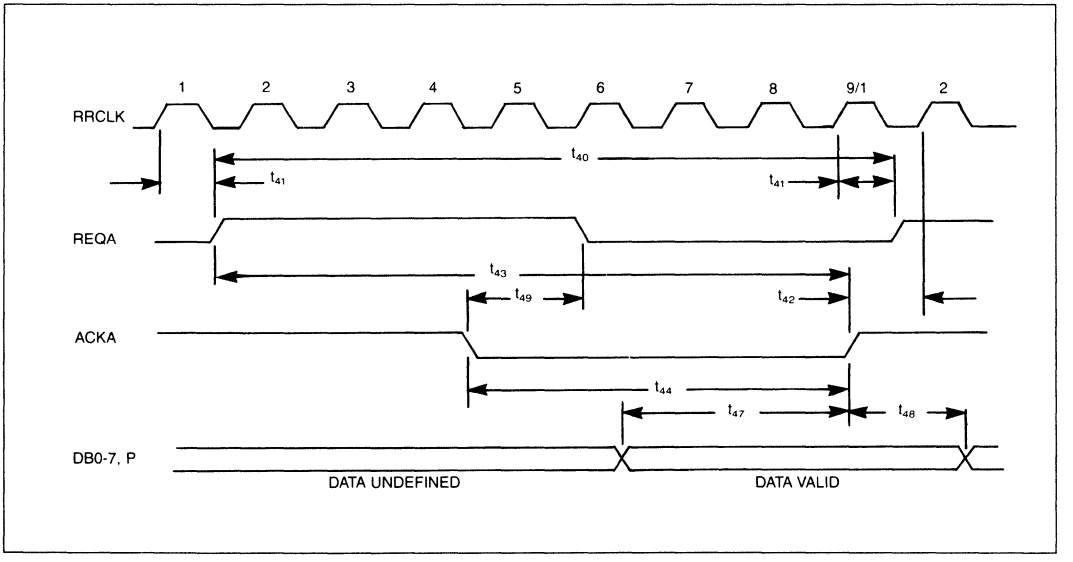


FIGURE 13A. ASYNCHRONOUS MODE DATA BUS WRITE TIMING

SERIAL DATA TIMING

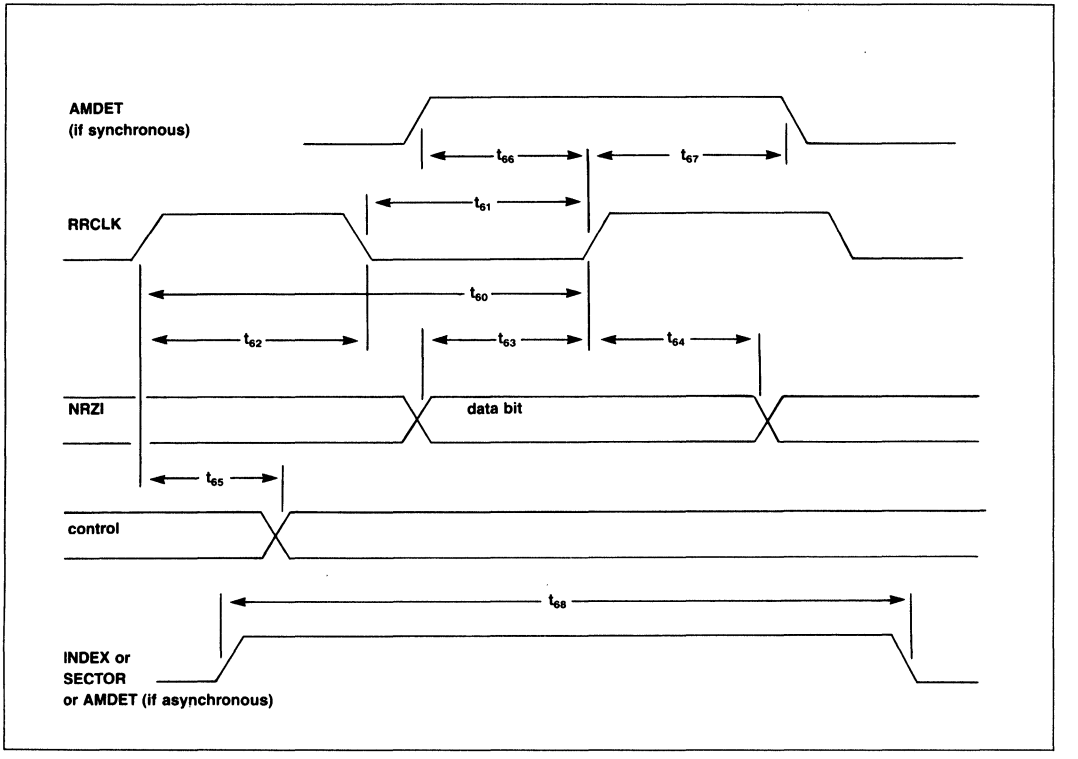


FIGURE 14. NRZ DATA INPUT TIMING

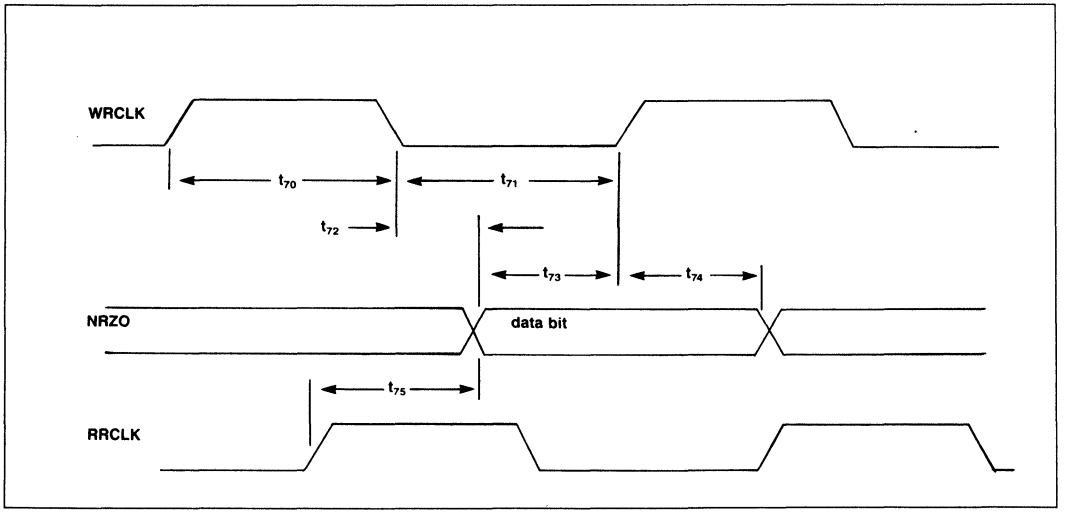


FIGURE 15. NRZ DATA OUTPUT TIMING

AC CHARACTERISTICS

CPUCLK AND OSC TIMING

Timing Parameter	Description	Min	Max	Units
t_1	TTL source X1 high or low (*1)	13		ns
t_2	TTL source X1 cycle time	40		ns
t_3	TTL source X1 rise or fall time (*1)		5	ns
t_4	OSC high or low when: (*2)			
	X1/1 crystal (*3)	10	---	ns
	X1/2 crystal (*3)	27	33	ns
	X1/1 TTL source (*5)	16	24	ns
	X1/2 TTL source (*4)	36	44	ns
t_5	CPUCLK high or low when: (*2)			
	X1/2 crystal (*3)	27	33	ns
	X1/3 crystal (*3)	36	54	ns
	X1/4 crystal (*3)	54	66	ns
	X1/6 crystal (*3)	81	99	ns
	X1/2 TTL source (*4)	36	44	ns
	X1/3 TTL source (*5)	48	72	ns
	X1/4 TTL source (*4)	72	88	ns
	X1/6 TTL source (*4)	108	132	ns
t_6	OSC cycle time when:			
	X1/1 crystal (*3)	30	125	ns
	X1/2 crystal (*3)	60	250	ns
	X1/1 TTL source (*4)	40	---	ns
	X1/2 TTL source (*4)	80	---	ns
t_7	CPUCLK cycle time when:			
	X1/2 crystal (*3)	60	250	ns
	X1/3 crystal (*3)	90	375	ns
	X1/4 crystal (*3)	120	500	ns
	X1/6 crystal (*3)	180	750	ns
	X1/2 TTL source (*4)	80	---	ns
	X1/3 TTL source (*4)	120	---	ns
	X1/4 TTL source (*4)	160	---	ns
	X1/6 TTL source (*4)	240	---	ns
t_8	CPUCLK and OSC rise or fall time (*2)		5	ns

NOTES:

(*1): Times are measured relative to V_{IH} and V_{IL}.

(*2): High and low times are measured relative to the midpoints between V_{OL} and V_{OH}. Rise and fall times are measured bewteen V_{OH} and V_{OL}.

(*3): Assumes 33.3 MHz crystal across X1 and X2 for min times, 8.0 MHz crystal for max times.

(*4): Assumes 25.0 MHz TTL source to X1.

(*5): Assumes 25.0 MHz TTL source to X1, 50/50 duty cycle.

CPU INTERFACE TIMING

NOTE: $\overline{RE}$ = $\overline{RD}$ or $\overline{CS}$. $\overline{WE}$ = $\overline{WR}$ or $\overline{CS}$.

Timing Parameter	Description	Min	Max	Units
t_{20}	address valid to $\overline{RE}$ or $\overline{WE}$	20		ns
t_{21}	$\overline{RE}$ pulse width	100		ns
t_{22}	$\overline{RE}$ or $\overline{WE}$ to address change	0		ns
t_{23}	$\overline{RE}$ true to data valid		95	ns
t_{24}	$\overline{RE}$ false to data hold	20	60	ns
t_{25}	input port setup to $\overline{RE}$ true (*1)	80		ns
t_{26}	$\overline{WE}$ pulse width	100		ns
t_{27}	data setup to $\overline{WE}$ false	80		ns
t_{28}	$\overline{WE}$ false to data hold	0		ns
t_{29}	$\overline{WE}$ false to output change (*2)		80	ns
t_{30}	$\overline{RST}$ pulse width	100		ns
t_{31}	$\overline{RST}$ true to stable outputs		150	ns
t_{32}	DRVFLT or COMPLT pulse width	100		ns
t_{33}	DRVFLT or COMPLT high to $\overline{INT}$ low		150	ns

NOTES:

(*1): Inputs are: PZ0-5, PY0-3 when defined as inputs, and AMDET when being used as a simple input pin.

(*2): Outputs are: PX0-7, and PY0-3 when defined as outputs.

BUFFER INTERFACE TIMING

Timing Parameter	Description	Min	Max	Units
t_{40}	DMA (REQA) cycle time (*1)		$8*t_{cyc}$	
t_{41}	RRCLK true to REQA true		40	ns
t_{42}	$\overline{ACKA}$ false to RRCLK true	20		ns
t_{43}	REQA true to $\overline{ACKA}$ false: (*1) REQTIM = 0 REQTIM = 1			 $8*t_{cyc}-t_{41}-t_{42}$ $9*t_{cyc}-t_{41}-t_{42}$
t_{44}	$\overline{ACKA}$ active low	100		ns
t_{45}	$\overline{ACKA}$ true to data valid		60	ns
t_{46}	$\overline{ACKA}$ false to data hold	10	60	ns
t_{47}	data setup to $\overline{ACKA}$ false	30		ns
t_{48}	$\overline{ACKA}$ false to data hold	5		ns
t_{49}	$\overline{ACKA}$ true to REQA false		35	ns

NOTES:
(*1): t_{cyc} is the RRCLK cycle time used.

SERIAL DATA TIMING

Timing Parameter	Description	Min	Max	Units
t_{60}	RRCLK cycle time	37		ns
t_{61}	RRCLK low (*1)	14		ns
t_{62}	RRCLK high (*1)	14		ns
t_{63}	NRZI setup to RRCLK high	10		ns
t_{64}	RRCLK high to NRZI hold	10		ns
t_{65}	RRCLK high to new control out (*3)		30	ns
t_{66}	AMDET setup to RRCLK high (*4)	10		ns
t_{67}	RRCLK high to AMDET hold (*4)	10		ns
t_{68}	asynchronous input width (*2) (*5)	$2*t_{cyc}$		ns
t_{70}	WRCLK high (*2) (*6)	t_{rlo}–6.0		ns
t_{71}	WRCLK low (*2) (*6)	t_{rhi}–6.0		ns
t_{72}	WRCLK low to NRZO change (*6)	–3.5	3.5	ns
t_{73}	NRZO setup to WRCLK high (*6)	t_{rhi}-9.5		ns
t_{74}	WRCLK high to NRZO hold (*6)	t_{rlo}-9.5		ns
t_{75}	RRCLK high to NRZO change		30	ns

NOTES:

(*1): High and low times measured relative to V_{IH} and V_{IL}.

(*2): t_{rlo} and t_{rhi} are the clock low and clock high (respectively) for the RRCLK input used. t_{cyc} is RRCLK cycle time used.

(*3): Control outputs are: SEQOUT, WG, RG, and AMENA.

(*4): When AMDET is supplied from a synchronous source.

(*5): Asynchronous inputs are: INDEX, SECTOR, and AMDET when it is supplied from an asynchronous source.

(*6): Where the RRCLK input is driven from 0.4V (V_{IL}) to 2.4V (V_{IH}).

PIN/SIGNAL SUMMARY

PIN	SIGNAL	I/O	FUNCTION	PIN	SIGNAL	I/O	FUNCTION
1	DB7	I/O	BUFFER	35	COMPLT	I	DISK CONTROL
2	DB6	I/O	BUFFER	36	CPUCLK	O	CPU INTERFACE
3	DB5	I/O	BUFFER	37	X1	I	CPU INTERFACE
4	DB4	I/O	BUFFER	38	X2	O	CPU INTERFACE
5	DB3	I/O	BUFFER	39	PZ5	I	DISK CONTROL
6	DB2	I/O	BUFFER	40	PZ4	I	DISK CONTROL
7	DB1	I/O	BUFFER	41	PZ3	I	DISK CONTROL
8	DB0	I/O	BUFFER	42	PZ2	I	DISK CONTROL
9	V_{SS}	I	GROUND	43	V_{SS}	I	GROUND
10	$\overline{CS}$	I	CPU INTERFACE	44	PZ1	I	DISK CONTROL
11	D0	I/O	CPU INTERFACE	45	PZ0	I	DISK CONTROL
12	D1	I/O	CPU INTERFACE	46	PY3	I,O	DISK CONTROL
13	D2	I/O	CPU INTERFACE	47	PY2	I,O	DISK CONTROL
14	D3	I/O	CPU INTERFACE	48	PY1	I,O	DISK CONTROL
15	D4	I/O	CPU INTERFACE	49	PY0	I,O	DISK CONTROL
16	D5	I/O	CPU INTERFACE	50	PX7	O	DISK CONTROL
17	D6	I/O	CPU INTERFACE	51	PX6	O	DISK CONTROL
18	D7	I/O	CPU INTERFACE	52	PX5	O	DISK CONTROL
19	$\overline{RD}$	I	CPU INTERFACE	53	PX4	O	DISK CONTROL
20	$\overline{WR}$	I	CPU INTERFACE	54	PX3	O	DISK CONTROL
21	A4	I	CPU INTERFACE	55	PX2	O	DISK CONTROL
22	A3	I	CPU INTERFACE	56	PX1	O	DISK CONTROL
23	A2	I	CPU INTERFACE	57	PX0	O	DISK CONTROL
24	A1	I	CPU INTERFACE	58	WG	O	DISK DATA
25	A0	I	CPU INTERFACE	59	RG	O	DISK DATA
26	V_{dd}	I	+5 VOLTS	60	V_{dd}	I	+5 VOLTS
27	$\overline{INT}$	O	CPU INTERFACE	61	$\overline{RST}$	I	CPU INTERFACE
28	SECTOR	I	DISK CONTROL	62	WRCLK	O	DISK DATA
29	INDEX	I	DISK CONTROL	63	NRZO	O	DISK DATA
30	AMDET	I	DISK DATA	64	RRCLK	I	DISK DATA
31	AMENA	O	DISK DATA	65	NRZI	I	DISK DATA
32	SEQOUT	O	DISK DATA	66	$\overline{REQA}$	O	BUFFER
33	OSC	O	CPU INTERFACE	67	$\overline{ACKA}$	I	BUFFER
34	DRVFLT	I	DISK CONTROL	68	DBP	I/O	BUFFER

ADS10C00 PROGRAMMERS BENCH REFERENCE (PBR)

Addr	Name	Dir	Size	Addr	Name	Dir	Size
00	SRESET	W	7–0	10	ECC0	W	7–0
01	SISR	R/W	7–0	11	ECC1	W	7–0
02	SIMR	R/W	7–0	12	ECC2	W	7–0
03	SEQSTS/PYC	R/W	7–0/3–0	13	ECC3	W	7–0
04	CSERR	R/W	3–0	14	ECC4	W	7–0
05	CSCTL	R/W	7–0	15	ECC5	W	7–0
06	CSVAL	R/W	7–2;7–0	16	do not use — test only		
07	CSCNT	R/W	7–4,0;7–0	17	SKIP	W	4–0
08	PORTX	R/W	7–0	18	ID0	R/W	7–0
09	PORTY	R/W	3–0	19	ID1	R/W	7–0
0A	PORTZ/AMC	R/W	5–0/7–0	1A	ID2	R/W	7–0
0B	SEQCTL	R/W	5–0	1B	ID3	R/W	7–0
0C	START	R/W	4–0	1C	ID4	R/W	7–0
0D	ECCZ/LOOP	R/W	7–0/4–0	1D	ID5	R/W	7–0
0E	ECCCTL	R/W	7–0	1E	ID6	R/W	7–0
0F	SECCNT	R/W	7–0	1F	ID7	R/W	7–0

TRUE = 1 FOR ALL BITS

SRESET (00)		SISR (01) AND SIMR (02)	
bit	**output**	**bit**	**input/output**
7	CLKDIV	7	GINT
6	OSCDIV	6	IDFULL
5	IDCHK	5	DXFER
4	DCHK	4	COMPLT
3	ECCSIZ	3	SEQSTP
2	REQTIM	2	SECEND
1	ID3$4	1	SM$IX
0	SRST	0	FAULT
SEQSTS (03)		**PYC (03)**	
bit	**input**	**bit**	**output**
7	DATFLD	7	
6	ECCEN	6	
5	LAST	5	
4	ID	4	
3	CHK	3	PY3OUT
2	WAIT	2	PY2OUT
1	AMDET	1	PY1OUT
0	SEQOUT	0	PY0OUT
CSERR (04)		**CSCTL (05)**	
bit	**input/output**	**bit**	**input/output**
7		7	SVSEL
6		6	CWSEL
5		5	WG
4		4	RG
3	FAIL	3	AM
2	RTY	2	CMPEN
1	DAC	1	SKPEN
0	SEQOUT	0	JMPEN
CSVAL (06)		**CSCNT (07)**	
bit	**input/output**	**bit**	**input/output**
7	BUFF	7	WDAM (COUNT)
6	NOXFER	6	WIAM
5	LAST	5	WIX
4	ID	4	WSM
3	CHK	3	
2		2	
1		1	
0		0	STOP

SEQCTL (0B)			ECCCTL (0E)		
bit	**input**	**output**	**bit**	**input**	**output**
7		RGERLY	7	ECCOUT	ECCINL
6			6	COR04B	ECCSHT
5	ECCERR		5	COR05B	ECCCLR
4	IDERR		4	COR06B	ECCSET
3	PTYERR	IXMASK	3	COR07B	ECCNIT
2	SYNCER	SMMASK	2	COR08B	DISCHK
1	CMPERR	RCMP	1	COR09B	DISPTY
0		KILL	0	COR10B	ECCINM
ECCZ (0D)					
bit	**input**	**output**			
7	COR11B				
6	COR12B				
5	COR13B				
4	COR14B				
3	COR15B				
2	COR16B				
1	COR17B				
0	COR18B				