APPLICATION NOTE

HOW TO CONVERT A TMS7742 BASED APPLICATION
TO TAKE ADVANTAGE OF THE NEW TMS77C82 CMOS MICROCONTROLLER WITH ON-CHIP EPROM

I - INTRODUCTION

The TEXAS INSTRUMENTS TMS7000 microcontroller family contains numerous
members designed to support a wide range of applications that require
more and more performance for a lower and lower cost. The TMS77C82 is
hardware & software compatible with the TMS7742 but provides the
required additional performance whilst reducing "glue logic" and
consuming much less power that the TMS7742.

This report brings the first support to the designers for advantageously
converting a TMS7742 NMOS EPROM on-chip microcontroller design into a
TMS77C82 CMOS EPROM on-chip MCU one.
It gives a detailed comparison between the two microcontrollers
focusing on key features, peripheral memory map, pinning, reset,
programmation and emulation. It is earnestly recommended that designers
refer to the TMS77C82 data sheet and the TMS7000 data manual edited by
TEXAS INSTRUMENTS technical library group.

For any further information related to the TMS77C82 call the nearest
TEXAS INSTRUMENTS sales office or regional technology center.

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II - KEY FEATURES

The major differences between both circuits are as follows :

	TMS77C82	TMS7742
TECHNOLOGY	CMOS	NMOS
MEMORY	8K-BYTE EPROM	4K-BYTE EPROM
EQUIVALENT EPROM	TMS27C64	TMS2732A
MEMORY EXPANSION	64K BYTES	64K BYTES
I/O	CMOS COMPATIBLE 24 BIDIRECTIONAL PINS	TTL COMPATIBLE I/O PINS 22 BIDIRECTIONAL PINS +2 INPUT PINS
SERIAL CLOCK	SCLK ON PIN A4 (10)	SCLK ON PIN A6(15)
TIMERS ON CHIP	TWO 16 BITS WITH 5 BITS PRESCALE ONE 8 BITS WITH 2 BITS PRESCALE CAPTURE LATCH, CASCADABLE	TWO 8 BITS WITH 5 BITS PRESCALE ONE 8 BITS WITH 2 BITS PRESCALE CAPTURE LATCH
INTERRUPTS	EXTERNAL INTERRUPT PRGM FOR EDGE OR EDGE/LEVEL TRIGGERING . FOR RISING AND FALLING EDGE DETECTION BY SOFTWARE.	PRIORITIZED BY SOFTWARE. EDGE OR EDGE/LEVEL TRIGGERING AT MASKING .
VCC	3V TO 6V	4.5V TO 5.5V
FREQUENCY OSC.	0.5 MHz TO 8 MHz	1 TO 5 MHz
CLOCK OPTION	XTAL	XTAL
PACKAGE	40 PIN	40 PIN (same mechanical data)

Because the TMS77C82 includes twice the EPROM capacity of the TMS7742 and
it is a CMOS processed chip, the TMS77C82 drastically reduces cost of design

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III - PERIPHERAL MEMORY MAP

	77C82 (70CX2)		7742 (70X2)		70CX0
IOCNT0	P0		P0	>0100	P0
IOCNT2	P1>	0101	-		-
T1(LS) DAT	P13>	010D	P2	>0102	P2
T1CTL(0)	P15>	010F	P3	>0103	P3
APORT	P4		P4	>0104	P4
ADDR	P5		P5	>0105	-
BPORT	P6		P6	>0106	P6
RESERVED	P7		P7	>0107	P7
CPORT	P8		P8	>0108	P8
CDDR	P9		P9	>0109	P9
DPORT	P10		P10	>010A	P10
DDDR	P11		P11	>010B	P11
T1MSDATA	P12>	010C	-		-
IOCNT1	P2>	0102	P16	>0110	-
RESERVED	P3>	0103	P1	>0101	P1
T1CTL1	P14>	010E	-		-
T2MSDATA	P16>	0110	-		-
T2LSDATA	P17>	0111	P18	>0112	-
T2CTL0	P19		P19	>0113	-
SMODE	P20>	0114	P17	>0111	-
SCTL0	P21>	0115	P17		-
SSTAT	P22>	0116	P17		-
T3DATA	P23>	0117	P20	>0114	-
SCTL1	P24>	0118	P21	>0115	-
RXBUF	P25>	0119	P22	>0116	-
TXBUF	P26>	011A	P23	>0117	-
RESERVED	P27- P35		-		-
NOT AVAILA (in single or PERIPH.	P36 - P255		P12 - P15 P24 - P255		P12-P255

IV - PINNING EQUIVALENCE

   When using the serial clock pin (SCLK), a modification of the
   application hardware is mandatory.

   SCLK is on pin #10 (A4) when using the TMS77C82.
                #15 (A6)   TMS7742

   Otherwise the two microcontrollers have exactly the same pin-out
   configuration.

V - INPUT/OUTPUT LEVELS

   77C82 input/output's are CMOS compatible, whereas on 7742 they are TTL
   compatible.
   Output current capabilities are shown in the following table :
   (For VCC=5V)

	TMS77C82	TMS7742
VOH min/IOH	3.9 V/-0.7 mA	2.4 V/-400 uA
VOL max/IOL	1.1 V/2.5 mA	0.4 V/3.2 mA

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VI - INITIALIZATION (reset functions)

     4.1) SERIAL PORT
          Should be programmed in the same manner than 7742 's, with the
          differences in the port register addresses.

          SMODE   is   P20   (P17 for the TMS7742)
          SCTL0   is   P21   (P17)
          TIMER 3   at   P23   (P20)
          SCTL1   is   P24   (P21)
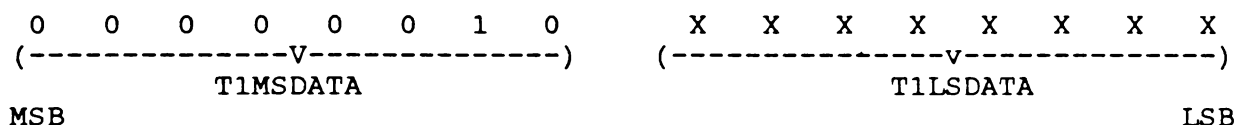
          The serial port can be reset in three ways : hardware reset (via
          the RESET pin) or software reset (via the UR bit in SCTL0), or by
          writing to the SMODE register.

     4.2) TIMERS
          Only differences between the two devices are shown here.
          Register for which there is no difference is T2CTL0 (P19).

Two 16 bit timers w/ 5 bit prescale	Two 8 bit timers w/5 bit prescale
internal clock source : Fosc /4	internal clock source : Fosc/16
T1LSDATA register is P13> 010D	T1DATA register is P2> 0102
T1CTL0 register is P15> 010F	T1CTL register is P3> 0103
T2LSDATA register is P17	T2DATA register is P18

Therefore each 16 bit timer data should be programmed as :

```
     0   0   0   0   0   0   1   0        X   X   X   X   X   X   X   X
    (---------------V--------------)     (---------------v--------------)
              T1MSDATA                             T1LSDATA
     MSB                                                              LSB
```
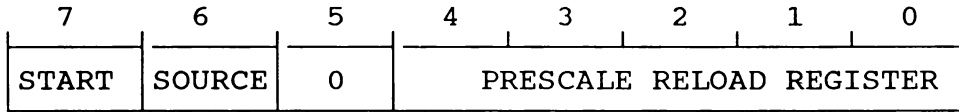
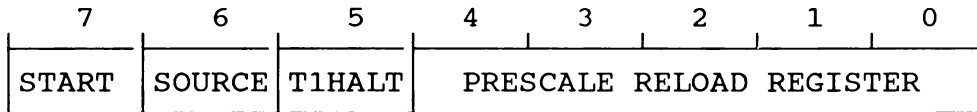to obtain same internal clock and 8 bit timer as in 7742, if using
internal clock source.

If external clock source is used then the 8 MSbits should be set at "0".
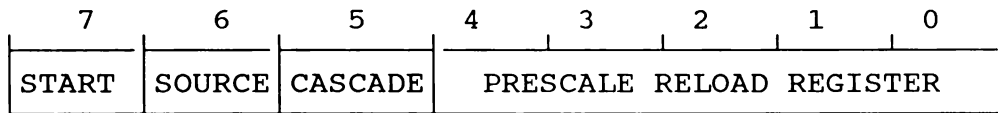
During write mode :

T1CTL / 7742

7	6	5	4	3	2	1	0
START	SOURCE	0	PRESCALE RELOAD REGISTER				

T1CTL0 / 77C82

7	6	5	4	3	2	1	0
START	SOURCE	T1HALT	PRESCALE RELOAD REGISTER				

0-TIMER 1 REMAINS ACTIVE DURING IDLE
1-TIMER 1 WILL HALT DURING IDLE

T2CTL / 7742

7	6	5	4	3	2	1	0
START	SOURCE	CASCADE	PRESCALE RELOAD REGISTER				

0- SOURCE BIT DETERMINE CLOCK SOURCE
1- CLOCK SOURCE IS TIMER 1
    RELOAD SIGNAL; OVERRIDES SOURCE BIT

T2CTL0 / 77C82

7	6	5	4	3	2	1	0
START	SOURCE	T2HALT	PRESCALE RELOAD REGISTER				
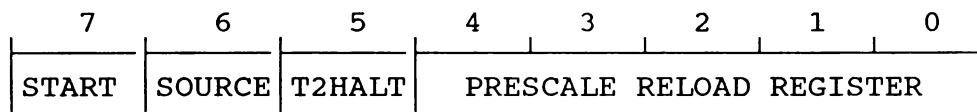
0-TIMER 2 REMAINS ACTIVE DURING IDLE
1-TIMER 2 WILL HALT DURING IDLE

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```
          T2CTL1 / 77C82
  7
+----------+-------+----+----+----+----+----+----+
| CASCADE  | T2OUT | X  | X  | X  | X  | X  | X  |
+----------+-------+----+----+----+----+----+----+
```

0-DATA REGISTER BIT B1
1-TIMER2-OUT TOGGLES B1 WHEN T1 DECREMENTS THROUGH 0

0-SOURCE BIT DETERMINES CLOCK SOURCE
1-CLOCK SOURCE IS TIMER1 RELOAD SIGNAL;OVERRIDES SOURCE BIT

If the cascade bit in timer 2 of the 7742 is set to 1, then the cascadet
bit of T2CTL1 should also be set to 1.

T1HALT bit of T1CTL0 in the 77C82 should always be set to 0.
T2HALT bit of T2CTL0 in the 77C82 should always be set to 0.
T2OUT bit of T2CTL1 in the 77C82 should always be set to 0.

4.3) INTERRUPT CONFIGURATION

Some 77C82 interrupts are programmable by software, and thus need
to be positionned initially :

```
          T2CTL0 / 77C82

   7     6     5      4     3     2     1      0
+-----+-----+------+------+-----+-----+------+------+
|  0  |  0  | INT3 | INT3 |  0  |  0  | INT1 | INT1 |
|     |     | EDGE | POL. |     |     | EDGE | POL. |
+-----+-----+------+------+-----+-----+------+------+
```

0- ACTIVE LOW/FALLING EDGE
1- ACTIVE HIGH/RISING EDGE

0- EDGE & LEVEL SENSITIVE
1- EDGE SENSITIVE ONLY

0- ACTIVE LOW/FALLING EDGE
1- ACTIVE HIGH/RISING EDGE

0- EDGE & LEVEL SENSITIVE
1- EDGE SENSITIVE ONLY

Therefore, depending on customer application : edge (7742), or
edge/level (EPP002), bits 5 and 1 shall be initialized at 1 or 0.
Bits 0 and 4 shall be initialized at 0.

VII - HOW TO PROGRAM A 77C82

On data I/O EPROM programmer (EPROM MODE)
    need : SOCKET 40-28 adaptor

    with   RESET (pin 14),
            INT1 (pin 13),
            INT3 (pin 12),
            XTAL2 (pin 17) grounded

On EVM (EVM-7000N or EVM-700C)
    need : SOCKET 40-28 adaptor
           same as the one used for data I/O .
    RESET (14) and XTAL2 (17) must be grounded
    during program and read operations.

VPP   : VPP for 77C82 is 12V

    On EVM, this option is programmed as follows :

    ? 12   (enter 12V calibrate command)
    ARE YOU SURE ? Y   (enter Y, adjust R32 for VPP)
    <ANY KEY>   (any key return to monitor)

TMS77C82		TMS27C64				TMS27C64		TMS77C82	
PIN	**FUNCTION**			**SOCKET**			**FUNCTION**	**PIN**	
	MC						Vcc		
36	——	Vpp		1	28		Vcc ——	25	
	A5						A6/SCLK		
16	——	A12		2	27		$\overline{PGM}$ ——	15	
	A0						NC		
6	——	A7		3	21			D0	
	A1			INTERFACE			A8 ——	27	
7	——	A6		4	25			D1	
	A2			SOCKET			A9 ——	26	
8	——	A5		5	24			D2	
	A3						A11 ——	24	
9	——	A4		6	23			A7/EC1	
	A4						$\overline{G}$ ——	11	
10	——	A3		7	22			D3	
	D7						A10 ——	23	
19	——	A2		8	21			D4	
	D6						$\overline{E}$ ——	22	
20	——	A1		9	20			C7	
	D5						Q8 ——	35	
21	——	A0		10	19			C6	
	C0						Q7 ——	34	
28	——	Q1		11	18			C5	
	C1						Q6 ——	33	
29	——	Q2		12	17			C4	
	C2						Q5 ——	32	
30	——	Q3		13	16			C3	
	VSS						Q4 ——	31	
40	——	GND		14	15				

VIII - SIMULATION

The set of instructions and cycle times of the TMS77C82 are identical to that of all TMS7000 microcontrollers.

For TMS77C82 emulation in microcontroller mode, the evaluation module, EVM 7000C-1 equipped with a TMS70C02 CPU together with the programmer socket part # RTC/PGM C82-06, provides a low-cost but complete development tool. Included in the firmware on the EVM are editor, monitor, assembler and debug functions such as single step etc.....

For development & emulation on XDS (TI extended development system) the version to be used is TMDX 70622A1.

The cross-assembler/linker software for TMS77C82 are available for both TI & IBM compatible PC'S (with part # TMDS 7040810-02) and for DEC vax computers (with part # TMDS 7040210-08). In addition a C-compiler exists for IBM compatible PC'S.

All these development tools (and technical literature) are available from TEXAS INSTRUMENTS & authorised distributors.

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TI Sales Offices

BELGIQUE/BELGIË
S.A. Texas Instruments Belgium N.V.
11, Avenue Jules Bordetlaan 11,
1140 Bruxelles/Brussel
Tel : (02) 242 30 80
Telex : 61161 TEXBEL

DANMARK
Texas Instruments A/S
Marielundvej 46E
2730 Herlev
Tel : 02 91 74 00
Telefax : 02 91 84 00
Telex : 35123 TEXIN

DEUTSCHLAND
Texas Instruments
Deutschland GmbH.
Haggertystraße 1
8050 Freising
Tel : 0 81 61/80-0 od. Nbst
Telex : 5 26 529 texin d
Btx : *280505 #

Kurfürstendamm 195-196
1000 Berlin 15
Tel : 030/8 82 73 65
Telex : 5 26 529 texin d

Düsseldorfer Straße 40
6236 Eschborn 1
Tel : 06196/80 70
Telex : 5 26 529 texin d

III. Hagen 43/Kibbelstraße 19
4300 Essen 1
Tel : 0201/24 25-0
Telex 5 26 529 texin d

Kirchhorster Straße 2
3000 Hannover 51
Tel : 0511/64 80 21
Telex : 5 26 529 texin d

Maybachstraße II
7302 Ostfildern 2 (Nellingen)
Tel. 0711/34 03-0
Telex 5 26 529 texin d

EIRE
Texas Instruments Ireland Ltd
7/8 Harcourt Street
Dublin 2
Tel : (01) 78 16 77
Telex : 32626

ESPAÑA
Texas Instruments España S.A.
C/José Lázaro Galdiano No. 6
28036 Madrid
Tel : (1) 458 14 58
Telex : 23634
Fax : (1) 457 94 04

C/Diputacion, 279-3-5
08007 Barcelona
Tel : (3) 317 91 80
Telex : 50436
Fax : (3) 301 84 61

FRANCE
Texas Instruments France
8-10 Avenue Morane Saulnier - B.P. 67
78141 Vélizy Villacoublay cedex
Tel : Standard : (1) 30 70 10 03
        Service Technique : (1) 30 70 11 33
Telex : 698707 F

HOLLAND
Texas Instruments Holland B.V.
Hogehilweg 19
Postbus 12995
1100 AZ Amsterdam-Zuidoost
Tel : (020) 5602911
Telex : 12196

ITALIA
Texas Instruments Italia S.p.A.
Divisione Semiconduttori
Viale Europa, 40
20093 Cologno Monzese (Milano)
Tel : (02) 25300 1
Telex : 332633 MITEX I

Via Castello della Magliana, 38
00148 Roma
Tel. (06) 5222651
Telex 610587 ROTEX I

Corso Svizzera, 185
10100 Torino
Tel. (011) 774545

Via Amendola, 17
40100 Bologna
Tel. (051) 554004

NORGE
Texas Instruments Norge A/S
PB 106
Refstad (Sinsenveien 53)
0585 Oslo 5
Tel : (02) 155090

ÖSTERREICH
Texas Instruments Ges.m.b.H.
Hietzinger Kai 101-105
A-1130 Wien
Tel : 0222/91000
Telex : 136 796

PORTUGAL
Texas Instruments Equipamento
Electronico (Portugal) LDA.
R. Eng. Frederico Ulrich, 2650
Moreira Da Maia
4470 Maia
Tel : (2) 948 1003
Telex : 22485

SCHWEIZ/SUISSE
Texas Instruments Switzerland AG
Riedstraße 6
CH-8953 Dietikon
Tel : (01) 740 22 20
Telex : 825 260 TEXIN

SUOMI FINLAND
Texas Instruments OY
Ahertajantie 3
P.O. Box 81,
0201 Espoo
Tel : (90) 0-461-422
Telex : 121457

SVERIGE
Texas Instruments
International Trade Corporation
(Sverigefilialen)
Box 30,
S-163 93 Stockholm
Visit address : Isafjordsgatan 7, Kista
Tel : (08) 793 91 70
Telefax : (08) 751 97 15
Telex : 10377 SVENTEX S

UNITED KINGDOM
Texas Instruments Ltd.
Manton Lane,
Bedford,
England, MK41 7PA
Tel : (0234) 270 111
Telex : 82178

Technical Enquiry Service
Tel : (0234) 223000

TI Regional Technology Centres

DEUTSCHLAND
Texas Instruments
Deutschland GmbH.
Haggertystraße 1
8050 Freising
Tel : (08161) 80 40 43

Frankfurt/Main
Düsseldorfer Straße 40
6236 Eschborn
Tel : (0 61 96) 80 74 18

Kirchhorster Straße 2
3000 Hannover 51
Tel : (0511) 64 80 21

Maybachstraße 11
7302 Ostfildern 2 (Nellingen)
Stuttgart
Tel : (0711) 34 03-0

FRANCE
Centre de Technologie
Texas Instruments France
8-10 Avenue Morane Saulnier, B.P. 67
78141 Vélizy Villacoublay cedex
Tel : Standard : (1) 30 70 10 03
        Service Technique : (1) 30 70 11 33
Telex : 698707 F

Texas Instruments France
B. P. 5
06270 Villeneuve-Loubet
Tel : 93 22 20 01
Telex : 470127 F

HOLLAND
Texas Instruments Holland B.V.
Hogehilweg 19
Postbus 12995
1100 AZ Amsterdam-Zuidoost
Tel : (020) 5602911
Telex : 12196

ITALIA
Texas Instruments Italia S.p.A.
Divisione Semiconduttori
Viale Europa, 40
20093 Cologno Monzese (Milano)
Tel : (02) 25300 I
Telex : 332633 MITEX I

SVERIGE
Texas Instruments
International Trade Corporation
(Sverigefilialen)
Box 30
S-163 93 Stockholm
Visit address : Isafjordsgatan 7, Kista
Tel : (08) 793 91 70
Telefax : (08) 751 97 15
Telex : 10377 SVENTEX

UNITED KINGDOM
Texas Instruments Ltd.
Regional Technology Centre
Manton Lane,
Bedford,
England, MK41 7PA
Tel : (0234) 270 111
Telex : 82178

Technical Enquiry Service
Tel : (0234) 223000

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