SONY

CXA1841AQ

Quadruple Speed RF Amplifier for CD Player and CD-ROM

Description

The CXA1841AQ is an IC for RF signal processing of CD Player and CD-ROM.

Features

- Supports quadruple speed. (RF signal ≥ 8MHz)
- RF equalizer (cosine equalization method)
- Peak hold circuit time constant of mirror circuit can be adjusted.
- APC (Automatic Power Control) function

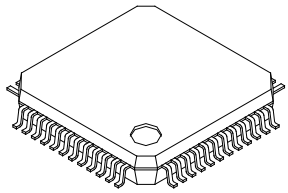
Absolute Maximum Ratings

• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	833	mW

Operating Conditions

Supply voltage	+4.5 to +5.5	V

48 pin QFP (Plastic)



Structure

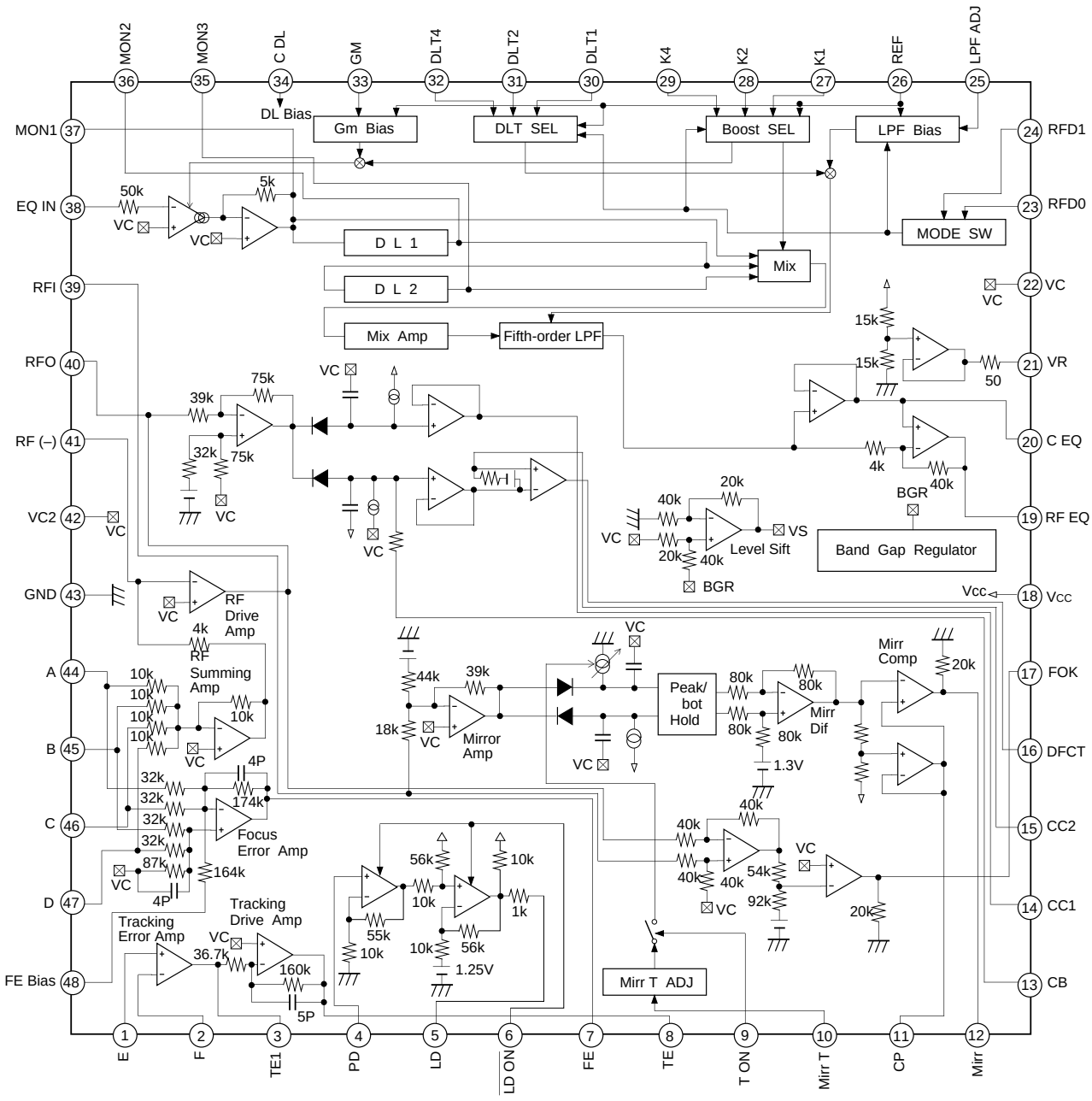
Bipolar silicon monolithic IC

Applications

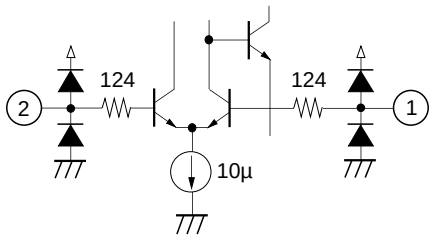
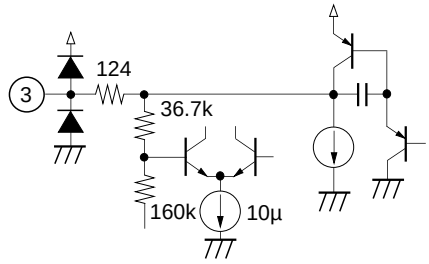
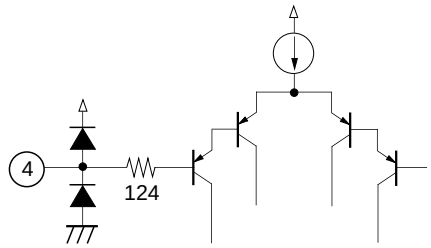
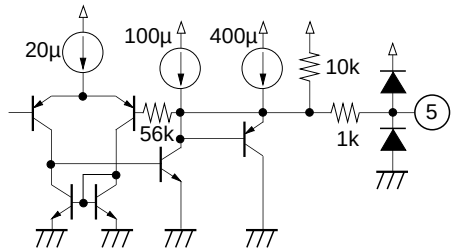
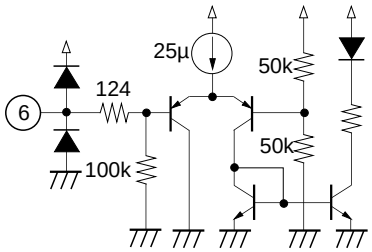
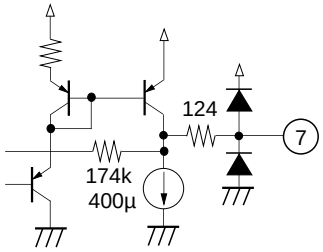
- CD players
- CD-ROM drive

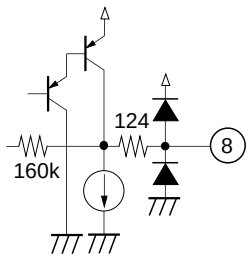
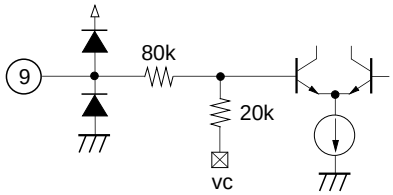
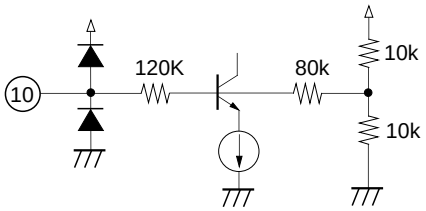
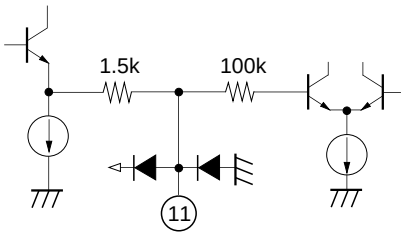
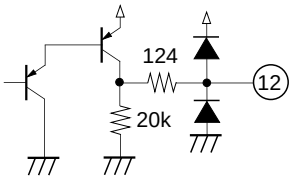
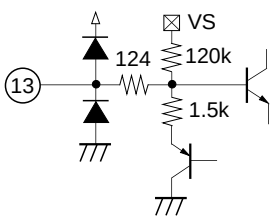
E95718A79

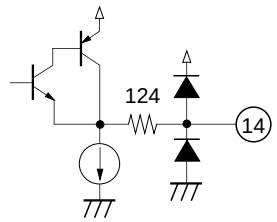
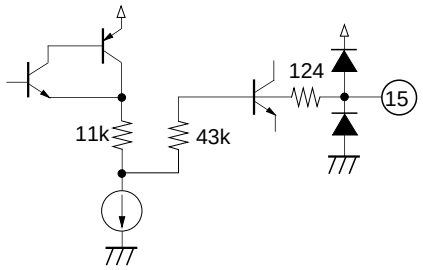
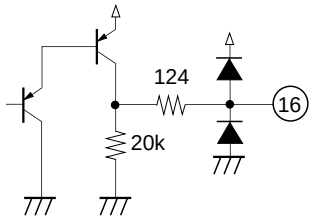
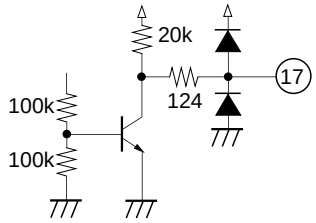
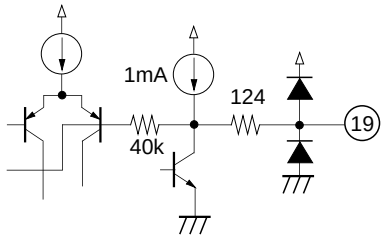
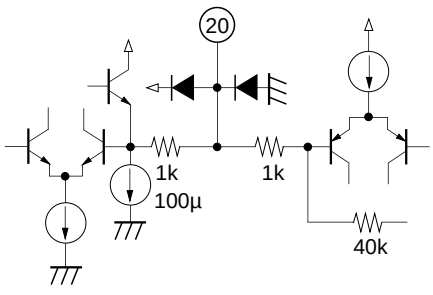
Block Diagram

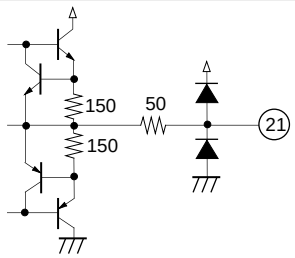
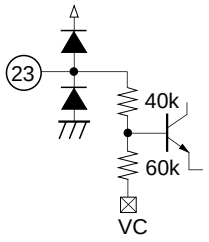
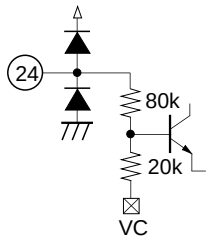
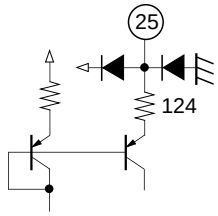
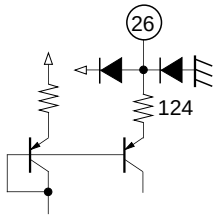
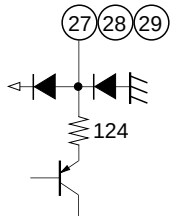


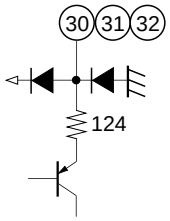
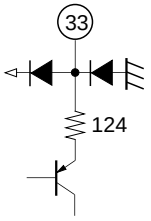
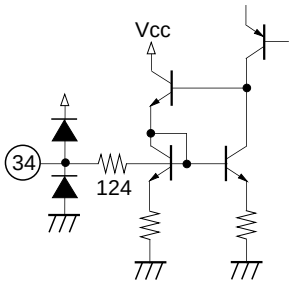
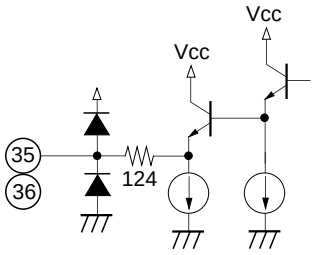
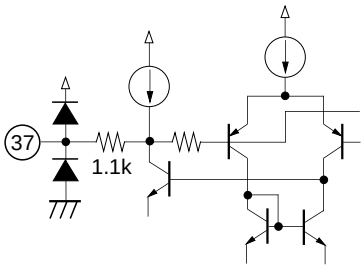
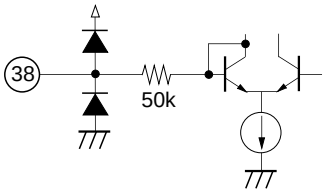
Pin Description

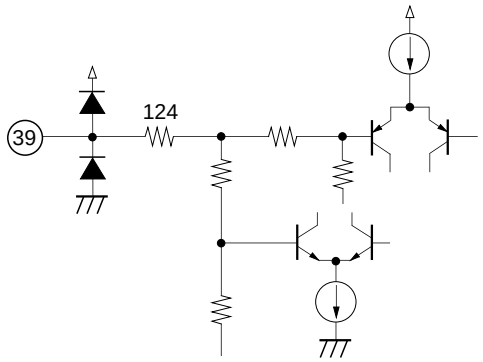
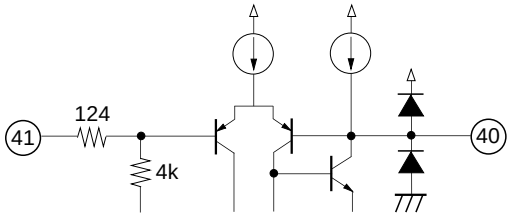
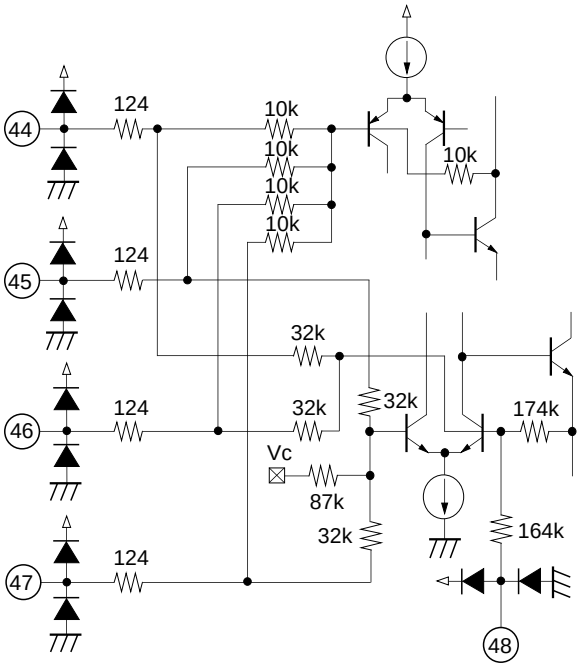
Pin No.	Symbol	I/O	Equivalent circuit	Description
1 2	E F	I I		Tracking error amplifier input.
3	TE1	O		Tracking error amplifier output and tracking error driver input.
4	PD	I		APC amplifier input.
5	LD	O		APC amplifier output.
6	$\overline{\text{LD ON}}$	I		APC amplifier ON/OFF switching. ON when connecting to GND; OFF when connecting to Vcc.
7	FE	O		Focus error amplifier output. (B + D) – (A + C) output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
8	TE	O		Tracking drive amplifier output.
9	T ON	I		Peak hold time constant switching. ON when connecting to Vcc; OFF when connecting to GND.
10	Mirr T	I		Peak hold time constant adjustment. This is the time constant which is adjusted when Pin 9 is ON.
11	CP	I		Capacitor connection of Mirror hold. Non-inversion input of Mirror comparator.
12	Mirr	O		Mirror comparator output.
13	CB	I		Capacitor connection of Defect bottom hold.

Pin No.	Symbol	I/O	Equivalent circuit	Description
14	CC1	O		Defect bottom hold output.
15	CC2	I		Input of Defect bottom hold output with capacitance coupled.
16	DFCT	O		Defect comparator output.
17	FOK	O		FOK comparator output.
18	Vcc			Vcc.
19	RF EQ	O		EQ output.
20	C EQ	I		Input of EQ hold amplifier with capacitance coupled.

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>21</td><td>VR</td><td>O</td><td> 
</td><td>(Vcc + GND)/2 DC voltage output.</td></tr>
<tr><td>22</td><td>VC</td><td>I</td><td></td><td>VC center voltage input.</td></tr>
<tr><td>23</td><td>RFD0</td><td>I</td><td rowspan="2"> 
</td><td rowspan="2">Mode switching input.
Mode setting is possible by connecting D0 and D1 pins to the pins shown in the table below.
<table>
<tr><th>D1 \ D0</th><th>Vcc</th><th>GND</th></tr>
<tr><td>Vcc</td><td>A MODE</td><td>B MODE</td></tr>
<tr><td>GND</td><td>C MODE</td><td>—</td></tr>
</table>
Delay time and mix ratio in each mode can be set by the external resistance value connected to the following pins.
<table>
<tr><th>MODE</th><th>Delay time</th><th>Mix ratio</th></tr>
<tr><td>A MODE</td><td>Pin 32</td><td>Pin 29</td></tr>
<tr><td>B MODE</td><td>Pin 31</td><td>Pin 28</td></tr>
<tr><td>B MODE</td><td>Pin 30</td><td>Pin 27</td></tr>
</table></td></tr>
<tr><td>24</td><td>RFD1</td><td>I</td><td> 
</td></tr>
<tr><td>25</td><td>LPF ADJ</td><td>I</td><td> 
</td><td>LPF cut-off frequency setting input.</td></tr>
<tr><td>26</td><td>REF</td><td>I</td><td> 
</td><td>Reference current setting input of equalizer mix ratio, delay time VCA gain, and LPF cut-off frequency.</td></tr>
<tr><td>27
28
29</td><td>K1
K2
K4</td><td>I
I
I</td><td> 
</td><td>Equalizer mix ratio setting input. The figure * of pins K* corresponds to the respective modes.</td></tr>
</table>

Pin No.	Symbol	I/O	Equivalent circuit	Description
30 31 32	DLT1 DLT2 DLT4	I I I		Delay line delay time setting. The figure * of pins DLT* corresponds to the respective modes.
33	GM	I		Low frequency gain setting of voltage control amplifier. To make the low frequency gain of equalizer block 0dB, set the external resistance value to 6.8kΩ.
34	C DL			Capacitor connection of approximately 0.01µF between delay line circuit and GND to reduce noise in the circuit.
35 36	MON3 MON2	O O		Monitoring output of delay line 1 and 2 circuits.
37	MON1	O		Monitoring output of voltage control amplifier.
38	EQ IN	I		Voltage control amplifier input; input of equalizer block.

Pin No.	Symbol	I/O	Equivalent circuit	Description
39	RFI	I		Input of RF summing amplifier output with capacitance coupled.
40	RFO	O		RF signal output; check point of eye pattern.
41	RF (–)	I		Inversion input of RF drive amplifier. Low frequency gain of RF drive amplifier is determined by the resistance value connected between this pin and RFO pin.
42	VC2	I		VC center voltage input.
43	GND			Ground.
44 45 46 47 48	A B C D FE Bias	I I I I I		Input of RF summing amplifier and focus error amplifier for Pins 44, 45, 46, and 47. Pin 48 is for focus bias adjustment.

Electrical Characteristics

(Ta = 25°C, V_{CC} = +2.5V, V_{EE} = –2.5V, V_C = GND)

Measure-ment No.	Measurement item		Symbol	SW conditions														Bais conditions				Mea-sure-ment point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	E1	E2	E3	E4						
1		Current consumption (+)	I_{CC}															300mV	0V	0V	0V	18		30	40	50	mA
2		Current consumption (–)	IEE															300mV				43		–50	–40	–30	mA
3	RF amplifier	Offset voltage	V1 1															0V				40	V3 = GND	–40	0	40	mV
4		Voltage gain	V1 2												O	O						40	V3 = 1kHz, 100mVpp	15.5	18.5	21.5	dB
5		Frequency response	V1 3												O	O						40	V3 = 8MHz, 100mVpp Ratio to V12	–3	—	—	dB
6		Maximum output amplitude H	V1 4												O	O	O				250mV	40		1.3	—	—	V
7		Maximum output amplitude L	V1 5												O	O	O				–250mV	40		—	—	–0.3	V
8	FE amplifier	Offset voltage	V2 1																		0V	7		–30	0	30	mV
9		Voltage gain 1	V2 2												O							7	V3 = 1kHz, 90mVpp	17.7	20.7	23.7	dB
10		Voltage gain 2	V2 3													O						7	V3 = 1kHz, 90mVpp	17.7	20.7	23.7	dB
11		Voltage gain difference	V2 4																				V2 4 = V2 2 –V2 3	–3	0	3	dB
12		Frequency response	V2 5												O							7	V3 = 100kHz, 90mVpp Difference for V2 2	–3	—	—	dB
13		Maximum output amplitude H	V2 6													O	O				300mV	7		1.9	—	—	V
14		Maximum output amplitude L	V2 7												O		O				300mV	7		—	—	–1.9	V
15	TE amplifier	Offset voltage	V3 1																		0V	8		–30	0	30	mV
16		Voltage gain 1	V3 2	O																		8	V3 = 1kHz, 90mVpp	17.9	20.9	23.9	dB
17		Voltage gain 2	V3 3		O																	8	V3 = 1kHz, 90mVpp	17.9	20.9	23.9	dB
18		Voltage gain difference	V3 4																				V3 4 = V3 2 –V3 3	–3	0	3	dB
19		Frequency response	V3 5																			8	V3 = 100kHz, 100mVpp Difference for V3 2	–3	—	—	dB
20		Maximum output amplitude H	V3 6		O												O				240mV	8		1.9	—	—	dB
21		Maximum output amplitude L	V3 7	O													O				240mV	8		—	—	–1.9	V

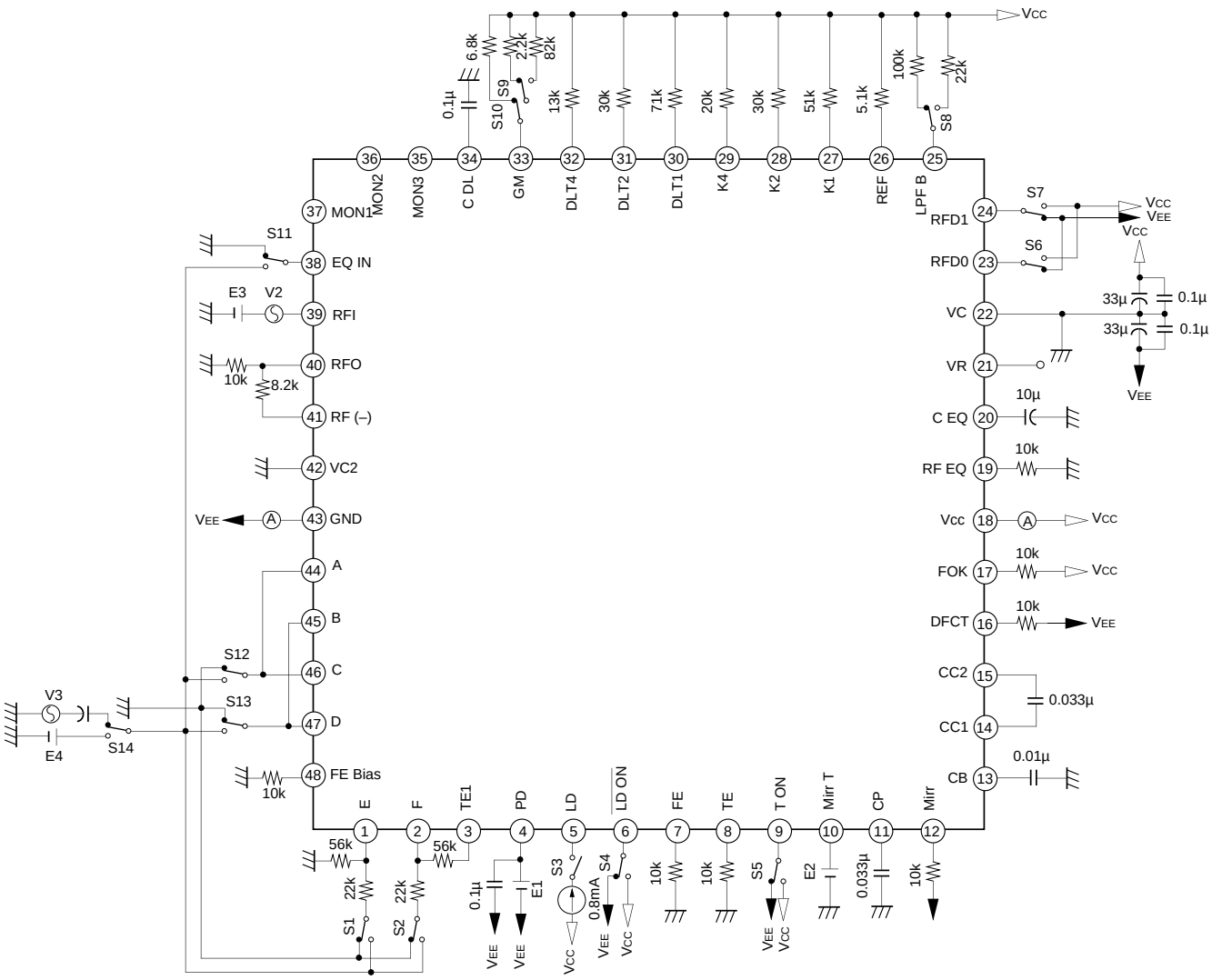
(Ta = 25°C, V_{CC} = +2.5V, V_{EE} = –2.5V, V_C = GND)

Measure-ment No.	Measurement item		Symbol	SW conditions														Bias conditions				Mea-sure-ment point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	E1	E2	E3	E4						
22	Equalizer	Offset voltage	V4 1															0V	0V	0V	0V	19		0	0.2	0.5	V
23		Voltage gain	V4 2											O								19	V3 = 1.0Vpp, f = 100kHz	–3	0	3	dB
24		VCA gain	V4 3										O	O								19	V3 = 1.0Vpp, f = 100kHz Difference for V4 2	5.0	6	8.4	dB
25		Mix ratio accuracy	K4 1											O								19	V3 = 0.5Vpp, f = 100kHz V3 = 0.5Vpp, f = 1/τ Accuracy for difference of (τ = τ (mon3) – τ (mon2))	–15	0	15	%
26		Delay time accuracy 1	T4 1											O								19	V3 = 1.0Vpp, f = 100kHz	–15	0	15	%
27		LPF cut-off accuracy	V4 4								O			O								19	Accuracy = Cut-off frequency / Boost frequency	–20	0	20	%
28		Effective output noise voltage	V4 5								O			O								19	Output noise value HPF: 400Hz LPF: 3MHz	—	2.2	—	mVrms
29		Maximum output amplitude H	V4 6											O								19	V3 = 5.0Vpp, f = 100kHz Maximum output voltage	1.0	—	—	V
30		Maximum output amplitude L	V4 7											O						↓		19		—	—	–1.0	V
31	FOK	Threshold	V5 1																	Variation		38	RFI – RFO voltage where the voltage of Pin 17 becomes GND	–400	—	–300	mV
32		High level output voltage	V5 2																	–375mV		17	E4 = –450	2.2	—	—	V
33		Low level output voltage	V5 3																	–375mV		17	E4 = –260	—	—	–1.8	V
34		Maximum operating frequency	V5 4																	–375mV		17	V2 = 1.0Vpp	45	—	—	kHz
35	DEFECT	High level output voltage	V6 1												O	O				0V		16	V3 = 90mVpp, 43mVDC f = 1kHz	1.8	—	—	V
36		Low level output voltage	V6 2												O	O						16		—	—	–2.0	V
37		Minimum operating frequency	F6 1												O	O						16	V3 = 90mVpp, 43mVDC	—	—	1	kHz
38		Maximum operating frequency	F6 2												O	O						16		2	—	—	kHz
39		Minimum operating input voltage	F6 3												O	O						16	V3 = 43mVDC f = 1kHz square wave Specification value is RFO output voltage.	—	—	0.5	Vpp
40		Maximum operating input voltage	F6 4												O	O		↓	↓	↓	↓	16		1.8	—	—	Vpp

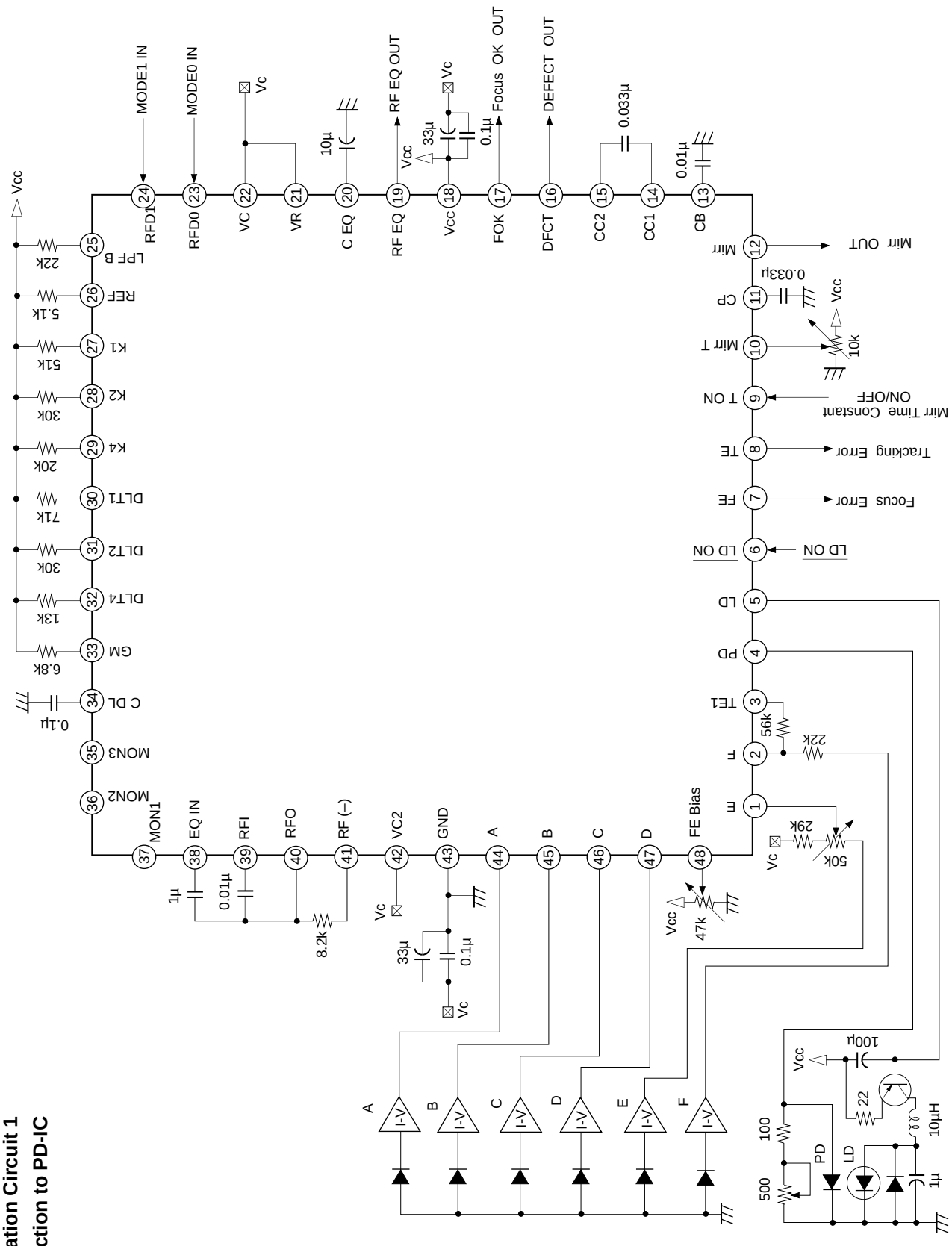
(Ta = 25°C, V_{CC} = +2.5V, V_{EE} = –2.5V, V_C = GND)

Measure-ment No.	Measurement item		Symbol	SW conditions														Bais conditions				Mea-sure-ment point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	E1	E2	E3	E4						
41	MIRR	High level output voltage	V7 1															0V	0V	–400mV	0V	12	V2 = 0.8Vpp f = 10kHz	1.8	—	—	V
42		Low level output voltage	V7 2																	–400mV		12	V2 = 0.8Vpp f = 10kHz	—	—	–2.2	V
43		Mirror hold frequency response	F7 1																	–200mV		12	V2 = 800mVpp, 55% AM modulation fcarrier = 500Hz	—	400	600	Hz
44		Bottom hold frequency response	F7 2																	–400mV		12	V2 = 800mVpp	—	550	900	Hz
45		Maximum operating frequency 1	F7 3																↓	–400mV		12	V2 = 800mVpp	30	—	—	kHz
46		Maximum operating frequency 2	F7 4					O											1.0V	–400mV		12	V2 = 800mVpp	80	—	—	kHz
47		Minimum operating input voltage	V7 3																0V	–400mV		12	f (V2) = 10kHz	—	0.1	0.2	Vpp
48		Maximum operating input voltage	V7 4															↓		–400mV		12	f (V2) = 10kHz	1.8	—	—	Vpp
49	APC	Output voltage 1	V8 1															69mV		0V		5		—	–1.7	–0.3	V
50		Output voltage 2	V8 2															123mV				5		–1.5	–0.8	1.1	V
51		Output voltage 3	V8 3															177mV				5		0.6	1.2	—	V
52		Output voltage 4	V8 4				O											0V				5		2.1	2.4	—	V
53		Output voltage 5	V8 5			O												0V				5	I1 = 0.8mADC	—	—	0	V
54	Center amplifier	Output voltage	V9 1															0V	↓	↓	↓	21		–0.1	—	0.1	V

Electrical Characteristics Measurement Circuit

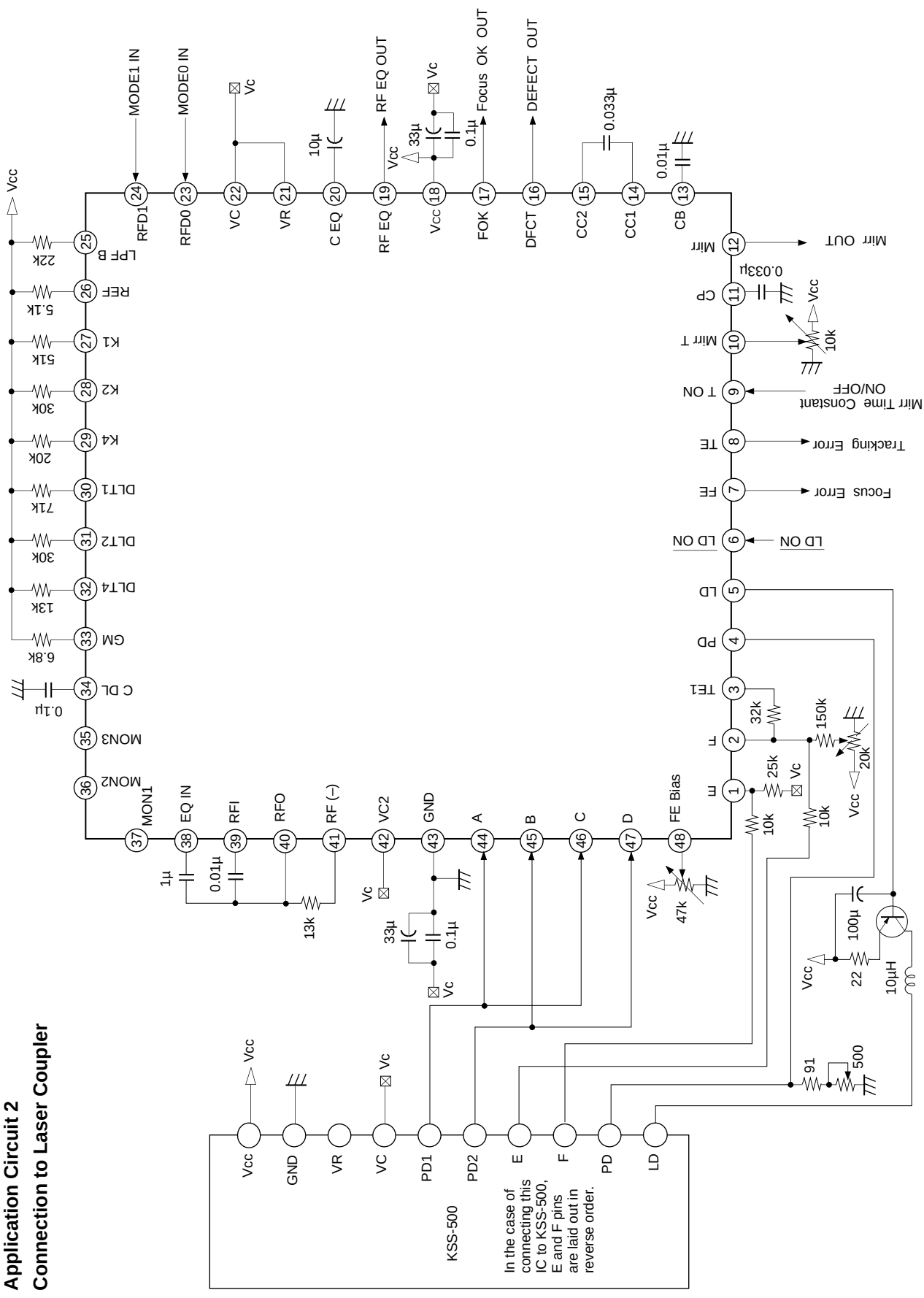


Application Circuit 1
Connection to PD-IC



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

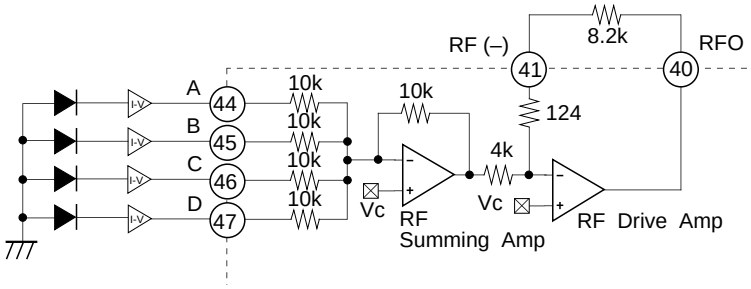
Application Circuit 2
Connection to Laser Coupler



Description of Operation

RF Amplifier

The signal currents from the photodiodes A, B, C and D are I-V converted, and input to Pins 44, 45, 46 and 47. These signals are added at the RF summing amplifier and output to Pin 40 via the RF drive amplifier.



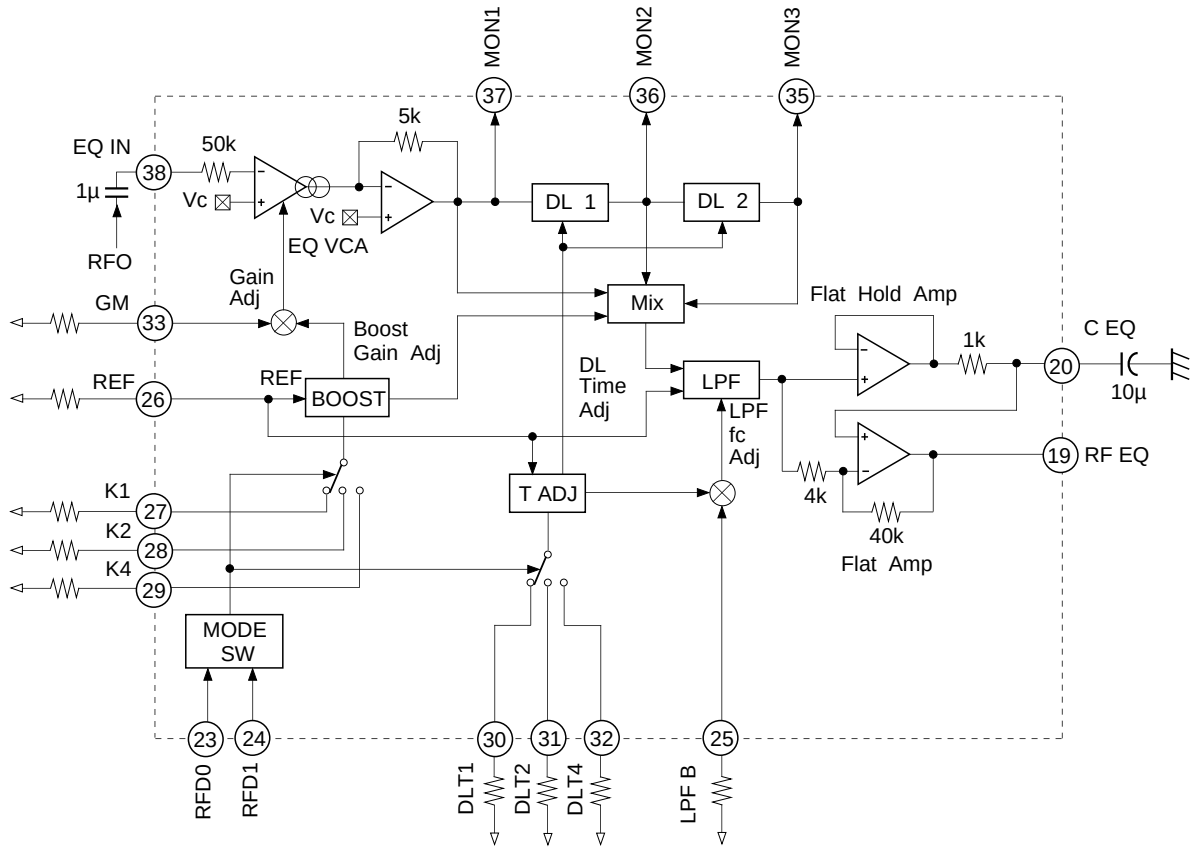
The low frequency gain of RFO output voltage is as follows:

$$V_{RFO} = \frac{10k}{10k} \times \frac{8.3k}{4k} \times (A + B + C + D)$$

$$= 2.1 \times (A + B + C + D)$$

Equalizer

This equalizer adopts the cosine equalization method. The DC component of the RFO output voltage is cut off by a capacitor and is then input to Pin 38. The equalized signal is output to Pin 19.



Voltage Control Amplifier

Low frequency gain of equalizer output voltage can be adjusted by the resistance value connected to Pin 33.
The low frequency gain is automatically adjusted to be constant even if the mix ratio is changed.
The output can be monitored with Pin 37.

Delay Line

Delay time can be adjusted in each of three modes by the resistance value connected to Pins 30, 31, and 32.
The output of delay lines 1 and 2 can be monitored with Pins 36 and 35, respectively.
Low frequency gain at the delay line is 0dB.

Boost Mix

Mix ratio can be adjusted in each of three modes by the resistance value connected to Pins 27, 28, and 29.
Low frequency gain at the mix block is 0dB.

Low Pass Filter

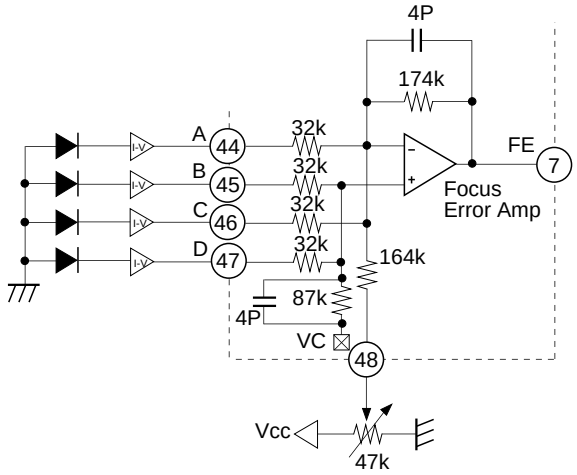
Fifth-order active filter.
Cut-off frequency can be adjusted by the resistance value connected to Pin 25. If the mode is switched and the delay time of delay line is changed, the cut-off frequency is automatically adjusted at the same rate as the variation of delay time.

Flat Amplifier

Operational amplifier with a low frequency gain of +20dB.
Equalizer output voltage is output to Pin 19.
Take care that the group delay for low frequency components varies if the capacitance value connected to Pin 20 is too small.

Focus Error Amplifier

The operation of (B + D) – (A + C) is performed and the resulting signal is output to Pin 7.



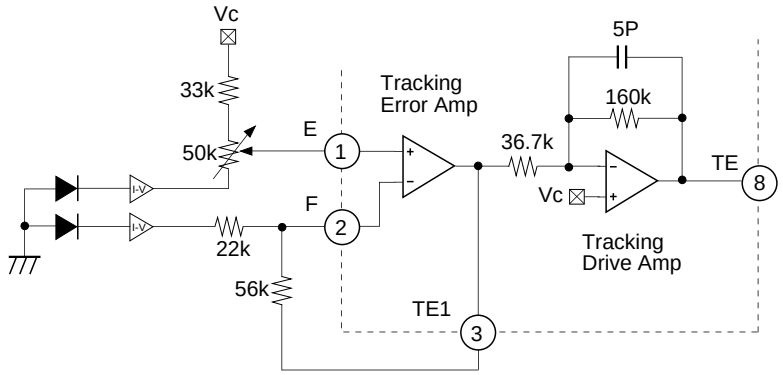
The low frequency gain of FE output voltage is as follows:

$$V_{FE} = \frac{174k}{32k} \times (B + D - A - C)$$

$$= 5.43 \times (B + D - A - C)$$

Tracking Error Amplifier

The signal current from the photodiode F is I-V converted and input to Pin 2 via an input resistor. The signal current from the photodiode E is I-V converted, and input to Pin 1 after its gain is adjusted by the volume. These signals undergo operational amplification at the tracking error amplifier and tracking drive amplifier, and are output to Pin 8. The input resistance and feedback resistance of the tracking error amplifier are configured with external resistors, so that the absolute errors and deviations of temperature characteristics for IC internal/external resistors are independent of the low frequency gain.



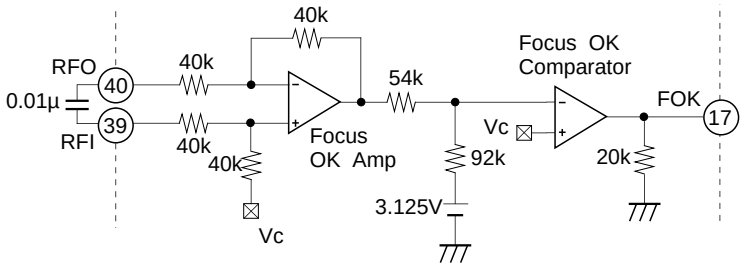
The low frequency gain of TE output voltage is as follows:

$$V_{TE} = \frac{56k}{22k} \times \frac{160k}{36.7k} \times (F - E)$$

$$= 11.1 \times (F - E)$$

Focus OK Circuit

The focus OK circuit creates the timing window okaying the focus servo from the focus search state.

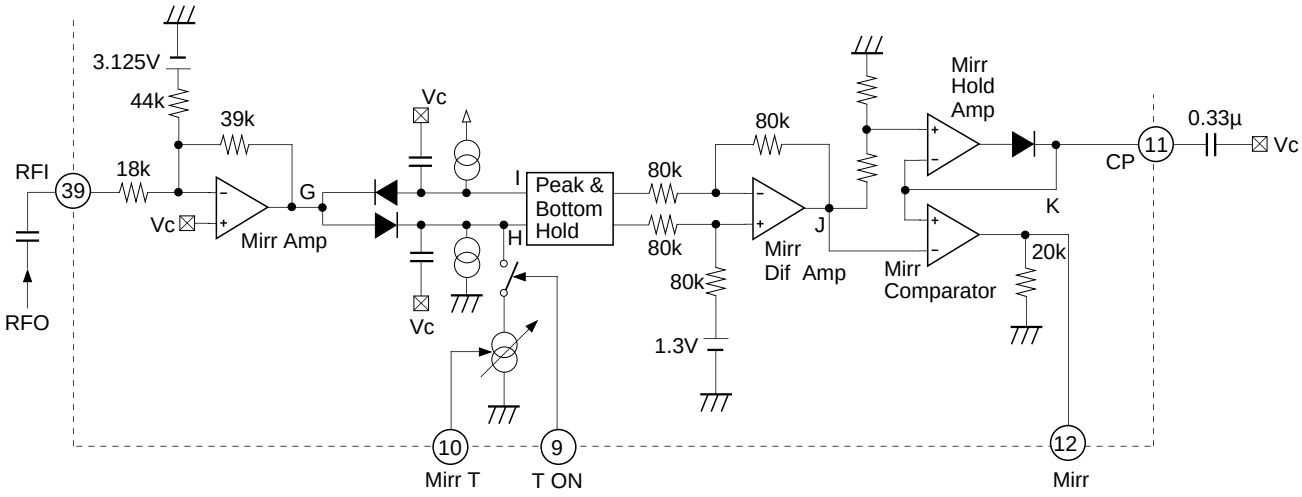


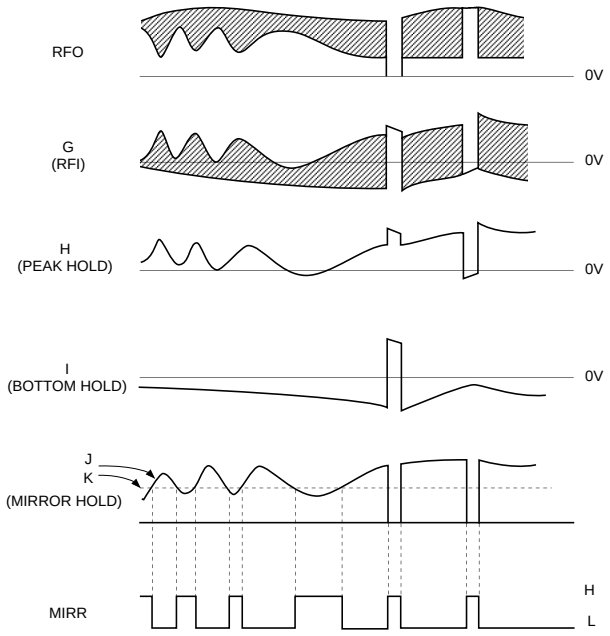
The low frequency component of RF can be gotten by obtaining the difference of the Pins 40 and 39 RF signals, whose low frequency components are removed, at the focus OK amplifier.

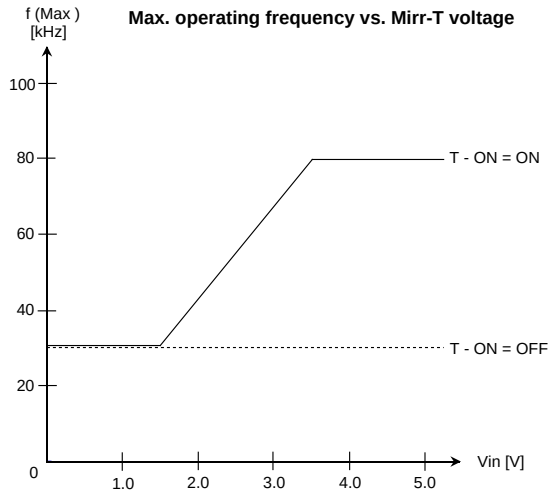
The focus OK output is inverted when $V_{RFI} - V_{RFO} \approx -0.37V$. The capacitance between Pins 39 and 40 is used to determine the time constants of the mirror circuit HPF and the focus OK amplifier LPF. In normal use, with C equal to 0.01µF selected, fc is equal to 1kHz, and block error rate degradation can be prevented which is caused by RF envelope defects due to scratched discs.

Mirror Circuit

Mirror circuit performs peak and bottom hold after RFT signal is amplified. The peak hold is executed for Pin 9 with the time constant which follows the traverse signal of 30kHz for OFF (connection to GND) and maximum 80kHz (adjustable with DC voltage of Pin 10) for ON (connection to Vcc). The bottom hold is executed with the time constant which follows the rotation cycle envelope fluctuation.





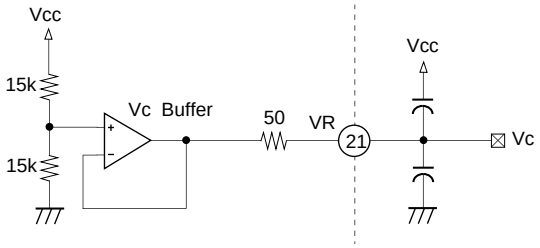


The mirror signal is output by comparing the signal J, where the difference of hold signals H and I is obtained, to the signal K (2/3 level of the J peak value which is peak-held with a large time constant). The mirror output is low for tracks on the disc and high for the area between tracks (the mirror areas). In addition, a high signal is output when a defect is detected. The mirror hold time constant must be sufficiently large in comparison with the traverse cycle.

Center Voltage Generation Circuit

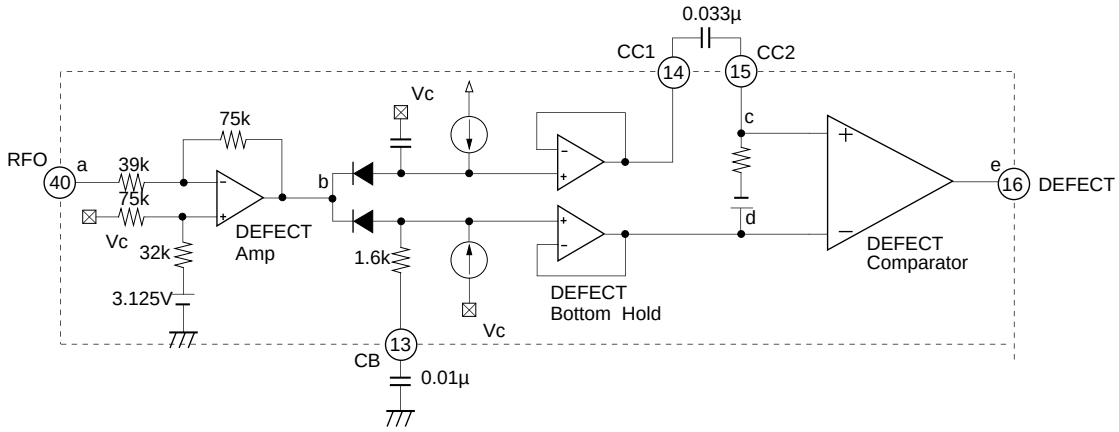
The center voltage of VR = (Vcc + GND)/2 is supplied.

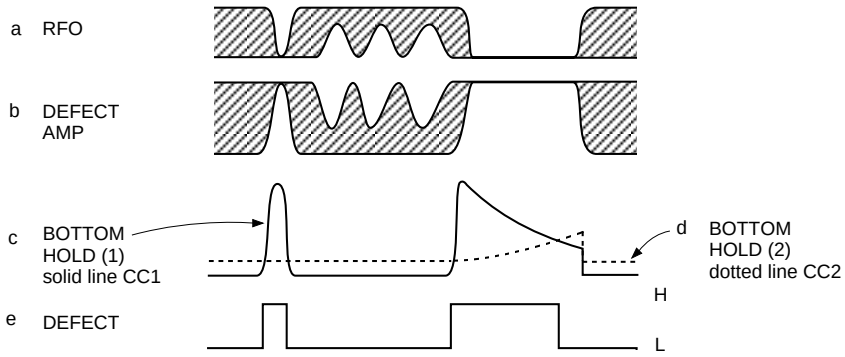
The maximum current is approximately ±3mA.



Defect Circuit

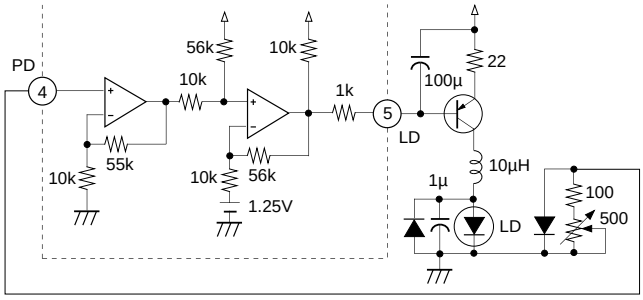
Bottom hold is performed on two time constants, long and short, after inverting the RFI signal. Short time constant bottom hold responds to the disc mirror defect for 0.1 ms or more, and the mirror level immediately prior to a defect is held by a long time constant bottom hold. The mirror defect detection signal is output by performing a differential + level shift with capacitor coupling and then comparing the signals.





APC Circuit

When the laser diode is driven with constant current, the optical output possesses large negative temperature characteristics. Therefore, the current must be controlled with the monitor photodiode to ensure the output remains constant. When LD ON pin is connected to GND, APC is ON; connected to Vcc, it is OFF.



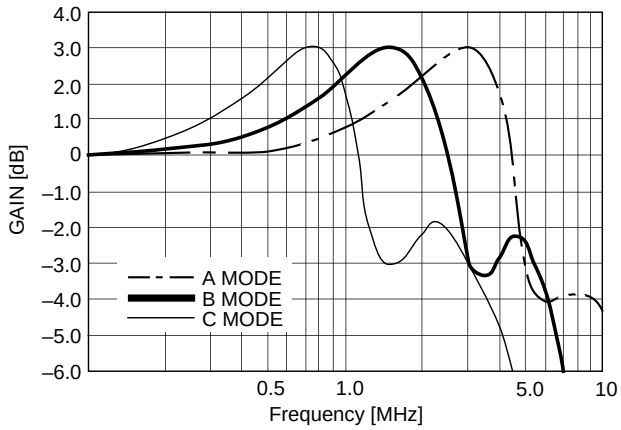
Note on Operation

Take care of handling the IC because the electrostatic discharge strength for Pins 41, 44, 45, 46 and 47 is weak.

Equalizer Characteristic Graphs

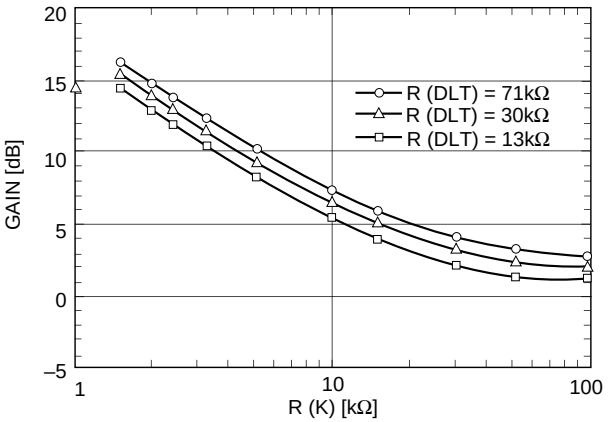
* Frequency response

Frequency response by mode in application circuit



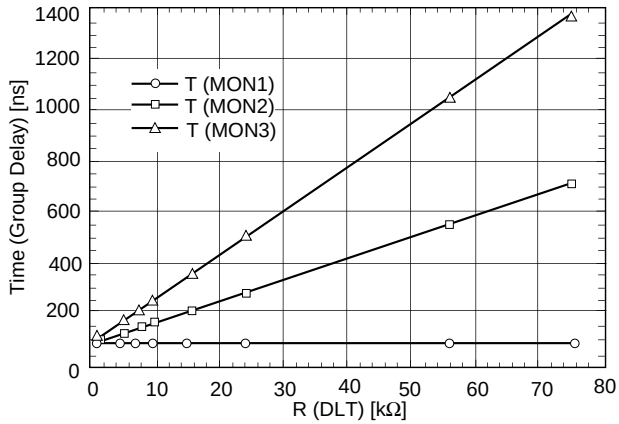
* Boost gain characteristics

R (K) vs. Boost gain characteristics



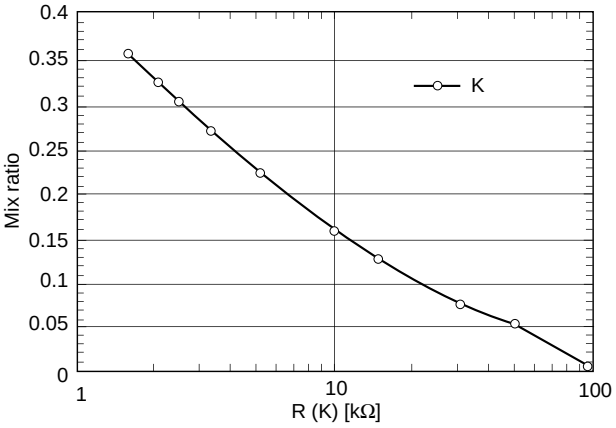
* Delay characteristics

Delay characteristics
Input signal frequency 100kHz



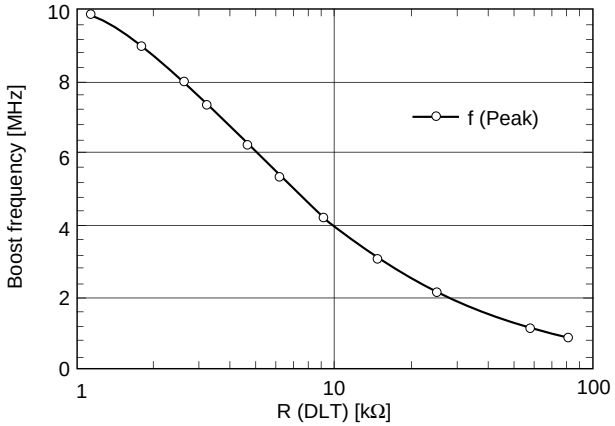
* Mix ratio characteristics

R (K) vs. Mix ratio characteristics



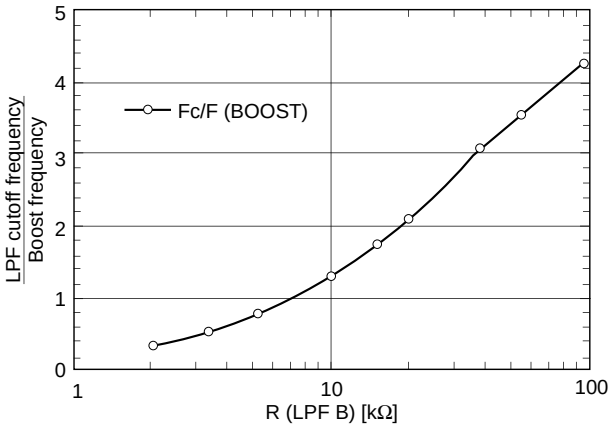
* Boost frequency response

R (DLT) vs. Boost frequency response



* LPF characteristics

R (LPF B) vs. Fc characteristics



In the graphs above,

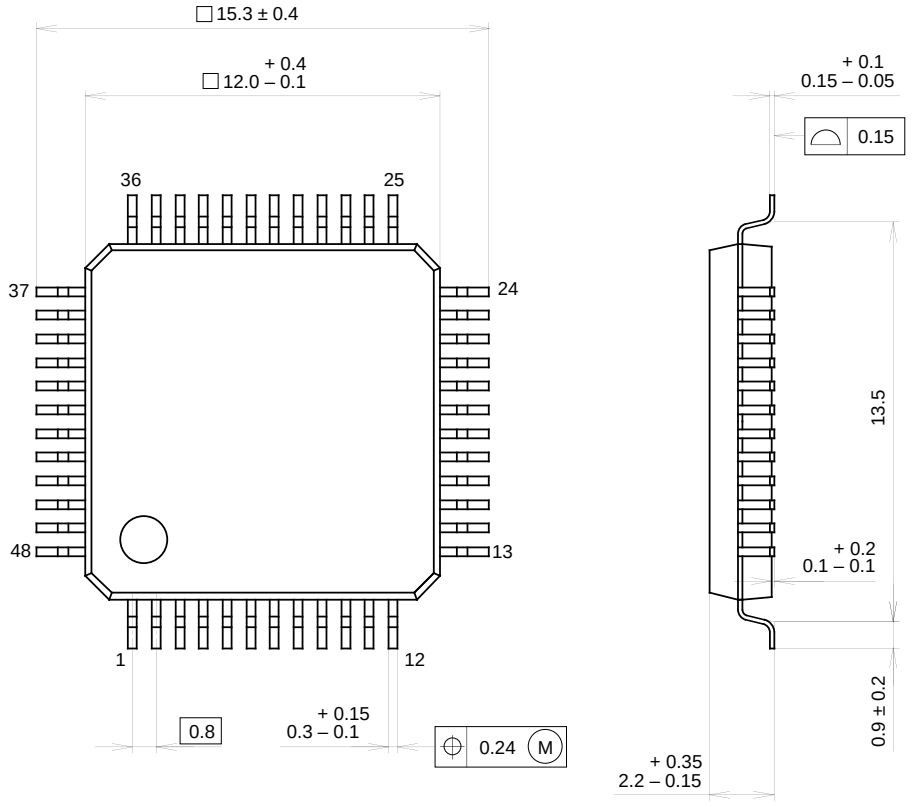
R (DLT): external resistance value for DLT* pins (Pins 30, 31, and 32)

R (K): external resistance value for K* pins (Pins 27, 28 and 29)

R (LPF B): external resistance value for LPF B pin (Pin 25)

Package Outline Unit: mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).