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Device Specification
and Incoming Inspection Standard for
TFT LCD Module

Model No.

LS055D1SX04

☐ CUSTOMER'S APPROVAL

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RECORDS OF REVISION

MODEL No: LS055D1SX04

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[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.

There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the counter measure (electrostatic earth:$1\times10^{8}\Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.

(15) Do not touch the COG‘s patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

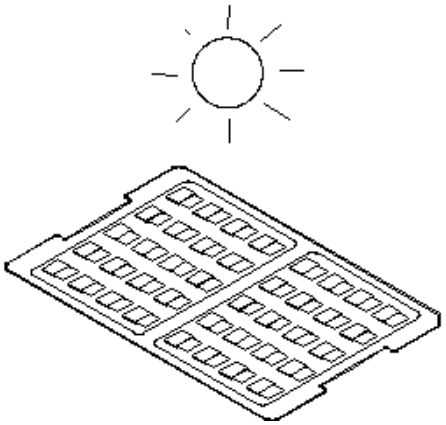
(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
(3) Keeping Method

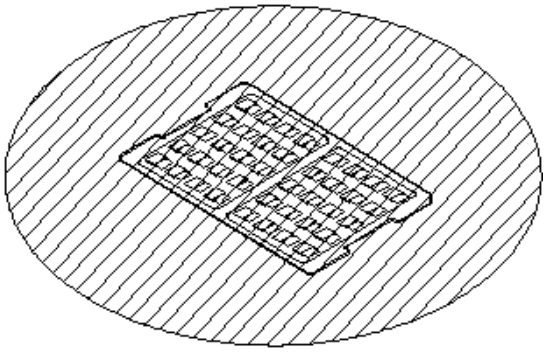
a. Don't keeping under the direct sunlight.

DON'T



b. Keeping in the tray under the dark place.

DO



(4) Do not operate or store the LCD module under outside of specified environmental conditions.
(5) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDDI-GND) are low when LCD module is working, place the de-coupling capacitor nearby LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) U/V glue (Liquid OCA) should not be attached on upper polarizer edge, when customer laminate cover glass and touch panel on LCD.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of active matrix 16,777,216 color LCD module.
Main color LCD module is controlled by Driver IC (NT35950).
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification.

2. Construction and Outline

This module is a color transmissive, high contrast, wide viewing angle and active matrix LCD module incorporating CG-Silicon TFT (Continuous Grain-Silicon Thin Film Transistor).

Construction: LCD panel, Driver (COG), FPC with electric components, 18 White LEDs, prism sheet, diffuser, light guide, Reflector, Bezel and plastic frame to fix them mechanically.

Outline: See page 36 (Fig.30 Outline dimensions)
Connection: B2B connector (AXT650124)

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

Rejection criteria shall be noted in Inspection Standard.

3. Mechanical Specification

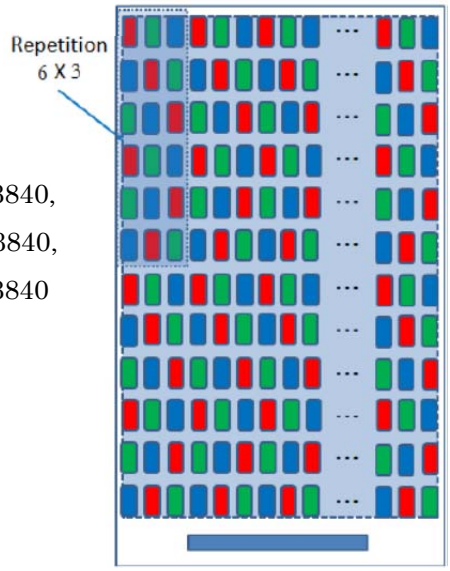
Table 1

Item	Specifications	Unit	Remarks
Screen size	138.78 (5.46” type) Diagonal	mm	
Active area	68.04(H)X120.96(V)	mm	
Pixel format	1440×(R)x3840 1440x(G)x3840 1440x(B)x3840	Pixel	
Pixel pitch	0.01575 (H) x 0.04725(V)	mm	
Pixel configuration	Rainbow-RGB	-	
Display mode	Normally Black	-	
LDC Driving method	DC Driving / Column Inversion	-	
Liquid Crystal Mode	New Mode2	-	
Number of colors	16,777,216	Colors	24 bits
Outline dimensions	70.54(W)×128.56 (H)×1.5(D) TYP	mm	Note 3-1
Mass	25	g	

Note 3-1) The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to Fig.29 Outline dimensions.

4. Pixel Configuration

(1,1)



1440X(R)X3840,
1440X(G)X3840,
1440X(B)X3840

Comment)

・If the power on sequence table of is issued, an initial direction of the LCD scanning is shown in a left figure (#Figure 1).

Fig.1

5. Input Terminal Names and Functions

Table 2

Pin No	Symbol	I/O	Description	Remarks
1	AVEE	-	Power supply for analog(-5.6V typ)	
2	VDDI	-	Power supply for I/O(1.88V typ)	
3	NC	-	Non-Connect	
4	VDDI	-	Power supply for I/O(1.88V typ)	
5	LEDPWM	O	Backlight LED driver PWM	
6	AVDD	-	Power supply for analog(5.8V typ)	
7	TE	O	TE signal	
8	RESX	I	Device reset signal	“L” Active
9	GND	-	Ground	
10	GND	-	Ground	
11	DSIB_D1_N	I	MIPI data1 negative signal of MIPI Port B	
12	DSIB_D0_N	I/O	MIPI data0 negative signal of MIPI Port B	
13	DSIB_D1_P	I	MIPI data1 positive signal of MIPI Port B	
14	DSIB_D0_P	I/O	MIPI data0 positive signal of MIPI Port B	
15	GND	-	Ground	
16	GND	-	Ground	
17	DSIB_D2_N	I	MIPI data2 negative signal of MIPI Port B	
18	DSIB_CLK_N	I	MIPI clock negative signal of MIPI Port B	
19	DSIB_D2_P	I	MIPI data2 positive signal of MIPI Port B	
20	DSIB_CLK_P	I	MIPI clock positive signal of MIPI Port B	
21	GND	-	Ground	
22	GND	-	Ground	
23	DSIA_D0_N	I/O	MIPI data0 negative signal of MIPI Port A	
24	DSIB_D3_N	I	MIPI data3 negative signal of MIPI Port B	
25	DSIA_D0_P	I/O	MIPI data0 positive signal of MIPI Port A	
26	DSIB_D3_P	I	MIPI data3 positive signal of MIPI Port B	
27	GND	-	Ground	
28	GND	-	Ground	
29	DSIA_CLK_N	I	MIPI clock negative signal of MIPI Port A	
30	DSIA_D1_N	I	MIPI data1 negative signal of MIPI Port A	
31	DSIA_CLK_P	I	MIPI clock positive signal of MIPI Port A	
32	DSIA_D1_P	I	MIPI data1 positive signal of MIPI Port A	
33	GND	-	Ground	
34	GND	-	Ground	-
35	DSIA_D3_N	I	MIPI data3 negative signal of MIPI Port A	I
36	DSIA_D2_N	I	MIPI data2 negative signal of MIPI Port A	I
37	DSIA_D3_P	I	MIPI data3 positive signal of MIPI Port A	I
38	DSIA_D2_P	I	MIPI data2 positive signal of MIPI Port A	I
39	GND		Ground	-
40	GND		Ground	-
41	NC		Non-Connect	-
42	NC		Non-Connect	-
43	NC		Non-Connect	-
44	NC		Non-Connect	-
45	LED_CA3		LED back light power negative3	-
46	NC		Non-Connect	-
47	LED_CA2		LED back light power negative2	-
48	NC		Non-Connect	-
49	LED_CA1		LED back light power negative1	-
50	LED_AN1		LED back light power positive1	-

Fitting connector: Panasonic AXT550124 (Socket)

6.Absolute Maximum Ratings

Table3 GND=0V

Parameter	Symbol	Conditions	Rated value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	AVDD	Ta=+25C Frm=60Hz	-0.3 to +6.6	V	Note6-1
Driver IC (Negative Analog) Power Supply Voltage	AVEE	Ta=+25C Frm=60Hz	+0.3 to -6.6	V	Note6-1
Driver IC (Digital) Power Supply Voltage	VDDI	Ta=+25C Frm=60Hz	-0.3 to +2.15	V	Note6-1
Temperature for storage	Tstg	Frm=60Hz	-30 to +70	°C	Note6-2
Temperature for operation	Topr	Frm=60Hz	-20 to +60	°C	Note6-2
LED Input electric current	ILED	Ta=+25C Frm=60Hz	Max 25	mA	Note6-3

Note6-1) Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V).
Always connect all GND externally and use at the same voltage.

Note6-2)Humidity: 95%RHMax.(at Ta≤40C). Maximum wet-bulb temperature is less than 39°C (at Ta>40C). Condensation of dew must be avoided.

Note6-3) Ambient temperature and the maximum input are fulfilling the following operating conditions.

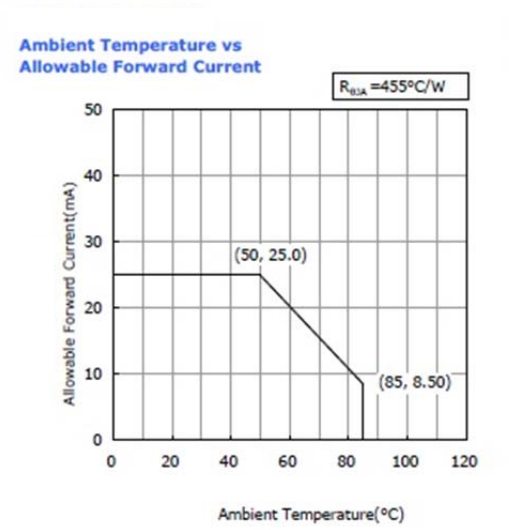


Fig.2

7. Electrical Specifications

7-1. TFT-LCD Panel Driving Section

Table4 Ta=+25C, Frm=60Hz, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Digital) Power Supply Voltage	VDDI	1.78	1.88	1.98	V	Note7-1
Driver IC(Positive Analog) Power Supply Voltage	AVDD	5.6	5.8	6.0	V	Note7-1
Driver IC(Negative Analog) Power Supply Voltage	AVEE	-5.8	-5.6	-5.4	V	Note7-1
Input voltage range Low(RESX)	V_{IL-R}	0	-	0.2 VDDI	V	Note7-2
Input voltage range High(RESX)	V_{IH-R}	0.8 VDDI	-	VDDI	V	Note7-2
Input voltage range Low(Except RESX)	V_{IL}	0	-	0.3 VDDI		Note7-2
Input voltage range High(Except RESX)	V_{IH}	0.7 VDDI	-	VDDI		Note7-2
Input current (Low)	I_{IL}	-1	-	-	μA	
Input current (High)	I_{IH}	-	-	1	μA	
Output voltage (Low)	V_{OL}	0	-	0.2 VDDI	V	
Output voltage (High)	V_{OH}	0.8 VDDI	-	VDDI	V	
Current consumption Command mode(Still image) 2port(VESA DSC)	I_{VDDI1}	-	TBD	TBD	mA	Note7-3 White
	I_{AVDD1}	-	TBD	TBD	mA	
	I_{AVEE1}	-	TBD	TBD	mA	
	I_{VDDI2}	-	TBD	TBD	mA	Note7-4 Max Load Current 2sub pixel Checker
	I_{AVDD2}	-	TBD	TBD	mA	
	I_{AVEE2}	-	TBD	TBD	mA	

Note7-1) Voltage shall be at the point of module input. Include Ripple Noise.

Note7-2) Applied overshoot

Note7-3) Measurement Conditions: Full screen white pattern, VDDI=1.88V, AVDD=5.80V, AVEE=-5.60V

Note7-4) Measurement Conditions: Full screen 2sub pixel Checker pattern, VDDI=1.88V, AVDD=5.80V, AVEE=-5.60V

7-2. Back Light Driving Section

Table5 Ta=+25C,GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
LED Voltage	V_{LED}	-	+17.1 x 3	-	V	Note7-5
LED Current	I_{LED}	-	20	-	mA	
Power Consumption	W_{LED}	-	1026	-	mW	Note7-6
LED Quantity			18		pcs	

Note7-5) at I_{LED}=20mA

Note7-6) $W_{LED}=V_L \times I_L$

7-3.Timing characteristics of LEDPWM signal

Table6 Ta=+25C,GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
LEDPWM Frequency	fLEDPWM	TBD	-	TBD	kHz	Note7-7

Note7-7) Base clock (FSOC) = 5MHz, 10MHz, 20MHz or 40MHz (Register Setting)

8. Timing characteristics of input signals

(8-1) MIPI Interface Characteristics for Video mode

Vertical Input Timing (MIPI-DSI)

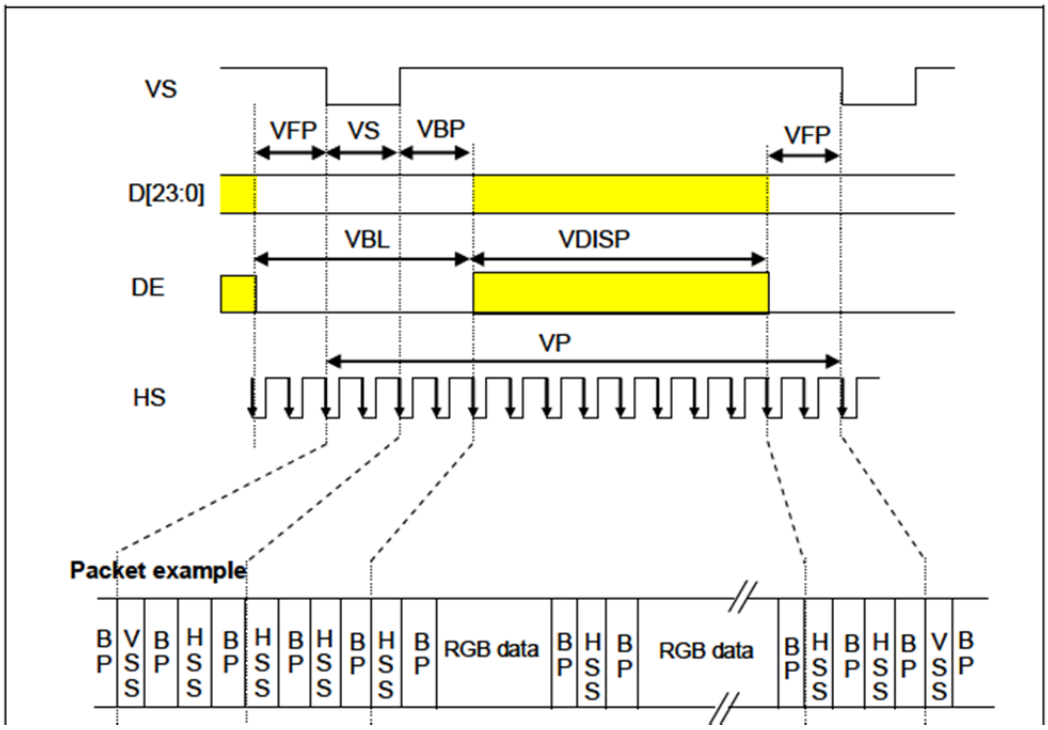


Fig.3

Table7 GND=0V, VDDI =1.88±0.1V, VSP=5.8±0.2V, VSN=-5.6±0.2V, Ta=+25C

Parameter	Symbol	MIN.	Typ.	MAX.	Unit
Vertical cycle	VP	-	2	-	Line
Vertical data start point	VS+VBP	-	12	-	Line
Vertical Front Porch	VFP	-	12	-	Line
Vertical active area	VDISP	-	3840	-	Line
Vertical Refresh Rate	VRR	59	60	61	Hz

※Please refer to specification of “Novatek NT35950” for detail.

Horizontal Input Timing (MIPI-DSI)

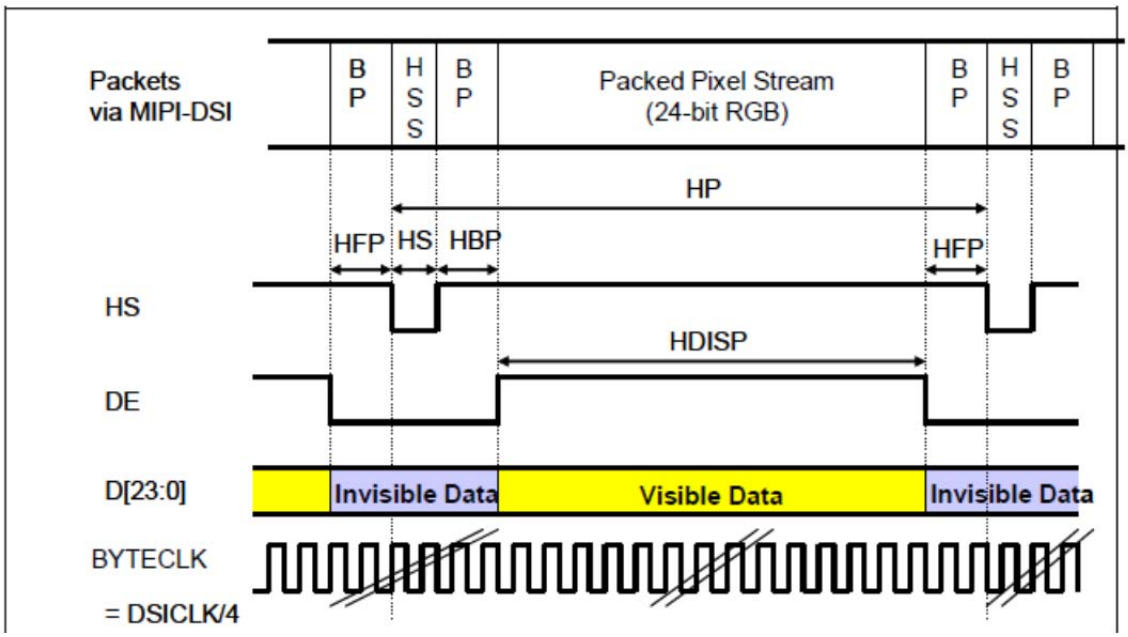


Fig.4

Table8 GND=0V, VDDI =1.88±0.1V, VSP=5.8±0.2V, VSN=-5.6±0.2V, Ta=+25C

Parameter	Symbol	MIN.	Typ.	MAX.	Unit
Horizontal front porch	HFP	-	105	-	BYTECLK (*1)
Horizontal data start point	HS+HBP	-	108	-	BYTECLK (*1)
Horizontal active area	HDISP	-	270	-	BYTECLK (*1)
Horizontal cycle	Hcyc	4.243	4.313	4.386	us (*2)

(*1) BYTECLK is generated by dividing DSICLK by 8, or pclk x 3/8

(*2) Horizontal cycle of MIPI DSI input is related to the frame rate. (1H=4.308us → Frm=60Hz)

The tolerance all over the operating temperature shall be within the spec.

MIPI DSI CLK & Data Timing

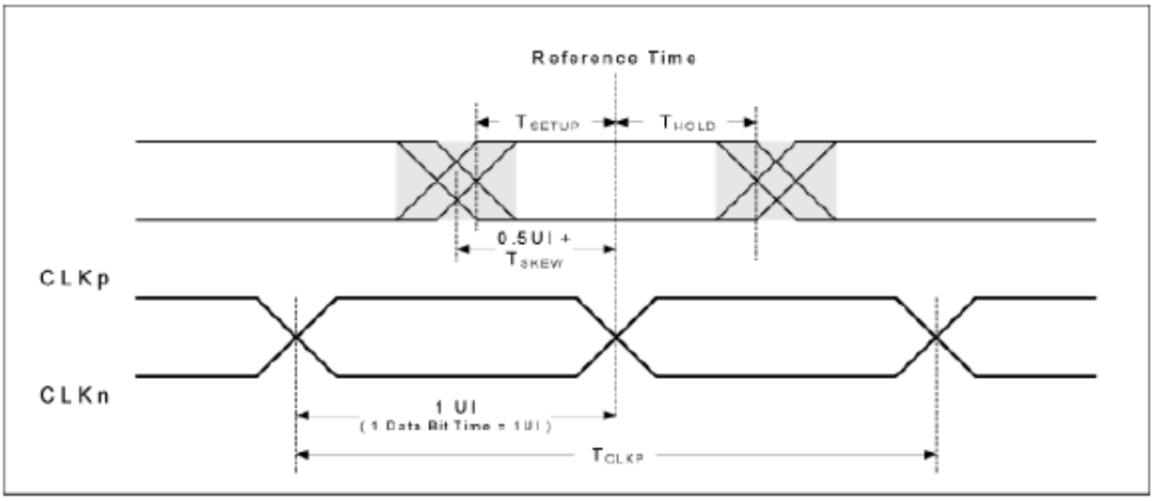


Fig.5

Table9 GND=0V, VDDI =1.88±0.1V, , VSP=5.8±0.2V, VSN=-5.6±0.2V, Ta=+25C

Parameter	Symbol	MIN.	Typ.	MAX.	Unit
DSICLK Frequency	fDSICLK	100	-	500	MHz
Data Transfer Rate (HS mode)	tDSIR	200	-	1000	Mbps
DSICLK Cycle time	tCLKP	2.0	-	8	ns
Data to Clock Setup Time	tSETUP	0.15	-	-	UI
		0.15	-	-	ns
Clock to Data Hold time	tHOLD	0.15	-	-	UI
		0.15	-	-	ns

8-2) Reset Timing Characteristics

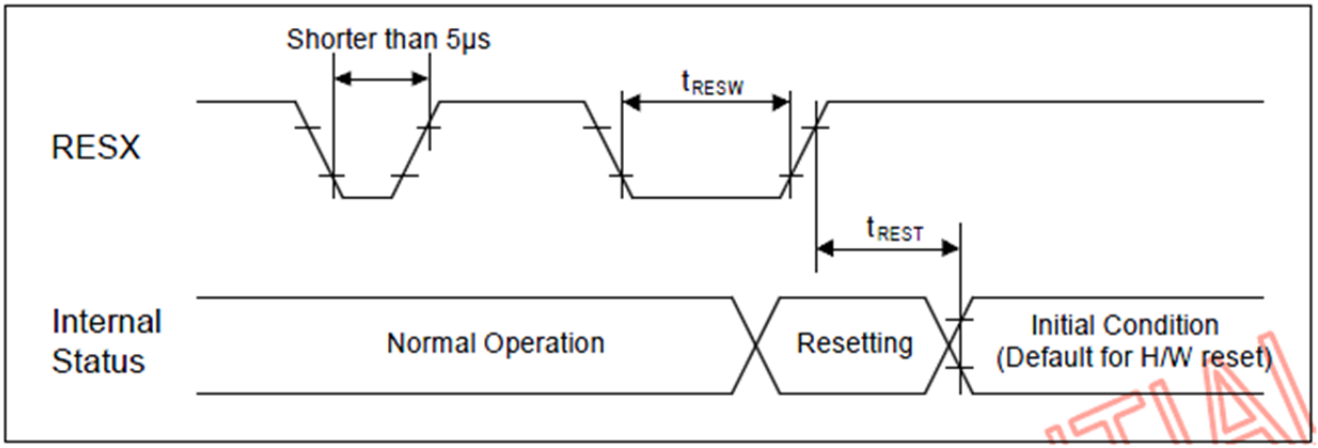


Fig.6

(DVSS=DVSS1=DVSS2=AVSS=VSSAM1=VSSAM2=0V, VDDI=1.65V to 1.95V, Ta=-30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 4

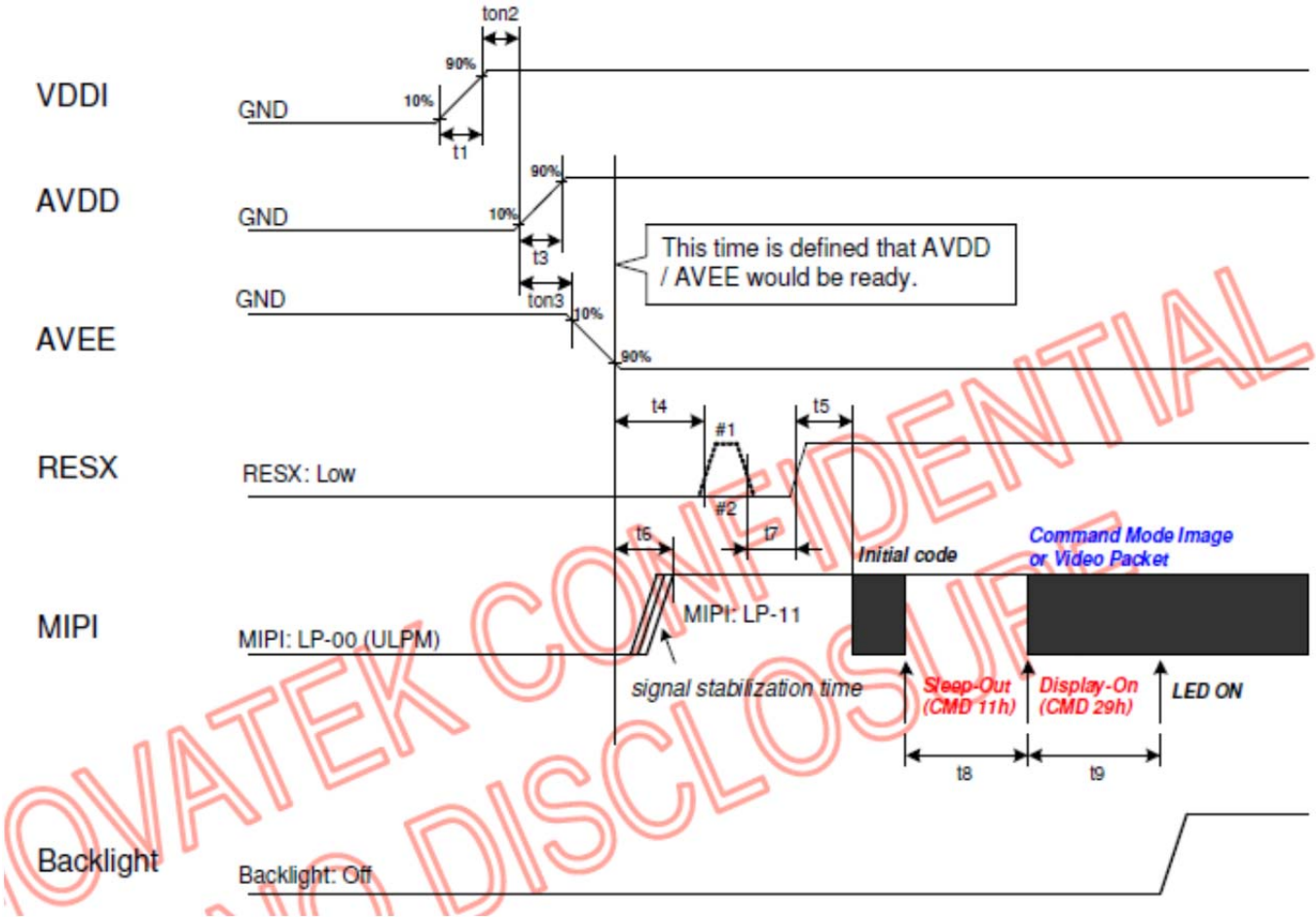
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

9. Power Sequence

(9-1)Power on sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	5	-	-	ms	EXT_DVDD_EN=0
~~ton2~~	~~0~~	~~-~~	~~-~~	~~ms~~	~~EXT_DVDD_EN=1~~
ton3	0	-	-	ms	BTM=0: |AVDD| ≥ |AVEE| during power rising BTM=1: |VGH| ≥ |AVDD| during power rising
ton4	0	-	-	ms	|VGH| ≥ |VGLX| during power rising
ton5	0	-	-	ms	|VGLX| ≥ |AVEE| during power rising
t1	0.2	-	5	ms	
t2	0.2	-	2	ms	
t3	0.2	-	5	ms	
t4	10	-	-	ms	
t5	10	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	us	
t8	120	-	-	ms	
t9	0	-	-	ms	



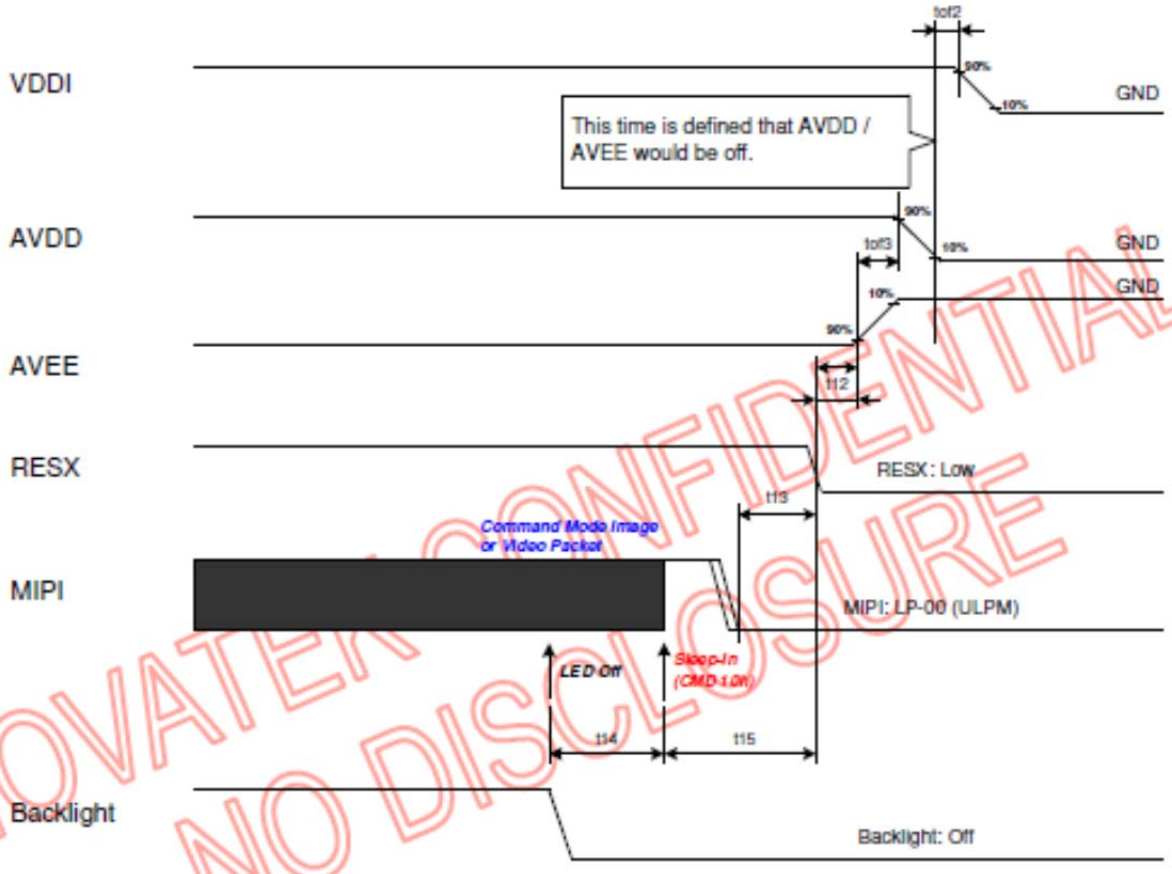
LCD Initialization Sequence table

Power ON Sequence (NT35950) –Command mode-

Display off -> Display on		ES1~ DrIC: NT35950		MIPI State		
No.		Addr.	Data	Data	CLK	Data Type
Power on						
1	Initial condition					
2	Power Supply VDDIO(Typ1.88V)					
3	Wait 10ms					
4	Power Supply AVDD(Typ5.80V)					
5	Wait 0ms					
6	Power Supply AVEE(Typ-5.60V)					
7	Wait 0ms					
8	Enter LP-11 state			LP11	LP11	
9	Wait 10ms			LP11	LP11	
10	RESX go High			LP11	LP11	
11	Wait 10ms			LP11	LP11	
12	RESX go Low			LP11	LP11	
13	Wait 15ms			LP11	LP11	
14	RESX go High			LP11	LP11	
15	Wait 20ms			LP11	LP11	
16	Sleep Mode On			LP11	LP11	
A) Initialization						
1	Data Compression Method Selection	90h	03h	LP	LP	15h
2	VESA DSC ON	03h	01h	LP	LP	15h
3	Page Select Page4	F0h	55h(1st_para)	LP	LP	39h
			AAh(2nd_para)	LP	LP	
			52h(3rd_para)	LP	LP	
			08h(4th_para)	LP	LP	
			04h(5th_para)	LP	LP	
4	VESA DSC Setting	C0h	03h	LP	LP	15h
5	Page Select Page7	F0h	55h(1st_para)	LP	LP	39h
			AAh(2nd_para)	LP	LP	
			52h(3rd_para)	LP	LP	
			08h(4th_para)	LP	LP	
			07h(5th_para)	LP	LP	
6	Display Mode Select(YYG Rainbow RGB)	EFh	01h	LP	LP	15h
7	Page Select Page0	F0h	55h(1st_para)	LP	LP	39h
			AAh(2nd_para)	LP	LP	
			52h(3rd_para)	LP	LP	
			08h(4th_para)	LP	LP	
			00h(5th_para)	LP	LP	
8	Set to "Display Data Path Control"(Command_Mode)	B4h	01h	LP	LP	15h
9	Tearing Effect Line ON	35h	00h	LP	LP	15h
10	Page Select(CMD3_Enable)	FFh	AAh(1st_para)	LP	LP	39h
			55h(2nd_para)	LP	LP	
			A5h(3rd_para)	LP	LP	
			80h(4th_para)	LP	LP	
11	Black_Image_Display_Set	6Fh	01h	LP	LP	15h
12		F3h	10h	LP	LP	15h
13	Page Select(CMD3_Disable)	FFh	AAh(1st_para)	LP	LP	39h
			55h(2nd_para)	LP	LP	
			A5h(3rd_para)	LP	LP	
			00h(4th_para)	LP	LP	
B) Set Display on						
1	Display On	29h	-	LP/HS	LP/HS	05h
C) Exit Sleep						
1	Exit sleep mode (Sleep out)	11h	-	LP/HS	LP/HS	05h
2	Wait 120ms(Wait more than 6frame)			LP11	LP11	
3	Display data transfer			HS	HS	
4	Backlight On					

(9-2)Power off sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
tof1	0	-	-	µs	
tof2	0	-	-	ms	
tof3	0	-	-	ms	
tof4	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100			ms	



Power OFF Sequence (NT35950)

Display on -> Display off		ES1~ DrIC: NT35950		MIPI State		
No.		Addr.	Data	Data	CLK	
D) Set Display off						
1	Display Off	28h	-	LP/HS	LP/HS	
2	Backlight Off			LP11	LP11	
3	Wait 10ms			LP11	LP11	
E) Sleep set						
1	Enter Sleep Mode	10h	-	LP/HS	LP/HS	
2	Wait 150ms			LP11	LP11	
3	Data transfer stop			LP11	LP11	
4	MIPI drive to LP-00			LP00	LP00	
Power off						
1	XRES=Low					
2	Wait 5ms					
3	Power off VSN(Typ-5.60V)					
4	Wait 5ms					
5	Power off VSP(Typ5.80V)					
8	Wait 5ms					
9	Power off VDDIO(Typ1.88V)					
Re-Power on						
1	(Wait more than 100ms)					
2	Power Supply VDDIO(Typ1.88V)					
	see Display on sheet for further sequence					

11. Optical Characteristic

Table10

VDDI=1.88V, AVDD=5.8V, AVEE=-5.6V, ILED=20mA/pcs, Ta = 25C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	θ=0°	800	1200	-	-	Note11-1,2
Response Time	τr + τd	θ=0°	-	-	40	ms	Note11-3
White Chromaticity	x	θ=0°	0.26	0.31	0.36	-	
	y		0.28	0.33	0.38	-	
Red Chromaticity	x		0.60	0.65	0.70	-	
	y		0.28	0.33	0.38	-	
Green Chromaticity	x		0.15	0.20	0.25	-	
	y		0.65	0.70	0.75	-	
Blue Chromaticity	x		0.10	0.15	0.20	-	
	y		0.02	0.07	0.12	-	
Brightness	L	θ=0°	300	450	-	cd/m²	I_{LED}=20mA
Uniformity	U	θ=0°	70	-	-	%	Note11-4
NTSC Ratio	S	θ=0°	-	70	-	%	
Gamma	γ	θ=0°	1.8	2.2	2.6	-	
Flicker	F	θ=0°	-	-	10	%	Note11-5
Crosstalk	CT	θ=0°	-	-	5	%	Note11-6

*The measuring method of the optical characteristics is shown by the following figure.

*A measurement device is TOPCON luminance meter SR-3. (Measurement angle 1°)

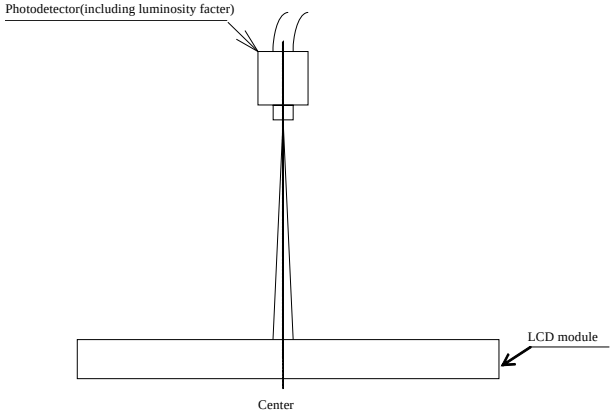


Fig.7

Note 11-1) Contrast / NTSC / GAMMA viewing angle is defined as follows.

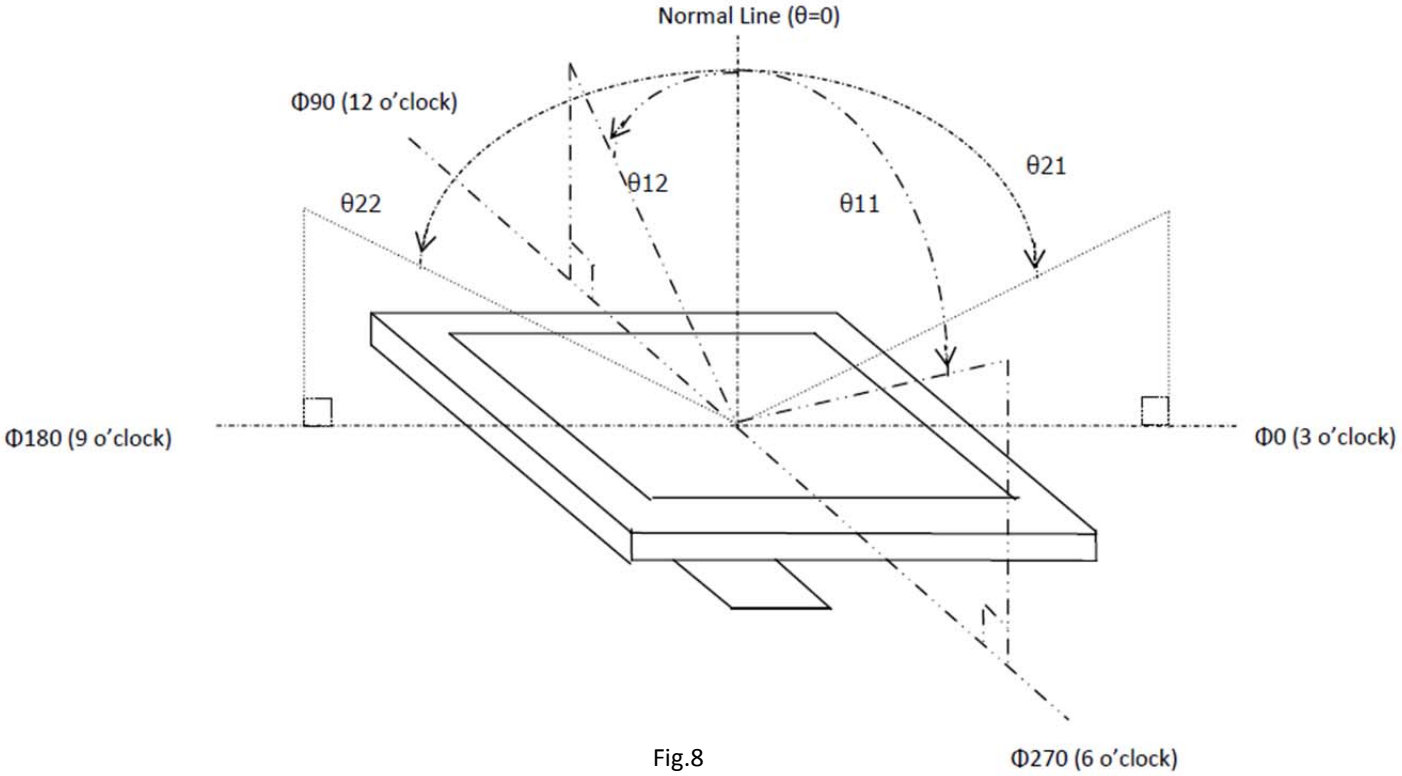


Fig.8

Note 11-2) Definition of contrast ratio:

The contrast ratio is defined as the follows:

$$Contrast\,ratio\,(CR) = \frac{Luminance(brightness)\,with\,all\,pixels\,white}{Luminance(brightness)\,with\,all\,pixels\,black}$$

Note 11-3) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white"

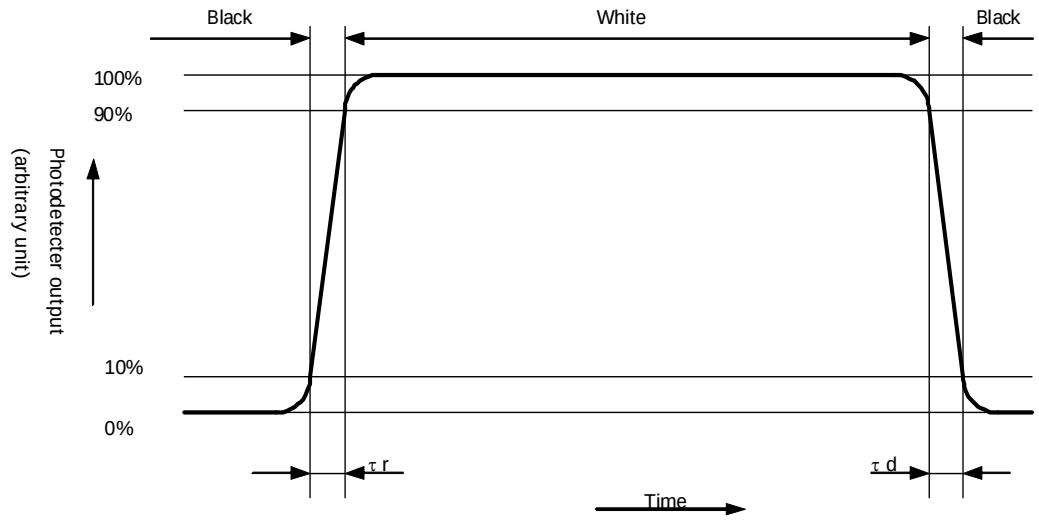


Fig.9

Note 11-4) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

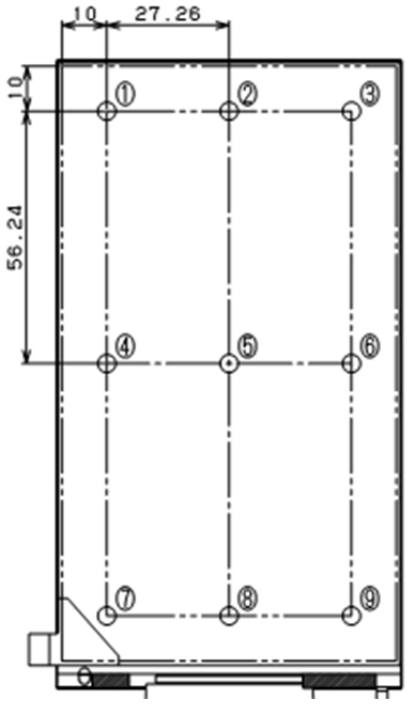


Fig.10

Note 11-5) Measuring systems: Yokogawa “3298”

- VDDI=1.88V, AVDD=5.8V, AVEE=-5.6V, ILED=20mA/pcs, Ta = 25C, LED back-light: ON, Environment brightness < 150 lx
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Measuring pattern “Middle gray(V127/V255)”.
- Flicker in measuring spot F0 according to Center of Display

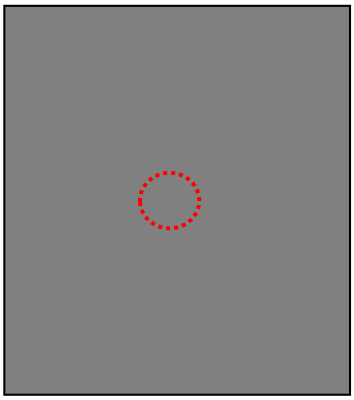


Fig.11

Note 11-6) Definition of Crosstalk

$$CT_B = \frac{|Y_B(x) - Y_G(x)|}{Y_G(x)} \times 100\,(\%)$$

$$CT_W = \frac{|Y_W(x) - Y_G(x)|}{Y_G(x)} \times 100\,(\%)$$

x=U, D, L or R

Gray level=V128

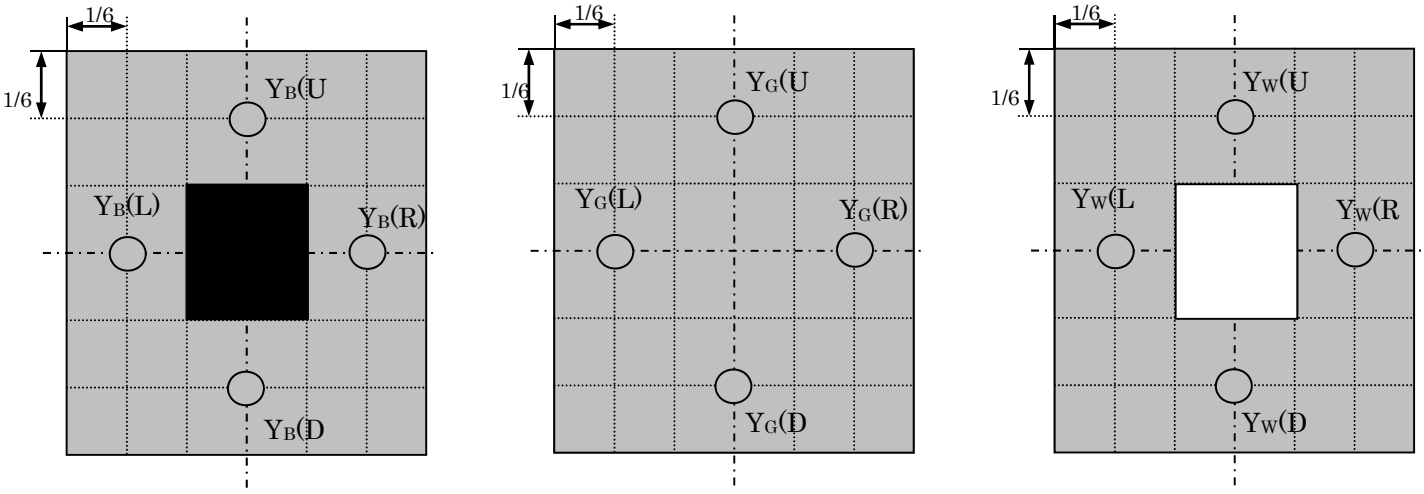


Fig.12

12. Reliability

Table 22

No.	Test item	Conditions
1	High temperature storage test	Ta = +70°C, 240h
2	Low temperature storage test	Ta = -30°C, 240h
3	High temperature operation test	Ta = +60°C, 240h
4	Low temperature operation test	Ta = -20°C, 240h
5	High temperature and high humidity operation test	Ta = +40°C95%RH, 240h (No condensation)
6	Heat shock test	Ta = -20℃(30min) ~ 70°C(30min), 5cycle
7	Electro static discharge test	±200V, 200pF(0Ω) to Terminals(Contact) (1 time for each terminals) None Operation
8	Packing Vibration test	Frequency: 5 to 50Hz (Round trip 3 minutes) Acceleration: 1G All Amplitude: 20 to 0.2mm Direction: Up/Down(60min), Left/Right(15min), Front/Back(15min) (3 Direction) Amplitude 20mm 0.2mm 20mm 0.2mm Frequency 5Hz 50Hz 5Hz 50Hz o——o——o——o |← 3 minutes →|
9	Packing Drop test	Height: 75cm, Drop times: 10 Drop (1 Conner,3 Edges and 6 Faces)

Note 12-1) As for the Reliability test item of No.1-No.6, LCD modules are checked by two hours later.

Note 12-2) Check items for other Test

In the standard condition, there shall be no practical problems that may affect the display function.

13. Indication of lot number

Attached location is shown in Fig. 30 Outline deimensions.

The lot number is shown on a label.

LS055R1SX04 Y M XXXXX R F

Sharp model number

*Detail of S/N

Y	: Manufacture year	/ 2015 = 5, 2016 = 6
M	: Manufacture month	/ January= A, ------- December=L
XXXXX	: Serial number (5 digits)	/ 00001~99999
R	: Revision code	/ A, B, --------
F	: Factory code	/ STECH=S, Others=A

14. Forwarding form

TBD

Condition for storage

Environment

(1) Temperature: 0 to 40°C

(2) Humidity: 60%RH or less (at 40°C)

(3) Atmosphere: Harmful gas, such as acid or alkali which erodes electronic components and/or wires, must not be detected.

(4) Period: about 3 months

(5) Opening of the package: In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.

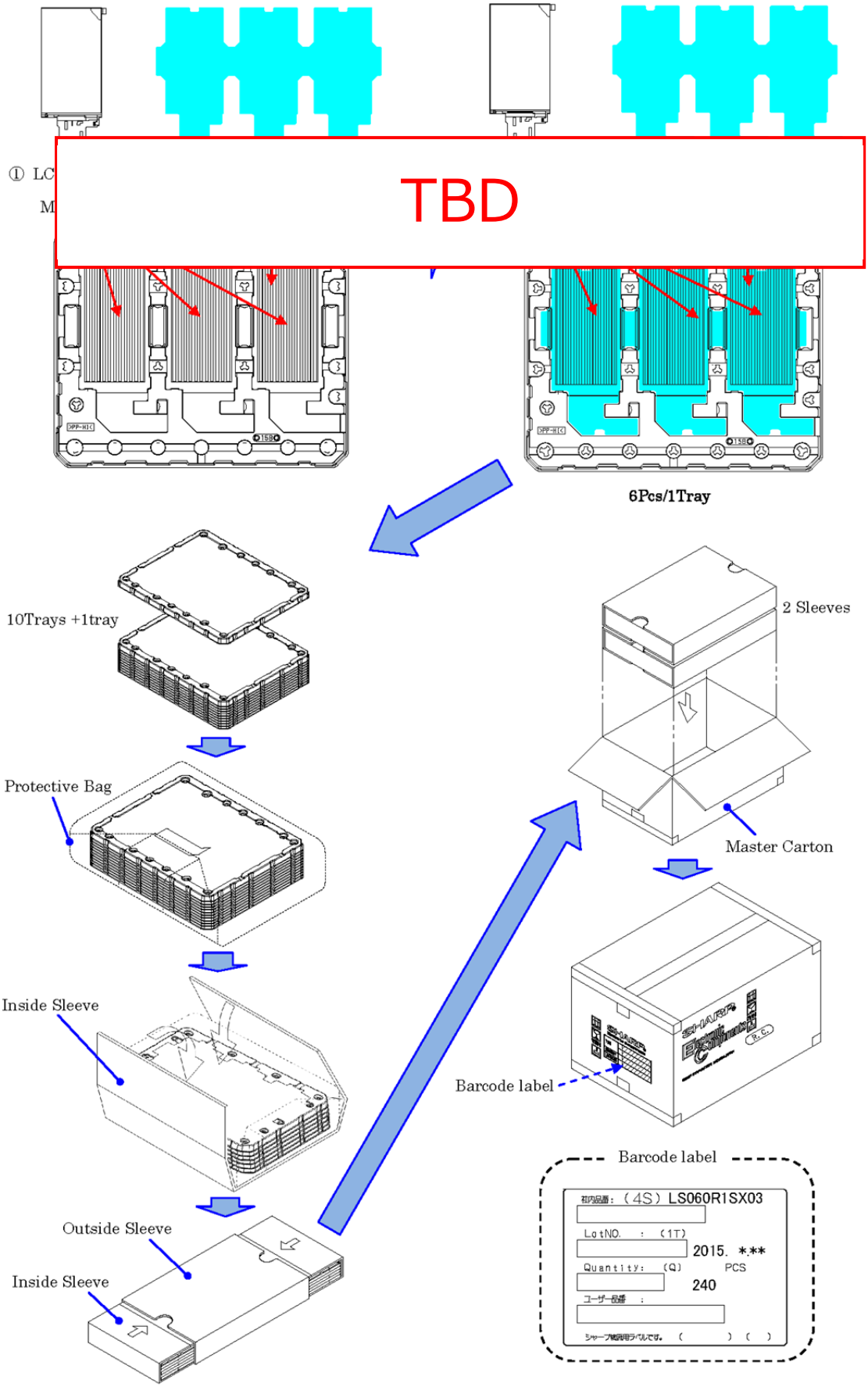
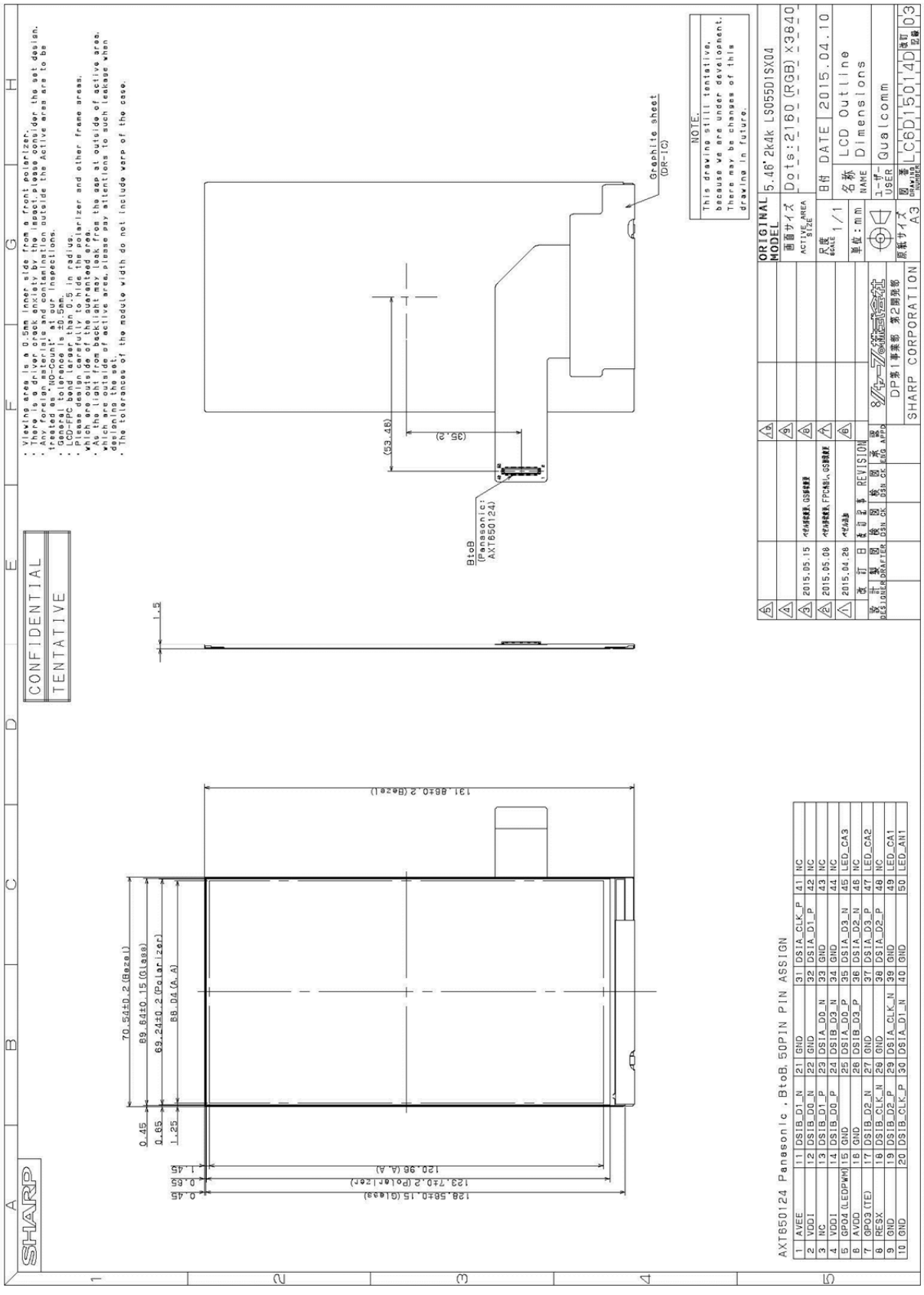


Fig. 13 Packaging style

15. Outline dimensions



1	AVEE	11	DSIB_D1_N	21	GND	31	DSIA_CLK_P	41	NC
2	VDDI	12	DSIB_D0_N	22	GND	32	DSIA_D1_P	42	NC
3	NC	13	DSIB_D1_P	23	DSIA_D0_N	33	GND	43	NC
4	VDDI	14	DSIB_D0_P	24	DSIB_D3_N	34	GND	44	NC
5	GPO4 (LEDPWM)	15	GND	25	DSIA_D0_P	35	DSIA_D3_N	45	LED_CA3
6	AVDD	16	GND	26	DSIB_D3_P	36	DSIA_D2_N	46	NC
7	GPO3 (TE)	17	DSIB_D2_N	27	GND	37	DSIA_D3_P	47	LED_CA2
8	RESX	18	DSIB_CLK_N	28	GND	38	DSIA_D2_P	48	NC
9	GND	19	DSIB_D2_P	29	DSIA_CLK_N	39	GND	49	LED_CA1
10	GND	20	DSIB_CLK_P	30	DSIA_D1_N	40	GND	50	LED_AN1

Fig.14 Outline dimension

16. FPC Schematic

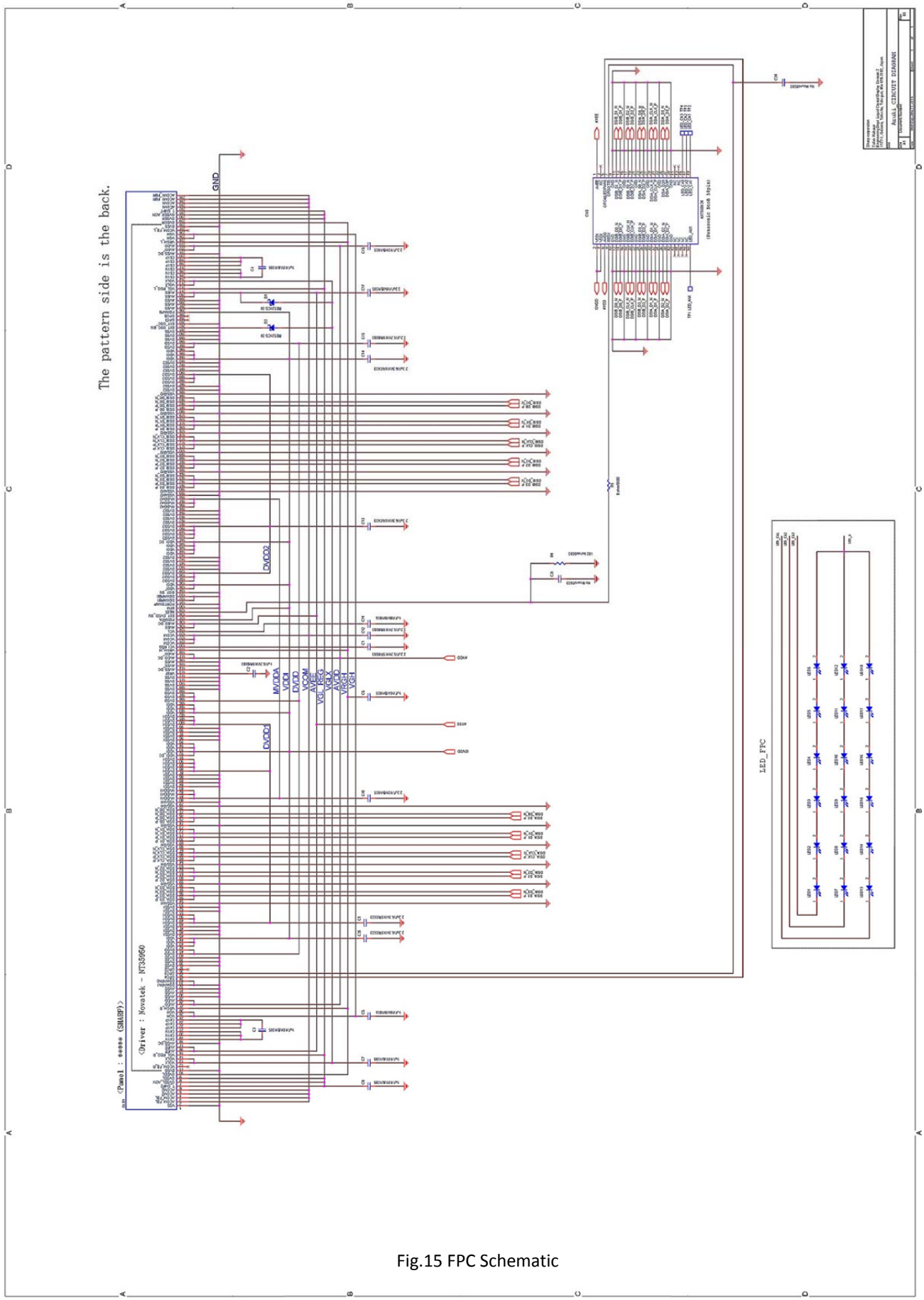


Fig.15 FPC Schematic

17. Incoming Inspection Standards for LCD module

17-1. Scope

These incoming inspection standards shall apply to TFT-LCD modules (hereinafter called "MODULE") supplied by Sharp Corporation (hereinafter called the "Seller") to Qualcomm Corporation. (Hereinafter called the "Buyer").

17-2. Incoming inspection

The Buyer shall have the right to conduct at its own cost and expense, an incoming inspection of the Module's at the destination specified in the relevant bills of lading in accordance with the Module's specifications separately agreed upon and the inspection standard set forth in this Article.

The Buyer shall notify the Seller writing of a result of such inspection judgment (acceptance or rejection) in accordance with the said inspection standard within 40 days after the date of the bills of lading.

Should the Buyer fail to so notify the seller within the said 40 days period, the Buyer's right to reject the Module's shall then lapse, and the said Module's shall be deemed to have been accepted by the Buyer.

17-3. Method of incoming inspection

Unless otherwise agreed in writing, the method of incoming inspection shall be in accordance with a sampling inspection based on ISO 2859-1.

a) Lot size : Quantity per shipment lot per model
b) Sampling type : Normal inspection, Single sampling
c) Inspection level : II
d) Sampling table : Table in ISO 2859-1

17-4. Acceptable quality level ("AQL")

The AQL for major and minor defects shall be respectively set forth below.

a) Major defects : AQL 0.65
b) Minor defects : AQL 0.65 Based on overall evaluation

17-5. Classification of defects

Defects are classified as major defect and a minor defect according to the degree of defect defined herein.

a) Major defect

A major defect is a defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose.

Function defect

Abnormal operation including distinct R, G, B line defects and /or white line defect.

b) Minor defect

A minor defect either is a defect that is not likely to reduce materially the usability of the product for its intended purpose, or is a departure from an established having little bearing on the effective use or operation of the product.

1. Dot Defect
2. Display non-uniformity
3. Afterimage
4. Extraneous substances
5. Scratches
6. Dents
7. Contrast ratio
8. Current dissipation

17-6. Determination of acceptability and subsequent disposal

If the number of defects found in the sample Module's from the lot is equal to or less than the applicable acceptance level, the lot shall be accepted.

If the number of defects is greater than the applicable acceptance level, the lot shall be rejected. The Buyer shall inform the Seller of a detailed result of such inspection within the time period stipulated in Article 2.

The disposal is as follows:

a) Accepted lot
An acceptance under the above incoming inspection shall constitute an acceptance by the Buyer of such lot of the Module's in terms of the landed quality thereof.

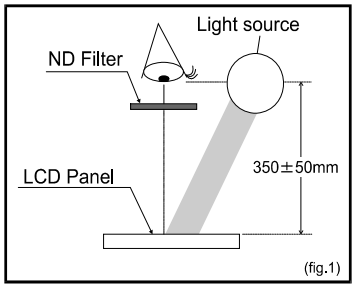
b) Rejected lot
If a lot of PRODUCTS is rejected under the above incoming inspection due to any defects for which the Seller is responsible and such a fact is clearly confirmed by the Seller, the Seller shall exercise one of the following three options. This must be determined with mutual consent and shall be confirmed by the Seller. The best choice of the options shall be left to the Seller's discretion and the Seller shall advise the Buyer of its choice not later than two weeks of receipt of the Buyer's advice:

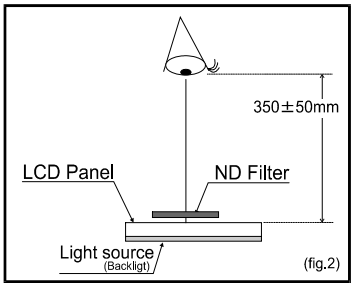
1. The Buyer shall return the defective lot to the place to be designated by the Seller and the Seller shall screen all of the PRODUCTS in the lot and repair defective PRODUCTS.
2. The Seller shall screen all of the PRODUCTS in the lot and repair defective products within a reasonable time period at the Buyer's facility.
3. The Buyer shall screen the entire lot for the good modules at the expense of the Seller to be separately agreed upon. The rejected PRODUCTS shall be returned to the place to be designated by the Seller.

17-7. Inspection conditions

Item	Inspection conditions	
	Reflection inspection	Back light inspection
Panel surface illumination	1000 ± 200lx (uniform lighting on the panel surface)	Use Backlight (Note 1)
Light source	Florescent tube	LED (Back light)
Ambient illumination	300 ~ 700 lx	←
Ambient temperature	20 ~ 25 C	←
Ambient Humidity	65±5% RH	←
Viewing distance	350 mm ± 50 mm	←
Direction of lighting	Set light tube without reflection on the panel surface	-
Viewing angle	The surface of the Module and the eyes of the inspector shall be 90 ± 5 degrees.	←
Check pattern (Bright dot)	Black picture position	←
Check pattern (Black dot)	White picture position	←
How to use ND filter	Use ND filter close to eyes (fig.1)	Use ND filter open to eyes (fig.2)

Note 1) Please refer to the panel surface brightness of the specifications





17-8. Inspection area

Item	Active area	Outline
Foreign particles(dot)	Do	-
Foreign particles(liner)	Do	-
Scratch	Do	-
Bubble	Do	-
Corner Chipping	-	Do
Edge Chipping	-	Do
Light leakage on the edge	-	Do
FPC	-	Do

17-9.Dot defect

Acceptable dot defects

Item			Maximum acceptable number	Inspection Pattern	Note
Dot defect (Note 2)	Bright dot	Red or Blue	2	All Black	Visible through 2% ND filter d≧5mm
		Green	0		
		adjacent dots	0		Not allowed
	Black dot	1 dot or 2 adjacent dots	Ignore	All White	Show the judgment sample to Page33 d≧5mm
		3~6 adjacent dots	6		
		7 adjacent dots	1		
		8 adjacent dots or more	0		
Total number			8		

Note 2) A defect whose area is more than 50% of the dot is regarded as a dot defect.

17-10. External inspection

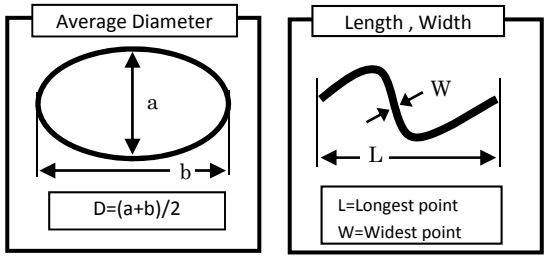
Extraneous Substances, Bubble, Scratch

Length : L (mm) , Average diameter : D (mm) , Width : W (mm)

Item	Inspection standards (Note 4)				Inspection Pattern	note
	Ignore	Count		NG		
Foreign Particles(dot) Black or white spot	D<0.1	0.1≤D≤0.2	N≤3	D>0.2	All Black All White	d≥5mm
Foreign Particles(liner) Black or white liner (Note 3)	W<0.01, L<3.0	0.01≤W≤0.05, L≤3.0	N≤1	W>0.05 or 3.0<L	All Black All White	d≥5mm
Scratch	-	W≤0.05, L≤3.0	N≤2	W>0.05 or 3.0<L	All Black All White	-
Bubble	D≤0.1	0.1<D≤0.5	N≤4	D＞0.5	All Black All White	-
Dent on polarizer	D≤0.1	0.1<D≤0.2	N≤2	D＞0.2	All Black All White	-
Defect Number	N≤7					

Note 3) Black wool, hair, Polarizer scratch, Salient point and Bubble

Note 4) Definitions for All Black / All White: All Black: V0/255, All White: V255/255



17-11.Mura

There should be no distinct non-uniformity visible through 2% ND filter.

17-12.Glass clack

Item	Maximum acceptable number	Note
Chip on glass corner (Part A)	L≤5mm, D≤1.0mm	Fig. 3-A Fig. 3
Chip on glass corner (Part B)	FPC and patterns are not affected.	Fig. 3-B Fig. 3
Chip on glass edge	L≤10mm, D≤1.0mm	Fig. 3

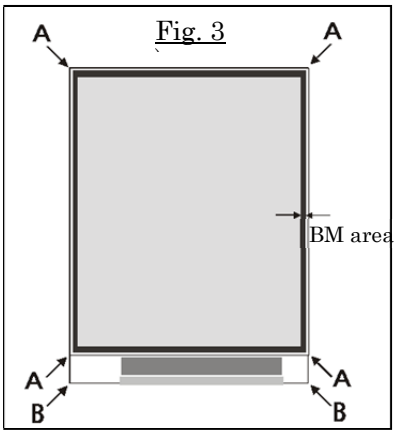


Fig. 3

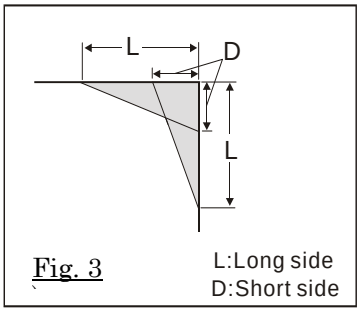


Fig. 3 L:Long side D:Short side

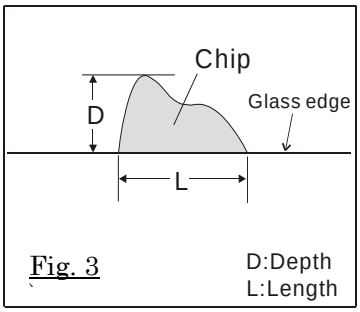


Fig. 3 D:Depth L:Length

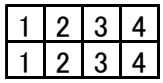
17-13. Others

Item	Maximum acceptable number	Note
Light leakage on the Glass edge	Ignore	
FPC	Pin and circuit damage are not allowed.	

17-14.Dot defect (Black dot) definition

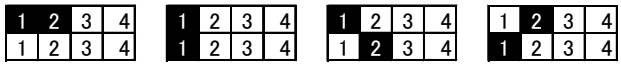
Count Section

Black dots jointed are counted as one black Dot Defect.
Black dots jointed are allowed within two Vertical x four Horizontal area.
(1,2,3)=(R,G,B)/(G,B,R)/(B,R,G)

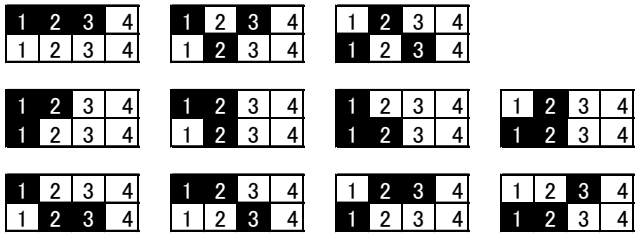


[Example]

Two black dots jointed are counted as one black Dot Defect.
(1,2,3)=(R,G,B)/(G,B,R)/(B,R,G)



Three black dots jointed are count as one black Dot Defect.
(1,2,3)=(R,G,B)/(G,B,R)/(B,R,G)



Four black dots jointed are count as one black Dot Defect.
(1,2,3,4)=(R,G,B,R)/(G,B,R,G)/(B,R,G,B)