4M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6 or -7) and power consumption(Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, self-refresh operation is available in L- version. This 4Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

• Part Identification

- KM416V4000A/A-L (3.3V, 8K Ref.)
- KM416V4100A/A-L (3.3V, 4K Ref.)

• Active Power Consumption Unit : mW

Speed	8K	4K
-5	396	540
-6	360	504
-7	324	468

• Refresh cycles

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM416V4000A*	8K	64ms	128ms
KM416V4100A	4K		

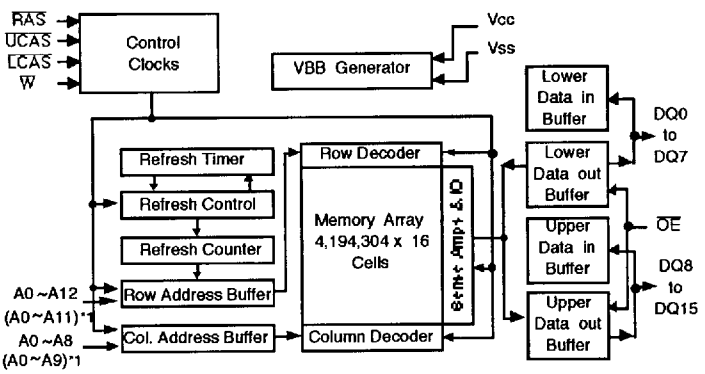
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

• Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	17ns	130ns	45ns

• Fast Page Mode operation
• 2 $\overline{CAS}$ Byte/Word Read/Write operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Self-refresh capability(L-ver only)
• LVTTL(3.3V) compatible inputs and outputs
• Early Write or output enable controlled write
• JEDEC Standard pinout
• Available in Plastic TSOP(II) package
• +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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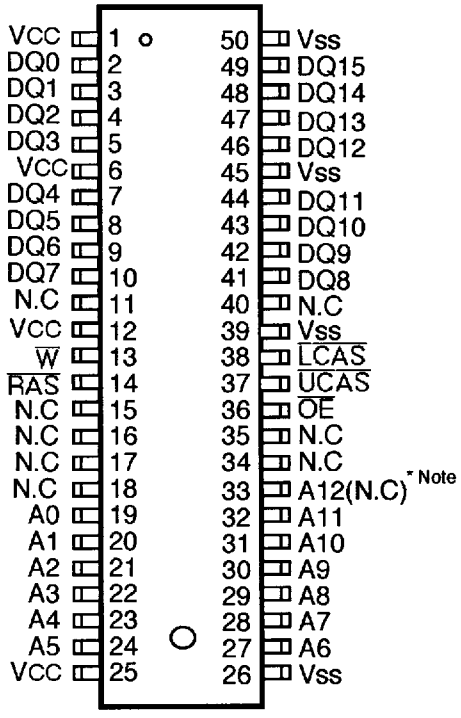
PIN CONFIGURATION (Top Views)

• **KM416V40(1)00AS**



* Note : A12 --> 8K Product(KM416V4000A)
N.C --> 4K Product(KM416V4100A)

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VCC	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	V

*1 : Vcc + 1.3V/15ns, Pulse width is measured at Vcc.
*2 : - 1.3V/15ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V4000A	KM416V4100A	
I_{CC1}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	2 2	2 2	mA mA
I_{CC3}	Don't care	-5 -6 -6	110 100 90	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	90 80 70	90 80 70	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	μA μA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	550	550	μA
I_{CC8}	L	Don't care	450	450	μA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$,Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
Din = Don't care, T_{RC}= 31.25μs, T_{RAS}=T_{RAS}min~300 ns

I_{CC8} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ15= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C, Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		153		180		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		17	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	10		10		15		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	16

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,19
Data hold time	tDH	10		10		15		ns	9,19
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		38		45		ns	7,15
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		83		95		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	14
Access time from $\overline{CAS}$(Fast page cycle)	tCACP		15		17		20	ns	
Access time from column address(Fast page)	tAAP		25		30		35	ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		17	ns	
$\overline{OE}$ to data delay	tOED	13		13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	13	0	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width(C-B-R self refresh)	tRASS	100		100		100		us	20
$\overline{RAS}$ precharge time (C-B-R self refresh)	tRPS	90		110		130		ns	20
$\overline{CAS}$ hold time (C-B-R self refresh)	tCHS	-50		-50		-50		ns	20

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		43		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		88		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		58		65		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		18		20		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and are not referenced to V_{oh} or V_{ol}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.

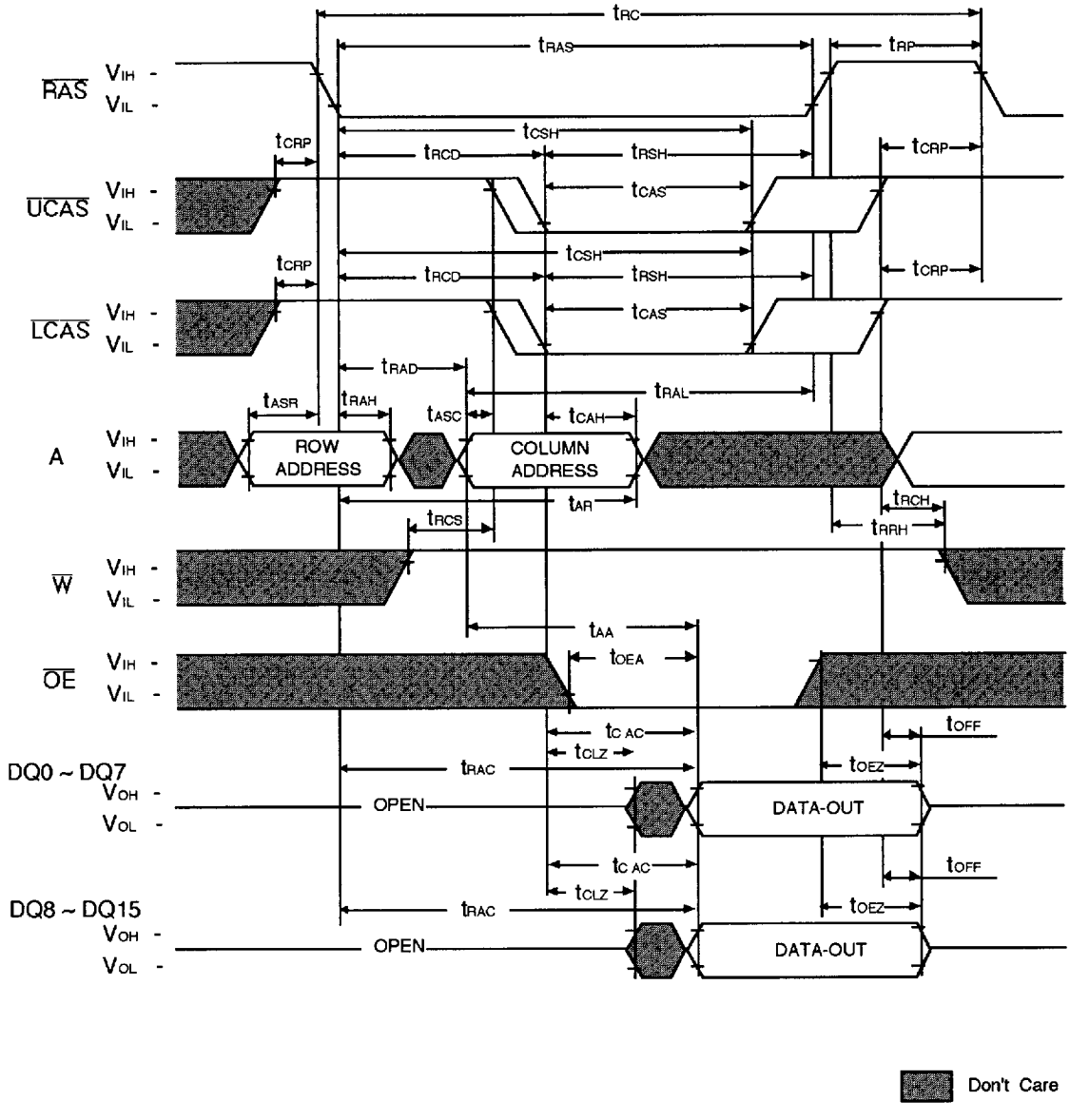
KM416V40(1)00A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

TIMING DIAGRAM

WORD READ CYCLE

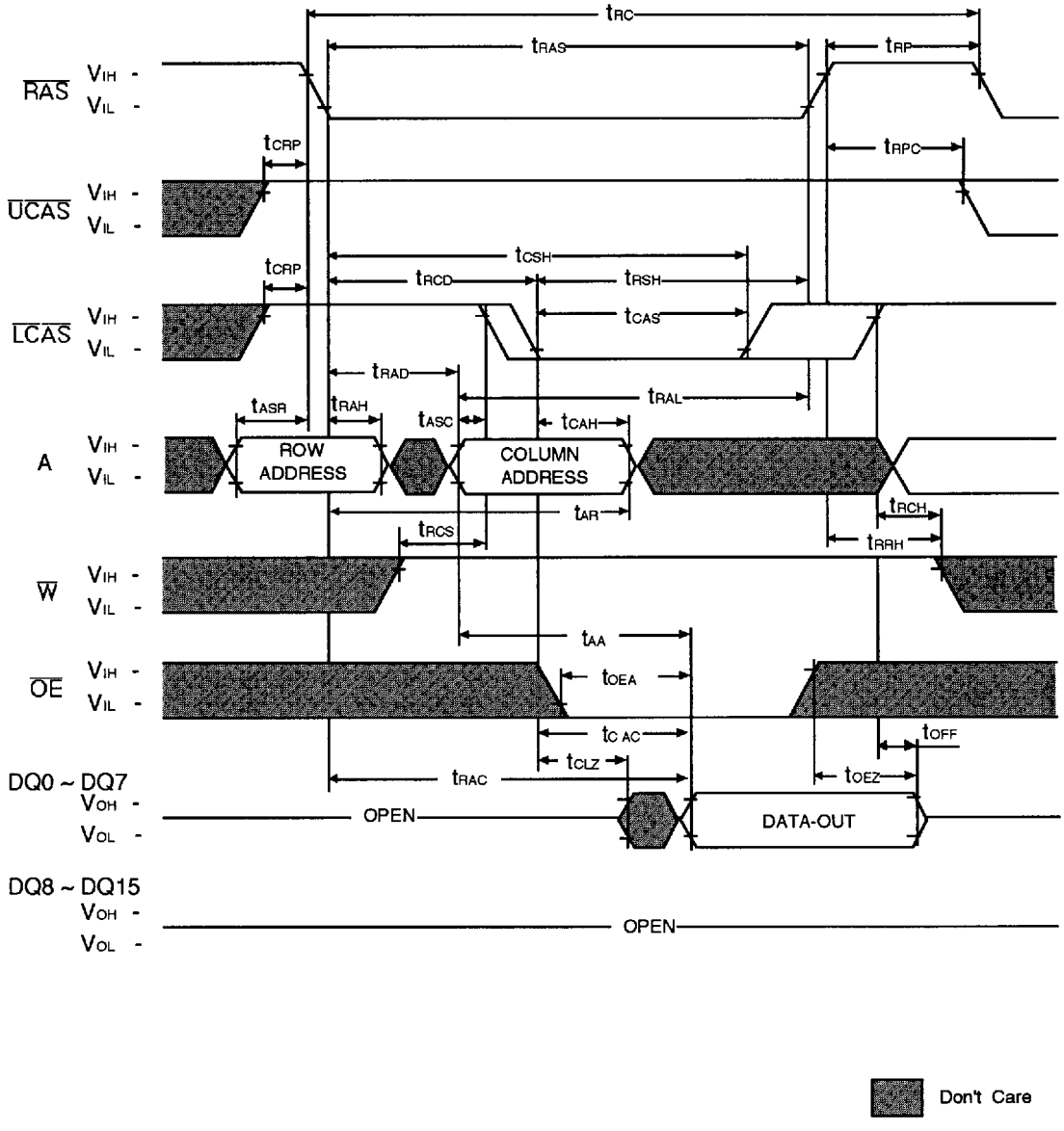
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

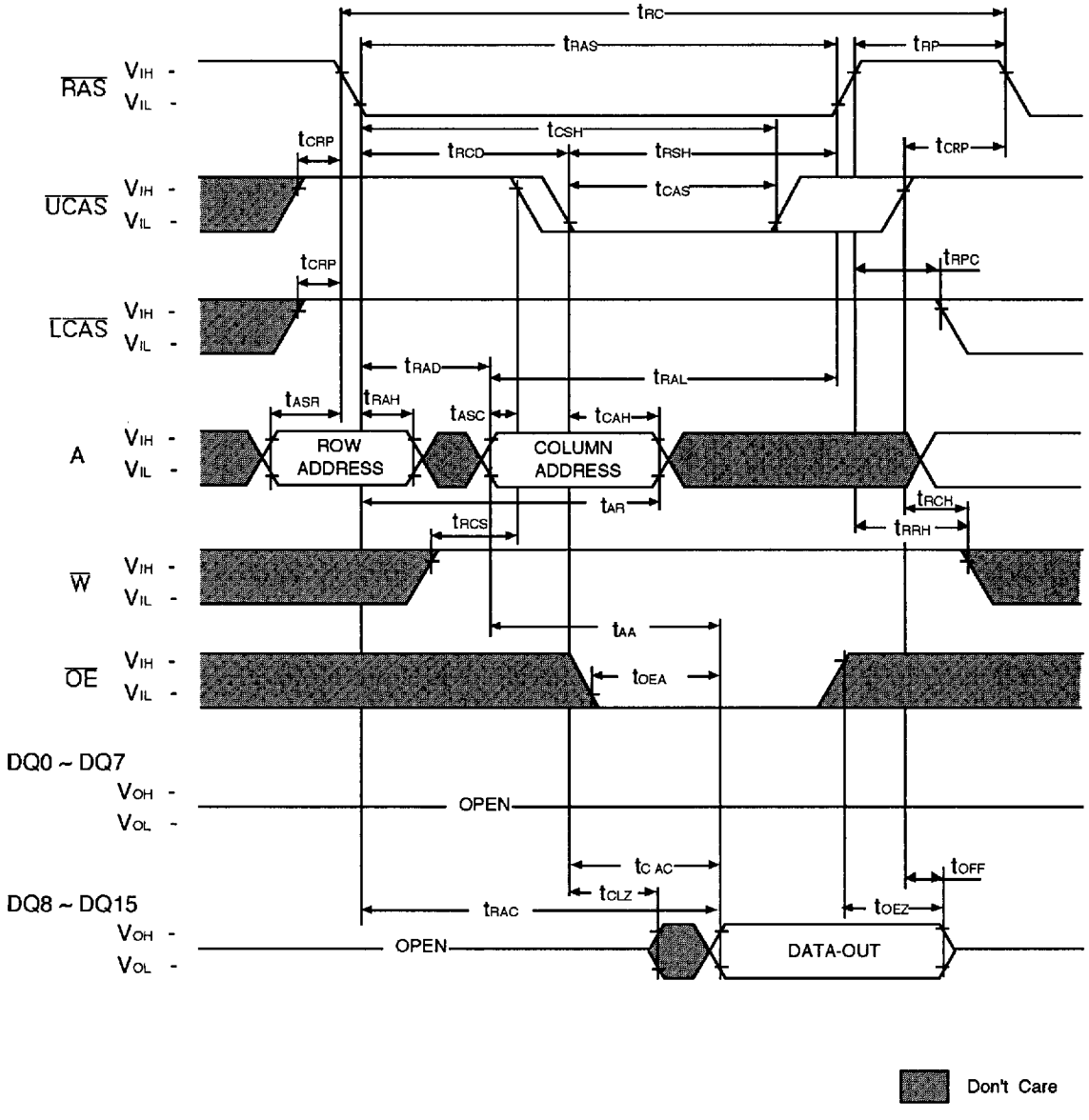
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

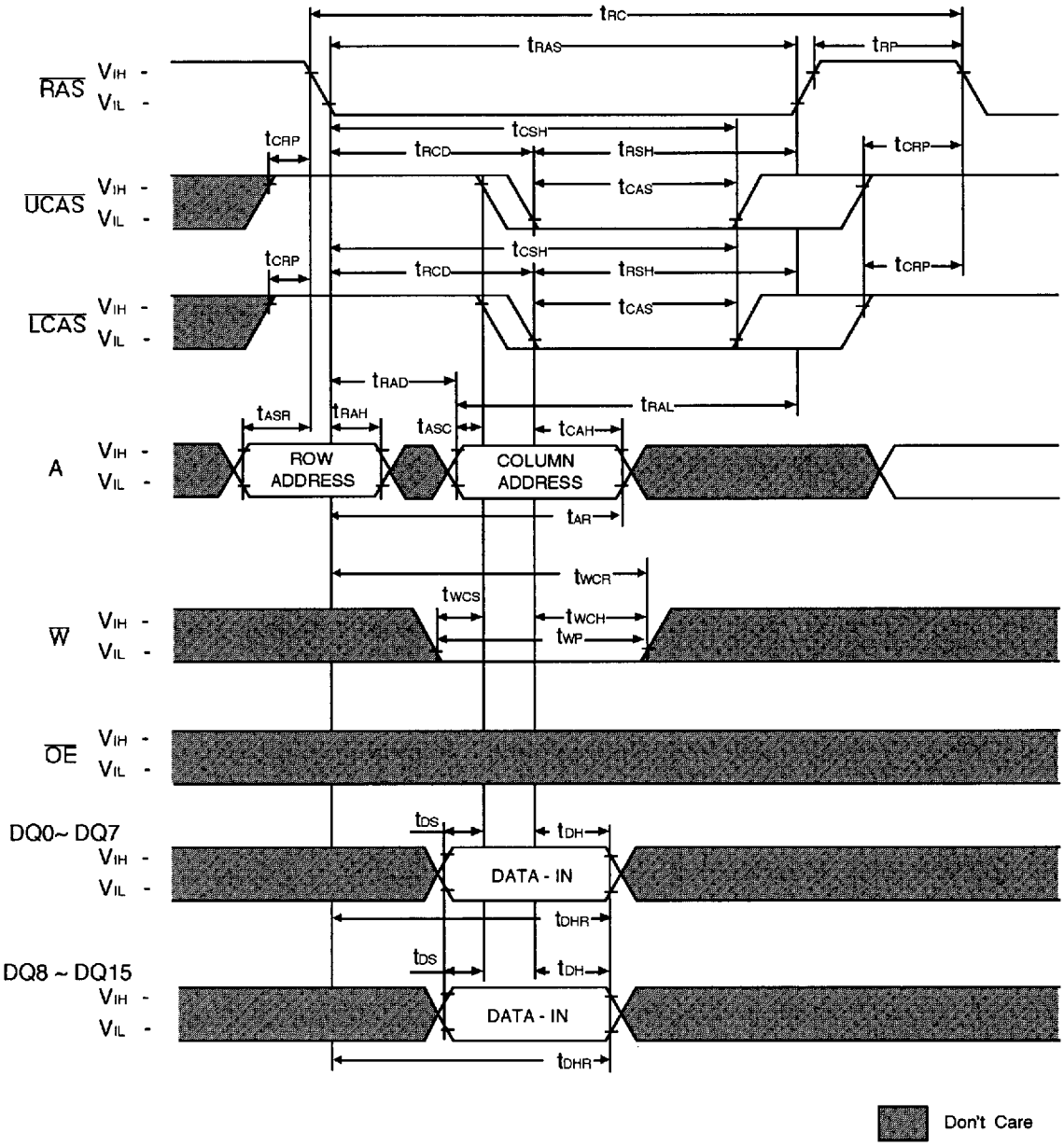
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



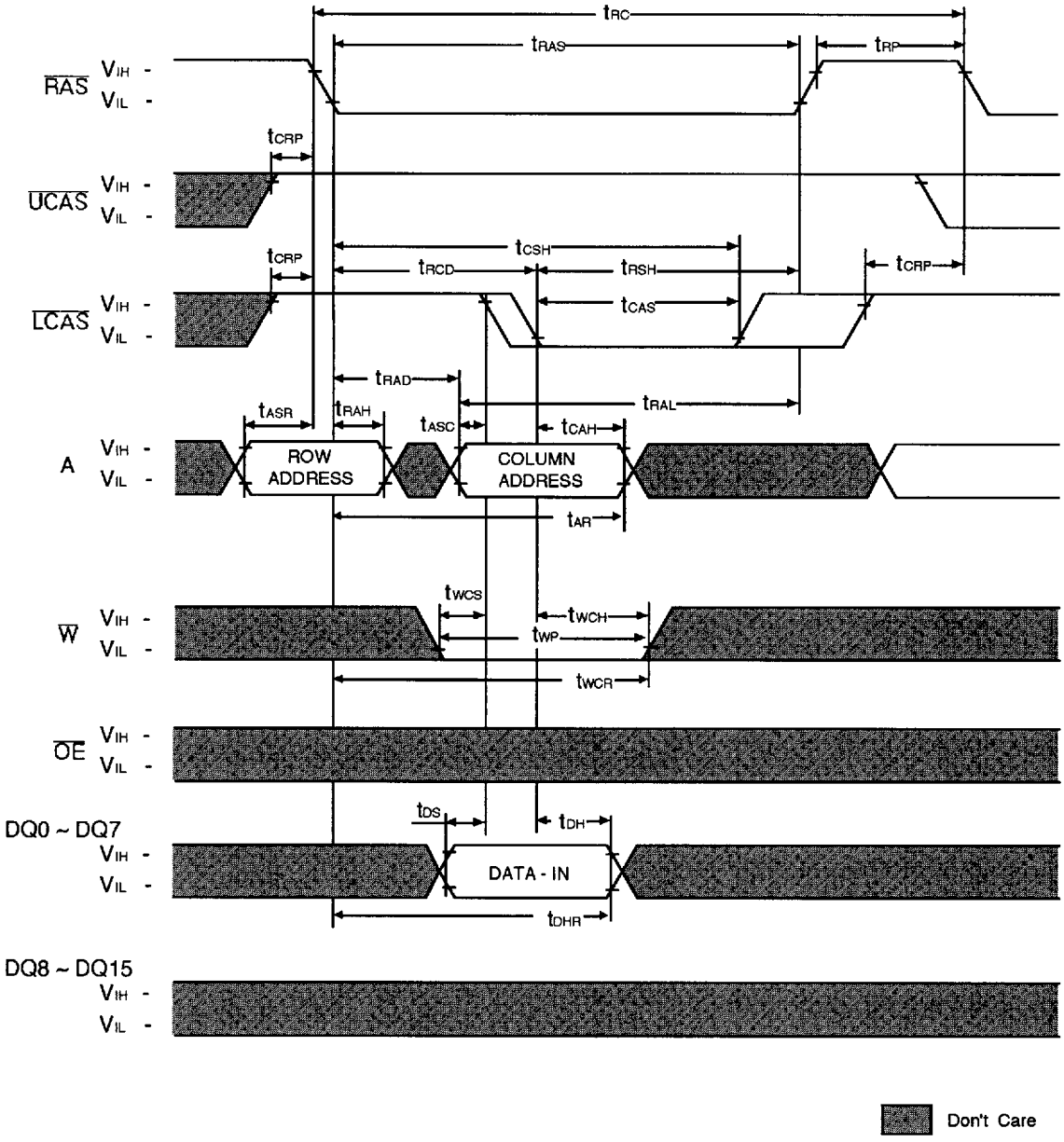
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



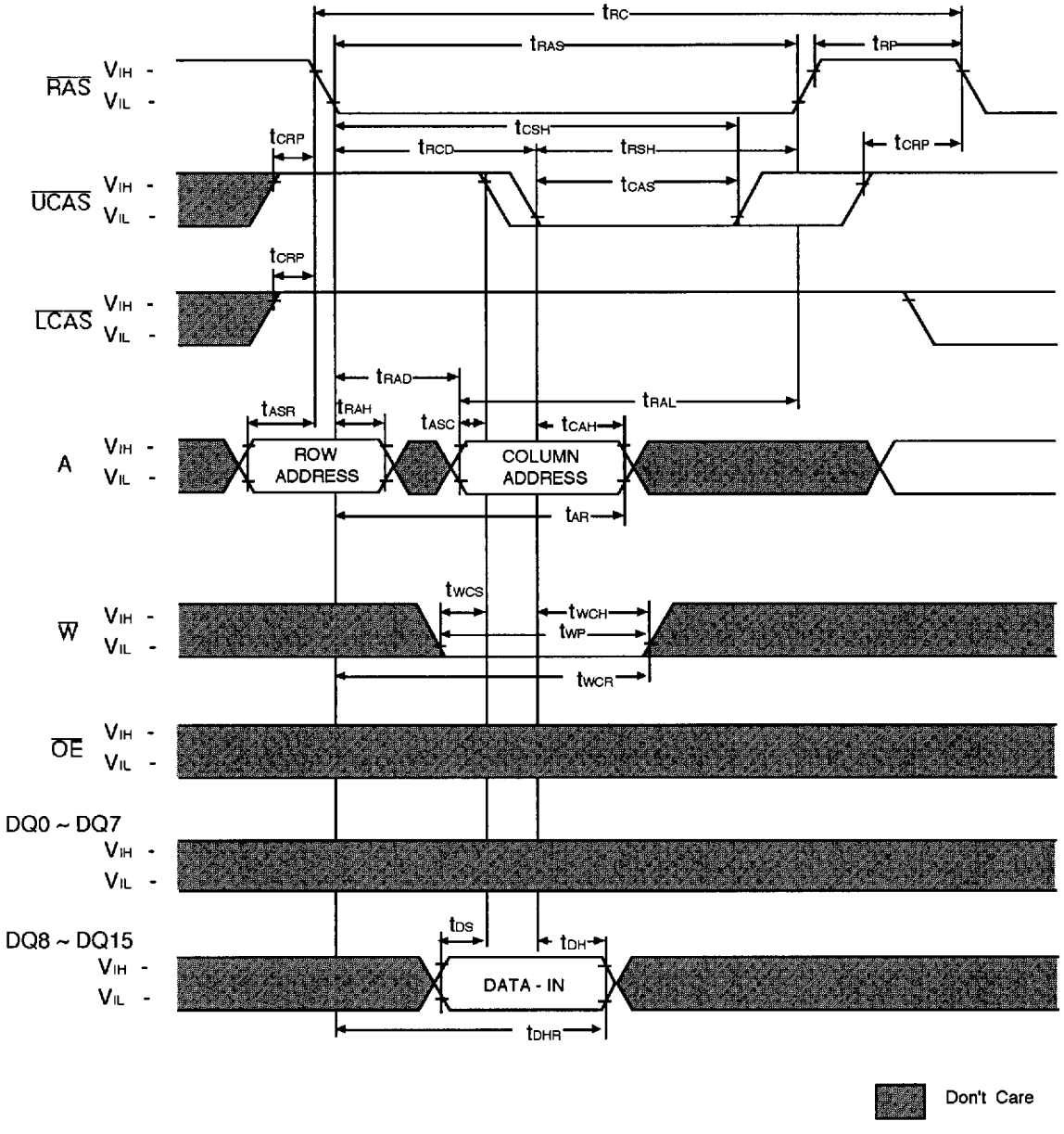
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



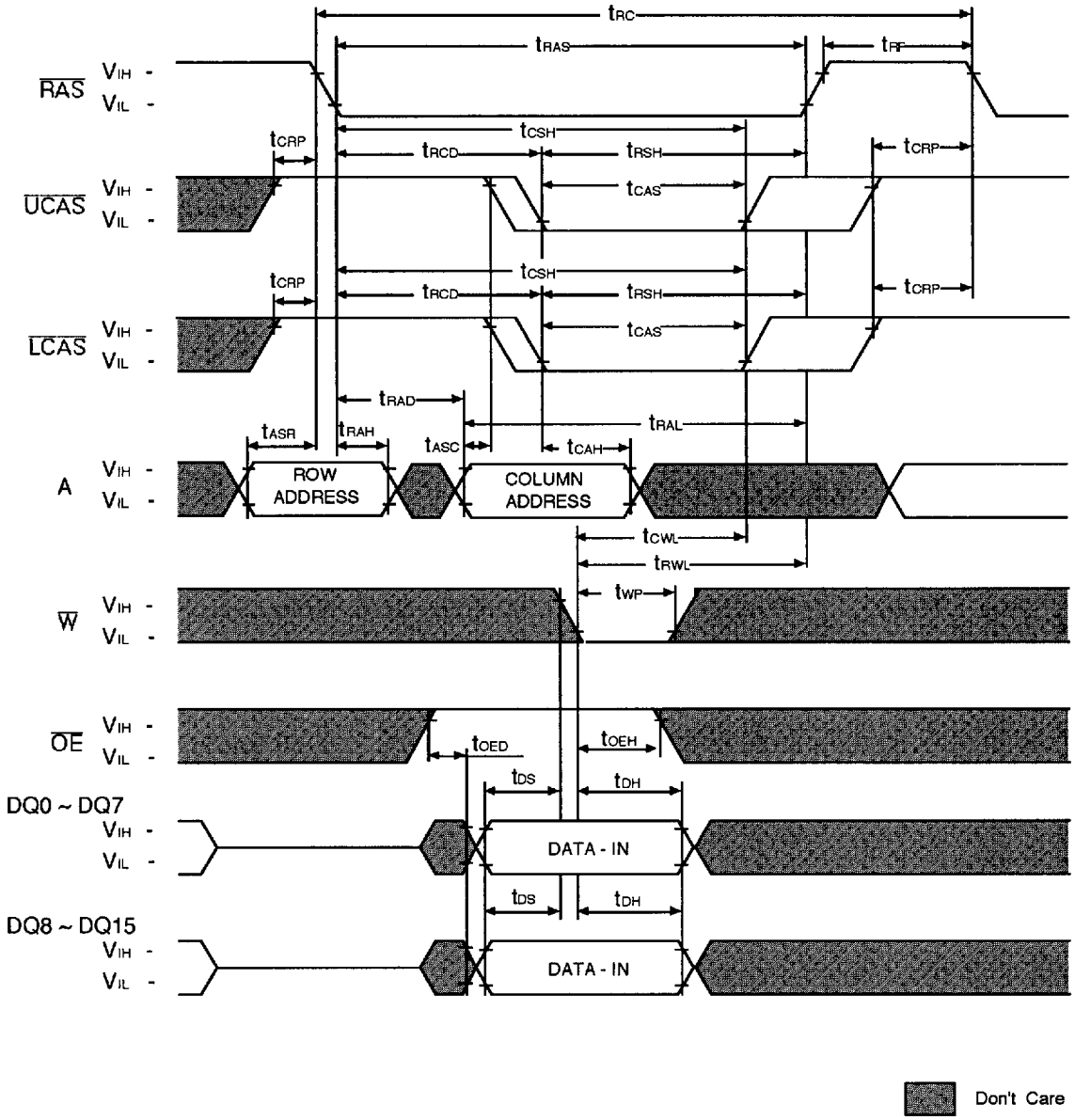
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



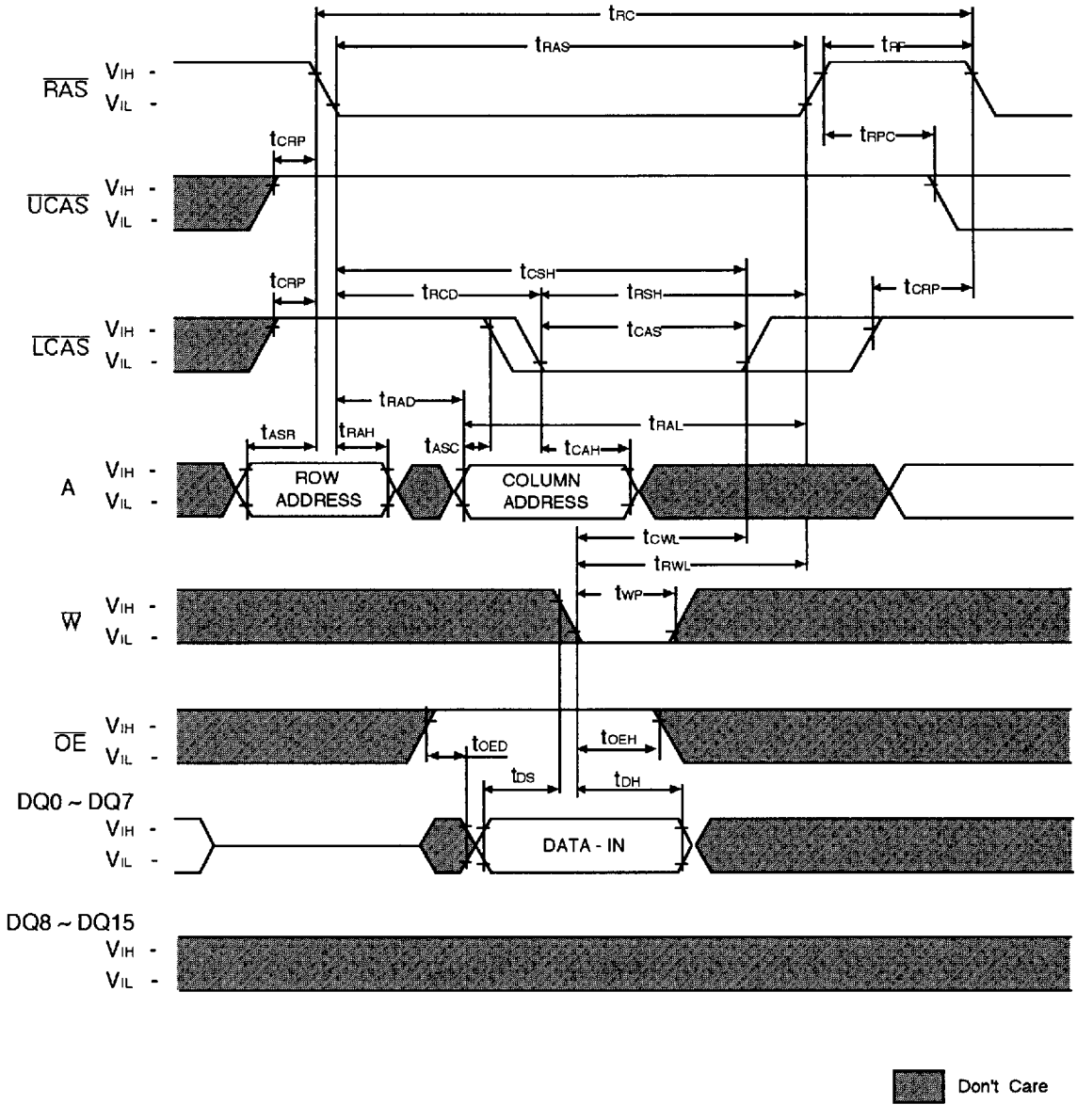
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



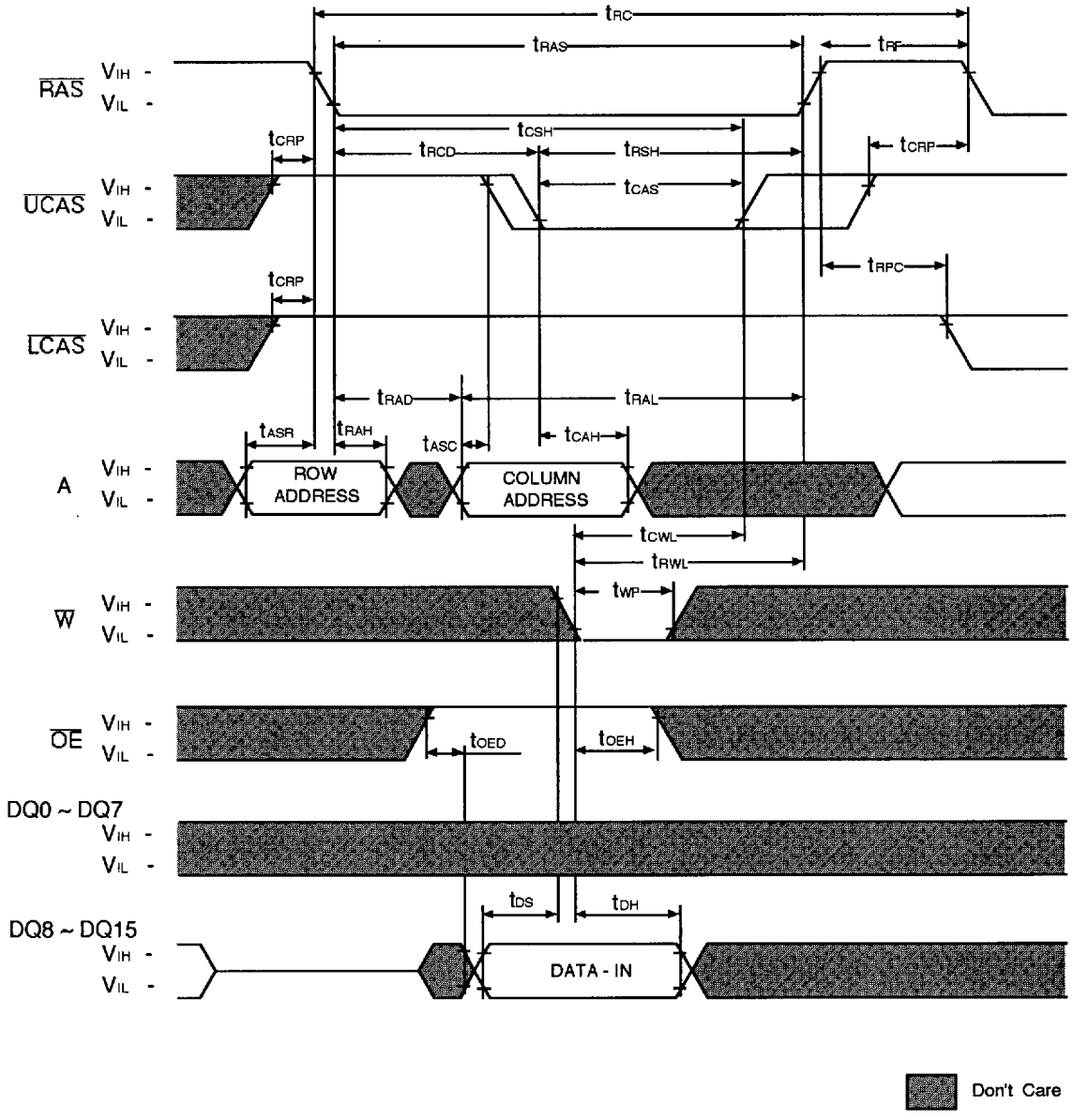
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

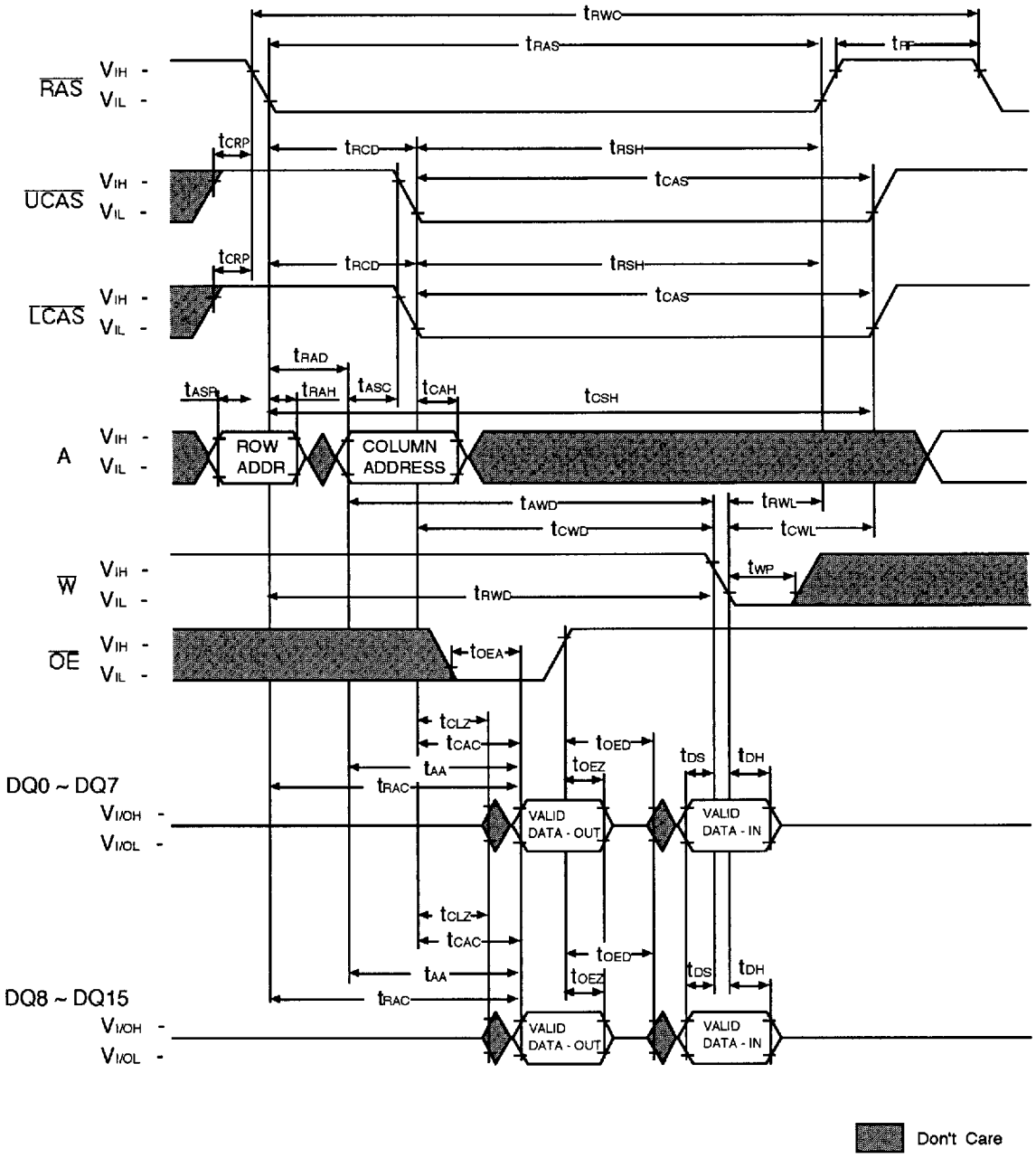


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

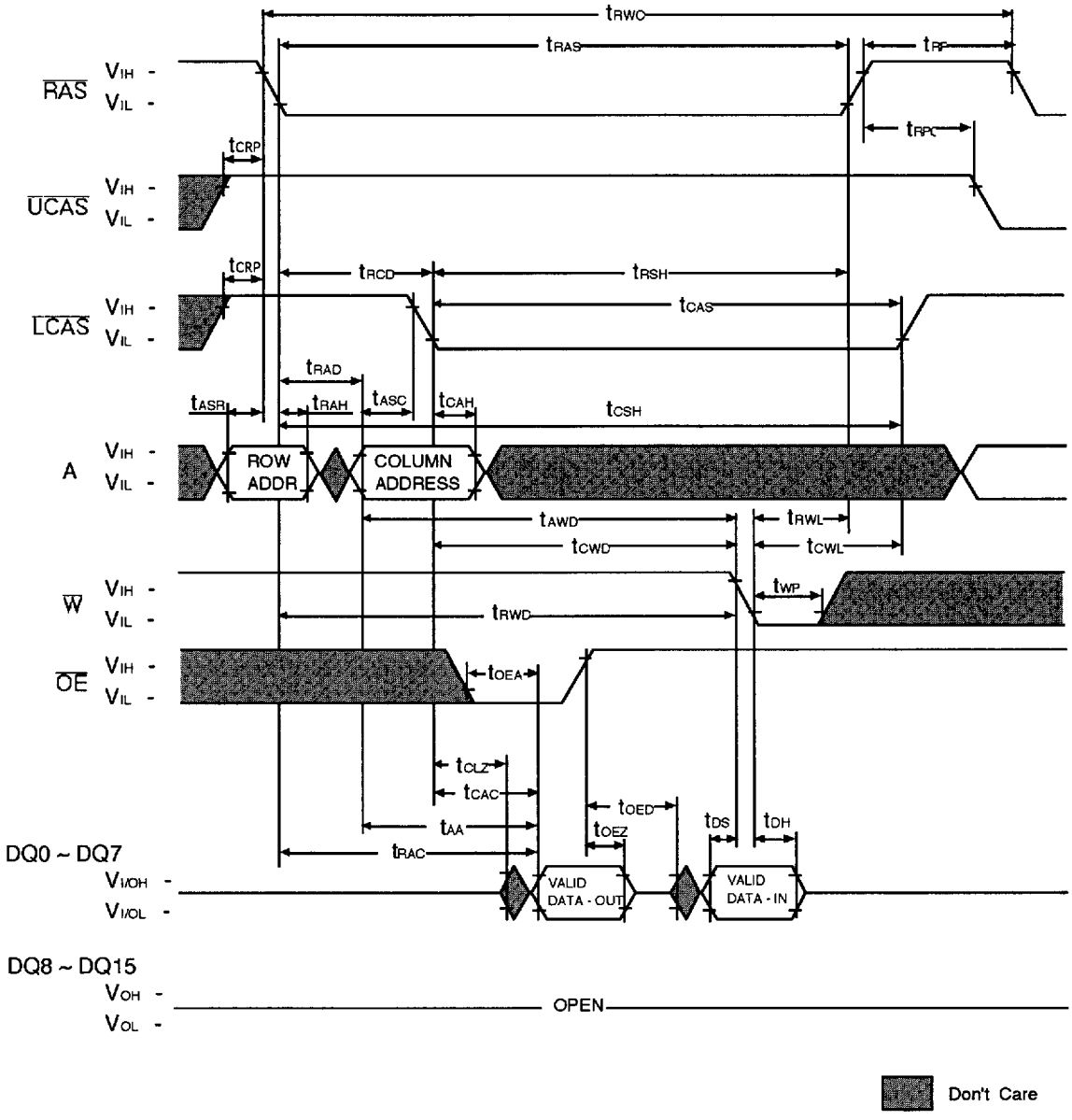
NOTE : D_{OUT} = OPEN



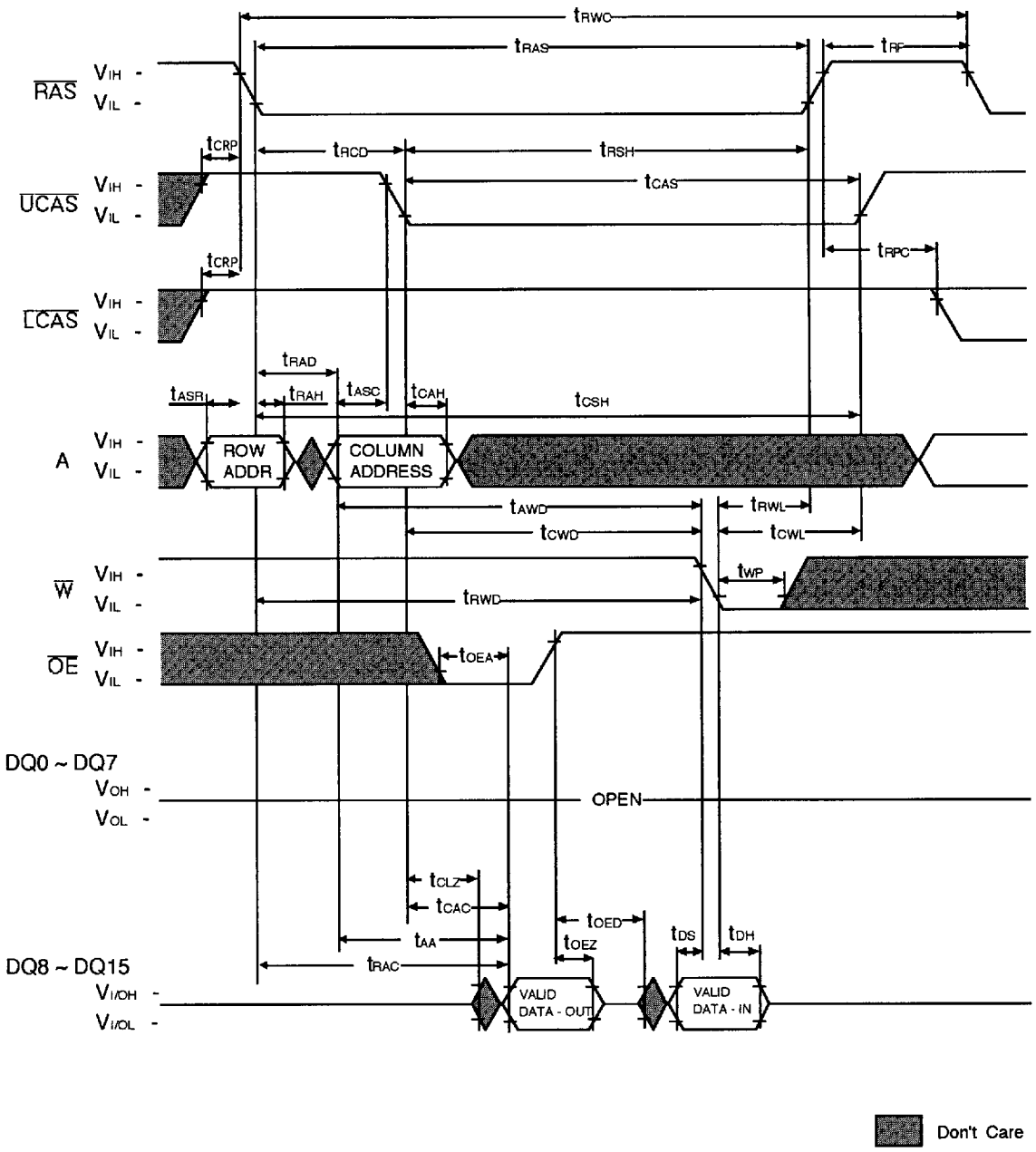
WORD READ - MODIFY - WRITE CYCLE



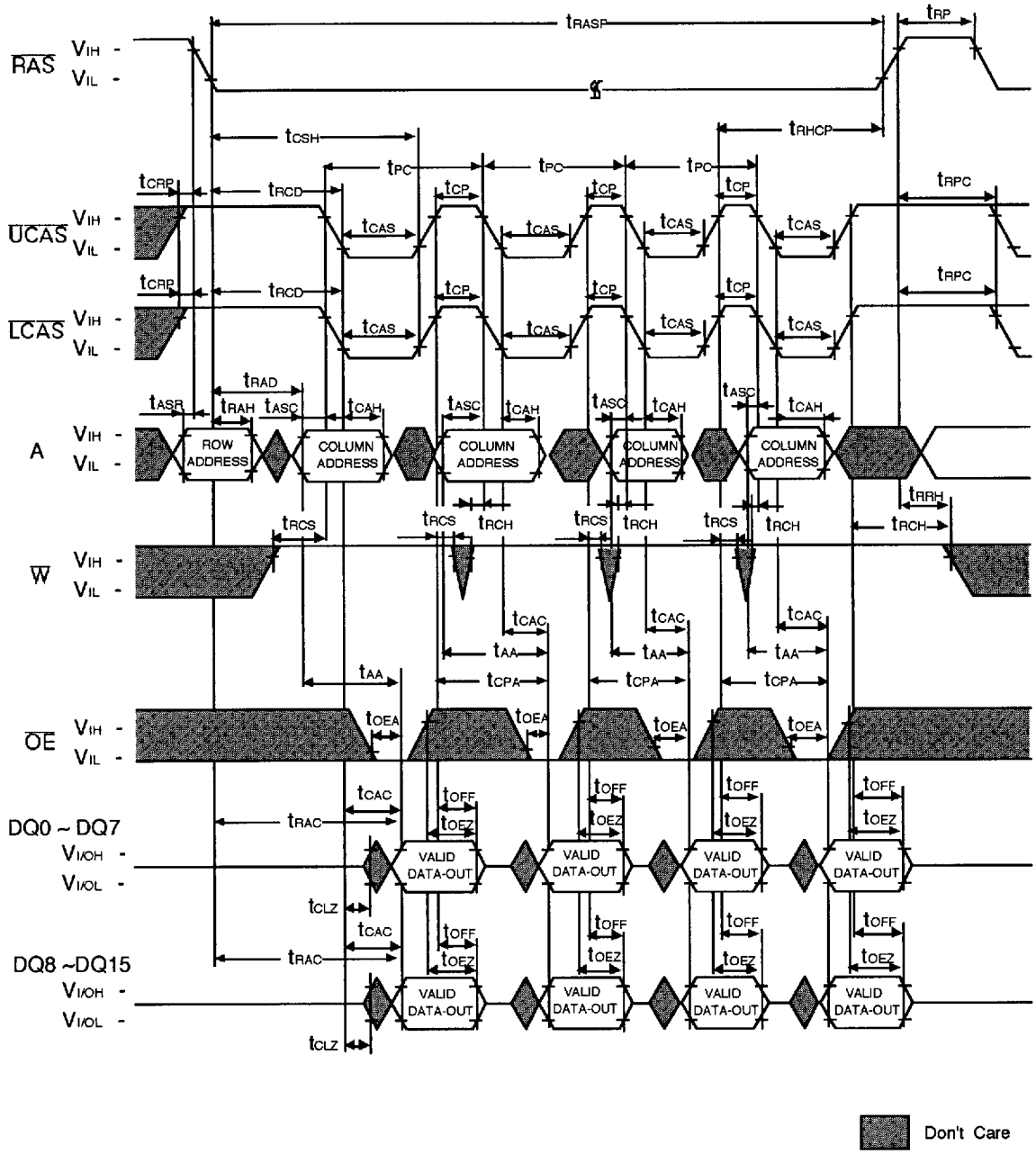
LOWER-BYTE READ - MODIFY - WRITE CYCLE



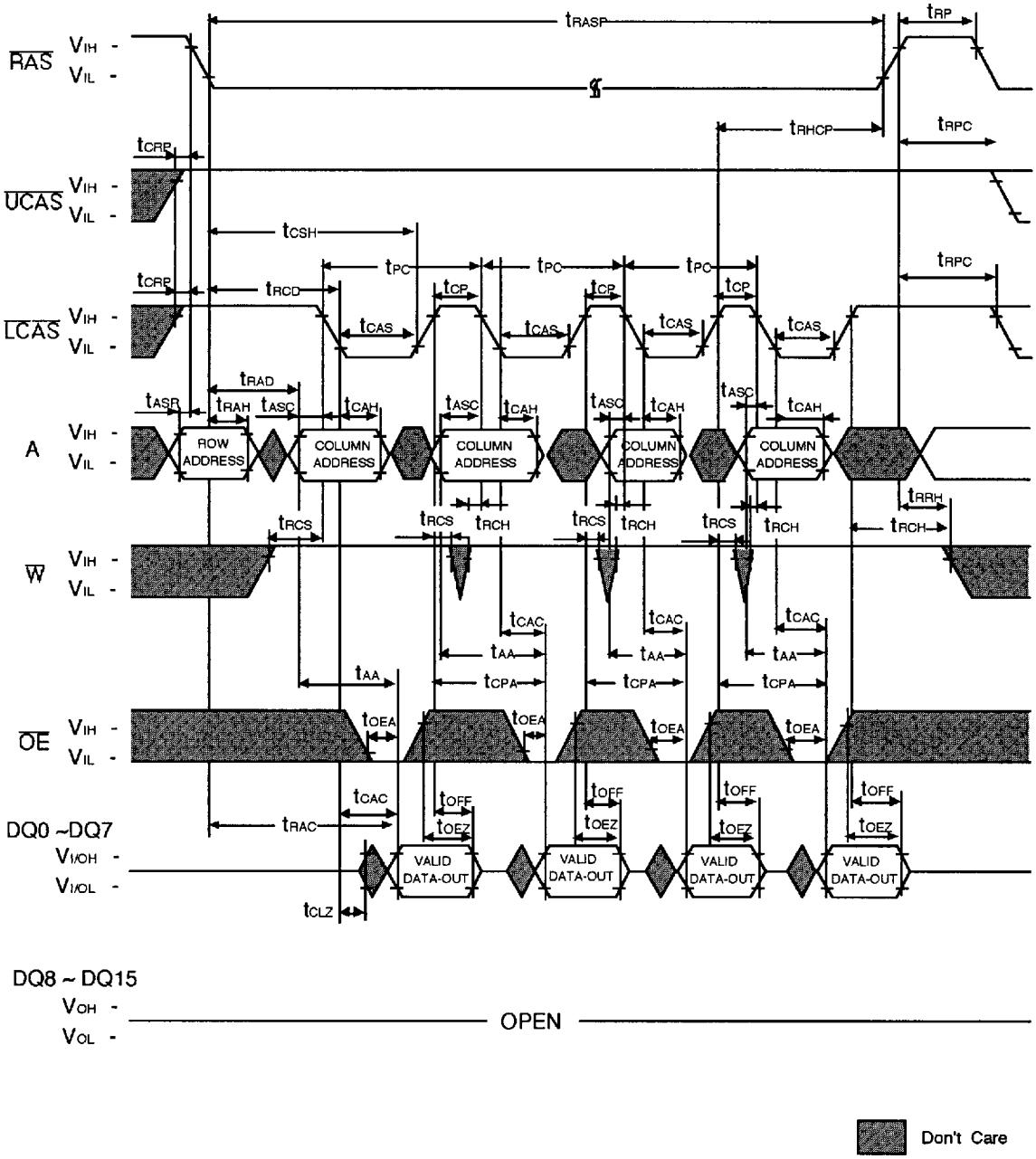
UPPER-BYTE READ - MODIFY - WRITE CYCLE



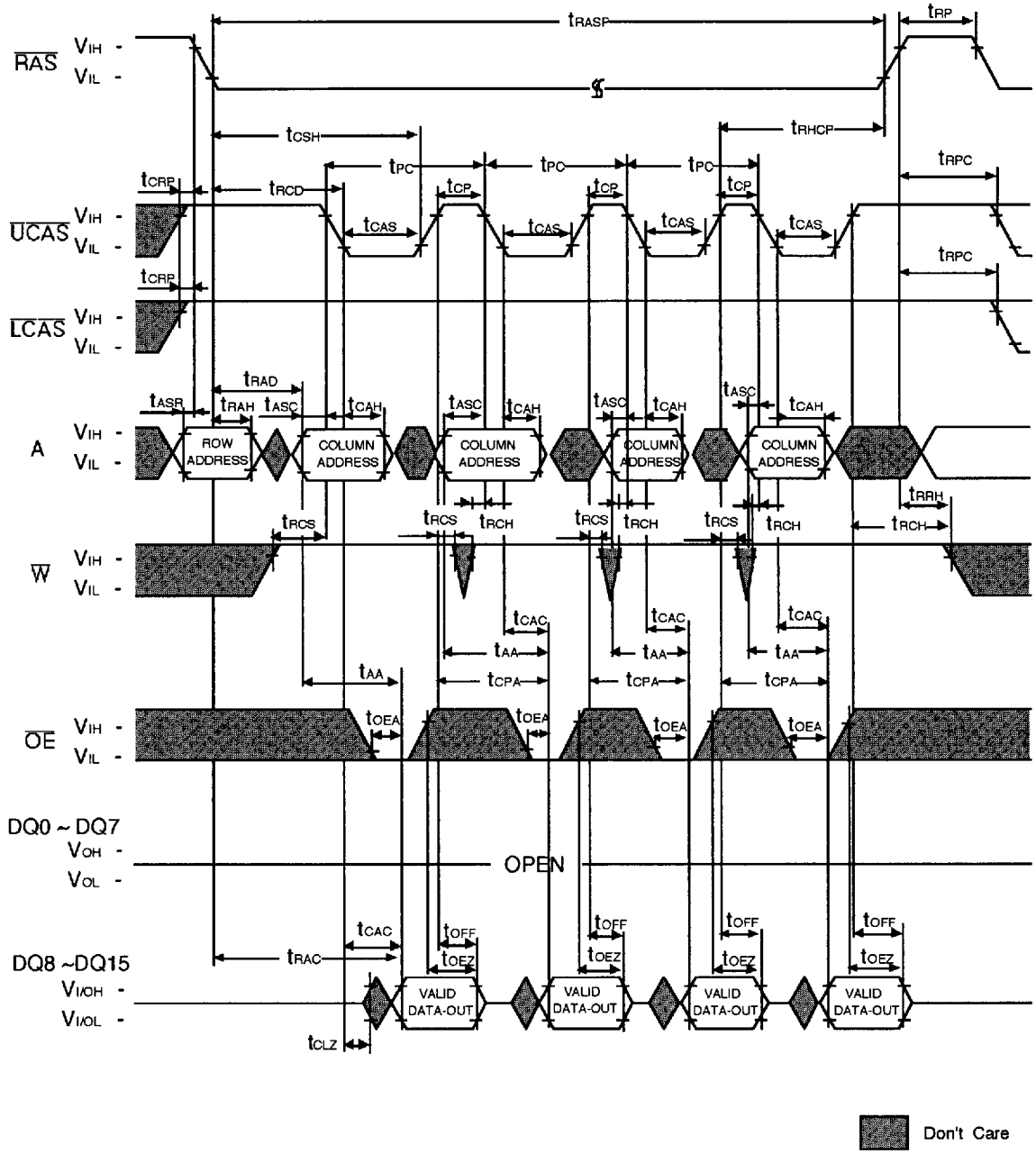
FAST PAGE MODE WORD READ CYCLE



FAST PAGE MODE LOWER BYTE READ CYCLE

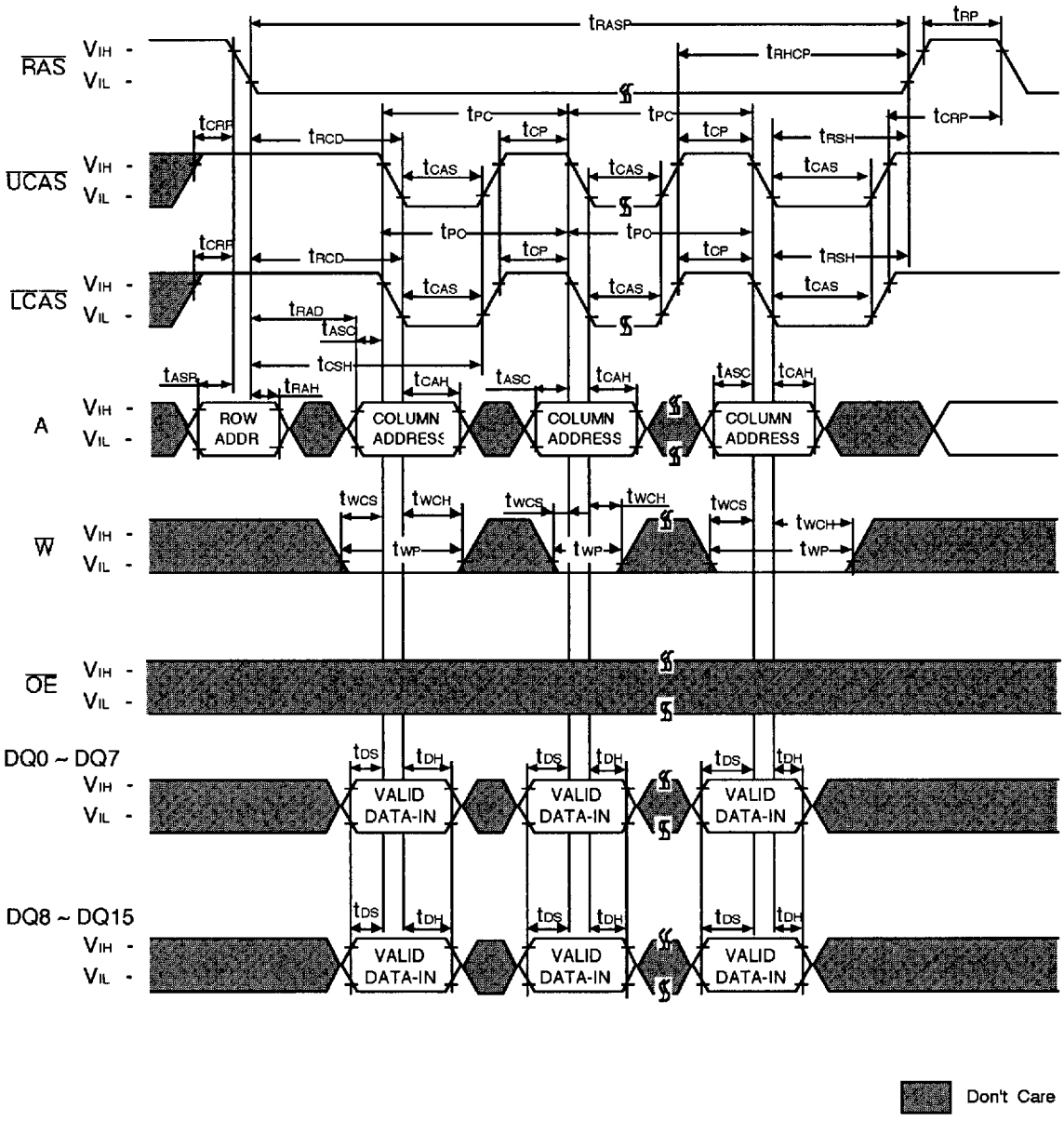


FAST PAGE MODE UPPER BYTE READ CYCLE



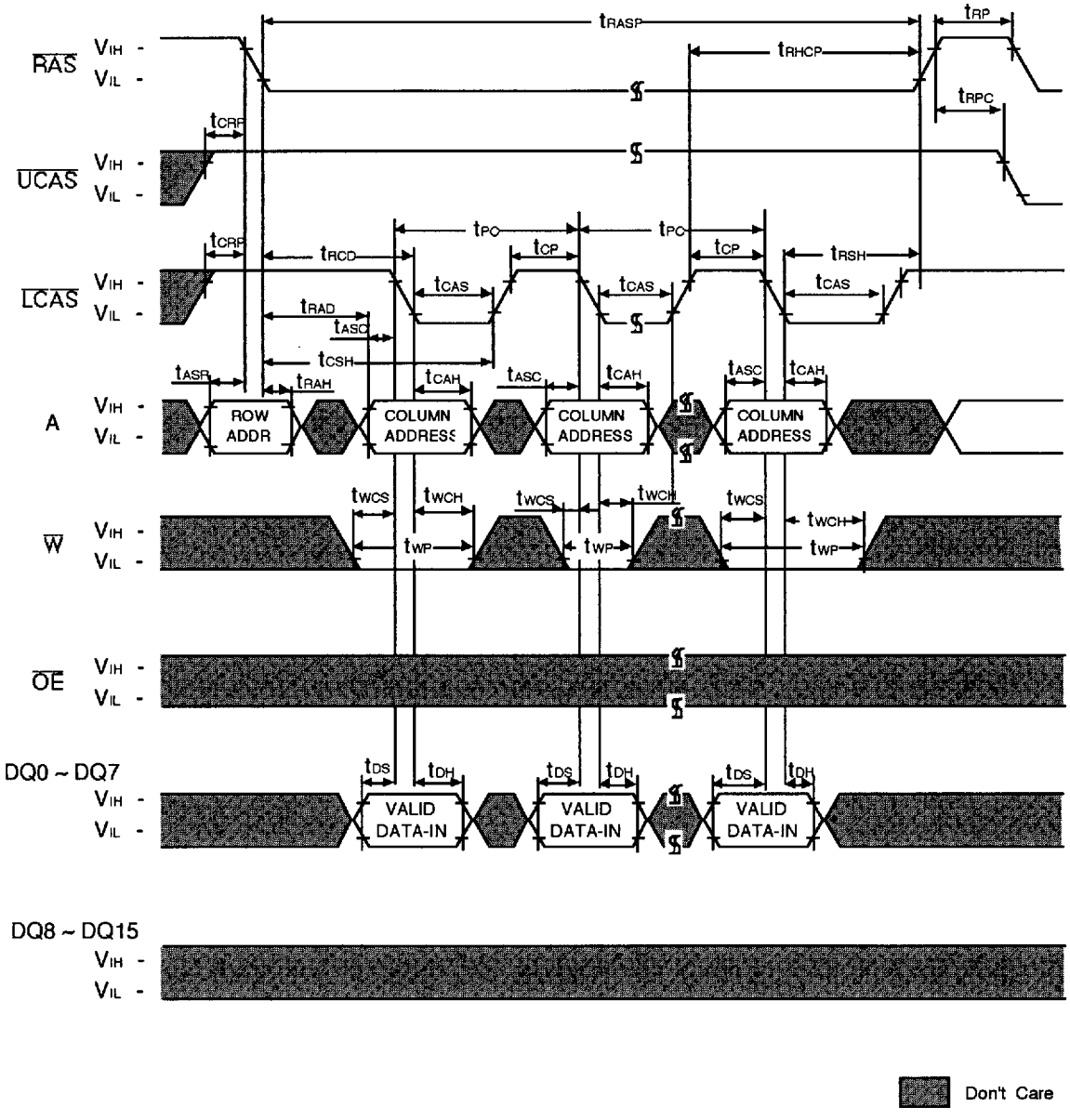
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



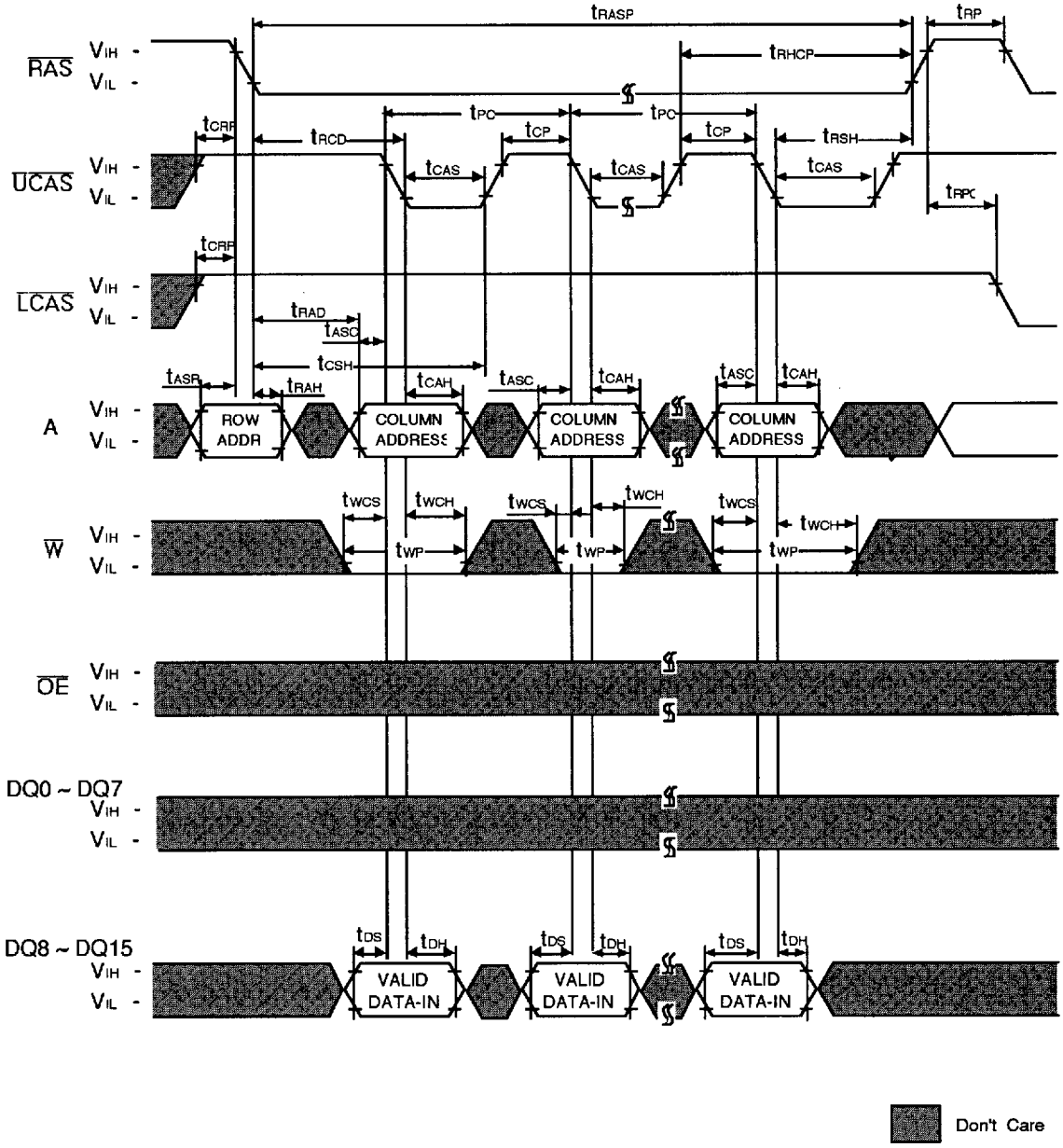
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

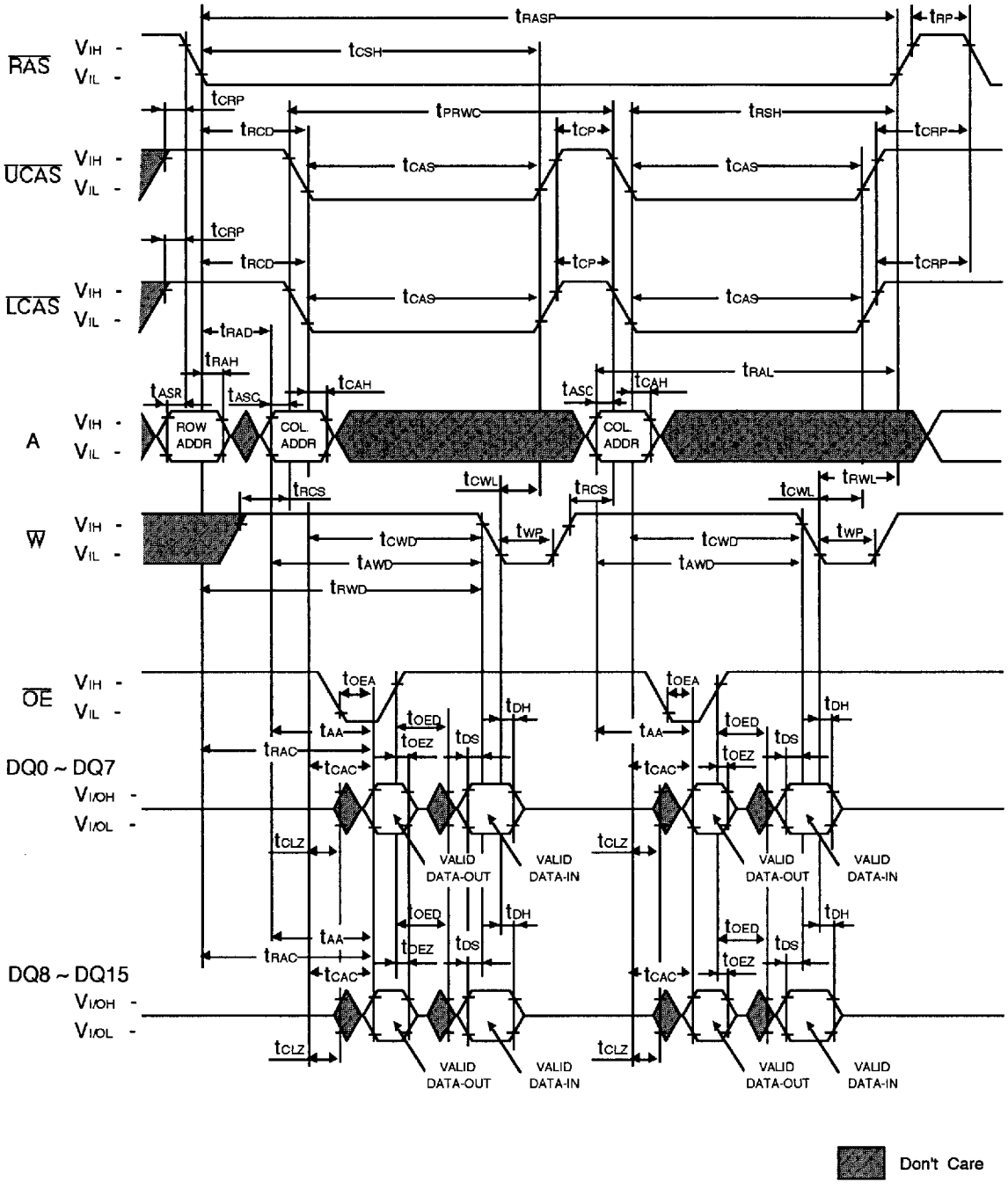


FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

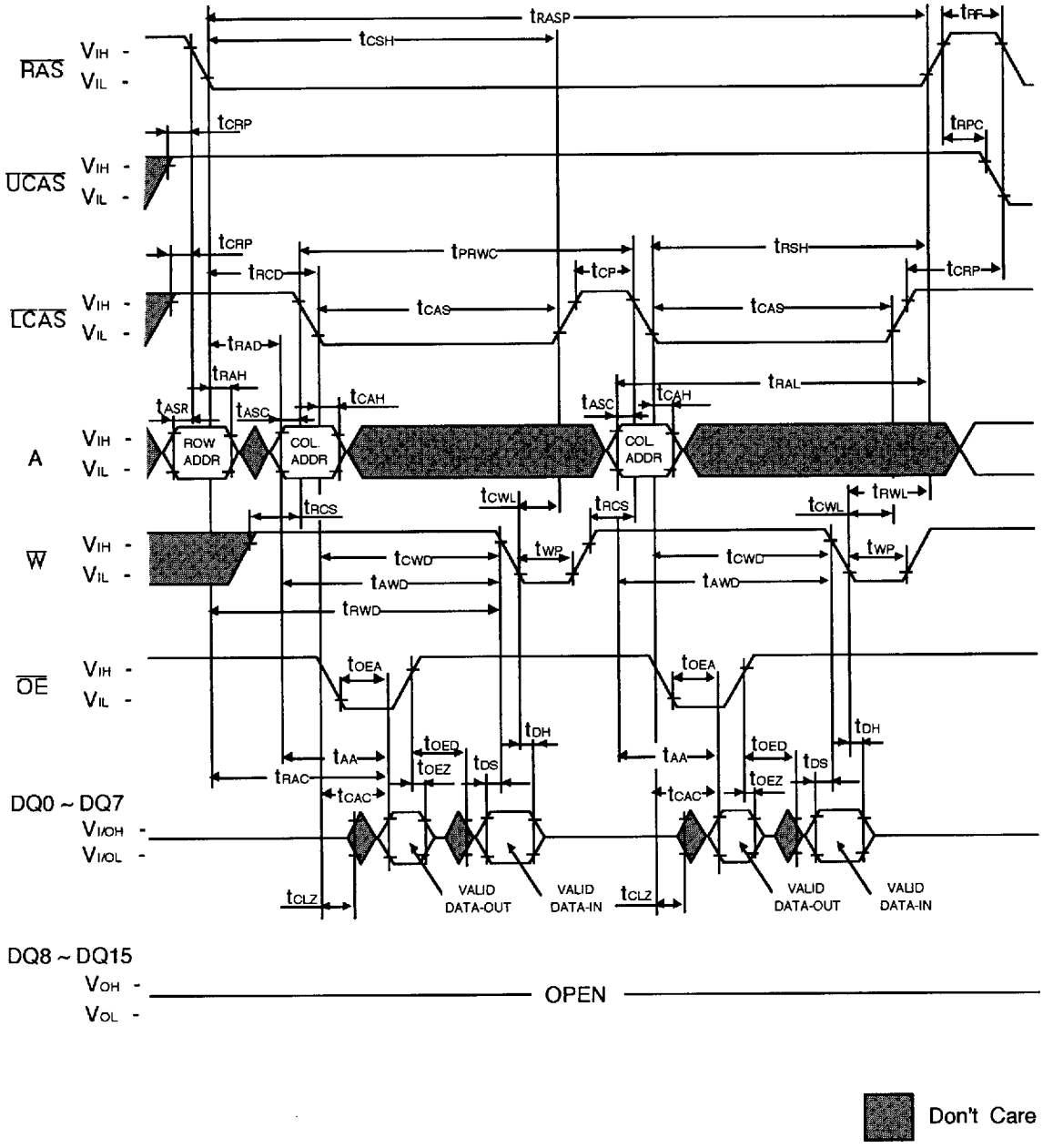
NOTE : D_{OUT} = Open



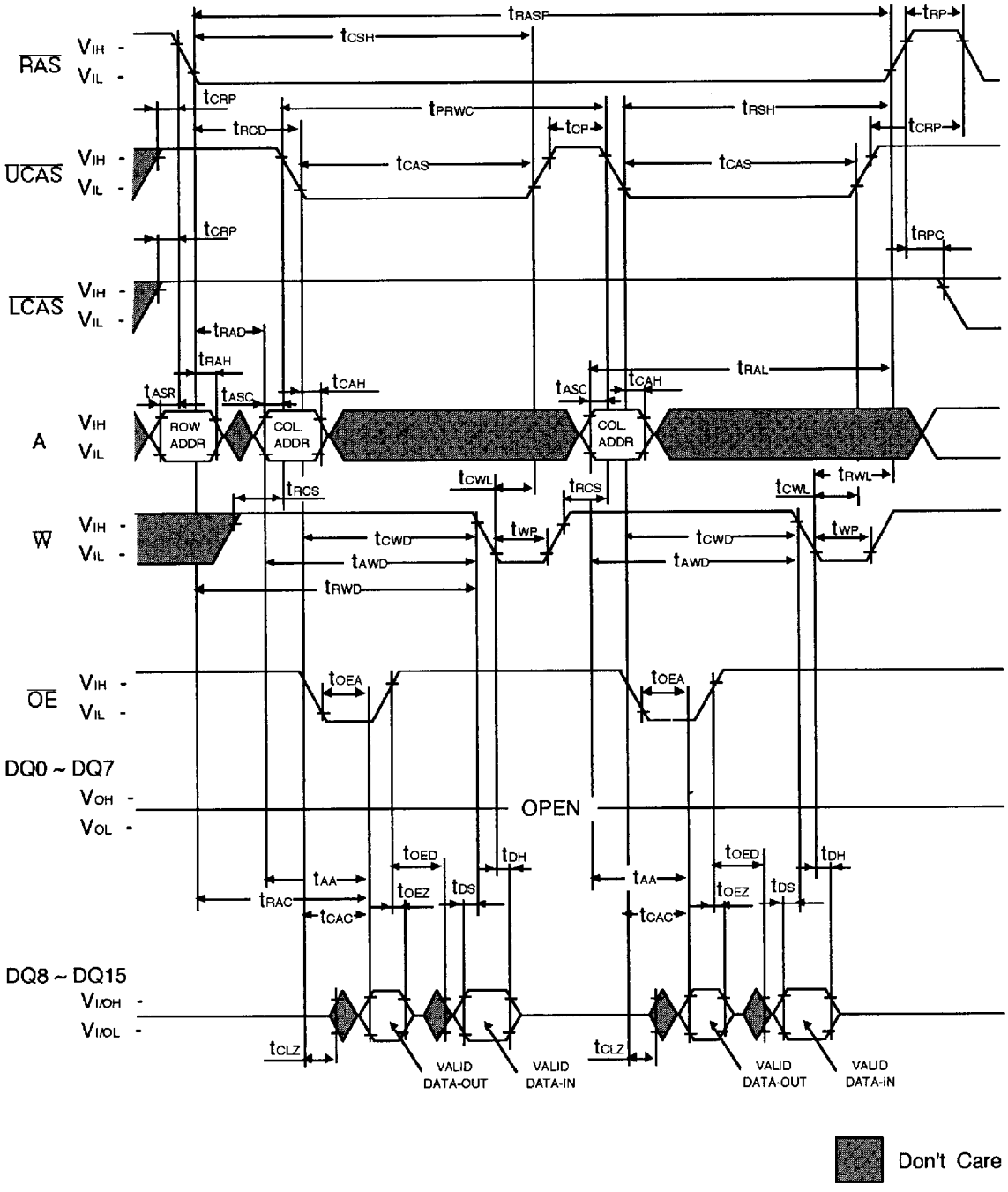
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE

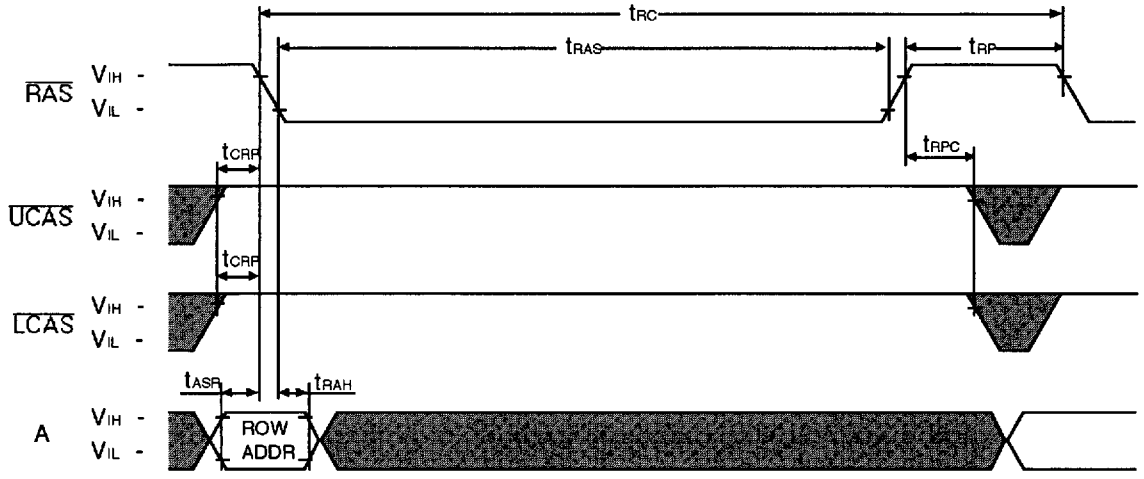


FAST PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



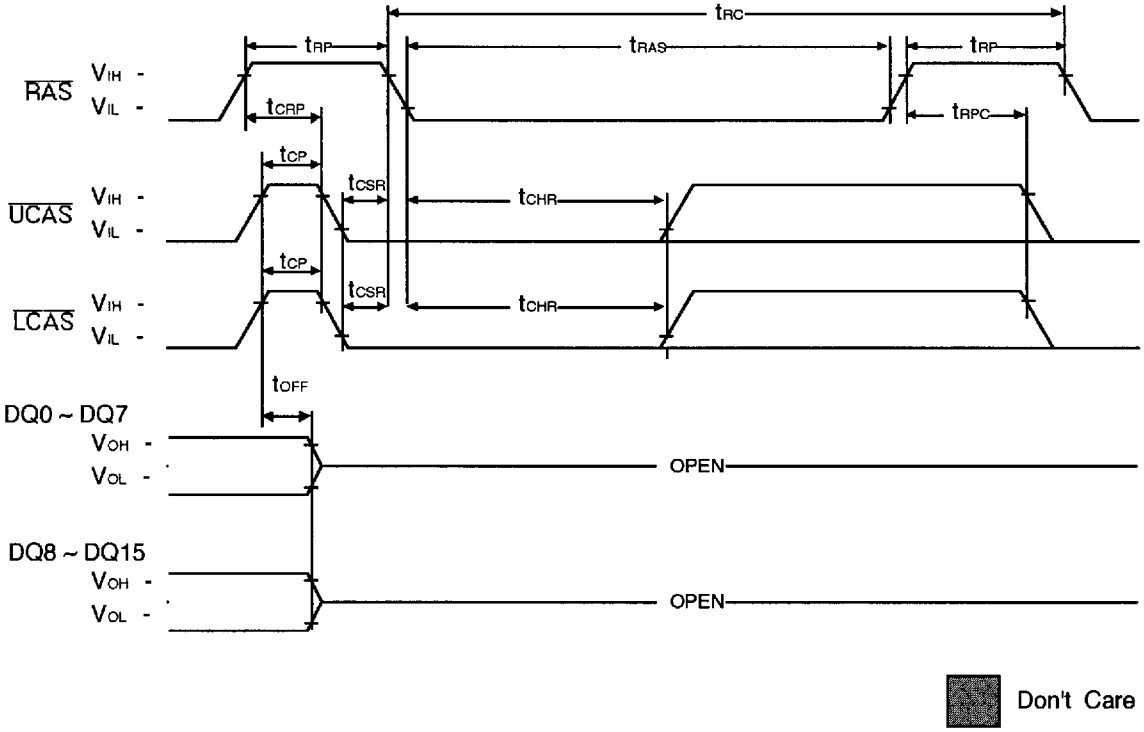
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



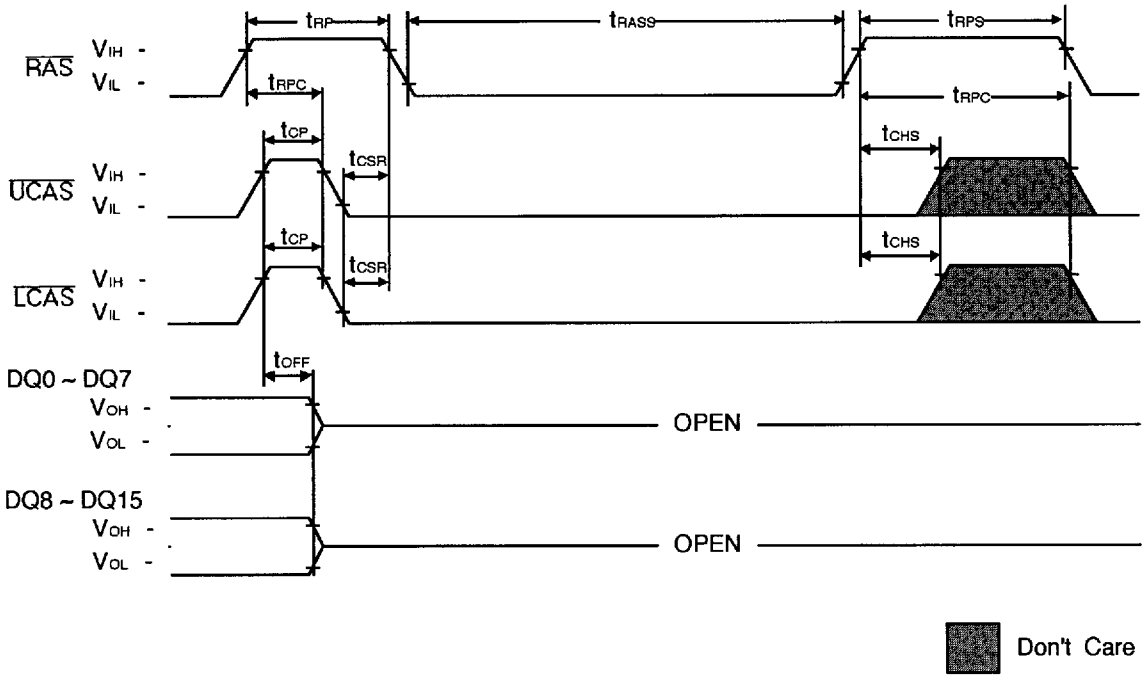
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

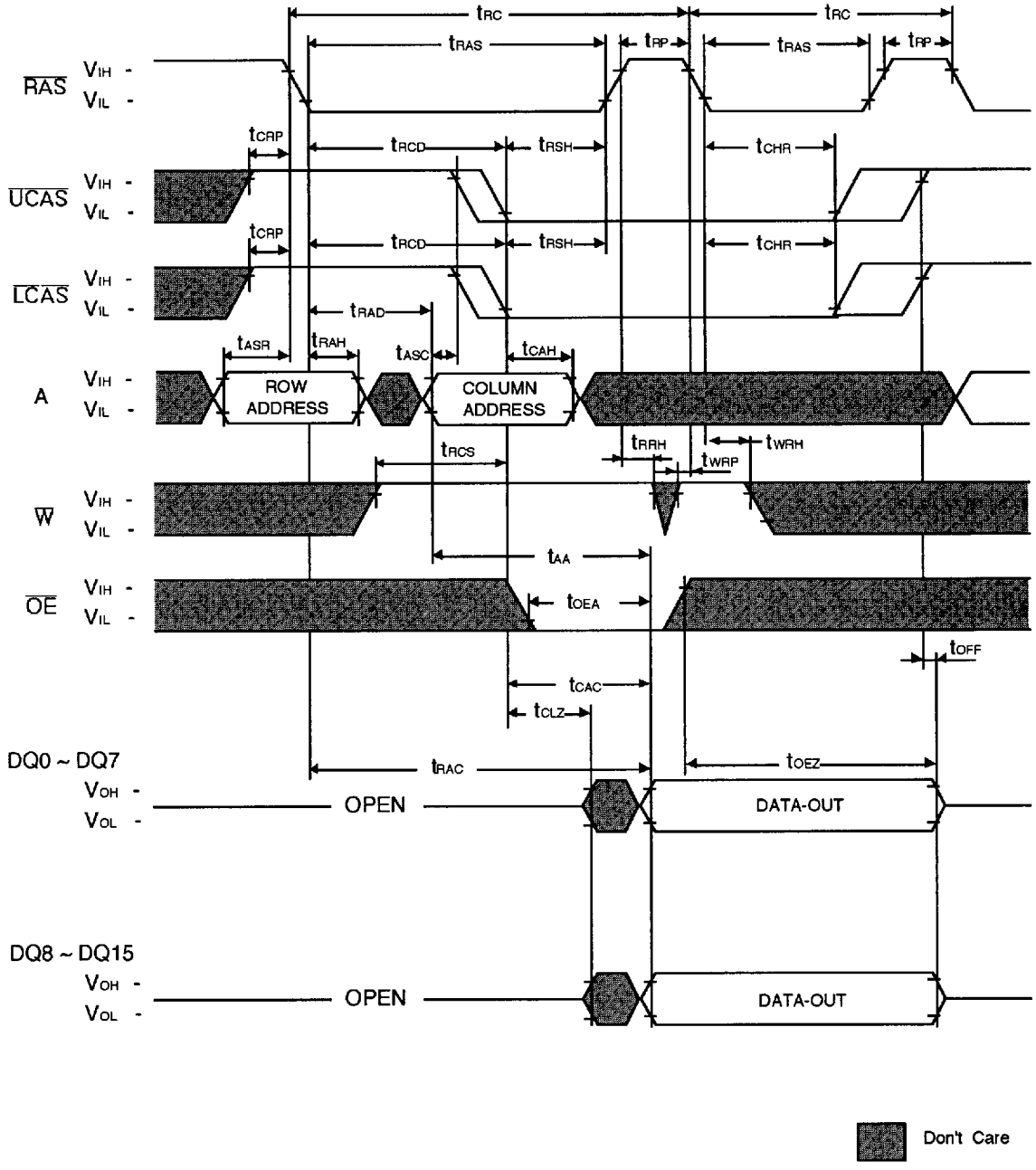


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

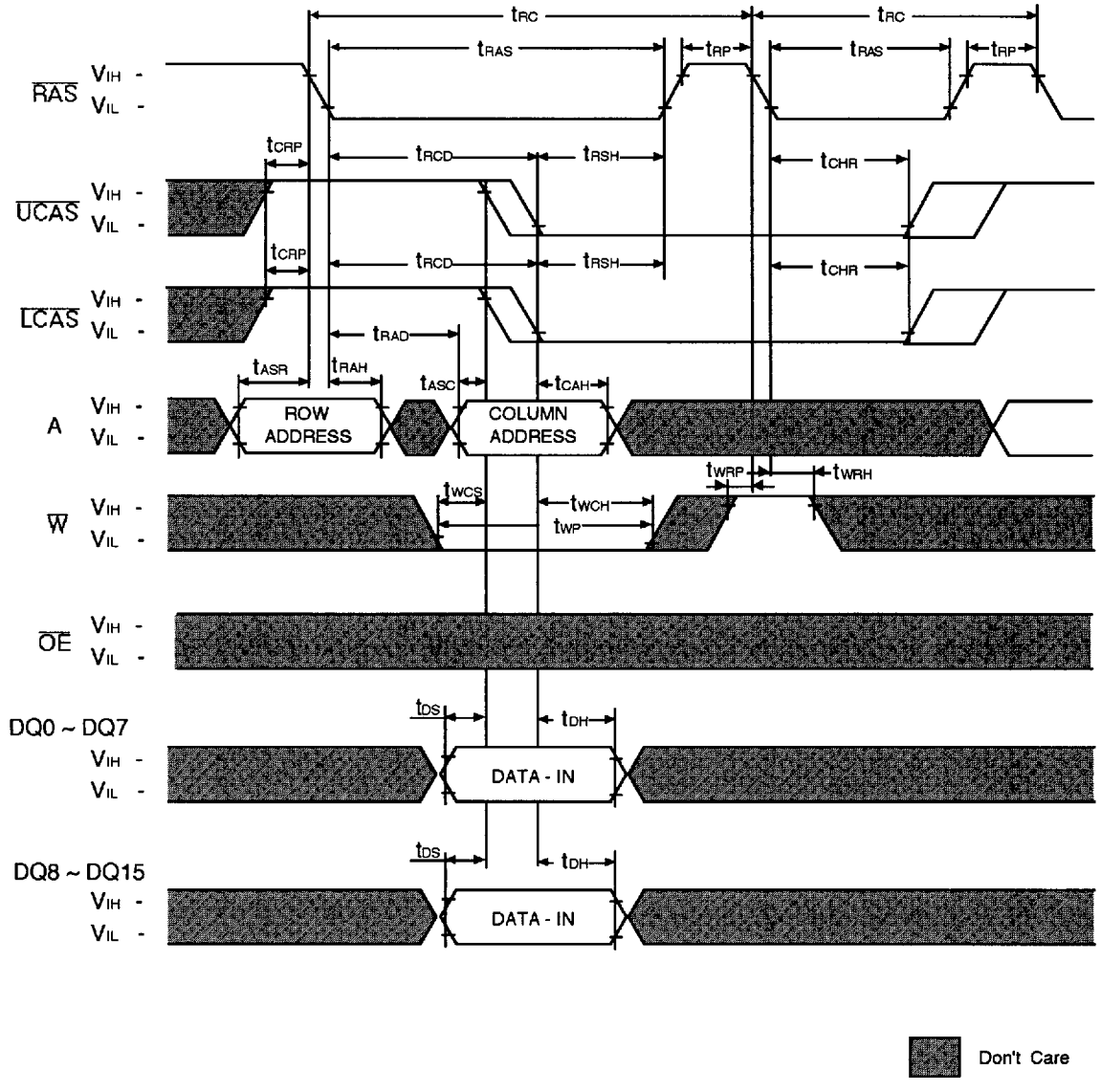


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE