NCR 53C710, 53C710-1 SCSI I/O Processor

NCR

Electrical Specifications Manual

Revision Record

Revision	Date	Affected Pages/Remarks
1.0	6/92	Electrical Specifications separated into individual manual. Updates to all timing information, addition of TolerANT Electrical Characteristics.

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Preface

This manual provides electrical characteristics and timings for the NCR 53C710 and 53C710-1. The 53C710 supports Bus Mode 1 (asynchronous) DMA timings up to 25 MHz, and Bus Mode 2 (synchronous) DMA timings up to 33 MHz. The 53C710-1 supports asynchronous timings up to 33 MHz and synchronous timings up to 40 MHz. As indicated in the body of this manual, the timing information for the 53C710-1 in Bus Mode 2 is Advance Information that may change at any time without notice. General information on functions and operations of both devices is provided in the 53C710 and 53C710-1 Data Manual.

Additional Information

NCR 53C710, 53C710-1 Data Manual
NCR 53C710 Programmer's Guide
NCR SCSI Engineering Note 829, Comparison of 53C710 to 53C700

SCSI Specifications

This data manual is not a SCSI specification. It assumes some prior knowledge of current and proposed SCSI standards. To obtain a copy of the proposed standard or background information on SCSI, write to:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900

Ask for document number: X3.131 – 1986 (SCSI-1)

Global Engineering Documents
2805 McGaw
Irvine, CA 92714
(800) 854-7179 or (714) 261-1455

Ask for document number:
X3.131-199x (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, California 95070
(408) 867-6642

Document Name:
SCSI Bench Reference

Prentice Hall
Englewood Cliffs, New Jersey 07632
(201) 767-5937

Ask for document number: ISBN 0-13-796855-8

Document Name: SCSI - Understanding the Small Computer System Interface

NCR SCSI Electronic Bulletin Board
(719) 574-0424

Table of Contents

DC Specifications

Absolute Maximum Stress Ratings

Parameter	Symbol	Min	Max	Units
Storage temperature	T_{STG}	-55	150	°C
Supply voltage	V_{DD}	-0.5	7.0	V
Input voltage	V_{IN}	V_{SS} - 0.5	V_{DD} + 0.5	V
Latch-up current	I_{LU}	$-2V < V_{PIN} < +8V$	±150	mA
Electrostatic discharge	ESD*	-	2K	V

** SCSI pins only. Test using the human body model, 100 pF at 1.5 K ohms*

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the *Operating Conditions* section of this specification is not implied.

Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}	4.75	5.25	V
Supply current (Static)	I_{DD}	-	1	mA
Supply current (Dynamic) - 53C710	I_{DD}	-	50	mA
- 53C710-1			60	
Operating temperature (free-air)	T_A	0	70	°C
Thermal resistance*				
(junction to ambient air)	θ_{JA}	-	46	°C/W
Power Dissipation	P_{DD}	-	0.26	W

**160-pin, QFP only.*

SCSI Signals – SD(7-0), SDP/, REQ/, MSG/, I_O/, C_D/, ATN/, ACK/, BSY/, SEL/, RST/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	I_{OL} = 48 mA
Hysteresis	V_{HYS}	300	-	mV	-
Input leakage current	I_{IN}	-10	10	µA	-
Input leakage – SCSI RST	I_{NR}	-200	50	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

Input Signals – BG/, BOFF/, RESET/, CS/, BS, BIG-LIT/, BCLK, SCLK

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} – 0.5	0.8	V	-
Input leakage current	I_{IN}	– 1.0	1.0	µA	-

Output Signals – SDIR(7-0), SDIRP, BSYDIR, SELDIR, RSTDIR, TGS, IGS

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = – 4 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 4 mA
Output high current	I_{OH}	– 2.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	4.0	-	mA	V_{OL} = 0.4 V

Output Signals – FETCH/, IRQ/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = – 8 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 8 mA
Output high current	I_{OH}	– 4.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	8.0	-	mA	V_{OL} = 0.4 V

Output Signals – SLACK/, MASTER/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = – 16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16 mA
Output high current	I_{OH}	– 8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V

Tristate Output Signals –A(31-6), FC(2-0), SC(1-0), UPSO-TT0/, CBREQ/-TT1/, BR/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V
Tristate leakage current	I_{OZ}	-10	10	µA	-

Bidirectional Signals – A(5-0), D(31-0), DP(3-0), DS/-DLE, AS/-TS/, RW/, SIZ(1-0), BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2	$V_{DD} + 0.5$	V	-
Input low voltage	V_{IL}	$V_{SS} - 0.5$	0.8	V	-
Output high voltage	V_{OH}	2.4	V_{DD}	V	$I_{OH} = -16$ mA
Output low voltage	V_{OL}	V_{SS}	0.5	V	$I_{OL} = 16$ mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD} - 0.5$ V
Output low current	I_{OL}	16.0	-	mA	$V_{OL} = 0.4$ V
Input leakage current	I_{IN}	-10	10	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

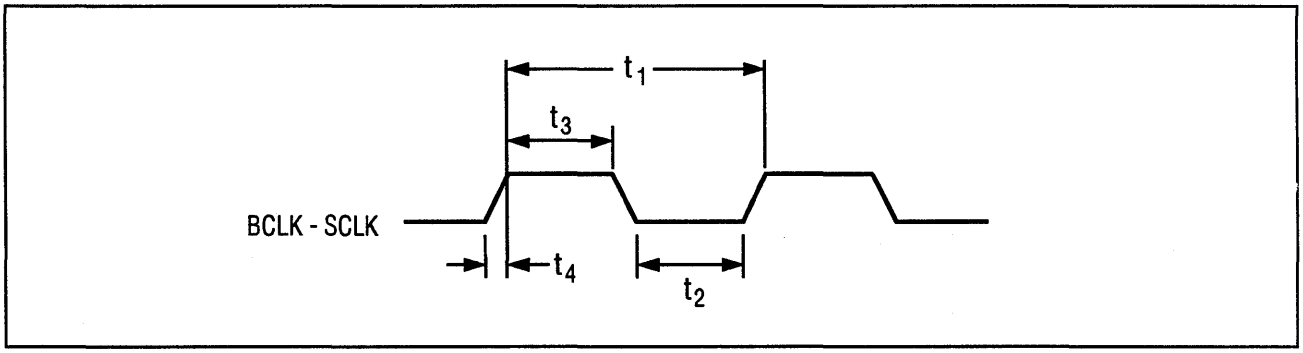
Capacitance

Parameter	Symbol	Min	Max	Units	Conditions
Input capacitance of input pads	C_I	-	7	pF	-
Input capacitance of I/O pads	C_{IO}	-	10	pF	-

AC Characteristics

The AC characteristics described in this section apply over the operating voltage and temperature range, $4.75 \geq V_{DD} \geq 5.25V$ and $0°C \geq T_A \leq 70°C$. Output timings are based on worst case conditions (4.75 V, 70°) and worst case processing using the following termination: the simulation load of the I/O pads is 120 pF; all timings in the specification are taken from the 10 % and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Figure 6-1. Clock Timing



53C710 Bus Mode 1 Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (t_{BCLK})	t_1	40	DC	ns
SCSI clock cycle time (t_{SCLK})*		15	60	ns
BCLK low time**	t_2	17	-	ns
SCLK low time**		7	-	ns
BCLK high time**	t_3	17	-	ns
SCLK high time**		7	-	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

53C710 Bus Mode 2 Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (t_{BCLK})	t_1	30	DC	ns
SCSI clock cycle time (t_{SCLK})*		15	60	ns
BCLK low time**	t_2	14	-	ns
SCLK low time**		7	-	ns
BCLK high time**	t_3	14	-	ns
SCLK high time**		7	-	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

53C710-1 Bus Mode 1 Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (t_{BCLK})	t_1	30	DC	ns
SCSI clock cycle time (t_{SCLK})*		15	60	ns
BCLK low time**	t_2	13	-	ns
SCLK low time**		7	-	ns
BCLK high time**	t_3	13	-	ns
SCLK high time**		7	-	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

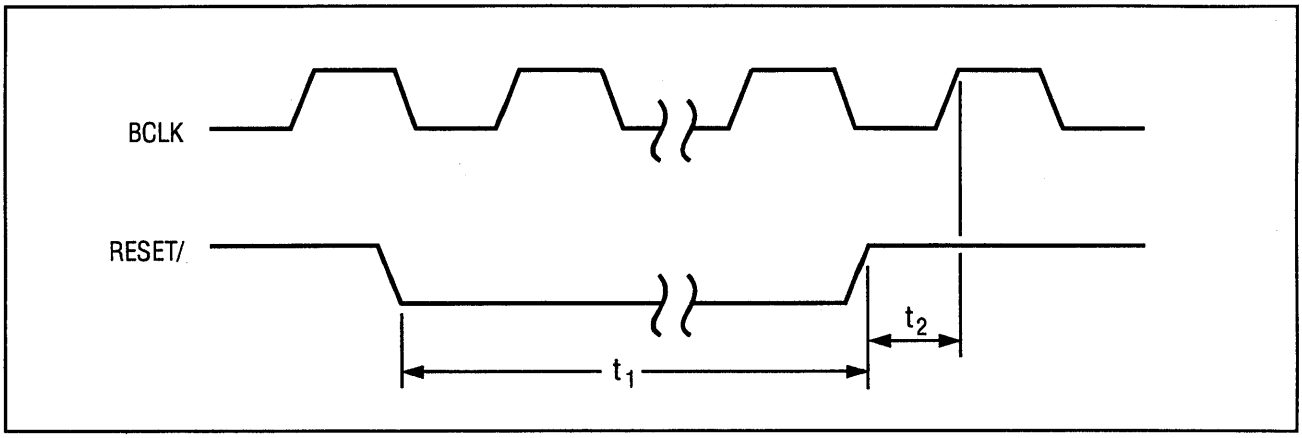
53C710-1 Bus Mode 2 Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (t_{BCLK})	t_1	25	DC	ns
SCSI clock cycle time (t_{SCLK})*		15	60	ns
BCLK low time**	t_2	11	-	ns
SCLK low time**		7	-	ns
BCLK high time**	t_3	11	-	ns
SCLK high time**		7	-	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

** This parameter must be met to insure SCSI timings are within specification.*

*** Duty cycle not to exceed 60/40.*

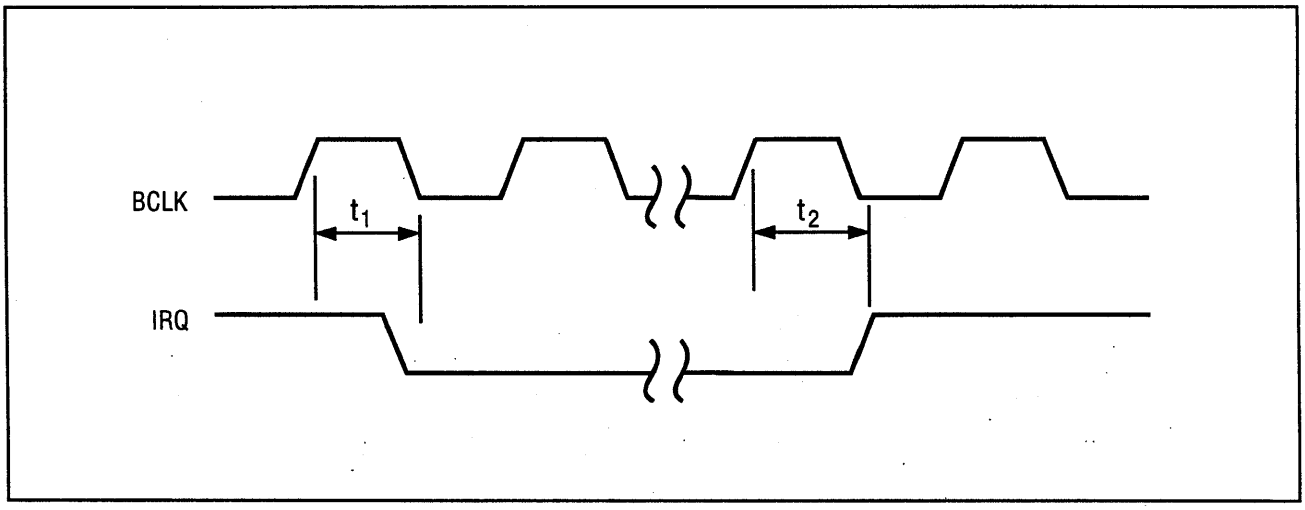
Figure 6-2. Chip Reset Timing



Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	t_{BCLK}
Reset deasserted setup to BCLK high	t_2	10	-	ns

***Note:** This timing is only required to ensure clock-for-clock repeatability after RESET/ is deasserted.*

Figure 6-3. IRQ Timing



Parameter	Symbol	Min	Max	Units
BCLK high to IRQ low	t_1	-	20	ns
BCLK high to IRQ high	t_2	-	58	ns
BCLK high to IRQ low	t_3	3	-	ns

Bus Mode 1 Slave Cycle

Bus Mode 1 Slave Read Sequence

1) The Read/Write, Address and Size lines are asserted by the CPU.
2) Address Strobe is asserted by the CPU.
3) Chip Select is validated by the 53C710 on any following rising edge of BCLK.
4) Cache Burst Acknowledge is deasserted by the 53C710.
5) Three clock cycles of wait state are inserted and the Data lines are asserted by the 53C710.
6) Slave Acknowledge is asserted by the 53C710 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7) Synchronous cycle termination is asserted by memory.
8) Address Strobe is deasserted by the CPU.
9) Slave Acknowledge or Bus Error is deasserted by the 53C710, and the Data lines are tristated by the 53C710.

53C710 Bus Mode 1 Slave Read Timings

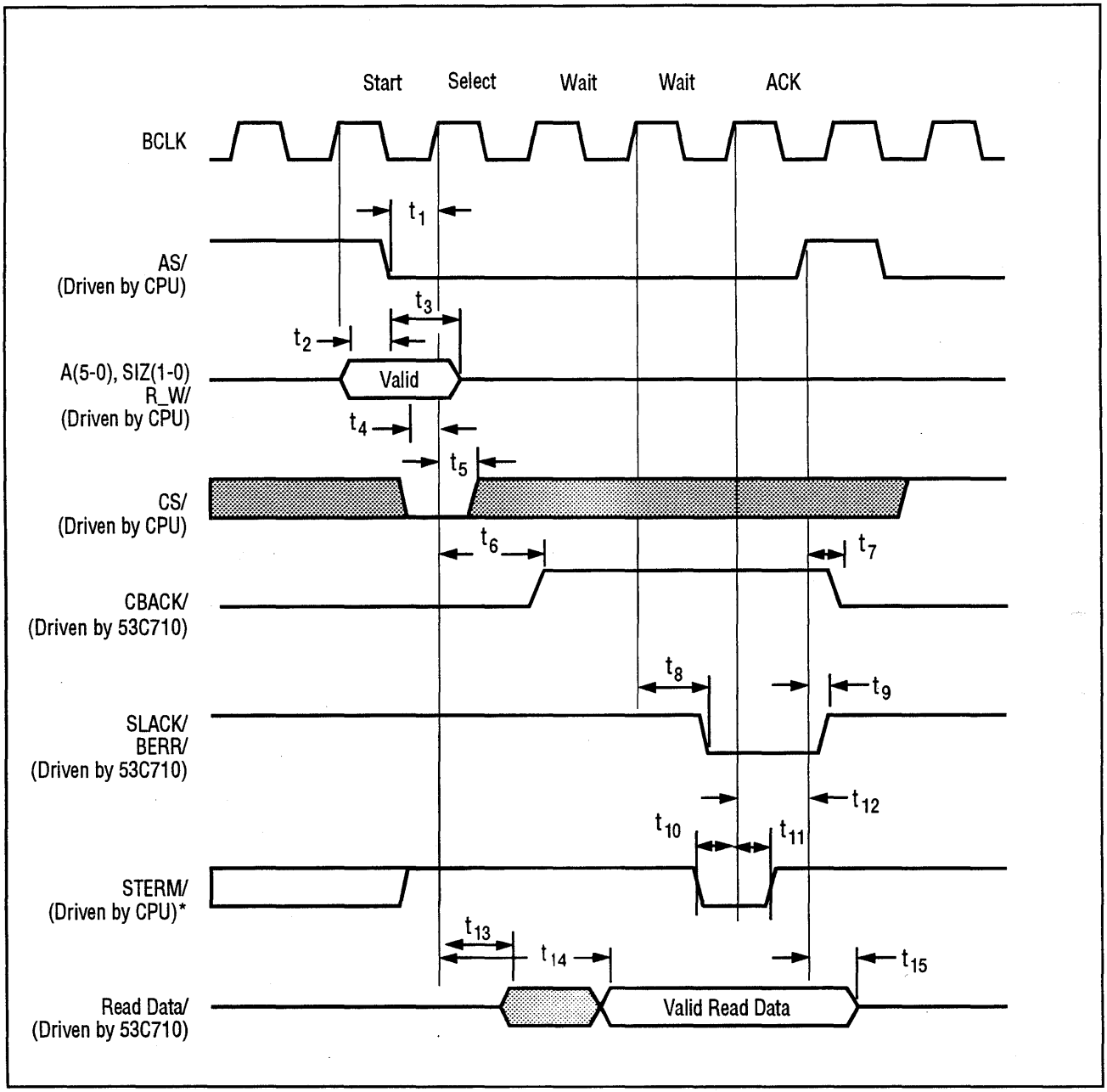
Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(5-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(5-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	26	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ (input) setup to BCLK high	t_{10}	3	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
STERM/ clocked active to AS/ high	t_{12}	-	1	clk
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
AS/ high to data bus hi-Z	t_{13}	7	28	ns

53C710-1 Bus Mode 1 Slave Read Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(5-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(5-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	20	ns
AS/ high to CBACK/ low	t_7	3	15	ns
BCLK high to SLACK/, BERR/ low	t_8	-	20	ns
AS/ high to SLACK/, BERR/ high	t_9	-	20	ns
STERM/ (input) setup to BCLK high	t_{10}	2	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
STERM/ clocked active to AS/ high	t_{12}	-	1	clk
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	60	ns
AS/ high to data bus hi-Z	t_{13}	7	28	ns

Note: The 53C710 must see address strobes paired up with synchronous cycle terminations, even though the slave cycle may not be intended for the 53C710.

Figure 6-4. Bus Mode 1 Slave Read Cycle



Note: Shaded area indicates that the signal is a don't care.

* This signal may be driven by the 53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 of the Data Manual for use of this signal as an output.

Bus Mode 1 Slave Write Sequence

1) The Read/Write, Address and Size lines are asserted by the CPU.
2) Address Strobe is asserted by the CPU.
3) Chip Select is validated by the 53C710 on any following rising edge of BCLK.
4) Cache Burst Acknowledge is deasserted by the 53C710.
5) The Data lines are asserted by the CPU.
6) Slave Acknowledge is asserted by the 53C710 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7) Synchronous cycle termination is asserted by the CPU.
8) Address Strobe is deasserted by the CPU.
9) Slave Acknowledge or Bus Error is deasserted by the 53C710 .

53C710 Bus Mode 1 Slave Write Timings

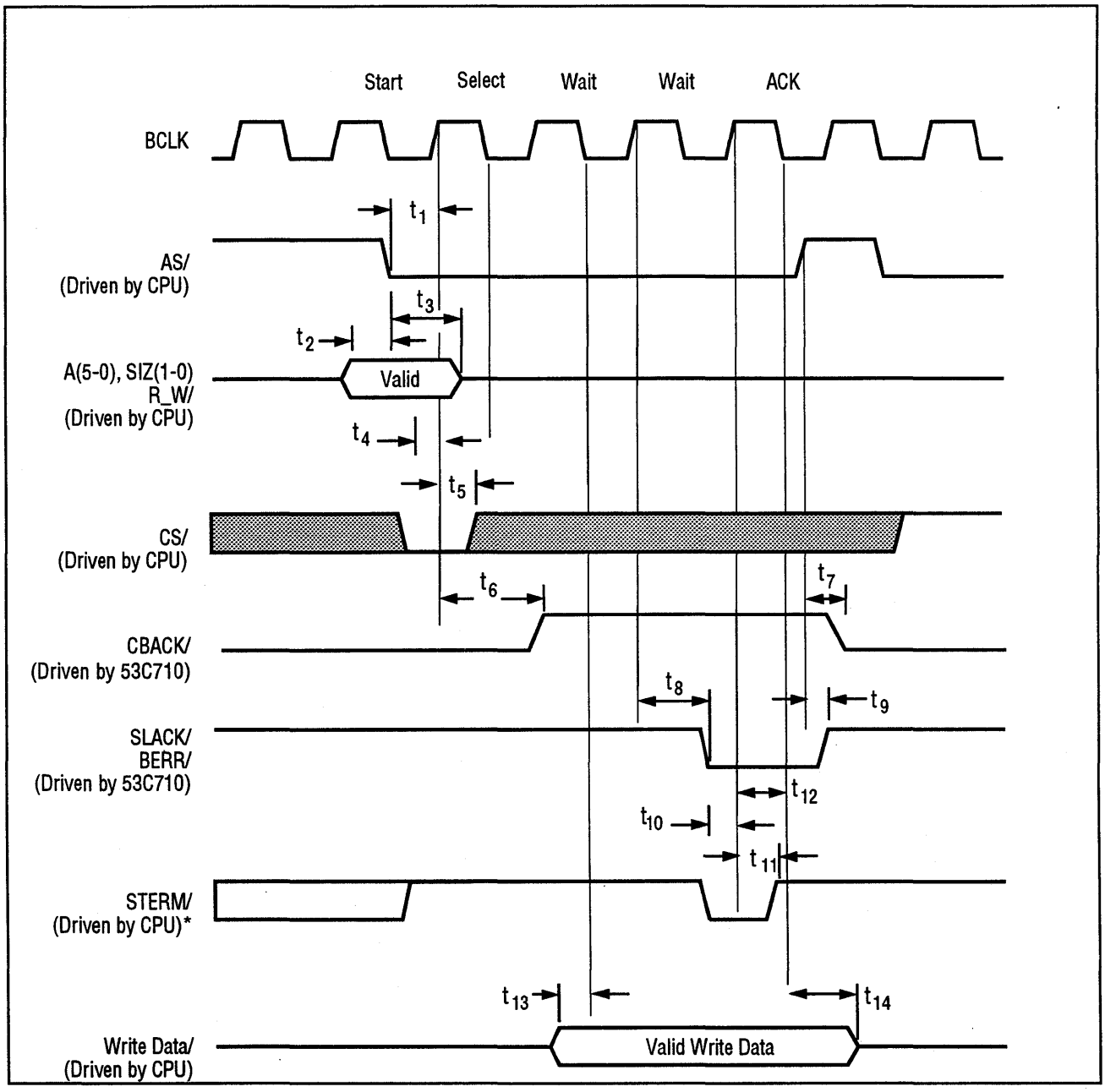
Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(5-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(5-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	26	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ (input) setup to BCLK high	t_{10}	3	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
STERM/ clocked active to AS/ high	t_{12}	-	1	CLK
Write data setup to BCLK low	t_{13}	4	-	ns
Write data hold from BCLK low	t_{14}	6	-	ns

53C710-1 Bus Mode 1 Slave Write Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(5-0), SIZ(1-0), R-W/ setup to AS/	t_2	4	-	ns
A(5-0), SIZ(1-0), R-W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	20	ns
AS/ high to CBACK/ low	t_7	3	15	ns
BCLK high to SLACK/, BERR/ low	t_8	-	20	ns
AS/ high to SLACK/, BERR/ high	t_9	-	20	ns
STERM/ (input) setup to BCLK high	t_{10}	2	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
STERM/ clocked active to AS/ high	t_{12}	-	1	CLK
Write data setup to BCLK low	t_{13}	4	-	ns
Write data hold from BCLK low	t_{14}	6	-	ns

Note: The 53C710 must see address strobes paired up with synchronous cycle terminations, even though the slave cycle may not be intended for the 53C710.

Figure 6-5. Bus Mode 1 Slave Write Cycle



Note: Shaded areas indicate that the signal is a don't care.

* This signal may be driven by the 53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 of the Data Manual for use of this signal as an output.

Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2) Bus Request is asserted.
3) The 53C710 waits for Bus Grant and checks that bus Grant Acknowledge is deasserted. Then the 53C710 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request on the next rising edge of BCLK.

53C710 Bus Mode 1 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SCO high to BR/ low*	t_1	1	2	BCLK
BCLK high to SCO low on start phase of last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	24	ns
BCLK high to BGACK/ high	t_9	3	15	ns
BCLK high to BGACK/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

* When the Snoop Mode bit (CTEST8 bit 0) is set to 1.

** During a Retry operation, FETCH/ will remain low until a successful completion of the opcode fetch or a fatal bus error.

Note: The 53C710 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will generate an interrupt, which the system may then service.

53C710-1 Bus Mode 1 Host Bus Arbitration Timings

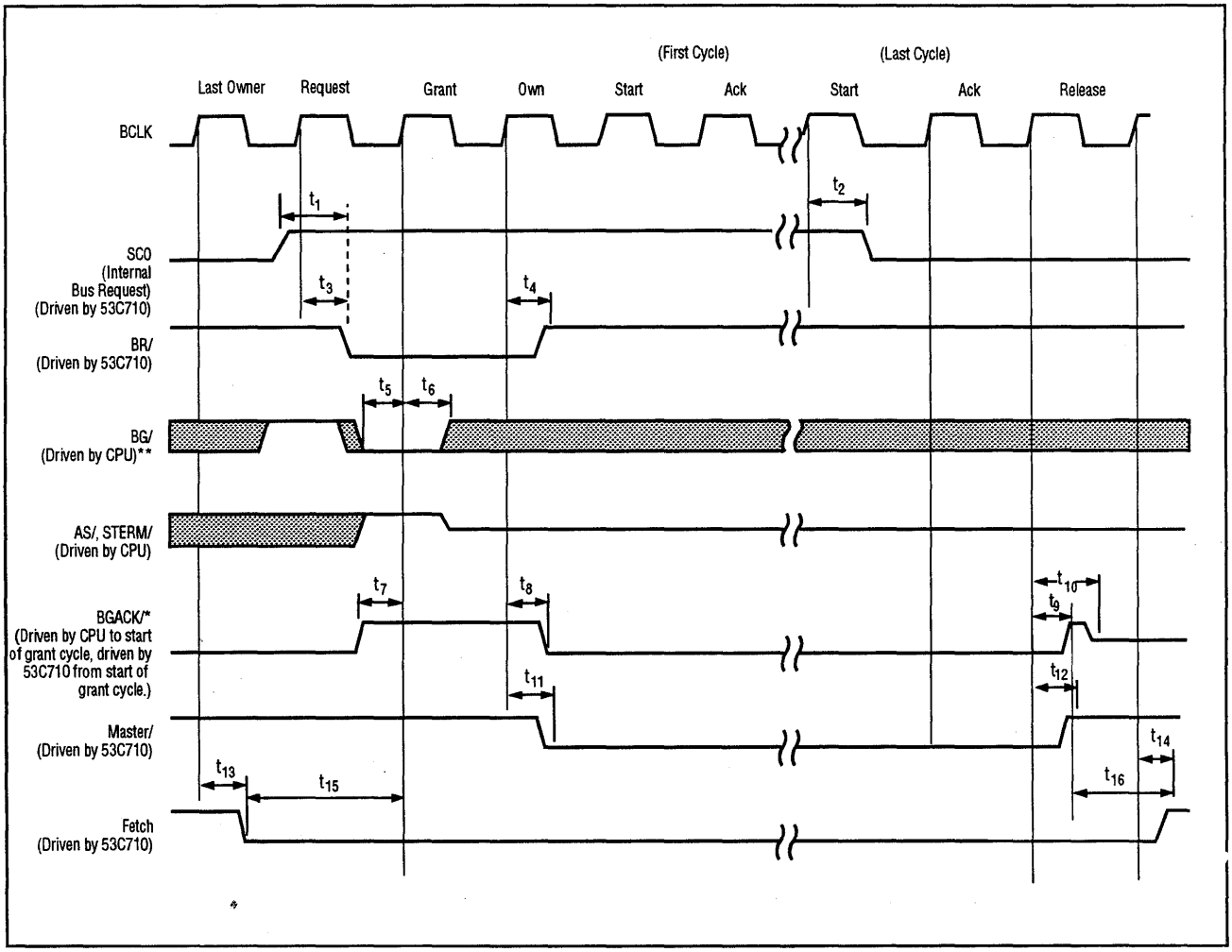
Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on start phase of last cycle*	t_2	5	22	ns
BCLK high to BR/ low	t_3	4	16	ns
BCLK high to BR/ high	t_4	5	21	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	20	ns
BCLK high to BGACK/ high	t_9	3	12	ns
BCLK high to BGACK/ high-Z	t_{10}	7	28	ns
BCLK high to MASTER/ low	t_{11}	5	18	ns
BCLK high to MASTER/ high	t_{12}	6	21	ns
BCLK high to FETCH/ low	t_{13}	5	28	ns
BCLK high to FETCH/ high	t_{14}	5	28	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

* When the Snoop Mode bit (CTEST8 bit 0) is set to 1.

** During a Retry operation, FETCH/ will remain low until a successful completion of the opcode fetch or a fatal bus error.

Note: The 53C710 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will generate an interrupt, which the system may then service.

Figure 6-6. Bus Mode 1 Host Bus Arbitration Cycle



Note: Shaded area indicates that the signal is a don't care.

* If the Fast Arbitration bit is set (DCNTL bit 1) the 53C710 will drive the Bus Grant Acknowledge signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

** In order for Bus Grant to be recognized, AS/ and STERM/ must be false.

Note: The 53C710 will insert a fairness delay of 5-8 clocks between host bus arbitrations.

Bus Mode 1 Fast Arbitration

Fast Arbitration Sequence

1) The 53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2) Bus Request is asserted.
3) The 53C710 waits for Bus Grant. The 53C710 becomes bus master asynchronously on the leading edge of BG/. Then the 53C710 asynchronously asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.
4) The 53C710 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the 53C710 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/.

53C710 Bus Mode 1 Fast Arbitration Timings

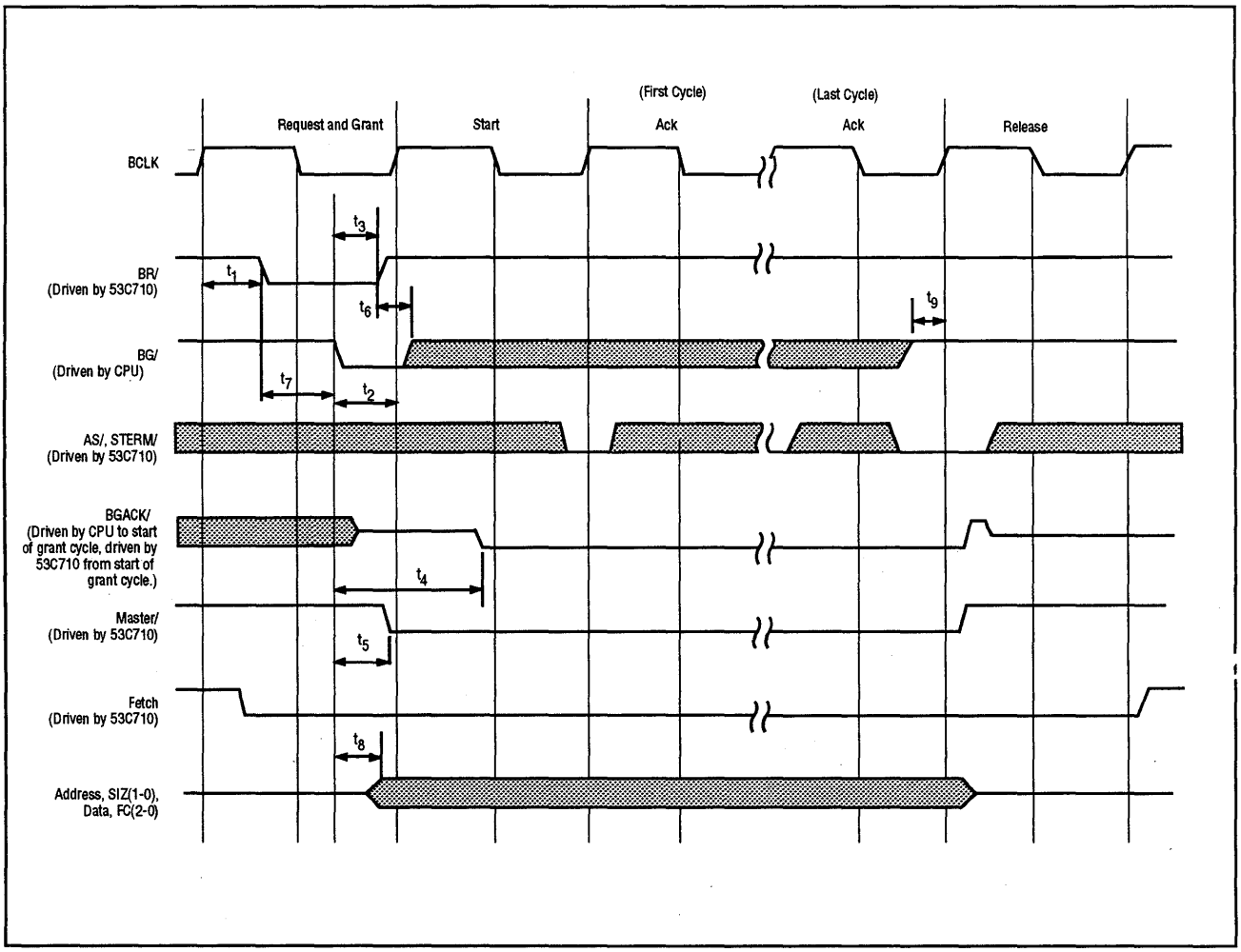
Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	-	16	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BGACK/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns
BG/ asserted to SIZ(1-0), Addr, Data	t_8	-	29	ns
BG/ to BCLK high in ACK phase of last cycle	t_9	-	29	ns

53C710-1 Bus Mode 1 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	16	ns
BG/ setup to BCLK high	t_2	-	16	ns
BG/ asserted to BR/ deasserted	t_3	-	18	ns
BG/ asserted to BGACK/ asserted	t_4	-	16	ns
BG/ asserted to MASTER/ asserted	t_5	-	14	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns
BG/ asserted to SIZ(1-0), Addr, Data	t_8	-	25	ns
BG/ to BCLK high in ACK phase of last cycle	t_9	-	29	ns

* *BG/ may not be asserted prior to BR/.*

Figure 6-7. Bus Mode 1 Fast Arbitration



Note: Shaded areas indicate the signal is a don't care.

Bus Mode 1 Bus Master Cycle

Bus Mode 1 Bus Master Read Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write, Snoop Control, Function Control and Transfer Type lines.
3) The 53C710 asserts the Address and Size lines.
4) The 53C710 asserts Address Strobe, Cache Burst Request (if appropriate) and Data Strobe.
5) The 53C710 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error and HALT.
   - If Cache Burst Acknowledge is asserted, attempt bursting.
   - If Bus Error and HALT are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or HALT, and the 53C710 requires more cycles, then return to step 3.
6) The 53C710 deasserts the Control and Address lines.
7) Upon acknowledgment of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

53C710 Bus Mode 1 Bus Master Read Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ hi-Z	t_6	7	34	ns
STERM/ (input) setup to BCLK high	t_7	3	-	ns
STERM/ (input) hold from BCLK high	t_8	7	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_9	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{10}	4	18	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO hi-Z	t_{13}	6	30	ns
Read Data setup to BCLK low	t_{14}	4	-	ns
Read Data hold from BCLK low	t_{15}	6	-	ns
BCLK high to DS/ driven	t_{16}	5	32	ns
BCLK low to DS/ low	t_{17}	3	16	ns
BCLK low to DS/ high	t_{18}	3	16	ns
BCLK high to DS/ hi-Z	t_{19}	7	34	ns
BCLK high to CBREQ/ driven	t_{20}	5	30	ns
BCLK low to CBREQ/ low	t_{21}	3	16	ns
BCLK low to CBREQ/ high	t_{22}	3	16	ns
BCLK high to CBREQ/ hi-Z	t_{23}	7	32	ns
CBACK/ setup to BCLK high	t_{24}	8	-	ns
CBACK/ hold from BCLK high	t_{25}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{26}	6	-	ns
BERR/, HALT hold from BCLK low	t_{27}	4	-	ns

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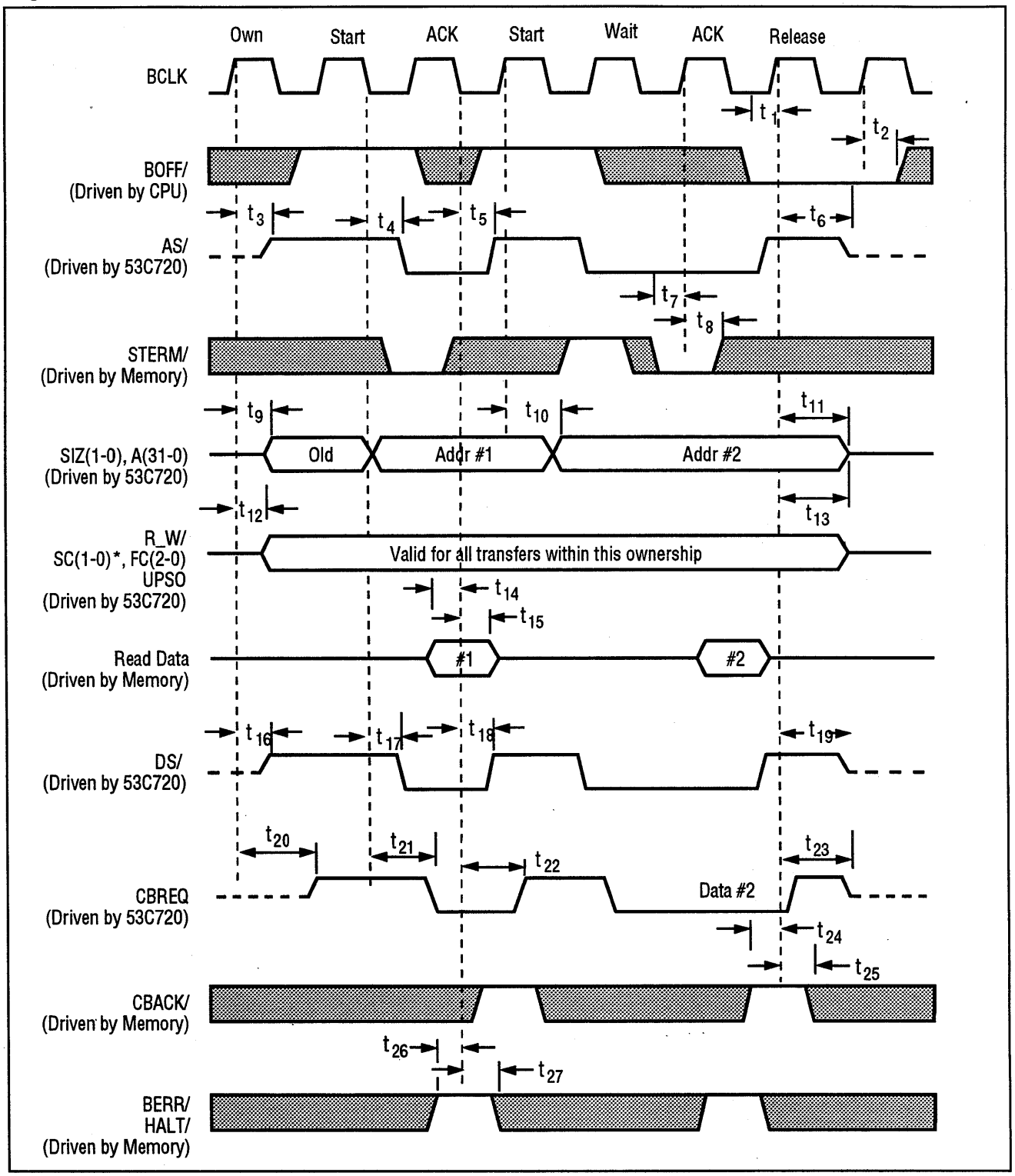
53C710-1 Bus Mode 1 Bus Master Read Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	26	ns
BCLK low to AS/ low	t_4	3	14	ns
BCLK low to AS/ high	t_5	3	14	ns
BCLK high to AS/ hi-Z	t_6	7	28	ns
STERM/ (input) setup to BCLK high	t_7	3	-	ns
STERM/ (input) hold from BCLK high	t_8	7	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_9	5	24	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{10}	4	15	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{11}	7	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	24	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO hi-Z	t_{13}	6	25	ns
Read Data setup to BCLK low	t_{14}	4	-	ns
Read Data hold from BCLK low	t_{15}	6	-	ns
BCLK high to DS/ driven	t_{16}	5	25	ns
BCLK low to DS/ low	t_{17}	3	14	ns
BCLK low to DS/ high	t_{18}	3	14	ns
BCLK high to DS/ hi-Z	t_{19}	7	28	ns
BCLK high to CBREQ/ driven	t_{20}	5	25	ns
BCLK low to CBREQ/ low	t_{21}	3	14	ns
BCLK low to CBREQ/ high	t_{22}	3	14	ns
BCLK high to CBREQ/ hi-Z	t_{23}	7	26	ns
CBACK/ setup to BCLK high	t_{24}	8	-	ns
CBACK/ hold from BCLK high	t_{25}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{26}	6	-	ns
BERR/, HALT hold from BCLK low	t_{27}	4	-	ns

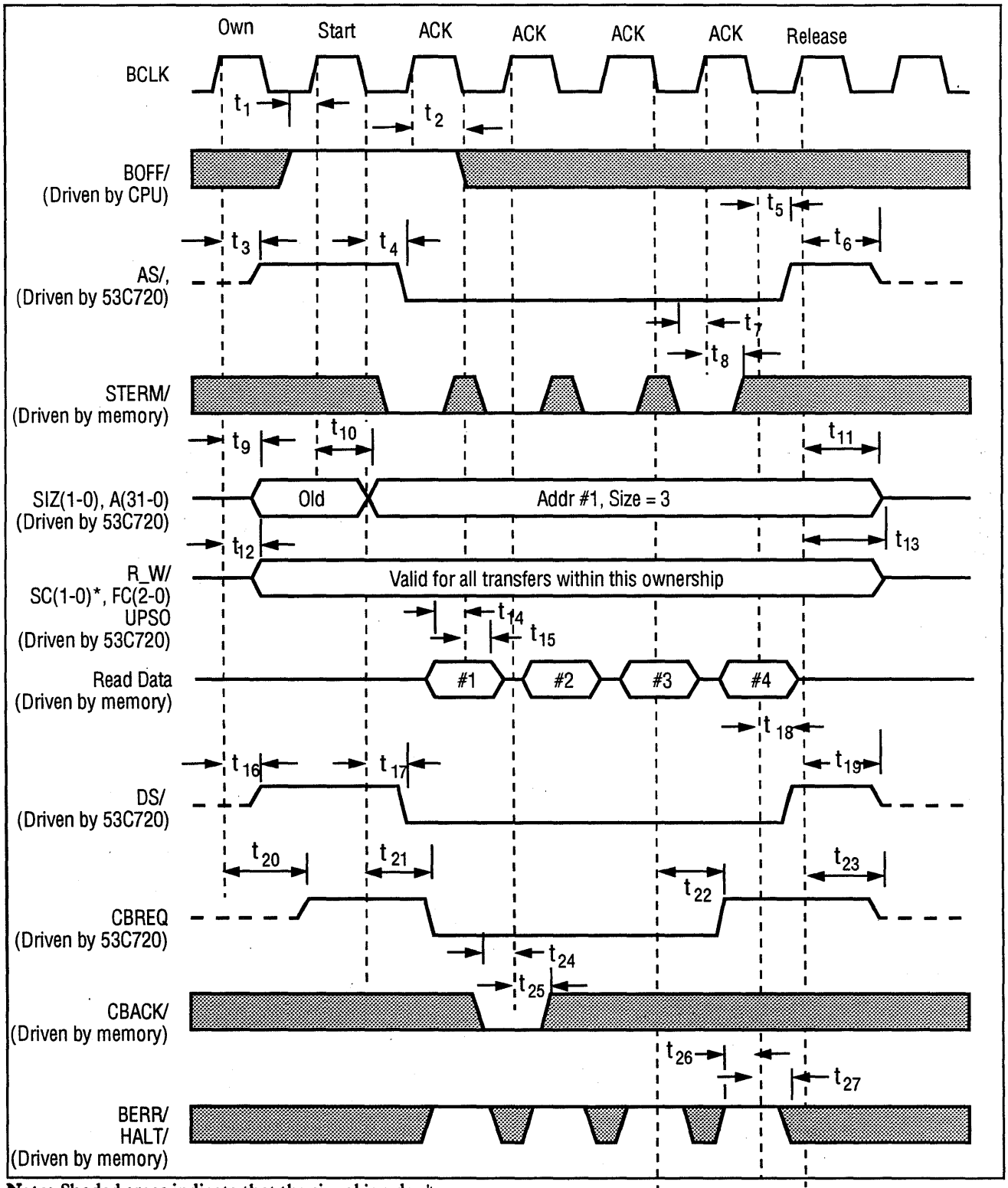
Figure 6-8. Bus Mode 1 Bus Master Read Cycle (Non-Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

* SC(1-0) timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6-9. Bus Mode 1 Bus Master Read Cycle (Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

* SC(1-0) timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Bus Mode 1 Bus Master Write Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write/, Snoop Control, Function Control and Transfer Type lines.
3) The 53C710 asserts the Address , Size and Data lines.
4) The 53C710 asserts Address Strobe and Cache Burst Request (and Data Strobe if Read).
5) The 53C710 asserts Data Strobe.
6) The 53C710 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the 53C710 requires more cycles, then return to step 3.
7) The 53C710 deasserts the Control, Address, and Data lines.
8) Upon acknowledgment of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

53C710 Bus Mode 1 Bus Master Write Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ hi-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_9	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{10}	4	18	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO hi-Z	t_{13}	6	30	ns
BCLK high to Write Data driven	t_{14}	6	34	ns
BCLK high to Write Data valid	t_{15}	6	24	ns
BCLK high to Data hi-Z	t_{16}	6	32	ns
BCLK high to DS/ driven	t_{17}	5	32	ns
BCLK low to DS/ low	t_{18}	3	16	ns
BCLK low to DS/ high	t_{19}	3	16	ns
BCLK high to DS/ hi-Z	t_{20}	7	34	ns
BCLK high to CBREQ/ driven	t_{21}	5	30	ns
BCLK low to CBREQ/ low	t_{22}	3	16	ns
BCLK low to CBREQ/ high	t_{23}	3	16	ns
BCLK high to CBREQ/ hi-Z	t_{24}	7	32	ns
CBACK/ setup to BCLK high	t_{25}	8	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

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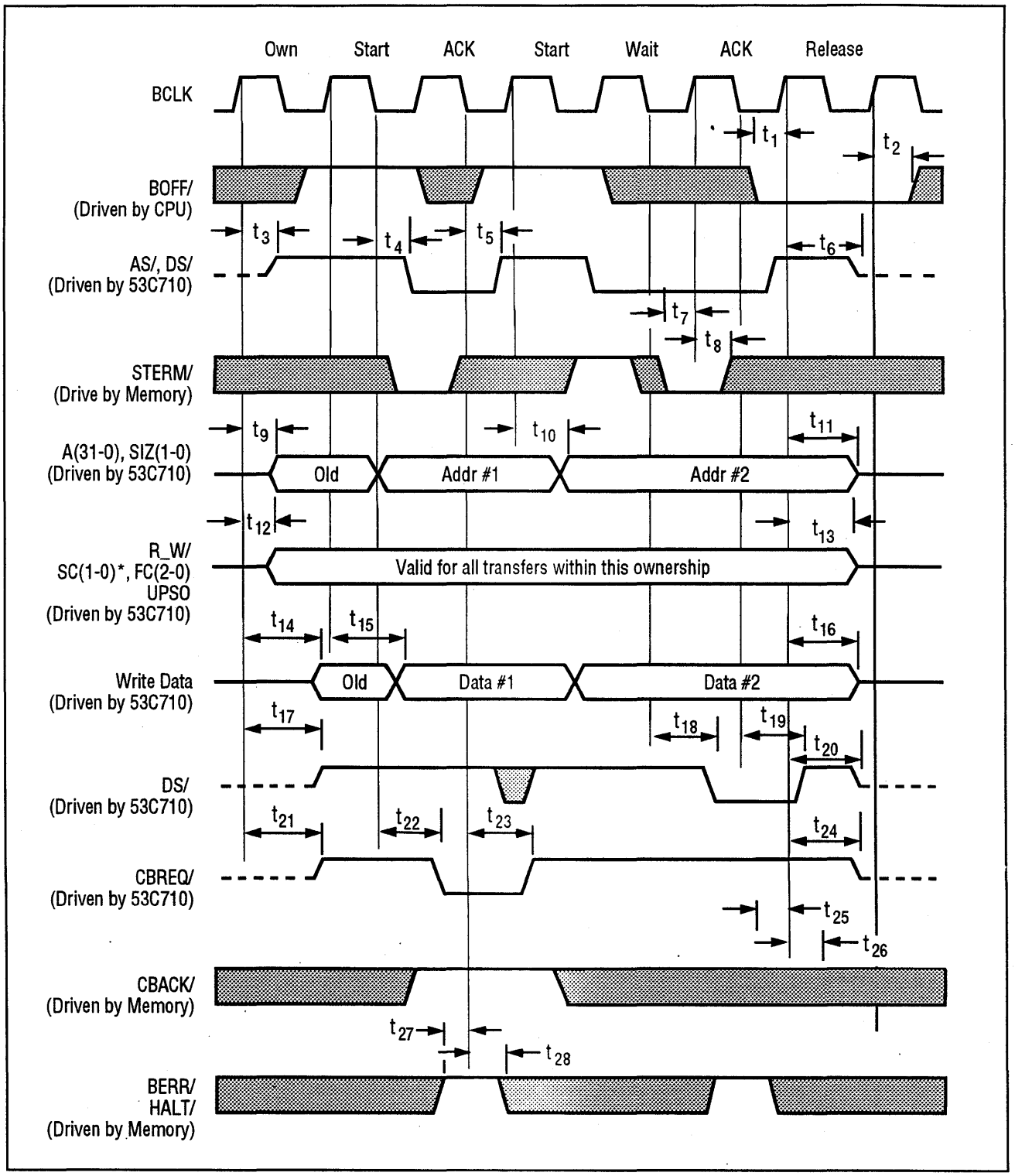
53C710-1 Bus Mode 1 Bus Master Write Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	26	ns
BCLK low to AS/ low	t_4	3	14	ns
BCLK low to AS/ high	t_5	3	14	ns
BCLK high to AS/ hi-Z	t_6	7	28	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_9	5	24	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{10}	4	15	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{11}	7	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	24	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO hi-Z	t_{13}	6	25	ns
BCLK high to Write Data driven	t_{14}	6	28	ns
BCLK high to Write Data valid	t_{15}	6	20	ns
BCLK high to Data hi-Z	t_{16}	6	26	ns
BCLK high to DS/ driven	t_{17}	5	25	ns
BCLK low to DS/ low	t_{18}	3	14	ns
BCLK low to DS/ high	t_{19}	3	14	ns
BCLK high to DS/ hi-Z	t_{20}	7	28	ns
BCLK high to CBREQ/ driven	t_{21}	5	25	ns
BCLK low to CBREQ/ low	t_{22}	3	14	ns
BCLK low to CBREQ/ high	t_{23}	3	14	ns
BCLK high to CBREQ/ hi-Z	t_{24}	7	26	ns
CBACK/ setup to BCLK high	t_{25}	8	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

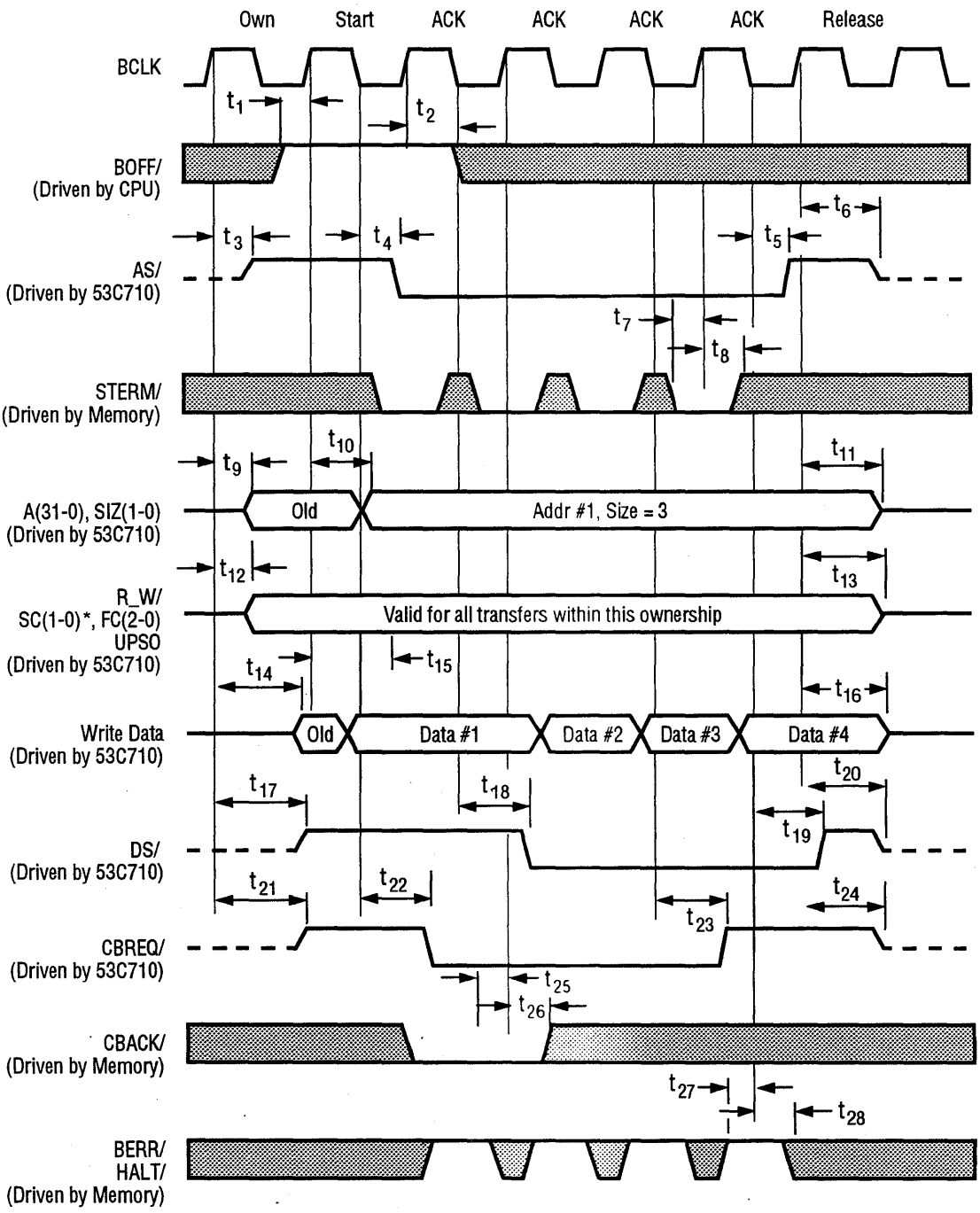
Figure 6-10. Bus Mode 1 Bus Master Write Cycle (Non-Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

* SC(1-0) timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6-11. Bus Mode 1 Bus Master Write Cycle (Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

* SC(1-0) timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Bus Mode 2 Slave Cycle

Bus Mode 2 Slave Read Sequence

1) The Read/Write, Address, Transfer Start and Size lines are asserted by the CPU.
2) Chip Select is validated by the 53C710 on any following rising edge of BCLK.
3) Transfer Burst Inhibit is asserted.
4) Transfer Start is deasserted by the CPU.
5) Three clock cycles of wait state are inserted and the Data lines are asserted.
6) Slave Acknowledge is asserted by the 53C710, if no errors are detected.
7) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8) Slave Acknowledge or Transfer Error Acknowledge is deasserted.
9) The 53C710 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10) The Data lines are tristated by the 53C710.

53C710 Bus Mode 2 Slave Read Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to any BCLK high after TS/	t_3	5	-	ns
CS/ hold from any BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus hi-Z	t_{13}	7	30	ns
A(5-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	4	-	ns
A(5-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns

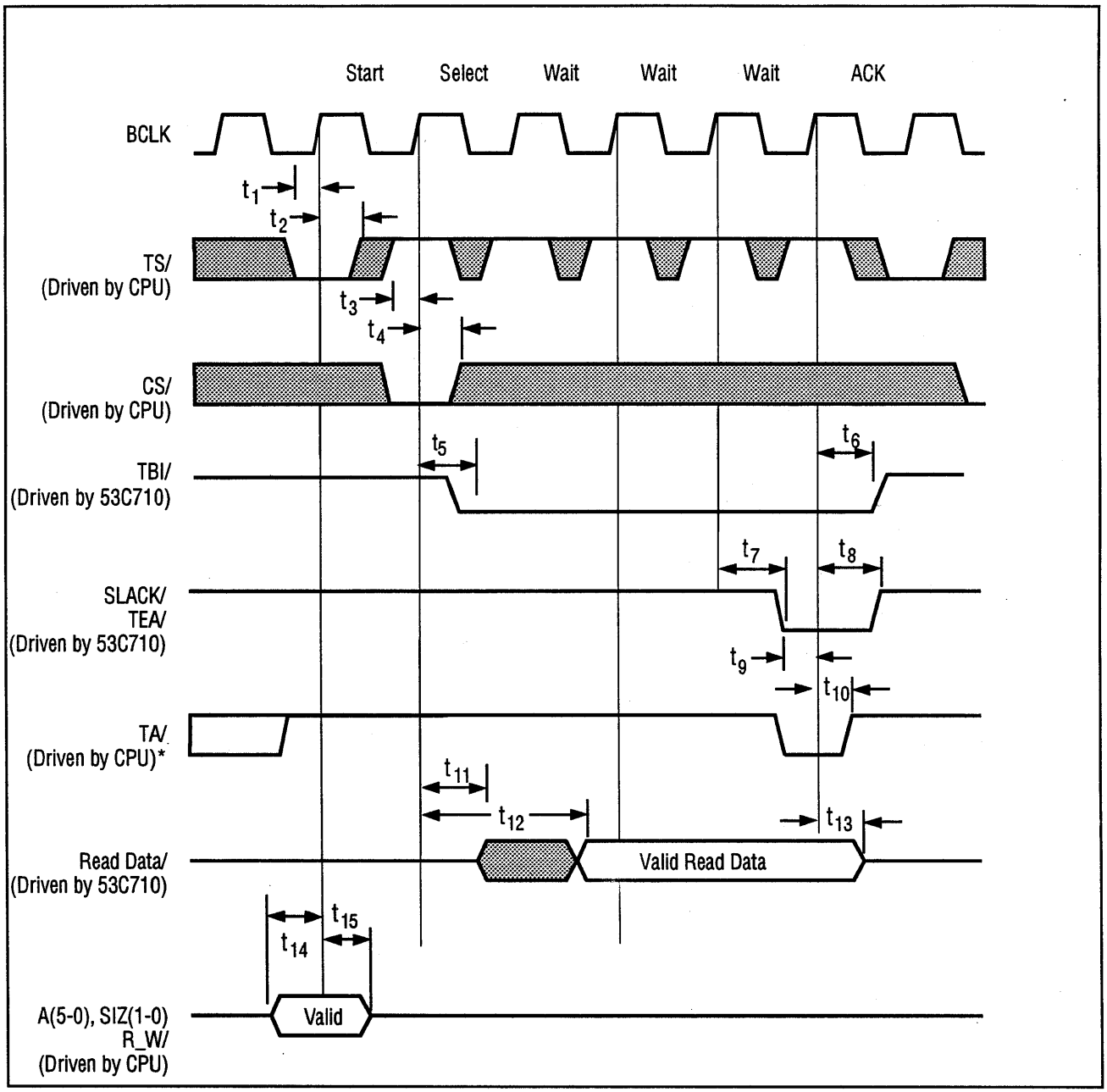
Note: The 53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the 53C710.

53C710-1 Bus Mode 2 Slave Read Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to any BCLK high after TS/	t_3	5	-	ns
CS/ hold from any BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	25	ns
BCLK high to TBI/ high	t_6	4	18	ns
BCLK high to SLACK/, TEA/ low	t_7	5	17	ns
BCLK high to SLACK/, TEA/ high	t_8	4	17	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	60	ns
BCLK high to data bus hi-Z	t_{13}	7	25	ns
A(5-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	4	-	ns
A(5-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns

Note: The 53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the 53C710.

Figure 6-12. Bus Mode 2 Slave Read Cycle



Note: Shaded areas indicate that the signal is a don't care.

* This signal may be driven by the 53C710 if the ENABLE ACK bit is set (DCNTL bit 5). See explanation in Chapter 2 of the Data Manual for use of this signal as an output.

Bus Mode 2 Slave Write Sequence

1) The Read/Write, Address, Transfer Start and Size lines are asserted by the CPU.
2) Chip Select is validated by the 53C710 on any following rising edge of BCLK.
3) Transfer Burst Inhibit is asserted.
4) Transfer Start is deasserted by the CPU.
5) The Data lines are asserted by the CPU.
6) Three clock cycles of wait state are inserted.
7) Slave Acknowledge is asserted by the 53C710, if no errors are detected.
8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9) Slave Acknowledge or Transfer Error Acknowledge is deasserted.
10) The 53C710 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.

53C710 Bus Mode 2 Slave Write Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	5	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(5-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	4	-	ns
A(5-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns

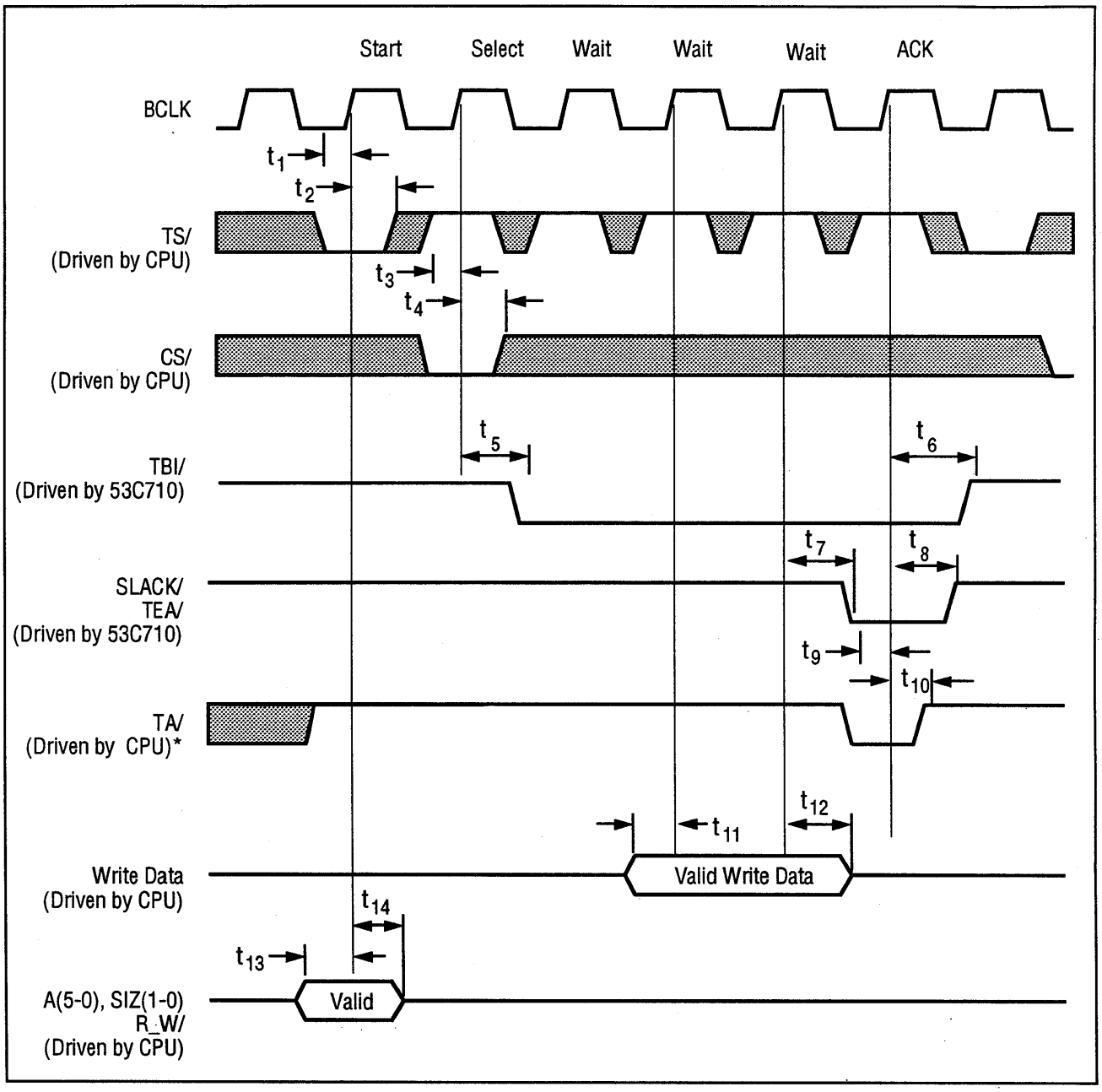
Note: The 53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the 53C710.

53C710-1 Bus Mode 2 Slave Write Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	25	ns
BCLK high to TBI/ high	t_6	4	18	ns
BCLK high to SLACK/, TEA/ low	t_7	4	17	ns
BCLK high to SLACK/, TEA/ high	t_8	4	17	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	5	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(5-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	4	-	ns
A(5-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns

Note: The 53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the 53C710.

Figure 6-13. Bus Mode 2 Slave Write Cycle



Note: Shaded areas indicate that the signal is a don't care.

* This signal may be driven by the 53C710 if the ENABLE ACK bit is set (DCNTL bit 5). See explanation in Chapter 2 of the Data Manual for use of this signal as an output.

Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2) Bus Request is asserted.
3) The 53C710 waits for Bus Grant and checks that bus Grant Acknowledge is deasserted. Then the 53C710 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.

53C710 Bus Mode 2 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on start phase of last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	15	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

53C710-1 Bus Mode 2 Host Bus Arbitration Timings

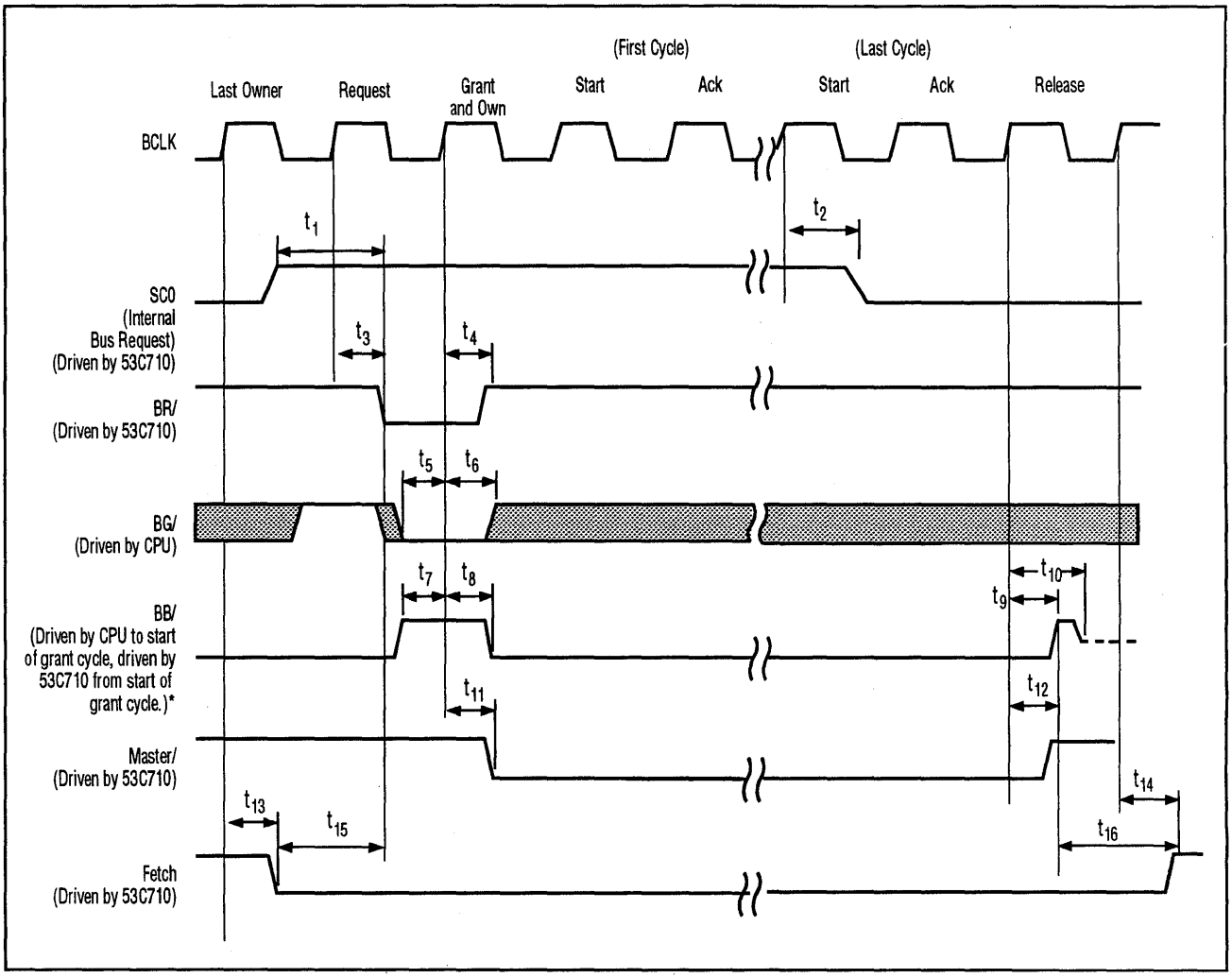
Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on start phase of last cycle*	t_2	5	22	ns
BCLK high to BR/ low	t_3	4	16	ns
BCLK high to BR/ high	t_4	5	21	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	20	ns
BCLK high to BB/ high	t_9	3	12	ns
BCLK high to BB/ high-Z	t_{10}	7	28	ns
BCLK high to MASTER/ low	t_{11}	5	18	ns
BCLK high to MASTER/ high	t_{12}	6	21	ns
BCLK high to FETCH/ low	t_{13}	5	28	ns
BCLK high to FETCH/ high	t_{14}	5	28	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

* When the Snoop Mode bit (CTEST8 bit 0) is set to 1.

** During a retry operation, FETCH/ will remain low until successful completion of an opcode fetch or a fatal bus error.

Note: The 53C710 will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access - it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt, which the system may then service.

Figure 6-14. Bus Mode 2 Host Bus Arbitration Cycle



Note: Shaded area indicates that the signal is a don't care.

*If the Fast Arbitration bit is set (DCNTL bit 1), the 53C710 will drive the Bus Grant Acknowledge signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

Note: the 53C710 will insert a fairness delay of 5-8 clocks between host bus arbitrations.

Bus Mode 2 Fast Arbitration

Fast Arbitration Sequence

1) The 53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2) Bus Request is asserted.
3) The 53C710 waits for Bus Grant. The 53C710 becomes bus master asynchronously on the leading edge of BG/. Then the 53C710 asynchronously asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.
4) The 53C710 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the 53C710 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.

53C710 Bus Mode 2 Fast Arbitration Timings

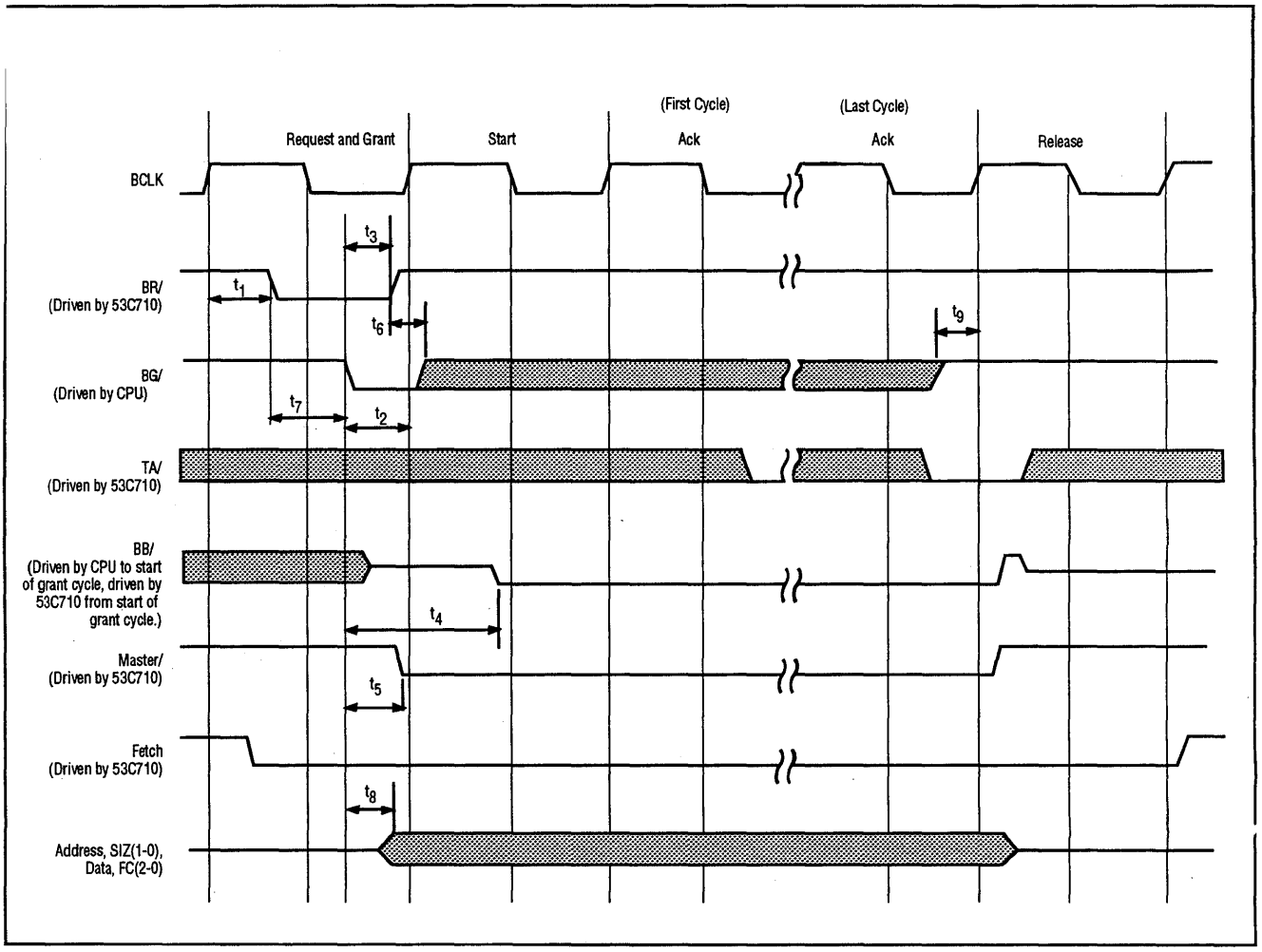
Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	-	16	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BB/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns
BG/ asserted to SIZ(1-0), Addr, Data	t_8	-	29	ns
BG/ to BCLK high, in ACK phase of last cycle	t_9	-	29	ns

53C710-1 Bus Mode 2 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	16	ns
BG/ setup to BCLK high	t_2	-	16	ns
BG/ asserted to BR/ deasserted	t_3	-	18	ns
BG/ asserted to BB/ asserted	t_4	-	16	ns
BG/ asserted to MASTER/ asserted	t_5	-	14	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns
BG/ asserted to SIZ(1-0), Addr, Data	t_8	-	25	ns
BG/ to BCLK high, in ACK phase of last cycle	t_9	-	29	ns

* BG/ may not be asserted prior to BR/.

Figure 6-15. Bus Mode 2 Fast Arbitration



Note: Shaded areas indicates the signal is a don't care.

Bus Mode 2 Bus Master Cycle

Bus Mode 2 Bus Master Read Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write/, Snoop Control, Function Control, and Transfer Type lines.

3a) The 53C710 asserts Transfer in Progress and Transfer Start.

3b) The 53C710 asserts the Transfer Start, Address, and Size lines.

4) The 53C710 deasserts Transfer Start.
5) The 53C710 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated on the next rising edge of BCLK.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C710 requires more cycles, then return to step 3b.
6) The 53C710 deasserts the Control and Address lines.
7) Upon acknowledgment of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

53C710 Bus Mode 2 Bus Master Read Cycle Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	17	ns
BCLK high to TIP/ high	t_5	3	16	ns
BCLK high to TIP/ hi-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	14	ns
BCLK high to TS/ high	t_9	4	13	ns
BCLK high to TS/ hi-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	5	18	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) hi-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	5	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
Read Data setup to DLE low	t_{20}	4	-	ns
Read Data hold from DLE low	t_{21}	6	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

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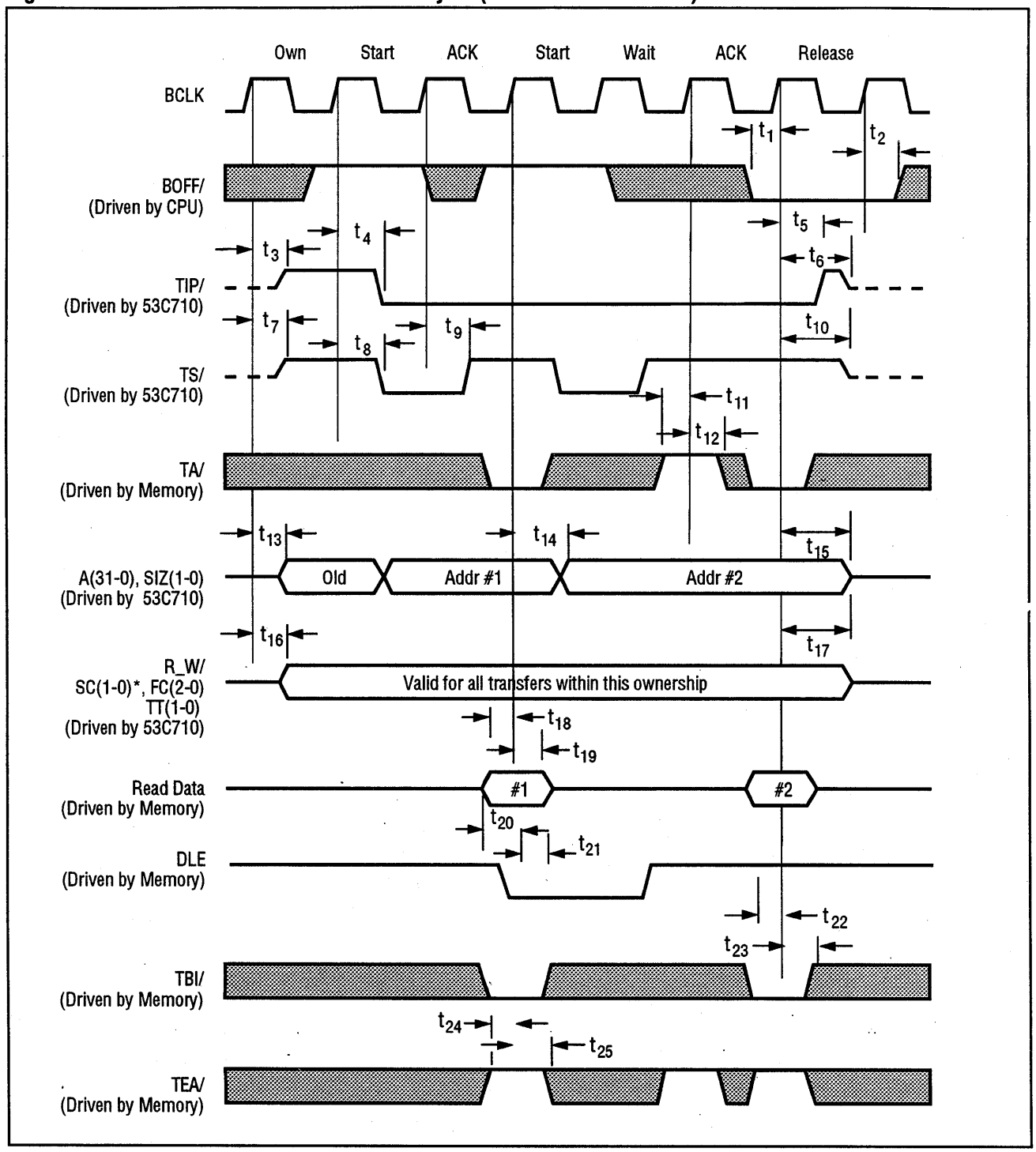
53C710-1 Bus Mode 2 Bus Master Read Cycle Timings (Non-Cache Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	26	ns
BCLK high to TIP/ low	t_4	3	14	ns
BCLK high to TIP/ high	t_5	3	14	ns
BCLK high to TIP/ hi-Z	t_6	7	28	ns
BCLK high to TS/ driven	t_7	5	25	ns
BCLK high to TS/ low	t_8	3	12	ns
BCLK high to TS/ high	t_9	4	12	ns
BCLK high to TS/ hi-Z	t_{10}	7	28	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	24	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	5	15	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{15}	7	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) driven and valid	t_{16}	5	25	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) hi-Z	t_{17}	-	28	ns
Read Data setup to BCLK high	t_{18}	5	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
Read Data setup to DLE low	t_{20}	4	-	ns
Read Data hold from DLE low	t_{21}	6	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

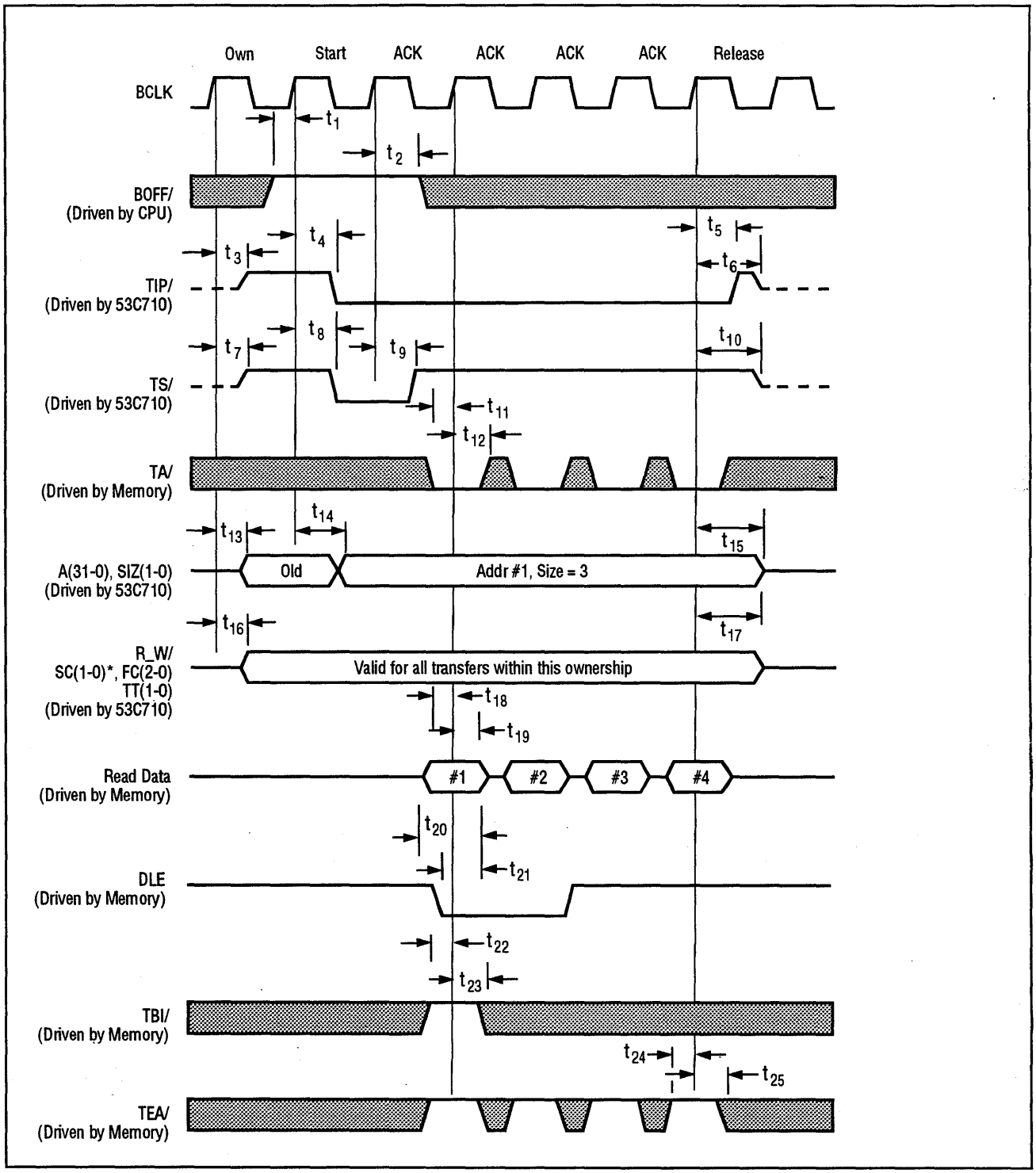
Figure 6-16. Bus Mode 2 Bus Master Read Cycle (Non-Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

*SC(1-0) timings apply only if the Snoop Mode bit (CTEST8 bit 0) is equal to zero.

Figure 6-17. Bus Mode 2 Bus Master Read Cycle (Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

*SC(1-0) timings apply only if the Snoop Mode bit (CTEST8 bit 0) is equal to zero.

Bus Mode 2 Bus Master Write Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C710 asserts Transfer in Progress and Transfer Start.

3b) The 53C710 asserts Transfer Start, Address, Size lines, and Data lines.

4) The 53C710 deasserts Transfer Start.
5) The 53C710 waits for Transfer Acknowledge, Transfer Burst Inhibit and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the 53C710 requires more cycles, return to step 3b.
6) The 53C710 deasserts the Control, Address and Data lines.
7) Upon acknowledge of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

53C710 Bus Mode 2 Bus Master Write Timings (Non-Cache-Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	17	ns
BCLK high to TIP/ high	t_5	3	16	ns
BCLK high to TIP/ hi-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	14	ns
BCLK high to TS/ high	t_9	3	13	ns
BCLK high to TS/ hi-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	18	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) hi-Z	t_{17}	-	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	7	24	ns
BCLK high to Write Data hi-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns

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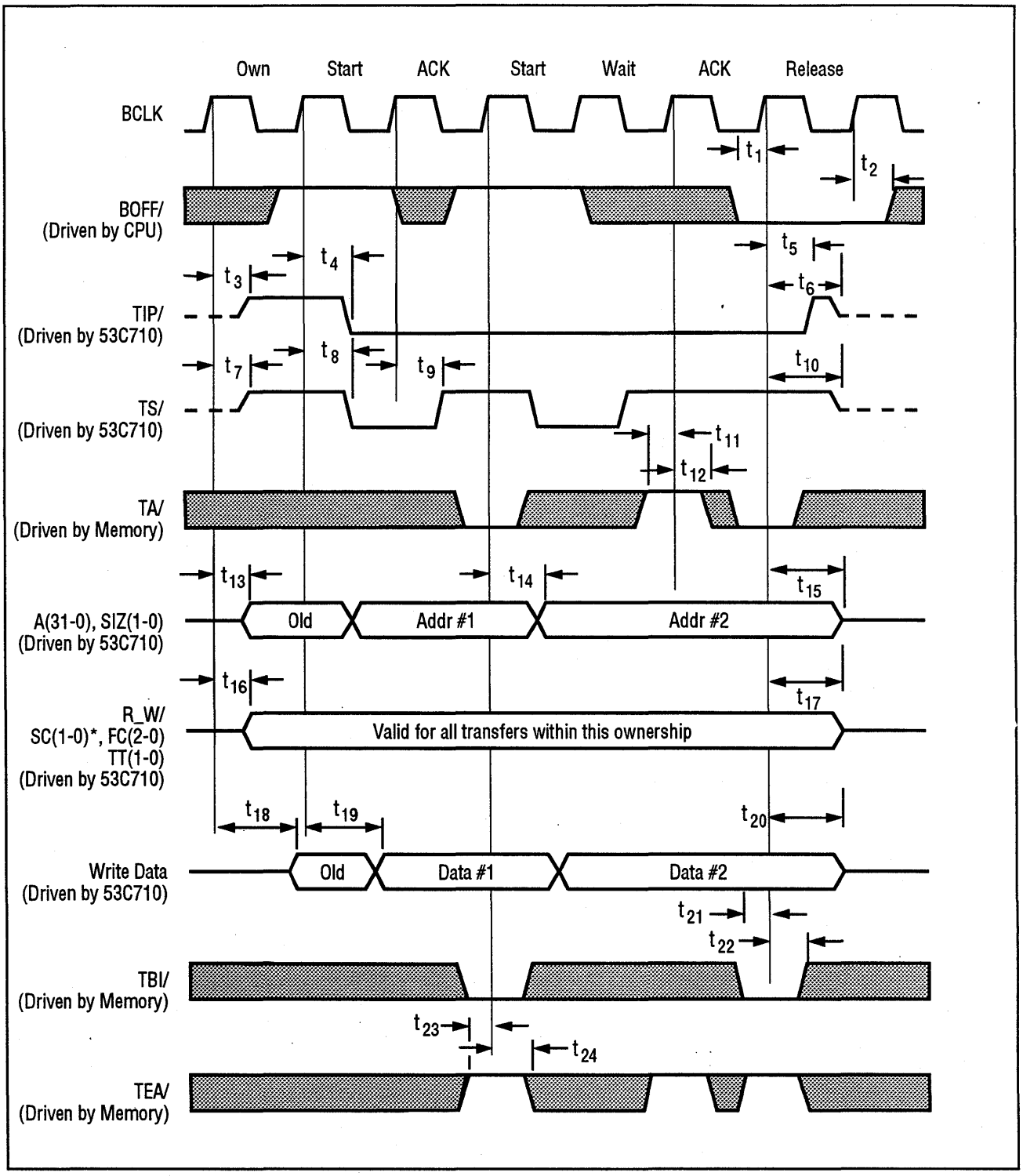
53C710-1 Bus Mode 2 Bus Master Write Timings (Non-Cache-Line & Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	26	ns
BCLK high to TIP/ low	t_4	3	14	ns
BCLK high to TIP/ high	t_5	3	14	ns
BCLK high to TIP/ hi-Z	t_6	7	28	ns
BCLK high to TS/ driven	t_7	5	25	ns
BCLK high to TS/ low	t_8	3	12	ns
BCLK high to TS/ high	t_9	3	12	ns
BCLK high to TS/ hi-Z	t_{10}	7	28	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	24	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	15	ns
BCLK high to A(31-0), SIZ(1-0) hi-Z	t_{15}	7	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) driven and valid	t_{16}	5	25	ns
BCLK high to R_W/, SC(1-0), FC(2-0), TT(1-0) hi-Z	t_{17}	-	28	ns
BCLK high to Write Data driven	t_{18}	5	28	ns
BCLK high to Write Data valid	t_{19}	7	18	ns
BCLK high to Write Data hi-Z	t_{20}	5	25	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns

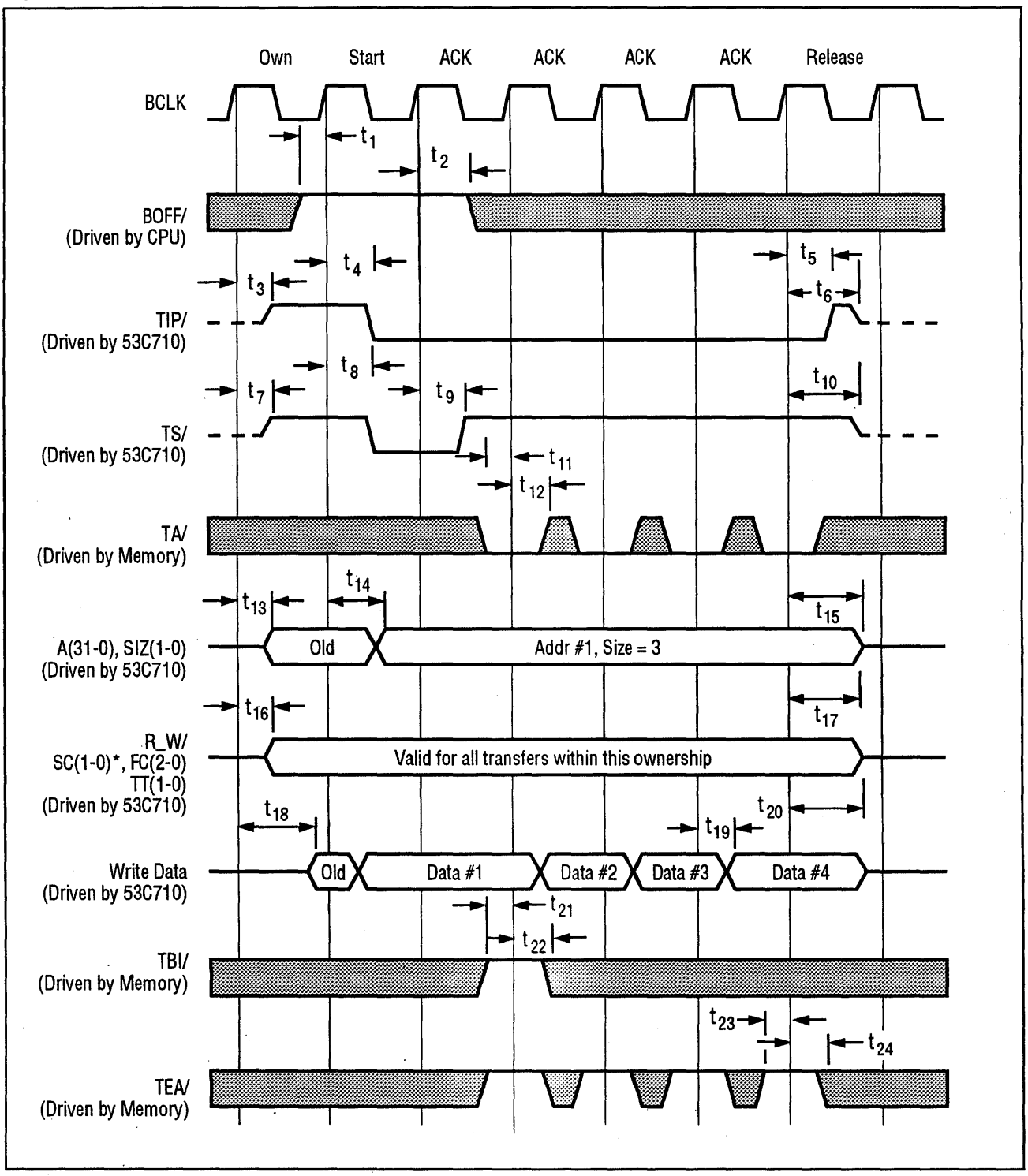
Figure 6-18. Bus Mode 2 Bus Master Write Cycle (Non-Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

*SC(1-0) timings apply only if the Snoop Mode bit (CTEST8 bit 0) is equal to zero.

Figure 6-19. Bus Mode 2 Bus Master Write Cycle (Cache Line Burst)



Note: Shaded areas indicate that the signal is a don't care.

*SC(1-0) timings apply only if the Snoop Mode bit (CTEST8 bit 0) is equal to zero.

Bus Mode 2 Mux Mode Operation

Mux Mode Read Cycle (Cache Line and Non-Cache Line Burst)

Mux Mode Read Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write/, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C710 asserts Transfer in Progress and Transfer Start.

3b) The 53C710 asserts the Transfer Start, Address, and Size lines.

4) The 53C710 deasserts Transfer Start and floats the Address lines.
5) The 53C710 waits for Transfer Acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C710 requires more cycles, then return to step 3b.
6) The 53C710 deasserts the Control lines.
7) Upon acknowledgment of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be tied to A(31-0) resistively.

53C710 Bus Mode 2 Mux Mode Read Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Address driven	t_1	6	22	ns
BCLK high to Address hi-z	t_2	-	23	ns
Read Data setup to BCLK high	t_3	5	-	ns
Read Data hold from BCLK high	t_4	6	-	ns

53C710-1 Bus Mode 2 Mux Mode Read Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Address driven	t_1	6	18	ns
BCLK high to Address hi-z	t_2	-	18	ns
Read Data setup to BCLK high	t_3	5	-	ns
Read Data hold from BCLK high	t_4	6	-	ns

Figure 6-20. Mux Mode Read Cycle (Non-Cache Line Burst)

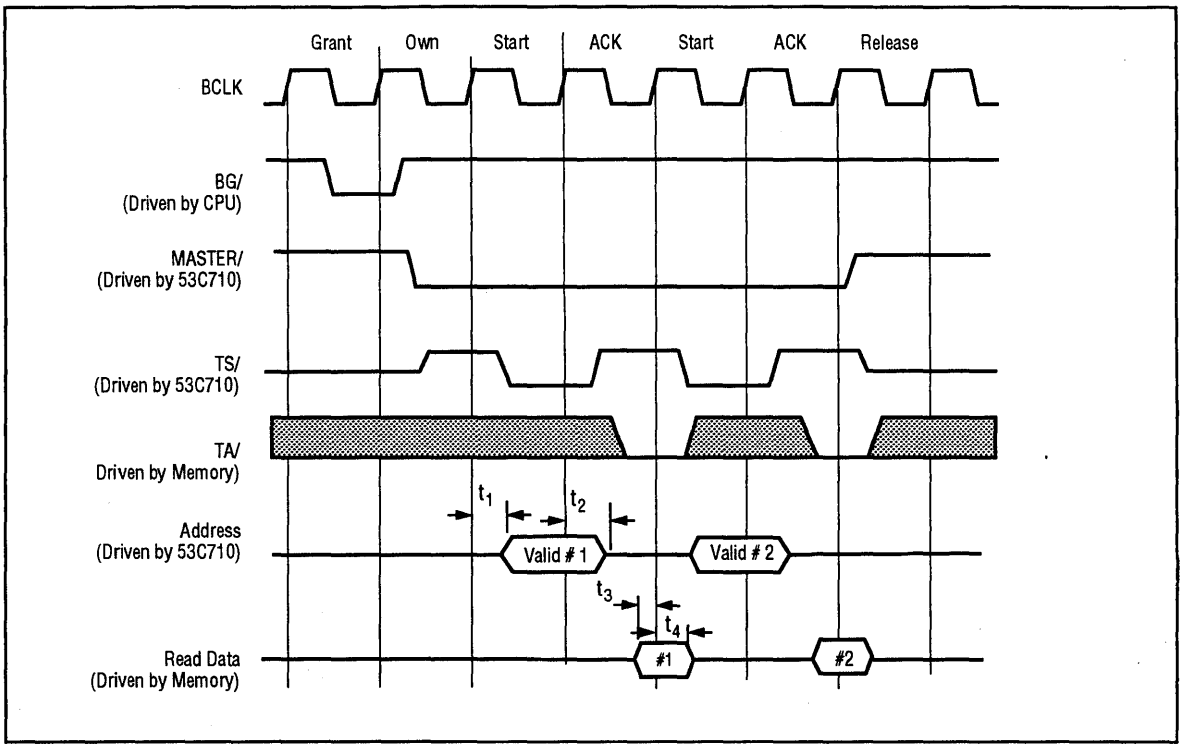
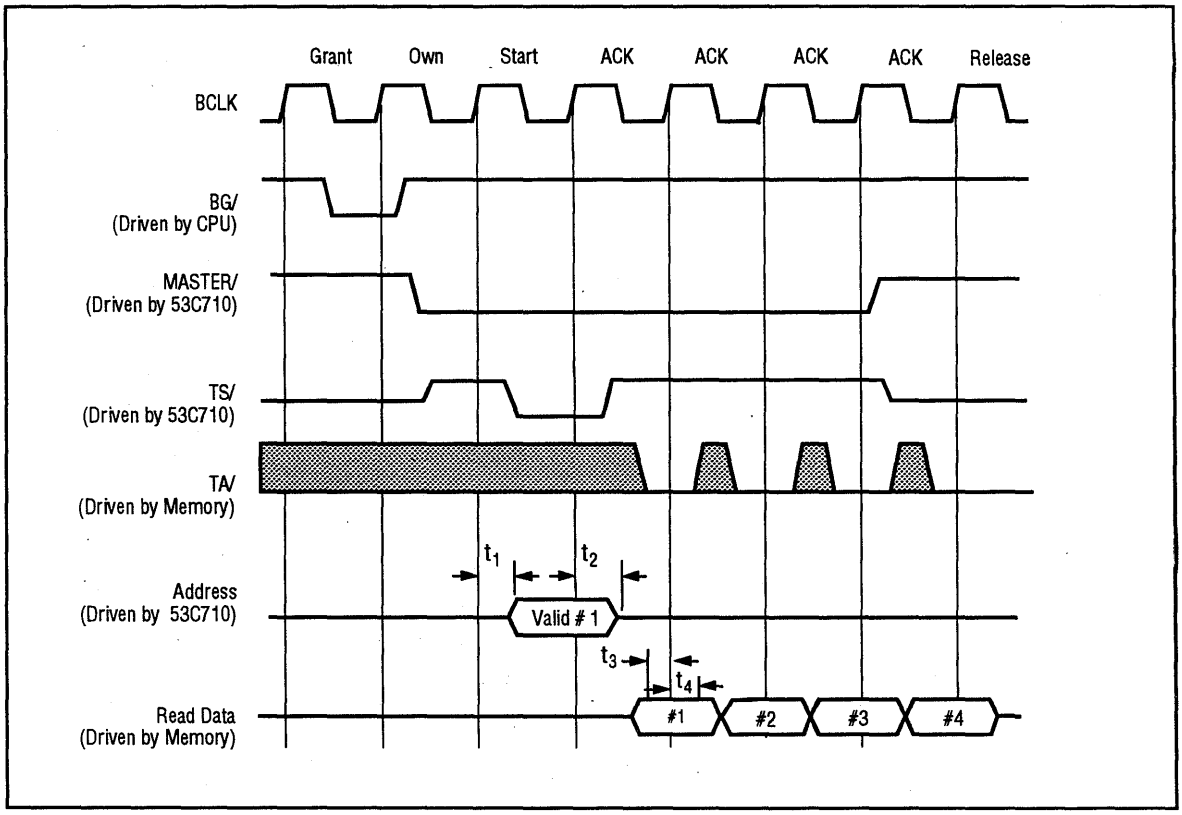


Figure 6-21. Mux Mode Read Cycle (Cache Line Burst)



Mux Mode Write Cycle (Cache Line and Non-Cache Line Burst)

Mux Mode Write Sequence

1) The 53C710 has attained bus mastership.
2) The 53C710 asserts the Read/Write, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C710 asserts Transfer in Progress and Transfer Start.

3b) The 53C710 asserts Transfer Start, Address, Size lines, and floats the Data lines.

4) The 53C710 deasserts Transfer Start, floats the address bus, and asserts the data bus.
5) The 53C710 waits for Transfer Acknowledge, Transfer Burst Inhibit and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the 53C710 requires more cycles, return to step 3b.
6) The 53C710 deasserts the Control and Data lines.
7) Upon acknowledge of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be physically tied to A(31-0) resistively.

53C710 Bus Mode 2 Mux Mode Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Old Data driven	t_1	-	34	ns
BCLK high to Address driven	t_2	6	22	ns
BCLK high to new Data driven	t_3	8	24	ns
Hi-z to Driven switching time	t_4	1	-	ns
BCLK high to Next Data	t_5	-	19	ns

53C710-1 Bus Mode 2 Mux Mode Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Old Data driven	t_1	-	28	ns
BCLK high to Address driven	t_2	6	18	ns
BCLK high to new Data driven	t_3	8	18	ns
Hi-z to Driven switching time	t_4	1	-	ns
BCLK high to Next Data	t_5	-	16	ns

Figure 6-22. Mux Mode Write Cycle (Non-Cache Line Burst)

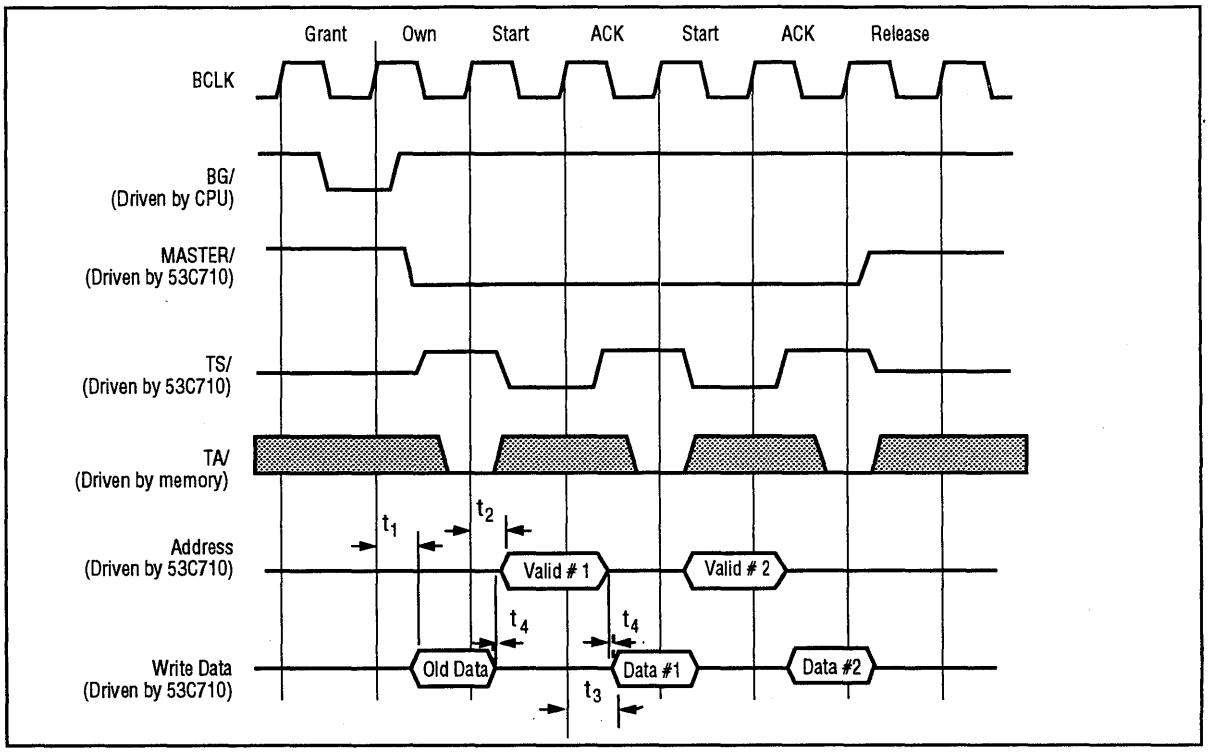
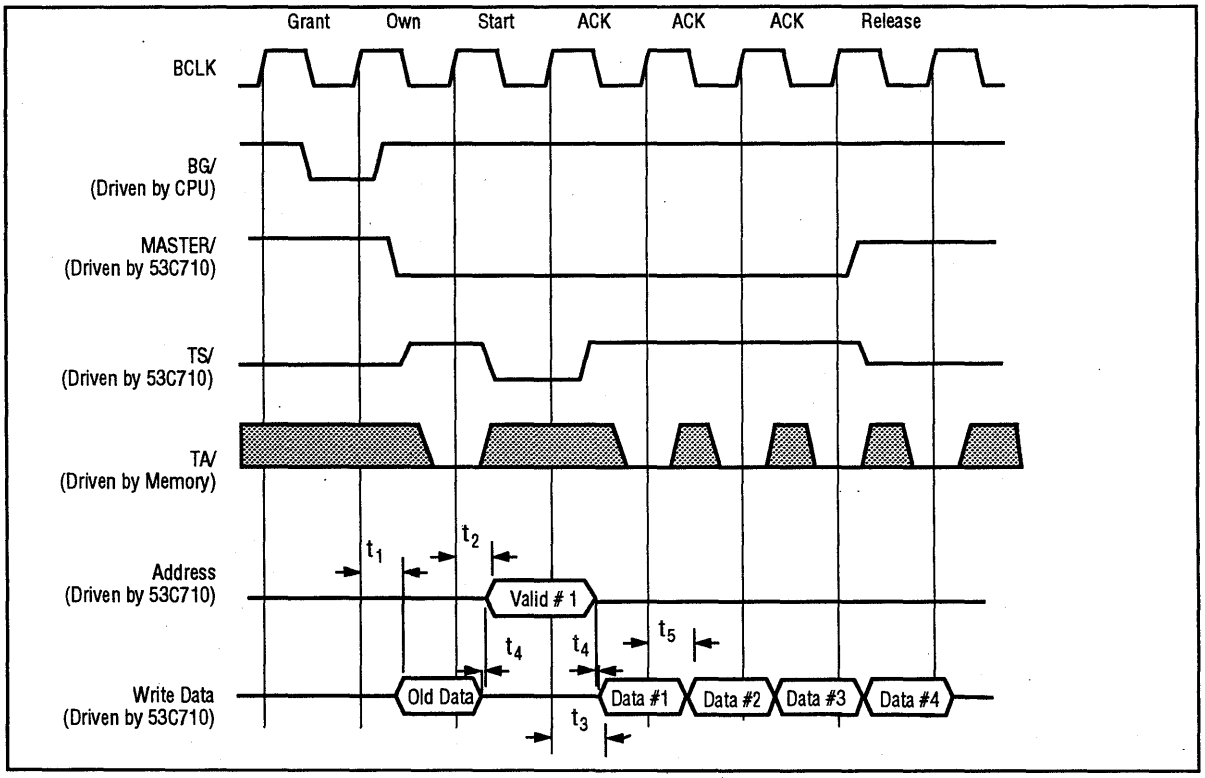


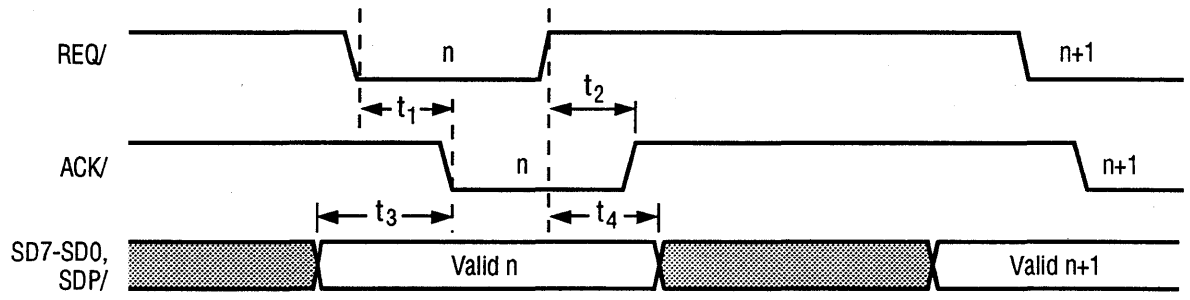
Figure 6-23. Mux Mode Write Cycle (Cache Line Burst)



SCSI Timings

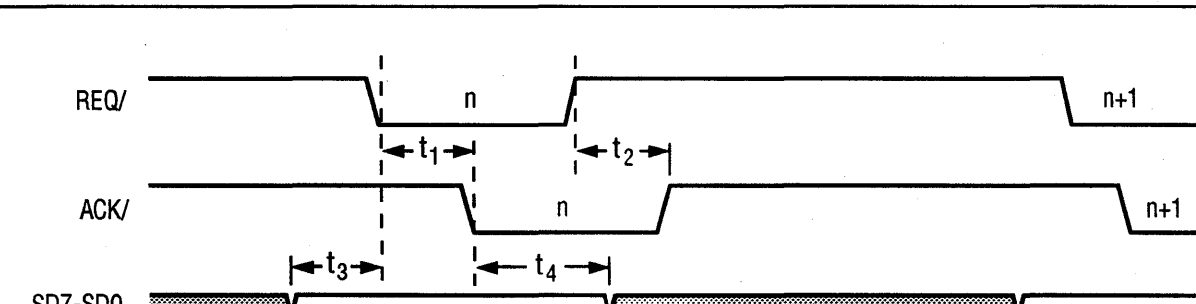
All unspecified SCSI timings meet the ANSI standard for SCSI-2.

Figure 6-24. Initiator Asynchronous Send



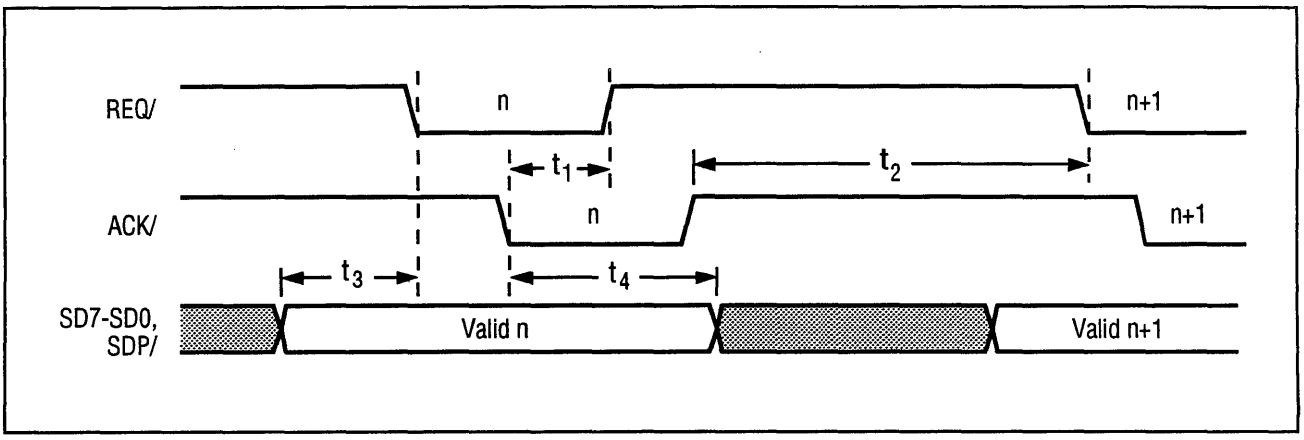
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	55	-	ns
Data hold from REQ/ deasserted	t_4	20	-	ns

Figure 6-25. Initiator Asynchronous Receive



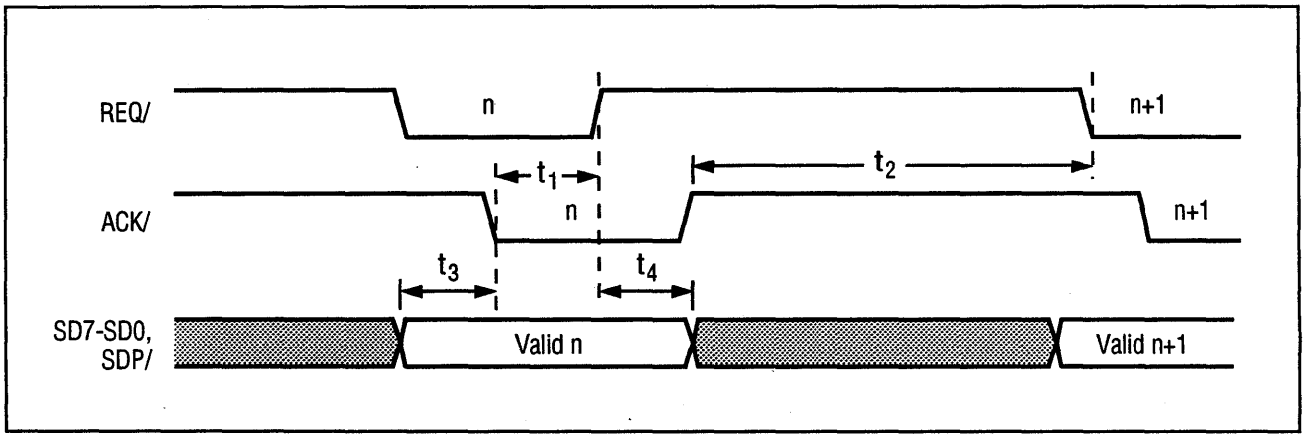
Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	0	-	ns
Data hold from ACK/ deasserted	t_4	0	-	ns

Figure 6-26. Target Asynchronous Send



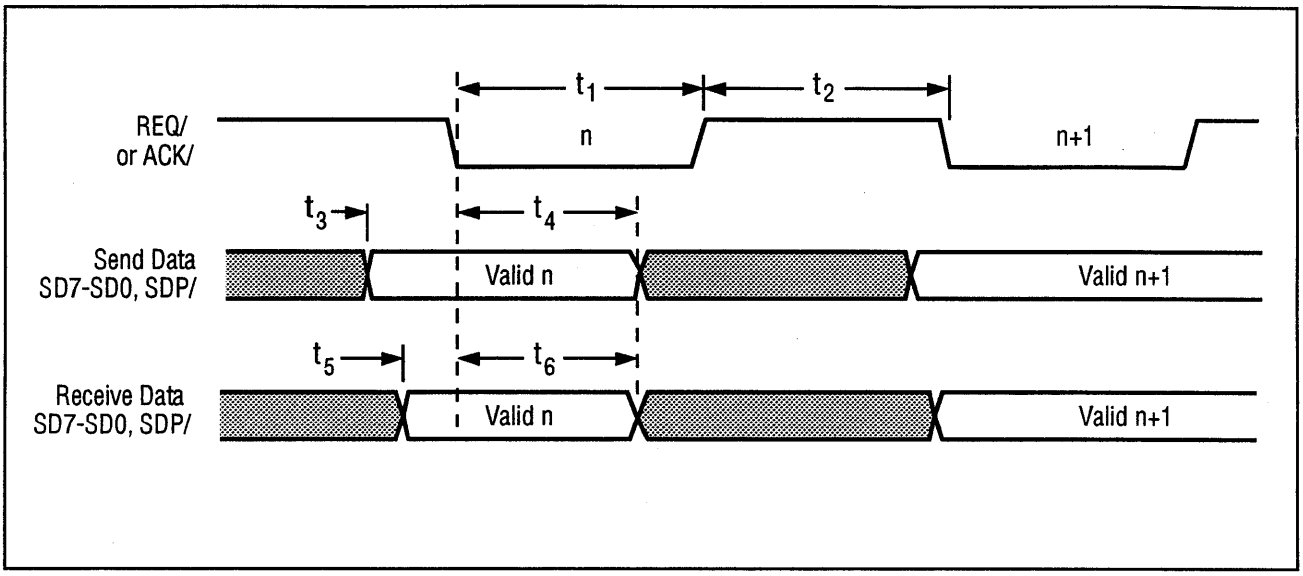
Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

Figure 6-27. Target Asynchronous Receive



Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	0	-	ns
Data hold from REQ/ deasserted	t_4	0	-	ns

Figure 6-28. Initiator and Target Synchronous Transfers



SCSI-1 Transfers (Single Ended, 5.0 MB/s)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	55	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	100	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

SCSI-1 Transfers (Differential, 4.17 MB/s)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	95	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	95	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	84	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	84	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	63	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	110	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

SCSI-2 Fast Transfers (10.0 MB/s, 40 MHz Clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	24	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	45	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

SCSI-2 Fast Transfers (10.0 MB/s, 50 MHz clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	24	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	24	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	40**	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

** Transfer period bits (Bits 6-4 in SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (Bit 7 in SCNTL1) is set.*

*** Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.*

***Note:** For fast SCSI, the Enable Active Negation bit (CTEST0 bit 5) should be set.*

NCR TolerANT™ Active Negation Technology Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH} [1]	Output high voltage	I_{OH} = 2.5 mA	2.5	3.1	3.5	V
V_{OL}	Output low voltage	I_{OL} = 48 mA	0.1	0.2	0.5	V
V_{IH}	Input high voltage		2.0		7.0	V
V_{IL}	Input low voltage	Referenced to V_{SS}	-0.5		0.8	V
V_{IK}	Input clamp voltage	V_{DD} = min; I_I = -20 mA	-0.66	-0.74	-0.77	V
V_{TH}	Threshold, high to low		1.1	1.2	1.3	V
V_{TL}	Threshold, low to high		1.5	1.6	1.7	V
V_{TH} - V_{TL}	Hysteresis		300	350	400	mV
I_{OH} [1]	Output high current	V_{OH} = 2.5 Volts	2.5	15	24	mA
I_{OL}	Output low current	V_{OL} = 0.5 Volts	100	150	200	mA
I_{OSH} [1]	Short-circuit output high current	Output driving low, pin shorted to V_{DD} supply[2]			625	mA
I_{OSL}	Short-circuit output low current,	Output driving high, pin shorted to V_{SS} supply			95	mA
I_{LH}	Input high leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V		0.05	10	µA
I_{LL}	Input low leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5V		-0.05	-10	µA
R_I	Input resistance	SCSI pins [3]		20		M
C_P	Capacitance per pin	Quad Flat Pack Package	6	8	10	pF

NCR TolerANT™ Active Negation Technology Electrical Characteristics, Continued

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_R[1]	Rise time, 10% to 90 %	Figure 6-29	9.7	15.0	18.5	ns
t_F	Fall time, 90% to 10%	Figure 6-29	5.2	8.1	14.7	ns
dV_H/dt	Slew rate, low to high	Figure 6-29	0.15	0.23	0.49	V/ns
dV_L/dt	Slew rate, high to low	Figure 6-29	0.19	0.37	0.67	V/ns
	Electrostatic Discharge	Mil Std 883C; 3015-7	2			KV
	Latch-up		100			mA
	Filter Delay	Figure 6-30	20	25	30	ns
	Extended Filter Delay	Figure 6-30	40	50	60	ns

Note: *These values are guaranteed by periodic characterization.*

[1] *Active Negation outputs only: Data, Parity, REQ, ACK*

[2] *Single pin only; irreversible damage may occur if sustained for 1 second*

[3] *SCSI RESET pin has 10KΩ pull-up resistor*

Figure 6-29. Rise and Fall Time Test Conditions

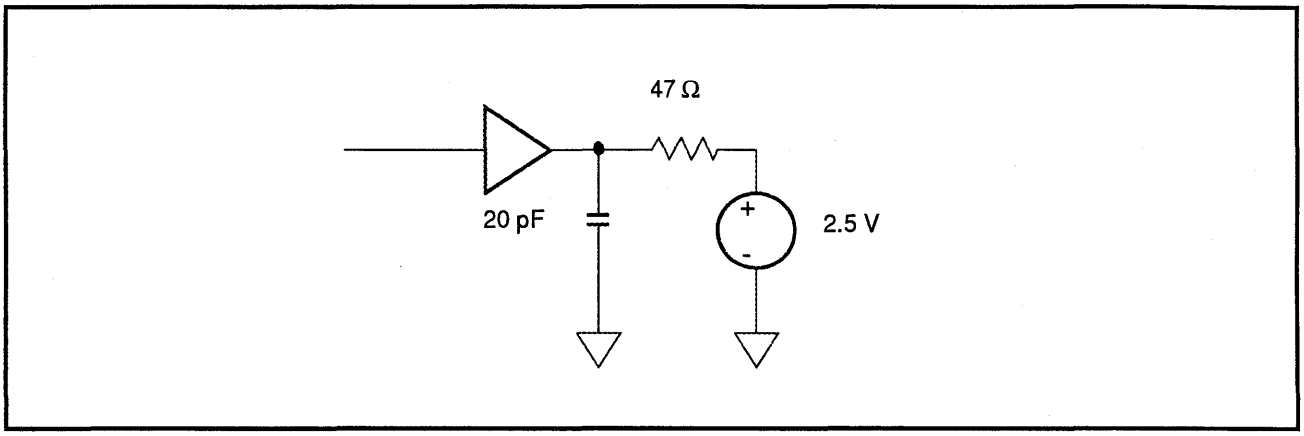
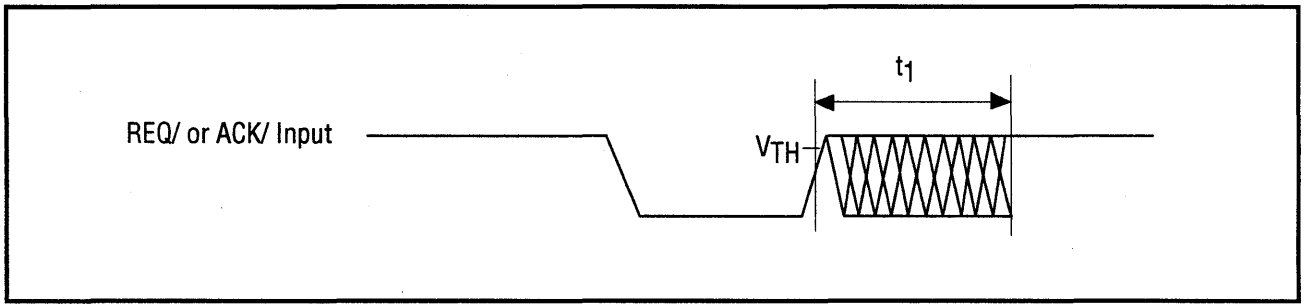


Figure 6-30. SCSI Input Filtering



t_1 = input filtering period, resistor-programmable to either 30 or 60 ns

Figure 6-31. Hysteresis of SCSI Receiver

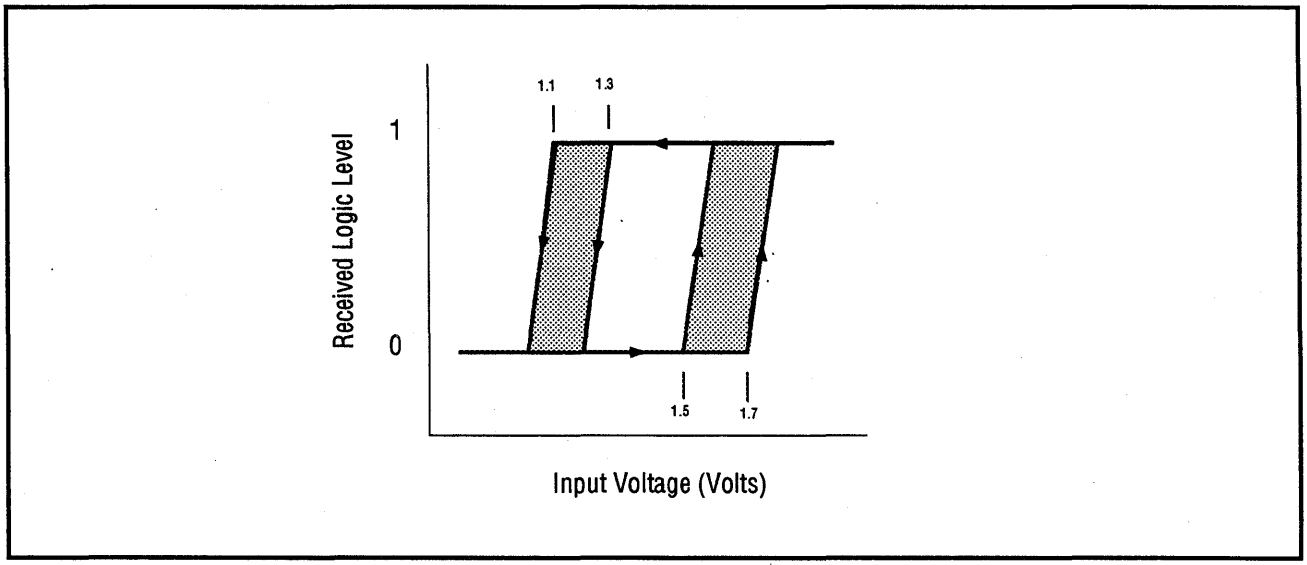


Figure 6-32. Input Current as a Function of Input Voltage

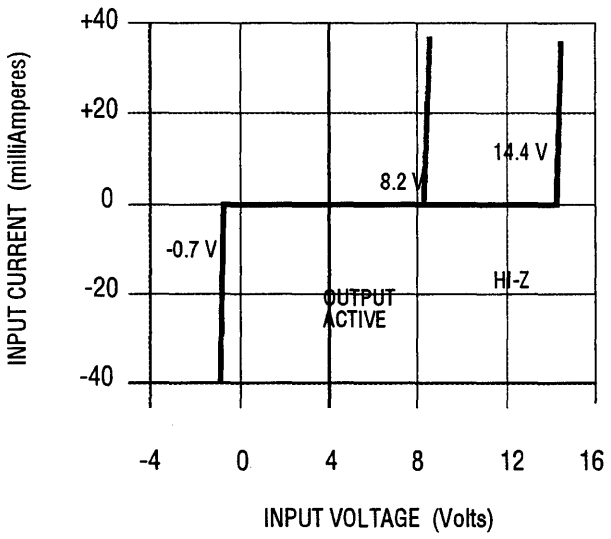
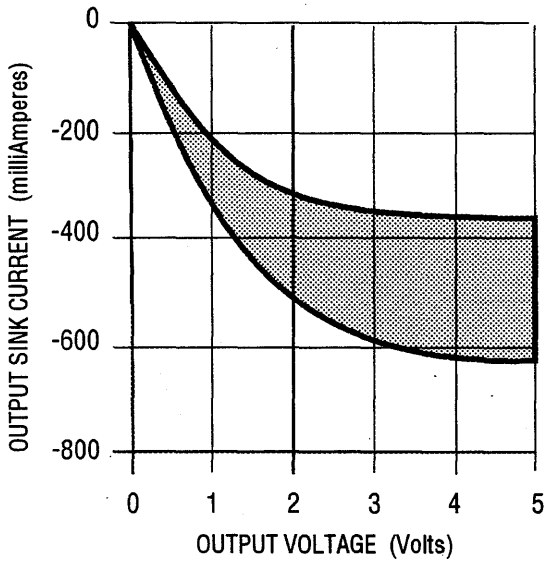
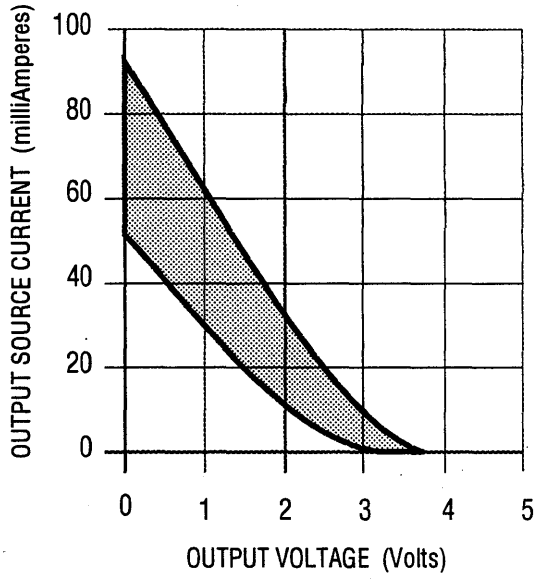


Figure 6-33. Output Current as a Function of Output Voltage



Output Sink Current as a Function of Output Voltage (I_{OL})



Output Source Current as a Function of Output Voltage (I_{OH})

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