Design Considerations Migrating from Intel® 80960RM/RN I/O Processor to Intel® 80303 I/O Processor

Application Note

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1.0 Objective

This document describes both hardware and software issues that should be considered when migrating from the Intel® 80960RM I/O processor or the Intel® 80960RN I/O processor (B-0 step), to the Intel® 80303 I/O processor.

Note: As with any design change, customers should perform thorough validation of their application hardware and software prior to production. See *Intel® i960® RM/RN I/O Processor Specification Update* (273164) for differences between A-0 step and B-0 step.

2.0 Summary

Table 1 summarizes the differences between the I/O processors.

Table 1. Intel® 80960RM/RN I/O Processor and Intel® 80303 I/O Processor Differences

Unit	Intel® 80960RM/RN I/O Processor	Intel® 80303 I/O Processor
Internal Bus	66 MHz/64-bit	100MHz/64-bit
PCI-to-PCI Bridge	• 33 MHz bus • 5 V PCI signaling • None • 128 Bytes upstream delayed read completion queue	• 66 MHz bus • 3.3 V and 5 V PCI signaling • six secondary PCI output clocks • 256 Bytes upstream delayed read completion queue
Memory Controller Unit	• 66 MHz SDRAM • Up to 128 Mbyte of 64-bit SDRAM • 16, 64 Mbit SDRAM • Supports 32- and 64-bit • ECC off option • DCLKOUT for external buffer	• 100 MHz SDRAM • Up to 512 Mbytes of 64-bit SDRAM • 64, 128, 256 Mbit SDRAM • No 32-bit SDRAM support • ECC always on • Four SDRAM output clocks
ATU Inbound Queues	128 Bytes	256 Bytes
AAU	128 Bytes	512 to 1 Kbytes (user programmable)
General Purpose I/O	None	Eight GPIO pins

2.1 Unit Descriptions

2.1.1 Core Processor

The 80303 I/O processor uses the 100 MHz Intel® 80960JT processor core, which is the same core that is used on the 80960RM/RN I/O processor. Therefore, the instruction set for the 80960RM/RN and 80303 I/O processors are the same. However, the internal bus is now 100 MHz verses the 66 MHz bus used on the 80960RM/RN I/O processors.

2.1.2 PCI-to-PCI Bridge

The PCI-to-PCI Bridge supports 64-bit/66 MHz PCI bus, which translates to 528 MB/s performance. If the primary PCI bus is programmed to operate at 66 MHz, the secondary bus is capable of operating at either 33 MHz or 66 MHz. If the primary PCI bus is programmed to operate at 33 MHz, the bridge forces the secondary bus to operate at 33 MHz.

The 80303 I/O processor provides six secondary PCI output clocks. These output clocks can be individually disabled by using the Secondary Clock Disable register listed in Table 5.

A voltage reference pin is provided for both the primary and secondary PCI busses. These pins should be strapped to 5 V or 3.3 V to determine which voltage reference to use. The secondary PCI bus does not have to use the same voltage reference as the primary PCI bus, and visa versa.

For upstream transactions (initiated on the secondary PCI bus), the bridge supports a larger set of queues to accommodate high PCI bandwidth targeted at the primary PCI bus. 516 bytes are dedicated for delayed read completion (DRC) data for upstream reads, organized as two 256 bytes queues and one 4 byte queue.

The bridge also includes VGA address support. To support a VGA device on the downstream bus of the 80303 I/O processor, the PCI-to-PCI bridge is able to recognize and forward VGA addresses on the primary PCI bus to the secondary PCI bus. The bridge does not support VGA palette snooping.

The bridge implements a special downstream memory window to support an external Hot Plug controller. This is enabled by the SPMEM# pin described in Table 2.

2.1.3 Address Translation Unit (ATU)

The primary and secondary inbound read and write queues have been increased from 128 Bytes to 256 Bytes.

2.1.4 Application Accelerator Unit (AAU)

The AAU has been increased from 128 Bytes to 1 KBytes. The user also has the option to configure it as 512 Bytes, by setting ACR.2. This new bit is listed in Table 6.

With the increased queue size it gives up to 15% RAID 5 performance improvements.

2.1.5 Memory Controller Unit (MCU)

The SDRAM interface of the MCU supports 100 MHz technologies and it supports between 32 and 512 Mbytes of 64-bit SDRAM.

32-bit SDRAM is not supported, therefore, the 32BITMEM_EN# pin function is no longer multiplexed with RAD[2], and SDCR.2 is now reserved.

To keep up with SDRAM technology, the memory controller supports 64, 128 and 256 Mbit technology.

ECC is always on, therefore, do not design an 80303 I/O processor based product without ECC implemented, this causes severe system errors. For the 80960RM/RN I/O processor, ECCR.3 can be cleared to disable ECC, but with the 80303 I/O processor, ECCR.3 is reserved.

The MCU provides four SDRAM clock outs, therefore no external clock buffer is required.

2.1.6 DMA Controller Unit

The only thing to note about the DMA, is that it has burst support up to 528 MB/s for both the PCI bus and the 80303 I/O processor internal bus. This is because the 80303 I/O processor now supports 64-bit/66 MHz PCI.

2.1.7 General Purpose I/O

There are eight general purpose I/O pins which can be individually used to control and monitor external devices in the I/O subsystem. Three new registers are defined for the GPI/O and are listed in Table 5.

2.1.8 Package and Ball Out

The 80303 I/O processor uses the same 540-lead HL-PBGA package as the 80960RM/RN. Due to additional pin functions, and to address customer inputs concerning the location of some specific pins, the 80303 I/O processor is not pin-compatible with the 80960RM/RN. For a complete list of all pins, ball out and package dimensions, see the *Intel® 80303 I/O Processor Datasheet* (273358).

The 80303 I/O processor has the same pin functions as the 80960RM/RN I/O processor, in addition to several new pins used to support product enhancements. Table 2 through Table 4 summarize the new pins implemented on the 80303 I/O processor which are not on the 80960RM/RN.

Table 2. Memory Controller Signals

Pin	Description
DCLK[3:0](output)	**SDRAM Output Clock.** Used to provide clocks to external SDRAM memory subsystem. Therefore, no need to have external clock buffers.
RAD[5]/ONCE# (I)	**ONCE**. No longer a dedicated pin, it is multiplexed with flash address/data bit 5 (RAD5).
RAD[2]/SPMEM# (I)	**Flash Address/Data Bus Bit 2 (RAD2)**. Now multiplexed with SPMEM#, which is used to enable a special downstream memory window, to support an external Hot Plug controller. If SPMEM# is asserted during processor initialization, this special downstream memory window opens by default. This window includes the addresses FEC0_0000h through FECF_FFFFh. The 32BITMEM_EN# pin function is no longer available.
SA12 (output)	**SDRAM Multiplexed Address Bus**. Now 13 bits to increase memory addressability.
SA13 (output)	**SDRAM Multiplexed Address Bus**. To provide proper addressing support for 256Mbx16 SDRAM, connect SA13 instead of SA12.

Table 3. Primary and Secondary PCI Bus Signals

Pin	Description
P_M66EN (input)	**Primary PCI Bus 66 MHz Enable**. Input pin indicates speed of primary PCI bus. EBCR.10 reflects the state of this pin.
R_CLKIN (input)	**Reference Input Clock**. Input clock drives internal PCI clocks. Must be connected to R_CLKOUT.
R_CLKOUT (output)	**Reference Feedback Clock**. Must be connected to R_CLKIN and the trace length must match the S_CLK[5:0].
S_CLK[5:0] (output)	**Secondary PCI Bus Output Clocks**. Output pins can be used to drive external logic on the secondary PCI bus.
S_HOLD# (input)	**Secondary PCI Bus Hold**. Input pin handles requests from an external secondary PCI device to acquire the bus. It functions similar to a secondary PCI bus request pin, except when S_HOLDA# is asserted, all other secondary PCI bus activity is halted.
S_HOLDA# (output)	**Secondary PCI Bus Hold Acknowledge**. Output pin indicates to an external secondary PCI device that it can now acquire bus. It functions similar to a secondary PCI bus grant pin, except when S_HOLDA# is asserted, all other secondary PCI bus activity is halted.
S_M66EN (input)	**Secondary PCI Bus 66 MHz Enable**. Input pin indicates speed of Secondary PCI bus. EBCR.11 reflects the state of this pin.

Table 4. Miscellaneous Signals

Pin	Description
GPIO[7:0]	**General Purpose Input/Output**. These pins can be selected on a per pin basis, as general-purpose inputs or outputs.
PWRDELAY (input)	**Power Fail Delay**. Used with external circuitry to enable a reset of memory controller power fail state machine during power up initialization.
VREF_P (input)	**Primary PCI Input Voltage Reference**. Strapped to primary PCI power rail. Used to clamp inputs to either 5 V or 3.3 V.
VREF_S (input)	**Secondary PCI Input Voltage Reference**. Strapped to secondary PCI power rail. It is used to clamp the inputs to either 5 V or 3.3 V.

2.1.9 Memory Mapped Registers (MMR)

Note: Customer must examine each of the following items and make appropriate changes to software.

Table 5 identifies new or changed registers:

Table 5. New or Changed Registers

Register Name	Internal Bus Address	Default Value	Register Description
ATUDID	0000 1202h	5309h	**ATU Device ID**. Identifies Intel® 80303 I/O processor in ATU PCI configuration header.
DIDR	00001002h	0309h	**Device ID**. Identifies 80303 I/O processor in Bridge PCI configuration header.
FBSR1	0000 1558h	0000 0008h	**Flash Bank Size Register 1**. Default value has changed to enable 8Mbyte bank size.
GPID	0000 1720h	0000 0000h	**GPIO Input Data**. Reflects state of appropriate pin.
GPOD	0000 1724h	0000 0000h	**GPIO Output Data**. Write value to be driven out on the appropriate pin.
GPOE	0000171Ch	Pin value during P_RST# assert.	**GPIO Output Enable**. Enables, on a per pin basis, the output value contained in GPOD onto appropriate pin.
RFR	0000 1568h	0000 0000h	**Refresh Interval**. he default value has changed from 300h on 80960RM/RN to 000h on 80303.
SCDR	0000 1056h	0000 0000h	**Secondary Clock Disable**. Used to selectively disable unused secondary PCI output clocks. Default value = all output clocks are enabled.

Table 6 identifies either new or changed bit functions.

Table 6. New or Changed Bit Functions (Sheet 1 of 2)

Bit Position	Internal Bus Address	Default value	Bit function
ACR.2	0000 1800h	0	**512 Byte Buffer Enable**. 0=uses 1Kbyte data buffer. 1= uses 512 Byte data buffer.
BCR.3	0000 103Eh	0	**Bridge Control**. VGA address forwarding enable. 0=VGA addresses are not forwarded.
EBCR.10	0000 1040h	varies w/ pin	**Extended Bridge Control**. Reflects state of P_M66EN pin. (Primary PCI bus speed)
EBCR.11	0000 1040h	varies w/ pin	**Extended Bridge Control**. Reflects state of S_M66EN pin. (Secondary PCI bus speed)
EBCR.12	0000 1040h	varies w/ pin	**Extended Bridge Control**. Reflects state of SPMEM# pin. (Special Downstream Memory Window)
ECCR.3	0000 1534h	reserved	**ECC Control**. Now reserved. ECC always on.
PATUSR.4	0000 1206h	1	**Primary ATU Status**. Indicates extended capabilities use.
PATUSR.5	0000 1206h	1	**Primary ATU Status**. Indicates 66 MHz PCI supported.
PATUSR[10:9]	0000 1206h	10	**Primary ATU Status**. Define slow decode
PIRSR[3:0]	0000 1050h	0	**Interrupt Routing Select**. 0 = P_INTx# and 1 = 80960 core. Opposite of the 80960RM/RN bit definition.
PSR.4	0000 1006h	1	**Primary Status**. Indicates extended capabilities use.
PSR.5	0000 1006h	1	**Primary Status**. Indicates 66 MHz PCI is supported.
PSR[10:9]	0000 1006h	10	**Primary Status**. Define slow decode

Table 6. New or Changed Bit Functions (Sheet 2 of 2)

Bit Position	Internal Bus Address	Default value	Bit function
SBR0.31	0000 150Ch	reserved	**SDRAM Technology**. Now reserved.
SBR0[7:3]	0000 150Ch	00000h	**SDRAM Boundary**. Boundary now defined by 5 bits and bit locations have been shifted.
SBR0[2:0]	0000 150Ch	reserved	Bits now reserved in the SDRAM Boundary register.
SBR1.31	0000 1510h	reserved	**SDRAM Technology**. Now reserved.
SBR1[7:3]	0000 1510h	00000h	**SDRAM Boundary**. Now defined by 5 bits and bit locations have been shifted.
SBR1[2:0]	0000 1510h	reserved	Bits now reserved in SDRAM Boundary register.
SDBR[31:25]	0000 1508h	0	**SDRAM Base Address**. Now 7 bits instead of 10 bits.
SDCR[12:11]	0000 1504h	00	**Address and Control Drive Strength**. Two bits now used to determine four distinct drive strengths.
SDCR[10:9]	0000 1504h	00	**Data Mask Drive Strength**. Two bits now used to determine four distinct drive strengths.
SDCR[8:7]	0000 1504h	00	**Chip Enable 1 Drive Strength**. Two bits now used to determine four distinct drive strengths.
SDCR[6:5]	0000 1504h	00	**Chip Enable 0 Drive Strength**. Two bits now used to determine four distinct drive strengths.
SDCR[4:3]	0000 1504h	00	**Data Bus Drive Strength**. Two bits now used to determine four distinct drive strengths.
SDCR.2	0000 1504h	reserved	**Data Bus Width**. Now reserved. Data bus cannot be 32-bits.
SSR.5	0000 101Eh	1	**Secondary Status**. Indicates 66 MHz PCI supported.

2.1.10 ACPI

The 80303 I/O processor supports ACPI and uses the same implementation as the 80960RM/RN B-0 stepping, except this feature is always on. For information on the ACPI implementation see these documents:

- ACPI Implementation for the *ACPI Implementation for the Intel® i960® RM/RN I/O Processor* (273255) located at: http://developer.intel.com/design/iio/applnots/273255.htm
- *Intel® i960® RM/RN I/O Processor Specification Update* (273164) located at: http://developer.intel.com/design/iio/specupdt/273164.htm

2.1.11 No Change

The following units are exactly the same as the 80960RM/RN I/O processor:

- Messaging Unit
- Performance Monitoring Unit
- I/O Processor Arbitration
- I^2C