HEWLETT hp PACKARD

PDP-11 UNIBUS™ INTERFACE

Model 10275A

OPERATING NOTE/JANUARY 1979

1. DESCRIPTION.

2. The HP Model 10275A PDP-11 Unibus Interface provides a method for easy, fast connection between a Hewlett-Packard Logic Analyzer and a PDP-11 minicomputer. The interface is a quad-height board which plugs directly into the PDP-11 Small Peripheral Control (SPC) slots and allows access to all 56 signals on the bus. Circuits on the interface board generate a clock signal for the Logic State Analyzer, from the asynchronous bus activity which allows address and data information to be captured. In addition, switches on the board provide qualification of Unibus activity so that reads, writes, interrupt vectors, or DMA (Direct Memory Access) transfers can be selectively captured for detailed analysis. Refer to table 1 for complete specifications.

Table 1. Specifications

BUS LOADING: one unit DEC™ load (type 956, P/N DEC 8640 Bus Receiver) with 12 pF maximum shunt capacitance at the edge connector (nominally 6 pF).

GENERAL

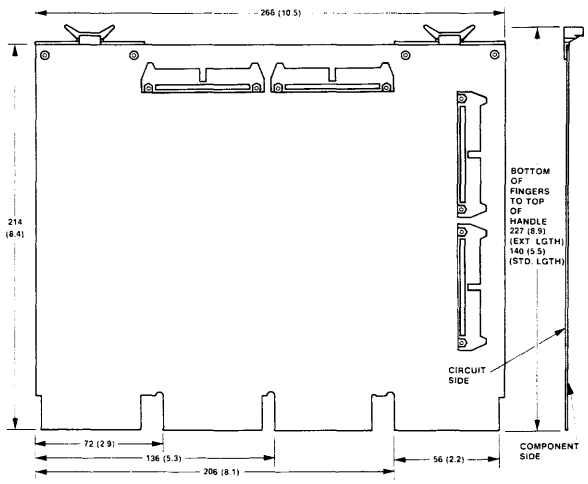
Weight: net, 0.28 kg (10 oz.).

Power: 900 mA maximum at 5 Vdc (nominally 550 mA), supplied by the minicomputer.

Dimensions: see outline drawing.

Operating Environment: temperature, +5°C to +40°C; humidity, to 95% relative humidity at +40°C; altitude, to 4600 m (15 000 ft); vibration, vibrated in three planes for 15 min. each with 0.3 mm (0.015 in.) excursions, 10 to 55 Hz.

RECOMMENDED ACCESSORY: Model 10277 Option 001 General Purpose Probe Interface.



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3. INTERFACE CONNECTIONS.

4. Ribbon cables from the HP Model 10277 (described in paragraph 6) may be connected to the 10275A Interface Board from the minicomputer, or Data and Clock Probe leads can be connected to pins on the interface connectors. Since certain minicomputers can be accessed from only the top or the side, two sets of output connectors (in parallel) are provided on the 10275A.

NOTE

Follow the computer manufacturer's instructions for removal and installation of printed circuit boards when using the Model 10275A.

5. ACCESSORY AVAILABLE.

6. For maximum measurement flexibility, an HP Model 10277 Option 001 General Purpose Probe Interface is available for easy connection to the Unibus interface. Connection to the system under test is accomplished with two ribbon cables between the interfaces, and the Logic Analyzer pods plug directly into the 10277. Changing of electrical configurations for analysis of signals is accomplished by simply changing a plug-in, wire-wrap board in the 10277.

7. APPLICATIONS.

8. SOFTWARE DEVELOPMENT. The HP 10275A combined with a Logic Analyzer becomes a very powerful software debugging tool because it captures program state flow in real time and permits analysis of software timing loops. Once the software is debugged, optimization can be achieved via information available from the Logic Analyzer.

9. SERVICE AND MAINTENANCE. System signals can be accessed quickly by simply plugging the 10275A into an available SPC slot in the minicomputer backplane. Detailed analysis of program execution or the bus arbitration process with elapsed time intervals between events permits rapid troubleshooting with minimum computer downtime when software techniques are marginal or cannot be used.

10. PRODUCTION. The ability to analyze program execution during integration allows you to observe how the system reacts as peripherals are added. By directing the analyzer to trace only the activity to a specific peripheral, problems can be detected and isolated.

Operating Note Part No. 10275-90902
Microfiche Part No. 10275-90802

For More Information, Call Your Local HP Sales/Service Office or, in U.S., East (201) 265-5000. Midwest (312) 677-0400. South (404) 436-6181. West (213) 877-1282. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. In Japan, YHP,1-59-1, Yoyogi, Shibuya-ku, Tokyo, 151.

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11. HARDWARE DEVELOPMENT. During the design of new devices, interactions on the Unibus can be viewed in real time. This permits checking handshake protocol and tracing program execution while recording the times to perform various functions.

12. PRINCIPLES OF OPERATION.

13. The Unibus does not have a distinct clock signal associated with address and data, but operates from asynchronous handshake signals. This allows address and data to be transmitted as fast as a master and slave device can respond. The Unibus is an open-collector, low-true bus. For a data out or write, the address, data, and control signals are made valid on the Unibus, and MSYN (Master Sync) is asserted low (see figure 1), indicating that address, data, and control signals can now be read. When SSYN (Slave Sync) is asserted low, it signals the master that the data has been received and strobed in. Next, the master releases MSYN signalling that address, data, and control signals are no longer valid; in response, SSYN is released high and the bus is returned to its quiescent state. The master can now begin the next bus transaction. For a write (signified by a C1 low), the 10275A interface generates a clock for the Logic Analyzer to strobe in address and data on the asserted edge of MSYN.

14. For a data in or read operation, address and control signals are made valid and MSYN is asserted low by the master. Some time later, the slave puts valid data on the bus and asserts SSYN low. After a deskew time of 75-100 ns from SSYN, the master accepts in data from the slave. Next, address and control signals are released and MSYN is released high. Finally, the data and SSYN are released high, returning the bus to its quiescent state. The 10275A generates a read clock (read signified by C1 high) for the Logic Analyzer to strobe in address and data 75-100 ns after the asserted edge of SSYN. Signals on the 10275A are buffered through DEC-type 8640 inverting buffers (see schematic, figure 3). For this reason, the load presented to the bus is less than or equal to a standard Unibus load. The signals on the 10275A are positive true logic while signals on the Unibus are negative true. All 56 Unibus signals are buffered and made available to the Logic Analyzer at the ribbon cable connector.

15. Since the 10275A can differentiate between reads and writes, Switch S2 permits selection of the transactions to be observed. This and the other qualifier switches on the 10275A allow efficient use of a Logic Analyzer by prequalification freeing all channels for data and address tracing.

16. The function of U7A and U3A is to generate a clock on the occurrence of SSYN asserted +75 ns while C1 is high or on MSYN asserted while C1 is low. The C1 qualifier is applied through U6 along with a qualifier for processor/nonprocessor to be discussed later. When the high-true qualifier is clocked into U3, the result is a high at the Q output which is gated through U1 to cause a clock output to the Logic Analyzer and is delayed and fed back to clear U3. U1 is used to select qualification for interrupts or for reads and writes. U4B, U7B, U5A, and U8A provide the function of constantly monitoring the bus arbitration signals governing processor/nonprocessor operations. U5A latches the fact that a processor or nonprocessor operation is upcoming, and U4B latches this information on BBSY (Bus Busy), signalling that the processor or nonprocessor device has taken control of the bus. U7B and U8A are used to restore U5A and U4B to their initial states. U2B qualifies the bus transaction for processor/nonprocessor operations.

17. Most Logic Analyzers have a Measurement Enable Output available on the rear panel. This signal is routed through the HP Model 10277 to a point on the 10275A labelled "Measurement Enable from Logic Analyzer" ("Trace Enable from Logic Analyzer" on Revision A board) and could be used to halt the processor (with some additional circuitry). A wire-wrap area is provided on the 10275A to allow additional circuitry that may be necessary for special functions.

18. When using a Timing Analyzer such as an HP Model 1615A, probe directly on the output of the 10275A buffers or at the backplane of the Unibus before the signals go through the 10275A. The 10275A ribbon cables and the HP 10277 are designed to pass signals of sufficient quality for logic state analysis, but because of the ribbon cable, cross coupling and ringing that is not actually occurring on the Unibus may be detected using a Timing Analyzer. See table 2 for signal connections.

19. REPLACEABLE PARTS.

20. Replaceable parts are listed in table 3 and illustrated in figure 2. To order a replaceable part from Hewlett-Packard, address the order to the nearest HP Sales/Service Office. Include the interface model number, reference designation of the part and the HP part number. If a part is not listed, provide a complete description of the part, including function and location.

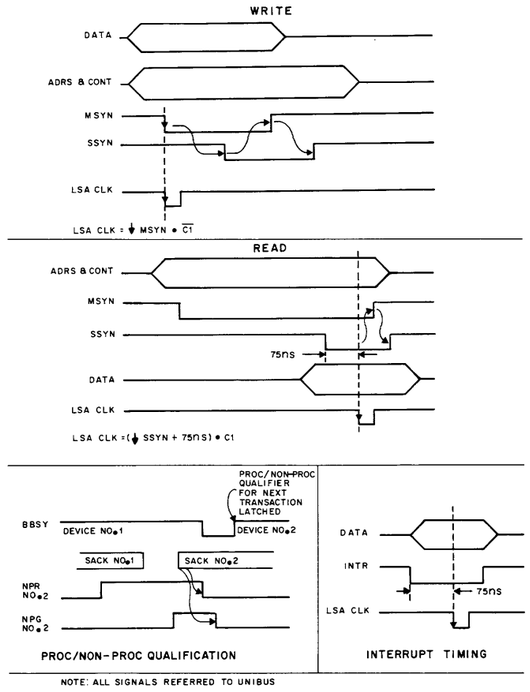


Figure 1. Timing Diagrams

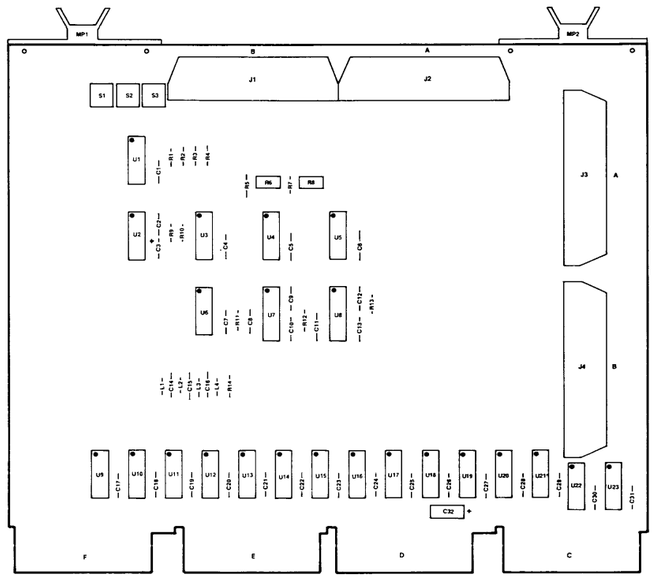


Figure 2. 10275A Component Locations

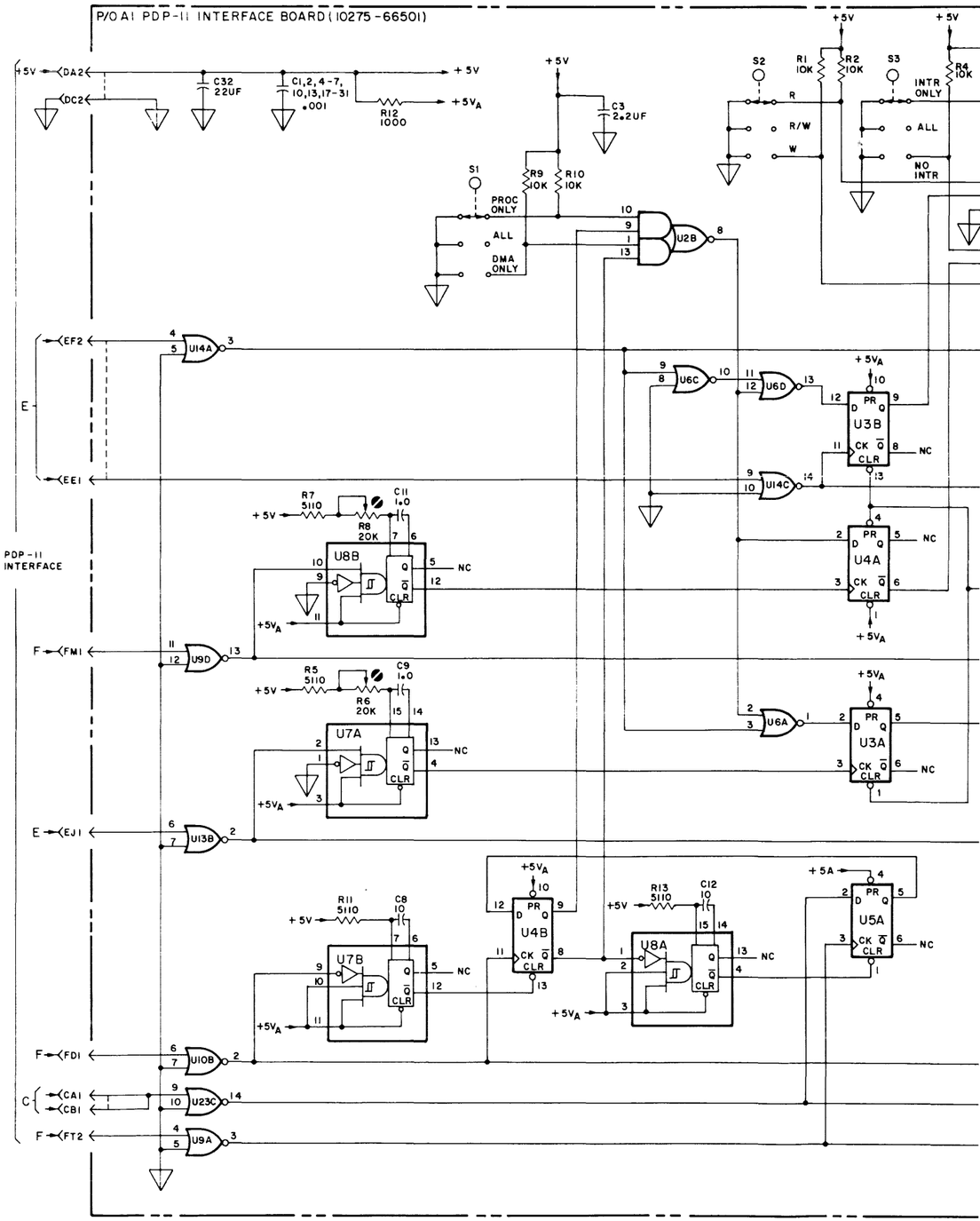
Table 3. Replaceable Parts

Ref Desig	HP Part No.	Qty	Description	Mfr Code	Mfr Part No.
A1	10275-66501	1	BOARD-PDP-11 INTERFACE	28480	10275-66501
C1	0160-3448	23	CAPACITOR-FXD 1000 PF ±10% 1KVDC CER	56289	CO16B102F471KS25-CDH
C2	0160-3448		CAPACITOR-FXD 1000 PF ±10% 1KVDC CER	56289	CO16B102F471KS25-CDH
C3	0180-2255	1	CAPACITOR-FXD 2.2 UF ±20% 20VDC TA	00656	CNI-NPO-8.2PF ±0.25PF
C4 THRU C7	0160-3448		CAPACITOR-FXD 1000 PF ±10% 1KVDC CER	56289	CO16B102F471KS25-CDH
C8	0160-2257	2	CAPACITOR-FXD 10PF ±5% 500VDC CER	04222	CNI-NPO-10PF ±5%
C9	0160-2236	2	CAPACITOR-FXD 1PF ±.25PF 500 VDC CER	04222	CNI-NPO-1.0PF ±.25%
C10	0160-3448		CAPACITOR-FXD 1000 PF ±10% 1KVDC CER	56289	CO16B102F471KS25-CDH
C11	0160-2236		CAPACITOR-FXD 1PF ±.25PF 500 VDC CER	04222	CNI-NPO-1.0PF ±.25%
C12	0160-2257		CAPACITOR-FXD 10PF ±5% 500VDC CER	04222	CNI-NPO-10PF ±5%
C13	0160-3448		CAPACITOR-FXD 1000PF ±10% 1KVDC CER	56289	CO16B102F471KS25-CDH
C14 THRU C16	0160-2261	3	CAPACITOR-FXD 15PF ±5% 500VDC CER	04222	CNI-NPO-15PF ±5%
C17 THRU C31	0160-3448		CAPACITOR-FXD 1000 PF ±10% 1 KVDC CER	56289	CO16B102F471KS25-CDH
C32	0180-0228	1	CAPACITOR-FXD 22UF ±10% 15VDC TA	56289	150D226X9015B2-DYS
F1	2110-0046	1	FUSE .5A 125V NORM-BLO .25 X .27 (NOT ON REV A BOARDS)	71400	GMW-1/2
J1 THRU J4	1251-3782	4	CONNECTOR 40-PIN M RECTANGULAR	76381	3432-1002
L1	9100-2259	2	COIL-MLD 1.5UH 10% Q=32 .095D×.25LG	02172	09-4436-2K
L2	9100-2261	2	COIL-MLD 2.7UH 10% Q=40 .095D×.25LG	02172	09-4436-5K
L3	9100-2261		COIL-MLD 2.7UH 10% Q=40 .095D×.25LG	02172	09-4436-5K
L4	9100-2259		COIL-MLD 1.5UH 10% Q=32 .095D×.25LG	02172	09-4436-2K
MP1	0403-0283	2	PC BOARD PULLER	28480	0403-0283
MP2	0403-0283		PC BOARD PULLER	28480	0403-0283
R1 THRU R4	0684-1031	6	RESISTOR-10K 10% .25W FC TC=—400+700	01121	CB1031
R5	0757-0438	4	RESISTOR-5.11K 1% .125W F TC =0±100	07716	CEA-993
R6	2110-3353	2	RESISTOR-TRMR 20K 10% C SIDE ADJ 1 TRN	73138	72-147-0
R7	0757-0438		RESISTOR-5.11K 1% .125W F TC =0±100	07716	CEA-993
R8	2100-3353		RESISTOR-TRMR 20K 10% C SIDE ADJ 1 TRN	73138	72-147-0
R9	0684-1031		RESISTOR-10K 10% .25W FC TC=—400+700	01121	CB1031
R10	0684-1031		RESISTOR-10K 10% .25W FC TC=—400+700	01121	CB1031
R11	0757-0438		RESISTOR-5.11K 1% .125W F TC =0±100	07716	CEA-993
R12	0684-1021	1	RESISTOR-1K 10% .25W FC TC=—400+600	01121	CB1021
R13	0757-0438		RESISTOR-5.11K 1% .125W F TC =0±100	07716	CEA-993
R14	0684-4711	1	RESISTOR-470 10% .25W FC TC=—400+600	01121	CB4711
S1 THRU S3	3101-2348	3	SWITCH-SPDT	28480	3101-2348
U1	1820-0691	1	IC-GATE TTL S AND-OR INV	01295	SN74S64N
U2	1820-1158	1	IC-GATE TTL S AND-OR INV DUAL 2-INP	01295	SN74S51N
U3 THRU U5	1820-0693	3	IC-FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74
U6	1820-1322	1	IC GATE TTL S NOR QUAD 2 INP	01285	SN74S02
U7	1820-0579	2	IC-MV TTL MONO STBL DUAL RETRIG	01295	SN74123N
U8	1820-0579		IC-MV TTL MONO STBL DUAL RETRIG	01295	SN74123N
U9 THRU U23	1820-2178	15	IC-8640 QUAD NOR UNIFIED BUS RCVR	27014	DS8640

Table 2. Control Signal Connections 10275A/10277

UNIBUS		
PIN NO.	**A**	**B**
1	PB	GND-ME
2	PA	GND-P4
3	INTR	MEAS ENBL
4	—	GND-P3
5	SACK	CLOCK
6	HALT REQ	GND-CLK
7	—	D15
8	LTC	GND-P2
9	ACLO	D14
10	HALT-GRT	GND-P1
11	DCLO	D13
12	GND	A15
13	A17	D12
14	+5V	A14
15	—	D11
16	BG7	A13
17	A16	D10
18	BG6	A12
19	—	D9
20	BG5	A11
21	INIT	D8
22	BBSY	A10
23	NPG	D7
24	—	A9
25	NDR	D6
26	GND	A8
27	BG4	D5
28	+5V	A7
29	BR4	D4
30	—	A6
31	MSYN	D3
32	—	A5
33	C1	D2
34	C0	A4
35	SSYN	D1
36	BR7	A3
37	—	D0
38	BR6	A2
39	—	A1
40	BR5	A0

— Indicates users spare



P/O A1 PDP-11 INTERFACE BOARD (10275-66501)

PDP-11 INTERFACE

+5V DA2 DC2 C32 22UF C1,2,4-7, 10,13,17-31 .001 +5V +5VA R12 100Ω

+5V C3 2.2UF S1 PROC ONLY ALL DMA ONLY R9 10K R10 10K U2B

S2 R R/W W S3 INTR ONLY ALL NO INTR R1 10K R2 10K R4 10K R3 10K

U1 CLOCK L1 1.5UH

+5V 14 A

1 POD GNDS B2-POD 4 B4-POD 3 B6-CLOCK B8-POD 2 B10-POD 1 B

5

E EF2 U14A EE1

U6C U6D U3B C14 15 C15 15 C16 15 L2 2.7UH L3 2.7UH

33 CI

U14C MSYN 31

U8B R7 511Ω R8 20K C11 1.0 NC

U4A L4 1.5UH R14 470 +5V +5VA U6B U2A

F FMI U9D INTR 3 A TO LOGIC ANALYZER

U7A R5 511Ω R6 20K C9 1.0 NC

U6A U3A NC

E EJ1 U13B SSYN 35

26

U4B U8A U5A R11 511Ω C8 10 R13 511Ω C12 10 +5A NC

U7B NC

F FDI U10B BBSY 22

C CA1 CB1 U23C NPG 23

F FT2 U9A SACK 5

P/O A1

C

CS2 CR2 CU2 CT2 CN2 CP2 CV2 CM2 CL2 CK2 CJ2 CH2 CH1 CF2 CE2 CD2 CV1 CN1 CD1 CP1 CR1 CC1 CS1 EP2 EN2 ER1 EP1

U19A U18D U20C U18A U21A U21C U22A U22C U18B U23B U19D U19B U12B U11C U19C U18C U20A U21B U21D U22B U22D U23A U20D U10B U23D U11D U11A

D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 ACLO DCLO LTC HALT REQ HALT GRT PA PB A07 A08 A09 A10

37 35 33 31 29 27 25 23 21 19 17 15 13 11 9 7 9 11 8 6 10 2 1 28 26 24 22

B A

TO LOGIC AN

LTC, HALT REQ, HALT GRT ARE USED ONLY ON PDP 11/04 AND PDP 11/34

IC SUPPLY CONFIGURATIONS

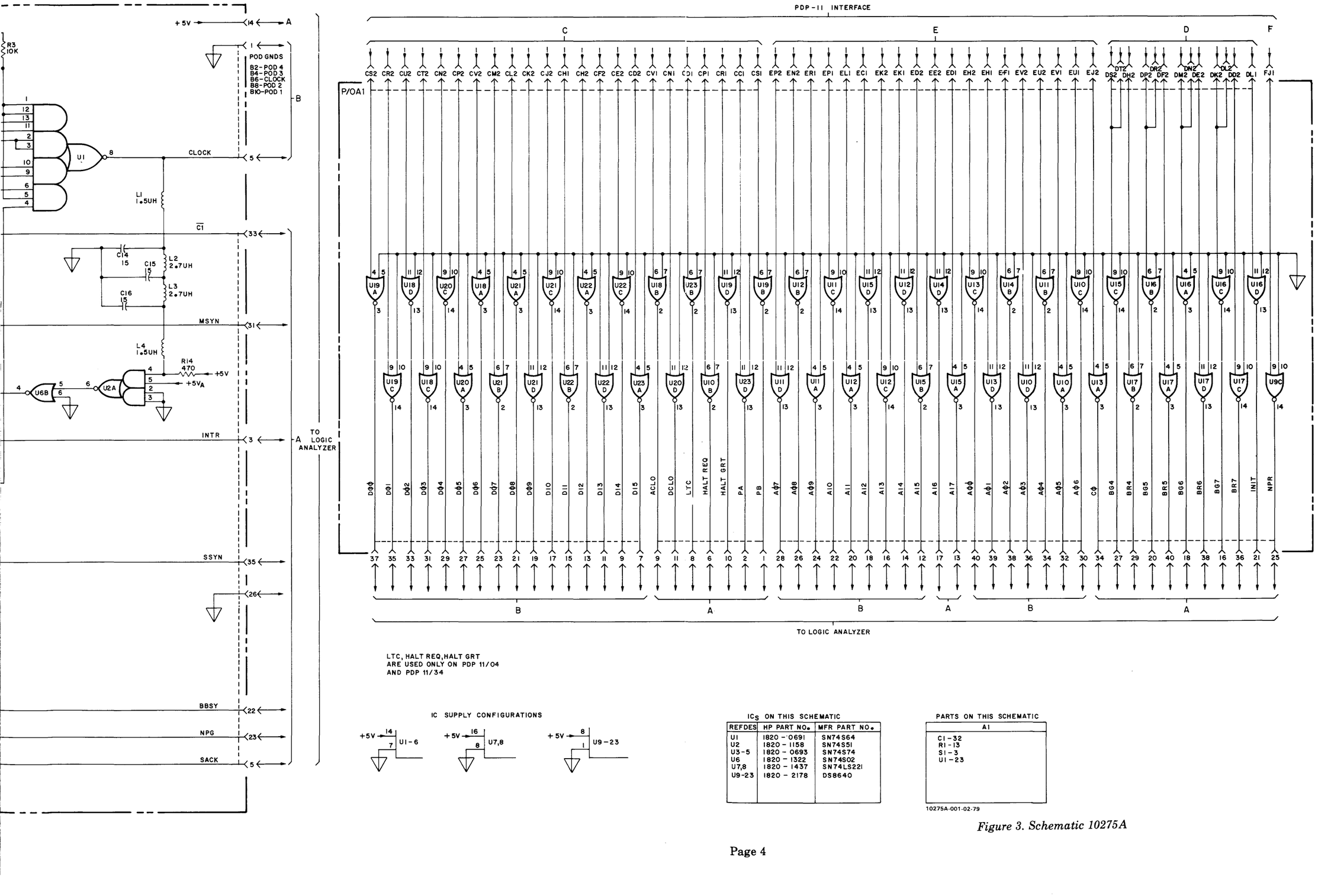
+5V 14 7 U1-6

+5V 16 8 U7,8

+5V 8 1 U9-23

ICs ON THIS SCHEMATIC

REFDES	HP PART NO.	MFR P
U1	1820-0691	SN74
U2	1820-1158	SN74
U3-5	1820-0693	SN74
U6	1820-1322	SN74
U7,8	1820-1437	SN74
U9-23	1820-2178	DS86



ICs ON THIS SCHEMATIC

REFDES	HP PART NO.	MFR PART NO.
U1	1820-0691	SN74S64
U2	1820-1158	SN74S51
U3-5	1820-0693	SN74S74
U6	1820-1322	SN74S02
U7,8	1820-1437	SN74LS221
U9-23	1820-2178	DS8640

PARTS ON THIS SCHEMATIC

A1
C1-32
R1-13
S1-3
U1-23

10275A-001-02-79

Figure 3. Schematic 10275A

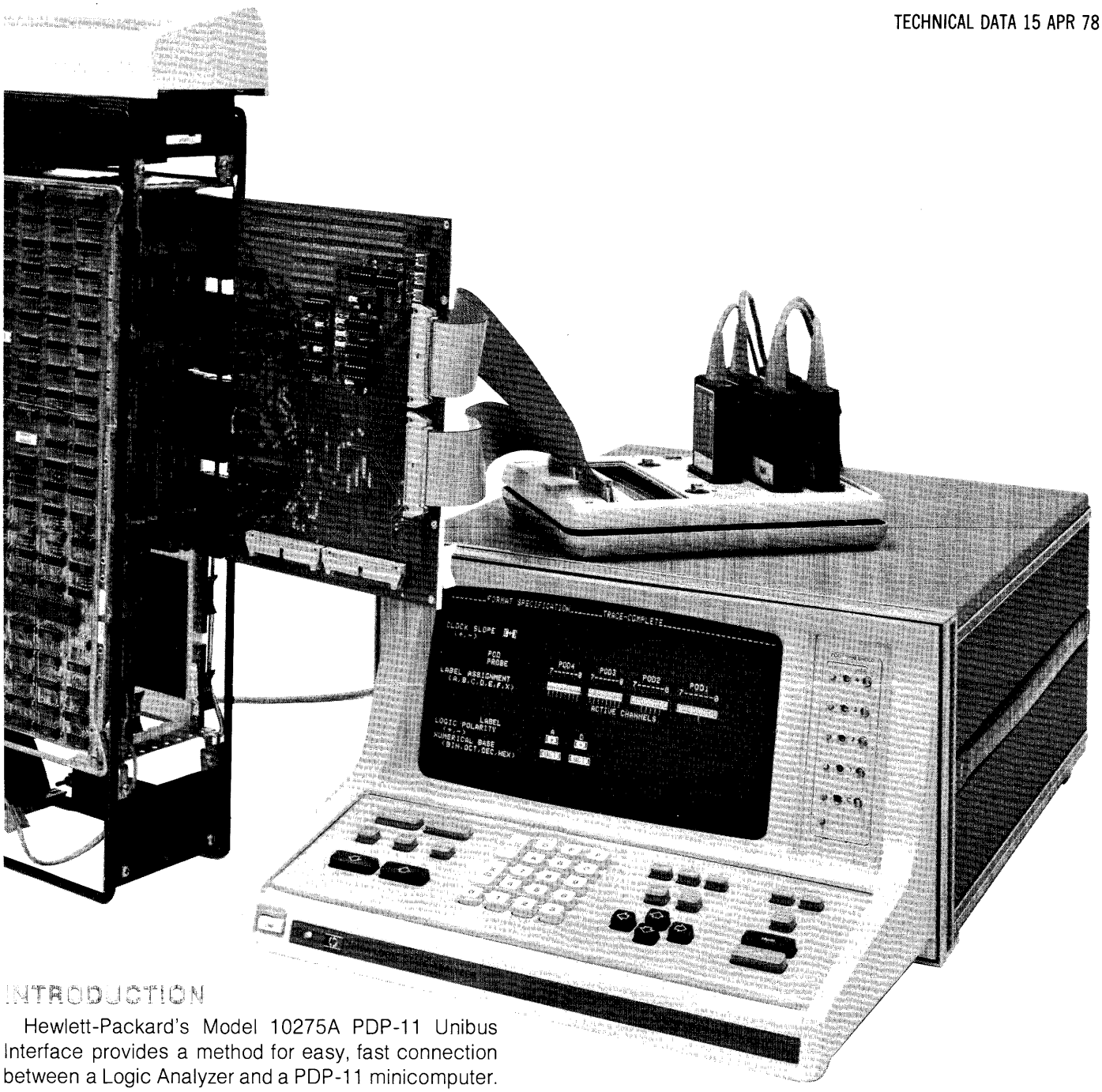
HEWLETT hp PACKARD

PDP-11 UNIBUS INTERFACE

for Hewlett-Packard Logic Analyzers

Model 10275A

TECHNICAL DATA 15 APR 78



INTRODUCTION

Hewlett-Packard's Model 10275A PDP-11 Unibus Interface provides a method for easy, fast connection between a Logic Analyzer and a PDP-11 minicomputer. The 10275A interface is a quad-height board which plugs directly into the PDP-11 Small Peripheral Control (SPC) slots and allows access to all 56 signals on the bus. Circuits on the interface board generate a clock signal for the Logic State Analyzer, from the asynchronous bus activity which allows address and data information to be captured. In addition, switches on the board provide qualification of unibus activity so that reads, writes, interrupt vectors, or DMA transfers can be selectively captured for detailed analysis.

The analyzer probes may be connected to the interface board from the side or the rear of the minicomputer. The probe leads can be connected to pins on the interface board connectors.

For More Information, Call Your Local HP Sales Office or, in U.S., East (301) 948-6370. Midwest (312) 255-9800. South (404) 955-1500. West (213) 877-1282. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. —In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. —In Japan, YHP 1-59-1, Yoyogi, Shibuya-ku, Tokyo, 151. —In Canada, 6877 Goreway Drive, Mississauga, Ontario, L4V-IM8 Canada—

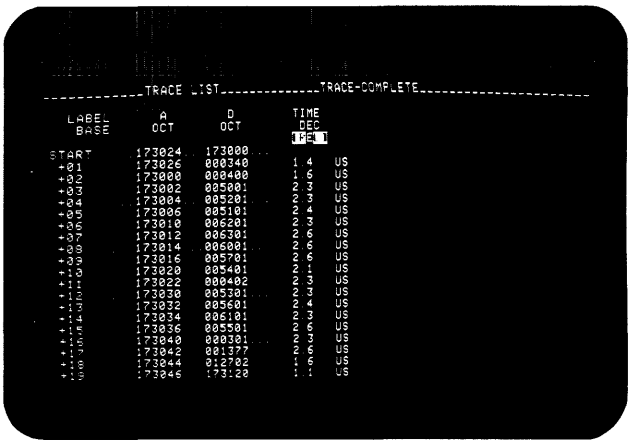


Figure 1. Direct interface to any PDP-11 Unibus and the ability to monitor 32 bits of address and data makes it easy to analyze program execution. This trace is the bootstrap of a PDP-11/04 which displays the bootstrap program counter vector 173000_8 being located at address 173024_8.

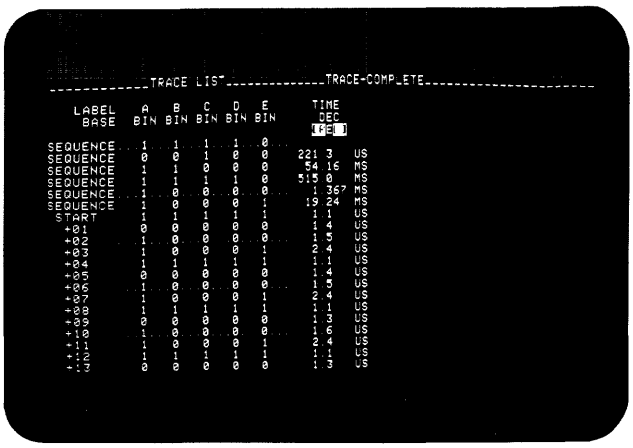


Figure 2. Time interval analysis of asynchronous events is possible by using a sequential triggering specification and an external 10 MHz clock. In this trace, the time intervals between handshake events or bus arbitration are determined between sequence triggers with a resolution of 100 ns.

For maximum measurement flexibility, a Model 10277A General Purpose Probe Interface is available for easy connection to the unibus interface. Connection to the system under test is accomplished with two ribbon cables between the interfaces; and the analyzer pods plug directly into the 10277A. Changing of electrical interface configurations for analysis of, for example, address and data flow or bus arbitration of handshake signals is accomplished by simply changing a wire-wrap board in the 10277A.

APPLICATIONS

Service and Maintenance

System signals can be accessed quickly by simply plugging the interface module into the minicomputer backplane. Detailed analysis of program execution or the bus arbitration process with elapsed time intervals between events permits rapid troubleshooting with minimum computer downtime when software techniques are marginal or cannot be used.

Production

The ability to analyze program execution during system integration allows you to observe how the system reacts as peripherals are added. Or, by directing the analyzer to trace only the activity to a specific peripheral, you can quickly determine what is causing a problem.

Front cover photo shows a Model 10275A interface board plugged into a minicomputer. The interface board is normally inside the computer however, for clarity in the photo, the 10275A is on an extender board. The 1610A Format Specification defines 16 bits of address and data to be displayed in octal base (figure 1). Also shown is a general purpose interface Model 10277A, which allows quick connection of the Analyzer probes to the 10275A through ribbon cables.

Engineering

During the design of new unibus interfaces, you can view program execution in real time. This allows you to check the actual handshake process or measure time intervals to evaluate peripheral access time which can reduce design time.

SPECIFICATIONS

BUS LOADING: one unit DEC load (type 956, P/N DEC 8640 Bus Receiver) with 12 pF maximum shunt capacitance at the edge connector (nominally 6 pF).

GENERAL

Weight: net, 0.28 kg (10 oz); shipping, 0.6 kg (1 lb 5 oz).

Power: 900 mA maximum at 5 Vdc (nominally 550 mA), supplied by the minicomputer.

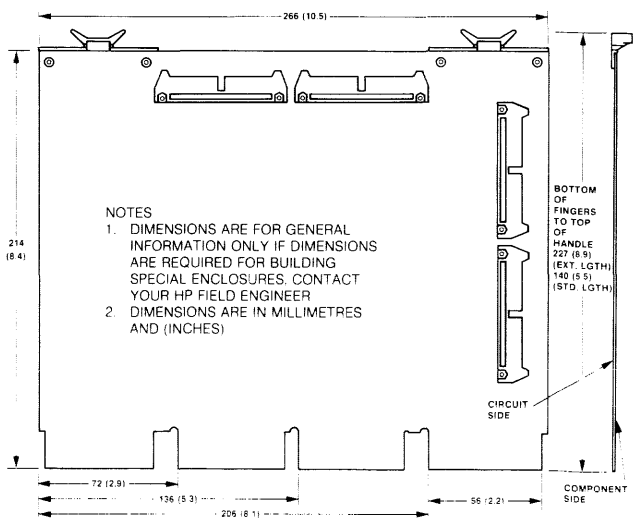
Dimensions: see outline drawing.

Operating Environment: temperature, +5°C to +40°C; humidity, to 95% relative humidity at +40°C; altitude, to 4600 m (15 000 ft); vibration, vibrated in three planes for 15 min. each with 0.3 mm (0.015 in.) excursions, 10 to 55 Hz.

Price: Model 10275A PDP-11 Unibus Interface ..... $300.

RECOMMENDED ACCESSORY: Model 10277A General Purpose Probe Interface.

Prices apply only to domestic U.S. customers.



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