



# THE FIRST IN-CIRCUIT VERIFIER FOR PROGRAMMABLE GATE ARRAYS.



# PROGRAMMABLE GATE ARRAY TECHNOLOGY.

In 1985, Xilinx<sup>™</sup> Corporation introduced a new type of ASIC to fill the gap between programmable logic devices (PLDs) and gate arrays: programmable gate arrays (PGAs). Like PLDs, PGAs can be programmed by the user, making them quick and inexpensive to customize. Like gate arrays, PGAs contain undedicated logic and have a flexible inter-

connection scheme for custom placement and routing. PGAs combine the benefits of userconfigurability with the level of integration comparable to mediumsized gate arrays.

The Xilinx PGA is called a Logic Cell<sup>™</sup> Array (LCA<sup>™</sup>) and is second-sourced by Advanced Micro Devices<sup>™</sup>. The LCA architecture is based on an array of configurable

logic blocks containing both storage and combinatorial logic elements. These configurable logic blocks are surrounded by a ring of I/O blocks for I/O pin buffering and storage. Both sets of blocks are interconnected with a grid of transistor switches configured-"programmed"-by data stored in the LCA's internal RAM. The LCA can be easily "reprogrammed" by downloading new configuration data, at any time. For example, during prototyping you can repeatedly download new design iterations as troubleshooting progresses. Or you can download test programs into the LCA to test your entire board, and then reconfigure the LCA to perform the intended design function.





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MESA-I was implemented entirely with LCAs, the first programmable gate arrays. So, Data I/O has a first-hand understanding of PGA design issues. And by taking advantage of the reprogrammability of RAM-based PGAs, we can offer easy hardware updates of MESA-I through software.



The 68- or 84-channel patented\*\* probe precisely controls impedance to guarantee signal integrity.

#### **NEW TOOLS FOR NEW TECHNOLOGIES.** Imple-

menting your design with PGAs can get complex products to market faster with less risk. But like every technology advance, PGAs are more complex to troubleshoot than their programmable predecessors. With their high level of integration, most of the signals and registers are internal and not directly observable. PGAs require new tools for design verification and troubleshooting. You must be able to:

#### SEE

See what is going on inside the device while it is operating in a target system.

#### CHANGE

Change stimulus to the device to isolate problems and observe the consequences.

#### EXPERIMENT

Experiment with design changes and observe the results.

# INTRODUCING MESA-I: THE FIRST IN-CIRCUIT VERIFIER FOR PROGRAMMABLE GATE ARRAYS.

MESA-I from Data I/O® is more than a new product. It's a new concept, defining a whole new category of instrumentation. MESA-I is the world's first in-circuit verifier, incorporating all the functions you need for troubleshooting programmable gate arrays, specifically Logic Cell Arrays (LCAs).

MESA-I pioneers new troubleshooting territory with its novel Shadow\* LCA concept. This allows you to run two LCA devices in parallel; the Target LCA in your target system, and the Shadow LCA in the MESA-I pod. Because the Shadow LCA receives all target system stimulus, but functions independently of your target system, you have the flexibility to observe, modify, and experiment with your LCA design.

MESA-I derives its name from the broad functions it performs. Like a modeler, it uses your device for design verification. Like an emulator, it gives you the device's true internal register data. Like a simulator, it allows you to use functional vectors to step through your design. And like a logic analyzer, it acquires pin states, and displays them with user-formattable software. With MESA-I you can verify your design in-circuit, using real system signals. MESA-I relieves you of the burden of generating stimulus; the target system generates it. This is especially helpful for complex systems that produce a wide range of stimulus. Create a design, download it to an LCA, and run it in-circuit: MESA-I provides you with immediate feedback to help shorten the overall development cycle.

The easily changeable structure of LCAs, together with MESA-I's unique shadow concept, gives you the freedom to experiment with your design while it is running in your target system. Verify that the configuration has occurred correctly, and watch what happens inside the LCA as it runs. Change and control stimulus from the target system by isolating specific signals and forcing them to various states.

MESA-I can also be used as an "instant breadboard," independent of a target system. Stimulate a design loaded in the Shadow LCA with functional vectors created in MESA-I software. MESA-I becomes an experimentation platform that can help you produce more creative, higher-quality designs.

#### **MESA-I ANSWERS ESSENTIAL LCA QUESTIONS.**

- Is my design downloaded correctly into the LCA?
- How can I see inside the LCA?
- How can I get a history of my design's operation?
- How can I test my design without using a simulator?
- How can I single-step my clock?
- How can I get a snapshot of my design while it's running?
- How can I make fault isolation easier?
- Do I have to burn a new EPROM every time I change my design?
- How can I experiment with my design before I have a board?



\* Data I/O patent pending\*

\*\* Tektronix patent

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SEE INTERNAL STATES: MESA-I OPENS A WINDOW INSIDE YOUR LCA DESIGN. MESA-I gives you three ways to view internal register states and external pins: random-sampled readback, synchronous readback, and real-time dynamic viewing.

In random-sampled readback, MESA-I samples and stores the contents of internal registers on either the Shadow or Target LCA while the target system is running. Because of the internal structure of the LCA, this type of readback is asynchronous to the real-time operation of the system, showing you register/pin activity. You



can observe the operation of a pseudo-static circuit, or look for stuck bits in a fast-changing design.

In synchronous readback, the Shadow and Target LCAs are loaded with the same design. Since both LCAs receive the same stimulus, they operate in parallel and the contents of each are identical.

When an external trigger occurs, MESA-I "freezes" the Shadow LCA, creating a chipwide "snapshot" of all pins and internal registers—a mirror of the Target LCA. This type of readback helps you examine register states in relation to one another at a given moment.

Real-time dynamic viewing is easier with MESA-I, too. One advantage of LCAs is that their internal nodes can be routed out to external pins for real-time viewing. Unfortunately, this is often difficult in the target system where external pins are at a premium or inaccessible, or where an LCA is so full that there is no room for more routing.

With two LCAs operating in parallel, MESA-I overcomes these problems. You can easily route out signals by removing circuitry and making outputs available on the Shadow LCA without affecting the target system. Attach a logic analyzer or oscilloscope to the square pins we provide, and capture a history of a design's internal operation.

# CHANGE

**CHANGE ANY SIGNAL: MESA-I GIVES YOU TOTAL CONTROL.** MESA-I's instrument-per-pin architecture lets you control your design pin-by-pin. For fast fault isolation, disconnect one or more suspect signals from the Shadow LCA, then use MESA-I to force pins to the desired states. The target system continues to run normally and all stimulus except the forced signals continue to be transmitted to the Shadow LCA. You can also use MESA-I software to force pins on both the Shadow and Target LCAs.

Forced pins can be used in conjunction with the asynchronous, synchronous, or real-time dynamic functions for full control of the design being observed.

Test your design by applying a series of forced pin states. Single step a clock line. Change the state of an input to the Shadow LCA. Stimulate a function that the target system is not yet providing. Or, verify that another component in the target system is operating correctly. If, by forcing signals, the circuit begins to work properly, you know you have isolated the problem.

MESA-I also gives you control of downloading configuration files to the Target LCA. Files can be taken from MESA-I or the target system. If loaded from the target system, the LCA design can be verified by reading back the configuration data and comparing it to the design file, all with a click of a mouse.

#### EXPERIMENT

**EXPERIMENT WITH YOUR DESIGNS: MESA-I GIVES YOU TOTAL FLEXIBILITY.** With MESA-I, you can step your design through a series of states using a sequence of functional verification vectors. Forced vectors work much the same way as forced pins, except that all pins are disconnected from the target system's stimulus and placed under the control of the MESA-I software. These are not the typical extensive set of vectors used for gate array simulation, but rather a small number aimed at verifying a specific function.

With the Target LCA out-of-circuit, MESA-I serves as an instant breadboard

> To keep bulk, weight, and cords to a minimum, the internal power supply has been eliminated. MESA-I runs off your personal computer's power supply.

Suspend the MESA-I pod overhead for convenient access to your board. With its nonconductive coating, the MESA-I pod can also be laid directly on top of your open design.

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for quick prototyping. Verify an LCA design before the system board is available, or experiment with design alternatives. Use the function with full vectors, or partial vectors plus external stimulus (e.g., a function generator). Or, run diagnostic tests on an LCA to verify that no pins are damaged.

MESA-I's tool-kit architecture lets you mix and match a wide variety of features for complete troubleshooting flexibility. It overcomes the inherent inobservability of highly integrated ASICs by giving you a view of every node in the LCA. This reduces the need for rigorous simulation which, in turn, shortens the development cycle.

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IT'S AS EASY AS IT LOOKS. We designed our icon-based graphical user interface to make MESA-I natural and easy to use. Running under Microsoft™ Windows, it makes the design analysis process quick and interactive. All main functions are accessible from the top layer of MESA-I's menu system.

Because MESA-I works on the same system you used for your LCA design, Xilinx XACT<sup>™</sup> design and symbolic names are automatically migrated to the MESA-I software. As you become familiar with MESA-I, you can easily tailor information displays to your specific needs by selecting different data and data formats.

To select a design file, symbol name, or software function, point and pick with the mouse or use your keyboard. Screens have visual, pictorial cues to make operations intuitive. If you have a question, context-sensitive help is always available.

Complete sessions and specific displays can be easily saved for future use.

Target LCA



#### SEE EXAMPLE 1. YOU'D LIKE TO SEE SIGNALS INSIDE YOUR LCA IN REAL-TIME.

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To Logic Analyzer

Load an alternative design, containing only a portion of your circuitry and pins, into the Shadow LCA. Since it runs independently of your target system, the Shadow LCA doesn't have to satisfy your system's requirements. This partial design frees enough pins, and leaves enough room, to route out signals of interest. Then with your logic analyzer, you'll be able to capture these signals in real time.

#### CHANGE

Target System

## EXAMPLE 2: YOUR DEVICE ISN'T PERFORMING PROPERLY AND YOU SUSPECT A FAULTY SIGNAL FROM YOUR TARGET SYSTEM.

MESA-I Pod

MESA-I's instrument-per-pin architecture allows you to experiment with individual signals and immediately observe the results. Disconnect the suspect signal from the Shadow LCA, and use MESA-I to force it to a zero or a one. The target system continues to run, transmitting all other stimulus as usual. This technique will help you quickly determine whether the problem lies in your LCA device or in the target system.



EXPERIMENT

## EXAMPLE 3. YOU'D LIKE TO OBSERVE YOUR DESIGN OUT-OF-CIRCUIT, INDEPENDENT OF A TARGET SYSTEM.

MESA-I gives you an instant breadboard for experimenting with your design out-of-circuit, using only the Shadow LCA. Run a series of functional vectors to step specific pins through a series of states. These vectors can be easily created with MESA-I software. Connect a function generator to add real-time stimulus to a particular pin.

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#### DATA I/O: THE EXPERT IN COMPLETE PROGRAM-MABLE GATE ARRAY SOLUTIONS. Data I/O is

committed to developing universal solutions for users of programmable integrated circuits. We were the first to offer complete design and programming support for programmable logic devices. These tools are now industry standards, supporting virtually every PLD on the market.

Our support for programmable gate arrays is a logical progression from our leadership in development tools for programmable logic devices. From design entry to in-circuit verification and programming support, Data I/O offers the complete LCA solution.

We demonstrated our commitment when we introduced DASH-LCA, a special version of FutureNet® DASH™ Schematic Designer for Xilinx LCA users.

DASH-LCA offers an easy upgrade path to full DASH. DASH gives you schematic-design power for your entire design, including LCAs, PLDs, gate arrays, and printed circuit boards. DASH's industry-standard output provides access to more CAD systems, service bureaus, and ASIC foundries than any other schematic design software.

Our most sophisticated design entry system, FutureNet FutureDesigner,<sup>™</sup> makes LCA design even easier. FutureDesigner gives you more choices of entry methods, target technologies and output formats. High-level logic synthesis capabilities optimize your design descriptions for the multi-level logic of LCAs.

With the introduction of MESA-I, in-circuit verification of PGAs is now available. For the first time you can observe every node of a PGA running in-circuit. This minimizes simulation, which in turn shortens the development process.

All of your LCA designs can be programmed in firmware with our UniSite<sup>™</sup> Universal Programmer. Using the most advanced programming technology on the market, the UniSite supports virtually every device available today in a single site.



#### WE SUPPORT OUR PRODUCTS FOR LIFE. Good

support is more than a convenience. It can have a dramatic impact on a product's effectiveness, how long it lasts, and how long it keeps you on the leading edge of technology. At Data I/O, we support our products for life, with a worldwide sales and service network. The Data I/O name is your guarantee of satisfaction.

#### THE BASIC MESA-I SYSTEM INCLUDES:

- Controller board, for the IBM<sup>®</sup> PC/AT (or compatible)
- Pod, which plugs into the controller board
- Probe, which connects the Shadow LCA to the target system
- Windows-based software, for ease of use
- Trigger cable, for interfacing to other instruments
- Documentation

#### **MESA-I CONFIGURATIONS:**

- 68-pin single-user system with controller board, 68-pin pod and probe, software
- 84-pin single-user system with controller board, 84-pin pod and probe, software
- Multi-user add-on with extra controller board, software, documentation
- Extra pod add-on with 68- or 84-pin pod and probe, expander cable for controller board

#### **COMPUTER SYSTEM REQUIREMENTS:**

(If you use Xilinx XACT, you already have all the hardware you need.)

- IBM PC/AT or bus-compatible computer
- 640K of base RAM
- EGA capable display



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# **GENERAL DESCRIPTION**

MESA-I™ is an in-circuit verification tool for rapid troubleshooting of Logic Cell™ Array (LCA™) and other programmable gate array designs. Its name derives from the four broad functions it covers:

Modelina Emulation Simulation Analysis

MESA-I runs from an IBM® AT or bus-compatible, via a plug in controller board. The board attaches to the MESA-I pod, allowing the pod to access files created in the LCA development environment. The pod interfaces to a target system through an impedance-controlled probe, which has a socket at the tip for the Target LCA. You control MESA-I with easily learned, Windows™-based software.

Much of MESA-I's power comes from a unique architectural feature: a site for a second LCA, called the Shadow,\* which resides in the pod. The Shadow LCA is connected to the probe tip through a flex cable, and can be stimulated by the target system and run in parallel with the Target LCA. But because it is not obligated to function in-circuit, the Shadow LCA becomes a powerful platform for design observation and experimentation.

MESA-I is constructed almost entirely from LCAs. A "downloader" LCA allows real-time configuration of the Target and Shadow devices, on demand from the system. A set of "pinlogic" LCAs intervenes between the Target and Shadow ICs and makes possible a wide range of functionality, including triggering to "freeze" the Shadow LCA. Even the PC controller board contains an LCA, used to implement high-speed serial communication with the pod. All of the LCA-based hardware is easily updatable by disk for future enhancement.

# **FEATURES**

## **Unique architecture**

- Two LCAs (Target and Shadow) operate in parallel
- Impedance-controlled probe plugs into target system
- LCA-based pod
- Pod attaches to IBM AT plug-in board
- Each AT board supports up to four pods
- Graphics-oriented Windows-based software

#### \* patent pending

Im MESA-I is a trademark of Data I/O Corporation. Data I/O Corporation acknowledges the trademarks of other organizations for their respective products or services identified in this document.

Specifications are subject to change without notice.

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#### **Configure user LCAs**

- Real-time on demand from system, in all modes
- Configure Target and Shadow LCAs from target system or MESA-I pod
- Verify integrity of configuration

#### Verify user LCA designs in-circuit

- Run Shadow LCA in parallel, with same design
  - Trigger "snapshot" of design: freeze Shadow LCA and observe internal states
- Run Shadow LCA in parallel with alternate design
  - Use Shadow LCA to "route-out" internal signals
- Monitor pins and internal states via software
- Force selected pins on Shadow or Target LCA

#### Verify user LCA designs out-of-circuit

- Experiment freely with designs
- Run full test vectors to Shadow LCA
- Observe pins and internal states between each single-step

# SYSTEM SPECIFICATIONS

#### Minimum host-system requirements:

- An AT or bus-compatible computer
- 640K RAM
- An EGA-capable display

#### Basic MESA-I system consists of:

- A controller board for the AT
- A pod, which plugs into the controller board
- A probe, which plugs into your target system
- Windows-based software for ease of use
- A trigger cable, for interfacing to other instruments (e.g., logic analyzer)
- Documentation

# ORDER CONFIGURATIONS

#### 68-pin single user

Controller board, 68-pin pod and probe, software

#### 84-pin single user

• Controller board, 84-pin pod and probe, software

#### Multi-user add on

• Extra controller board, software and documentation

#### Extra-pod add on

 68- or 84-pin pod and probe, expander cable for controller board

