L201
16_MHZ
OSCILATOR
OSC
74AS04
U241F
U241B
U241C
L206
L205
475-31
IOCLK~ (SHT.10)
CLK~ (SHT.4,5,7)
A(0:23) (SHT.2)
(SHT.10) GATEA20
GATEA20
CPUA20
74AS08
U259C
A20
RP209
390
RP214
33
C219
.047uf
RP203
10K
CLK286
U218
80286-8
CAP
CLK
READY
HOLD
INTR
NMI
PEREQ
BUSY
RESET
ERROR
BHE
PEACK
HLDA
LOCK
COD/INTA
M/IO
S0
S1
(SHT.4) RDY286~
(SHT.10) INTR
(SHT.10) NMI
(SHT.3) BSY286~
(SHT.5) RST286
(SHT.6) RA1
(SHT.6) RA2
(SHT.3) CODF
(SHT.2) SA0~
(SHT.6) RA3
(SHT.3) S2F~
(SHT.10) DEC7~
(SHT.6) RA4
(SHT.3) IOW~
(SHT.3) IOR~
(SHT.3) RST287
(SHT.4) PCLK
74AS11
U249C
74ALS00
U257D
74AS02
U244D
J204
CLK287
CLK286
J203
R202
10K
CLK286/3~
80287-8
U219
R201
4.7K
RP217
4.7K
D203
(56-87)
D201
(56-87)
COD (SHT.3)
S2~ (SHT.3)
S0~ (SHT.3,4)
S1~ (SHT.3,4)
BHE~ (SHT.3)
D(0:15) (SHT.2)
NPS1~ (SHT.3)
PEACK~
RP205
1K
74S05
U229E
U229D
I16~ (SHT.5,10)
BSY287~ (SHT.3)
ERROR_87 (SHT.3)
IRQ13 (SHT.10)
ERROR_87~
L204
475-31

Z248 0WS CPU/MEMORY SCHEMATIC
CPU/COPROCESSOR LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M. NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 1 OF 12	REV: A

ZENITH DATA SYSTEMS St. Joseph, Michigan (616) 982-3200

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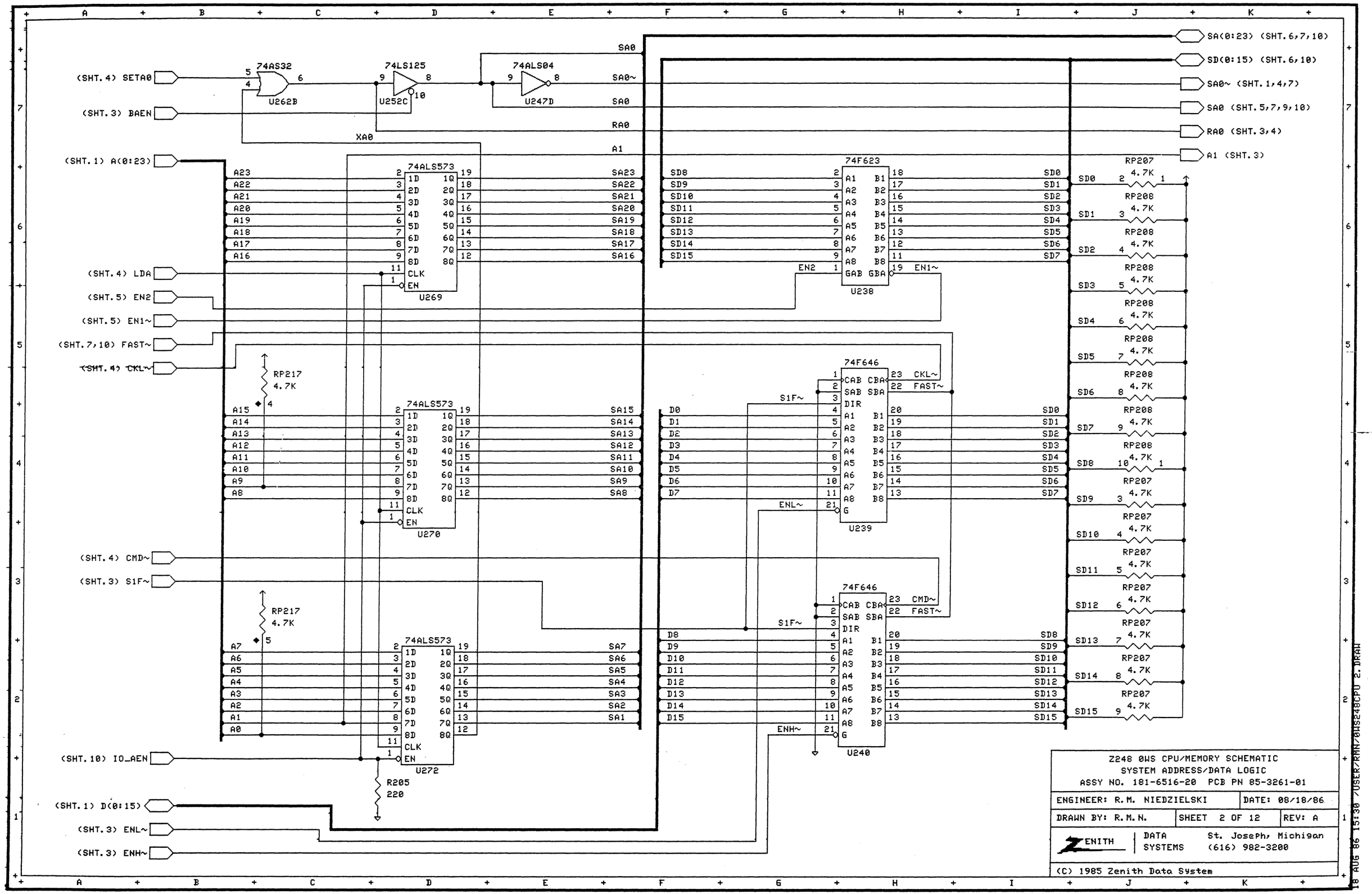
18 AUG 86 15:29 /USER/RMN/0WS248CPU 1.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
SYSTEM ADDRESS/DATA LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M. NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 2 OF 12	REV: A

ZENITH DATA SYSTEMS St. Joseph, Michigan (616) 982-3200

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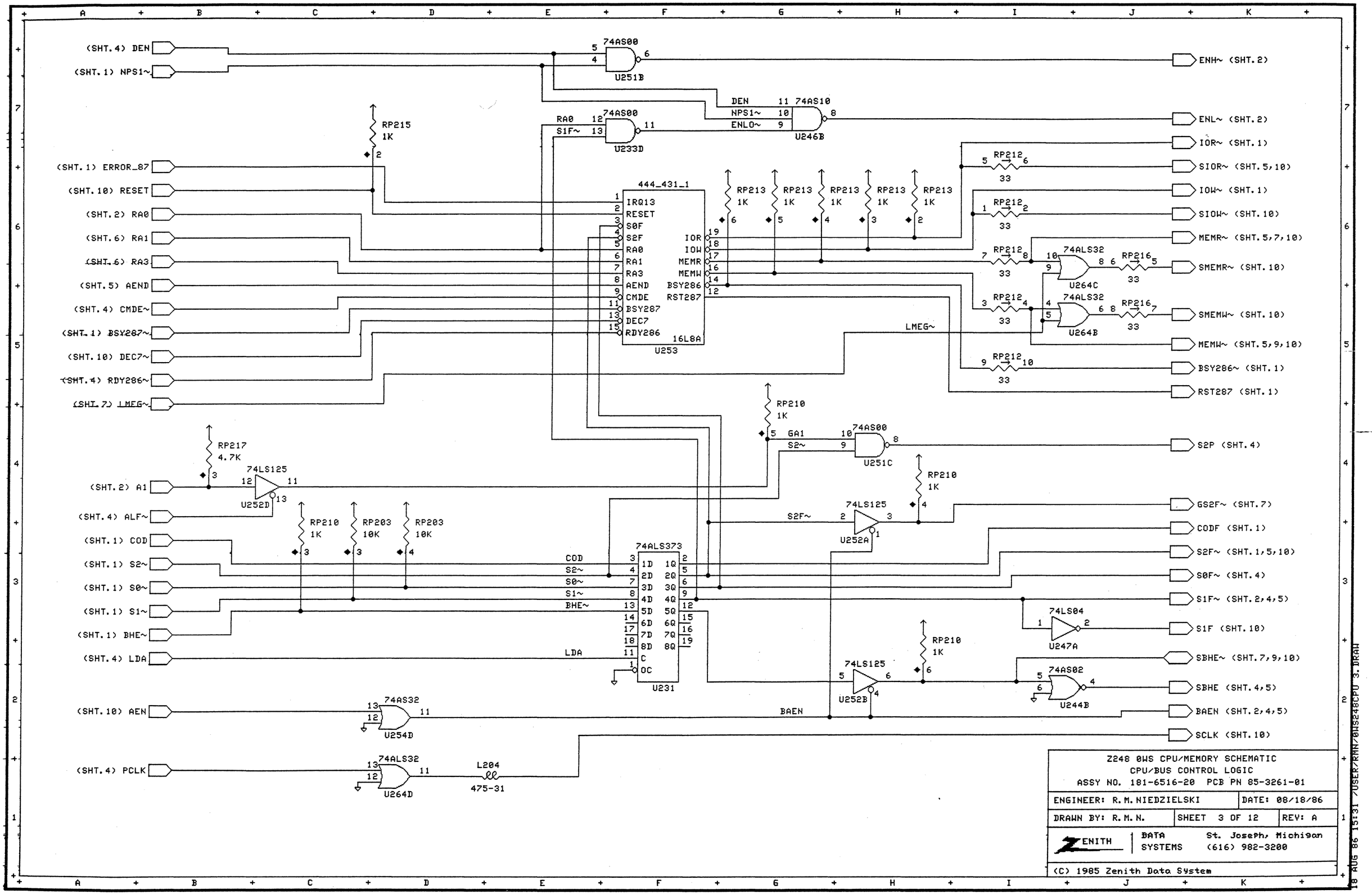
18 AUG 86 15:30 /USER/RMN/0WS248CPU 2.DRAW


(SHT.4) DEN
(SHT.1) NPS1~
74AS00
U251B
ENH~ (SHT.2)
DEN
NPS1~
ENLO~
74AS10
U246B
ENL~ (SHT.2)
RA0
S1F~
74AS00
U233D
RP215
1K
(SHT.1) ERROR_87
(SHT.10) RESET
(SHT.2) RA0
(SHT.6) RA1
(SHT.6) RA3
(SHT.5) AEND
(SHT.4) CMDE~
(SHT.1) BSY287~
(SHT.10) DEC7~
(SHT.4) RDY286~
(SHT.7) LMEG~
444_431_1
IRQ13
RESET
S0F
S2F
RA0
RA1
RA3
AEND
CMDE
BSY287
DEC7
RDY286
IOR
IOW
MEMR
MEMW
BSY286
RST287
16L8A
U253
RP213
1K
RP212
33
74ALS32
U264C
U264B
RP216
33
IOR~ (SHT.1)
SIOR~ (SHT.5,10)
IOW~ (SHT.1)
SIOW~ (SHT.10)
MEMR~ (SHT.5,7,10)
SMEMR~ (SHT.10)
SMEMW~ (SHT.10)
MEMW~ (SHT.5,9,10)
BSY286~ (SHT.1)
RST287 (SHT.1)
LMEG~
RP210
1K
74AS00
U251C
S2~
GA1
S2P (SHT.4)
RP217
4.7K
74LS125
U252D
(SHT.2) A1
(SHT.4) ALF~
RP210
1K
RP203
10K
RP203
10K
(SHT.1) COD
(SHT.1) S2~
(SHT.1) S0~
(SHT.1) S1~
(SHT.1) BHE~
(SHT.4) LDA
74ALS373
U231
COD
S2~
S0~
S1~
BHE~
LDA
S2F~
74LS125
U252A
RP210
1K
GS2F~ (SHT.7)
CODF (SHT.1)
S2F~ (SHT.1,5,10)
S0F~ (SHT.4)
S1F~ (SHT.2,4,5)
74LS04
U247A
S1F (SHT.10)
74LS125
U252B
RP210
1K
74AS02
U244B
SBHE~ (SHT.7,9,10)
SBHE (SHT.4,5)
BAEN (SHT.2,4,5)
(SHT.10) AEN
74AS32
U254D
BAEN
SCLK (SHT.10)
(SHT.4) PCLK
74ALS32
U264D
L204
475-31
Z248 0WS CPU/MEMORY SCHEMATIC
CPU/BUS CONTROL LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01
ENGINEER: R.M.NIEDZIELSKI
DATE: 08/18/86
DRAWN BY: R.M.N.
SHEET 3 OF 12
REV: A
ZENITH DATA SYSTEMS
St. Joseph, Michigan
(616) 982-3200
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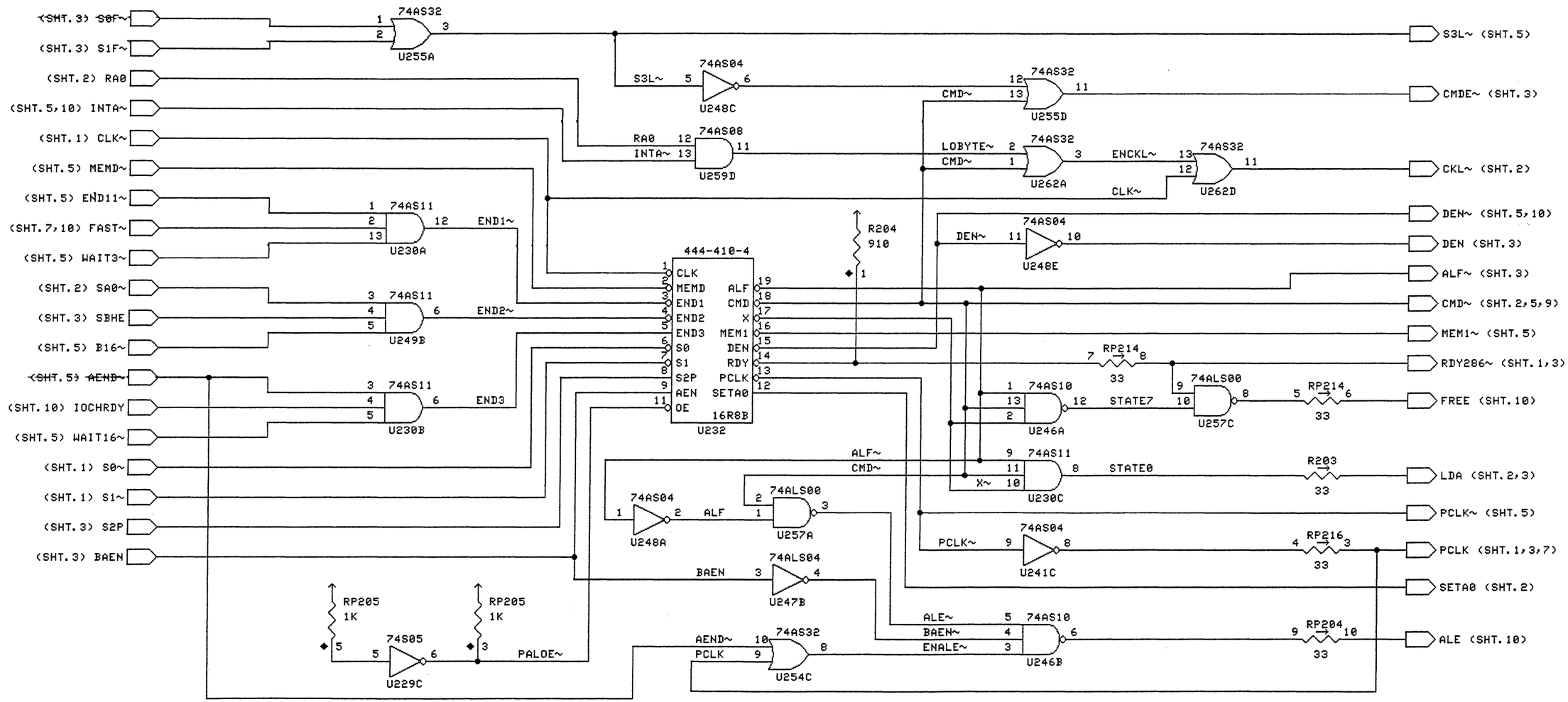
18 AUG 86 15:31 /USER/RMN/0WS248CPU 3.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
CPU CONTROL LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R. M. NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R. M. N.	SHEET 4 OF 12	REV: A

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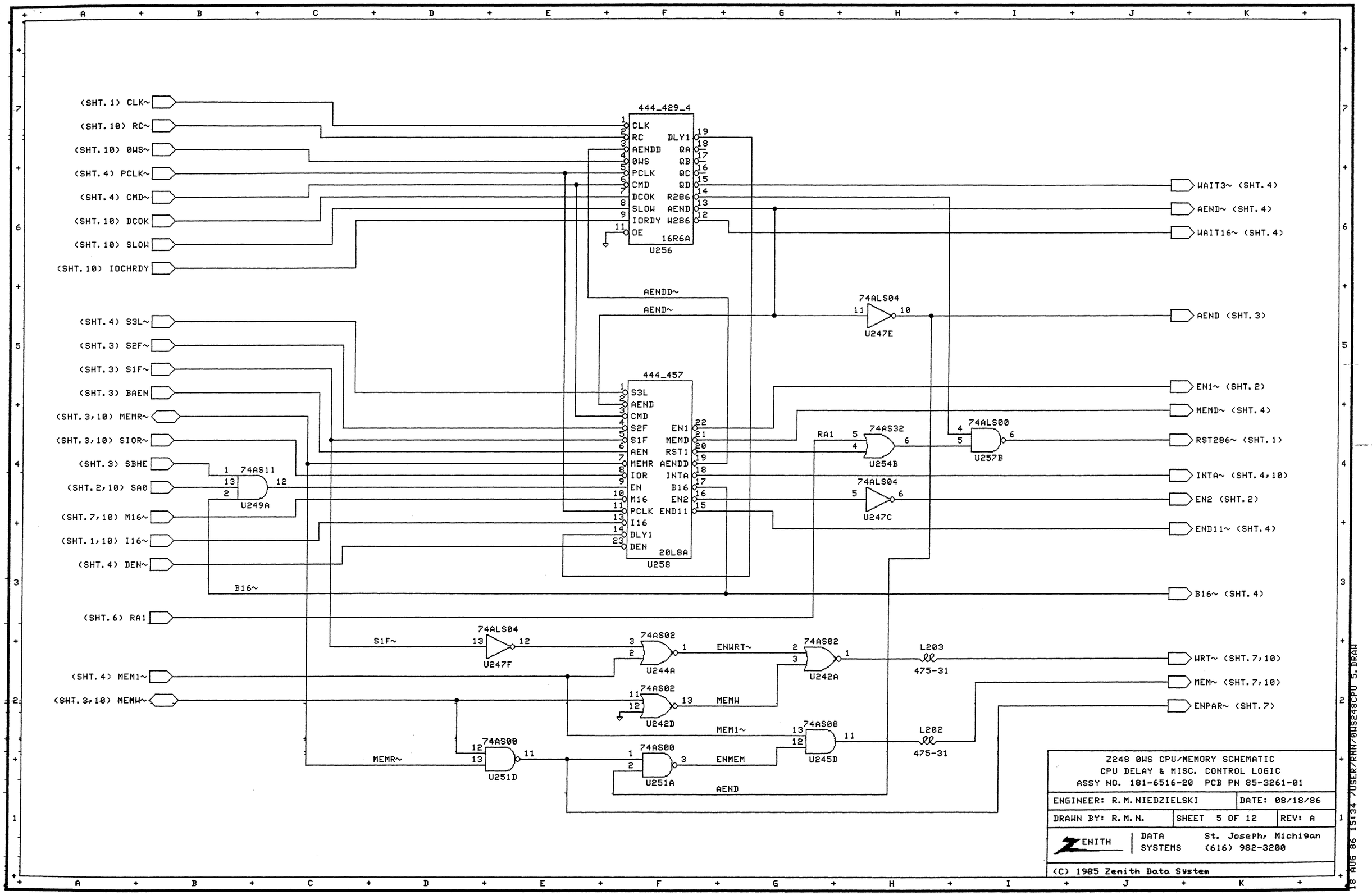
18 AUG 86 15:32 /USER/RMN/0WS248CPU 4.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
CPU DELAY & MISC. CONTROL LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 5 OF 12	REV: A

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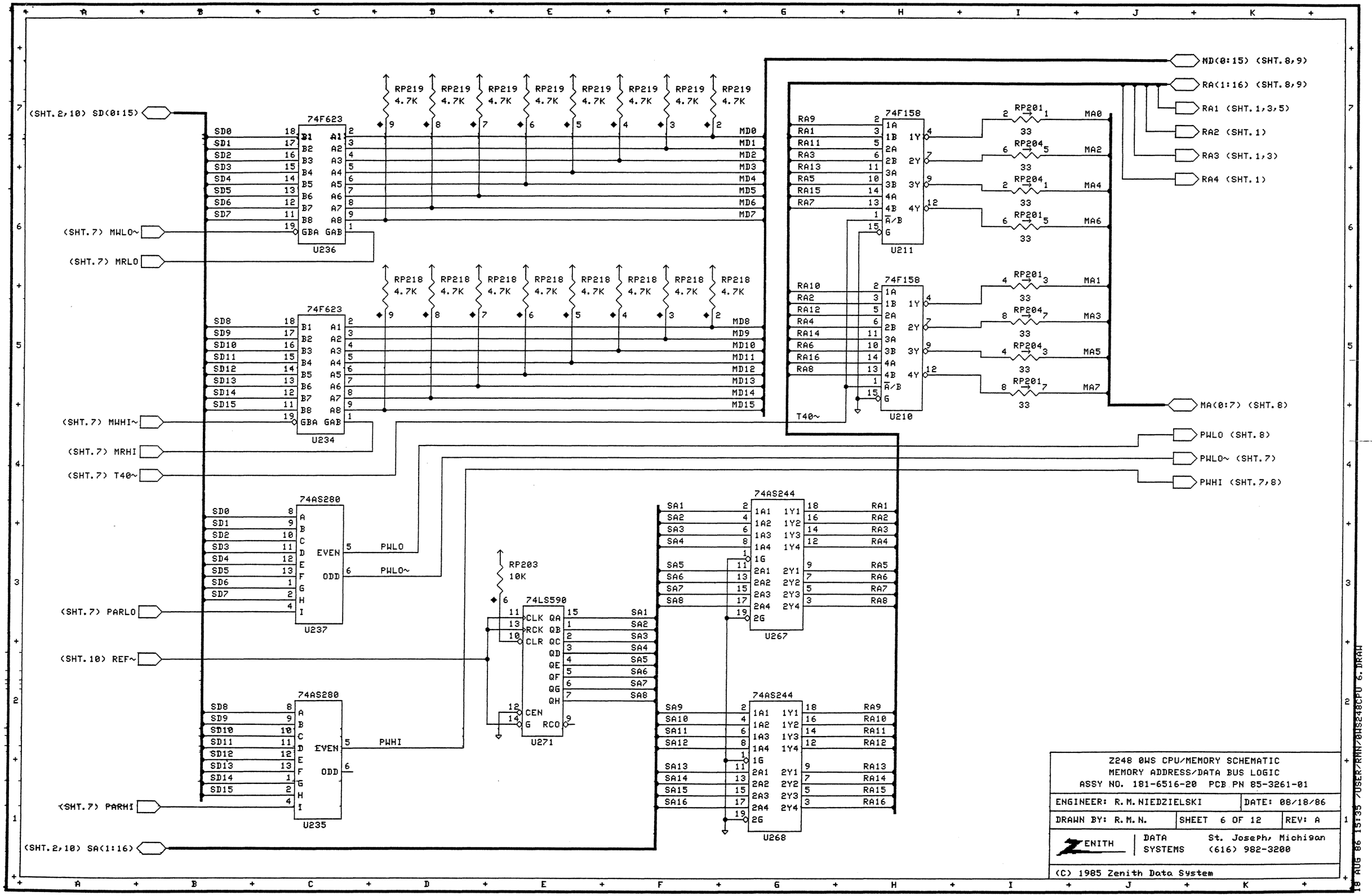
18 AUG 86 15:34 /USER/RMN/0WS248CPU 5.DRAW


(SHT.2,10) SD(0:15)
74F623
U236
U234
RP219 4.7K
RP218 4.7K
(SHT.7) MWLO~
(SHT.7) MRLO
(SHT.7) MWHI~
(SHT.7) MRHI
(SHT.7) T40~
74AS280
U237
U235
RP203 10K
74LS590
U271
(SHT.7) PARLO
(SHT.7) PARHI
(SHT.10) REF~
(SHT.2,10) SA(1:16)
74AS244
U267
U268
74F158
U211
U210
RP201 33
RP204 33
T40~
MD(0:15) (SHT.8,9)
RA(1:16) (SHT.8,9)
RA1 (SHT.1,3,5)
RA2 (SHT.1)
RA3 (SHT.1,3)
RA4 (SHT.1)
MA(0:7) (SHT.8)
PWLO (SHT.8)
PWLO~ (SHT.7)
PWHI (SHT.7,8)
Z248 0WS CPU/MEMORY SCHEMATIC
MEMORY ADDRESS/DATA BUS LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01
ENGINEER: R.M.NIEDZIELSKI
DATE: 08/18/86
DRAWN BY: R.M.N.
SHEET 6 OF 12
REV: A
ZENITH DATA SYSTEMS
St. Joseph, Michigan
(616) 982-3200
(C) 1985 Zenith Data System
10 AUG 86 15:35 /USER/RMN/0WS248CPU 6.DRAW

SA0~
74AS08 U245C
MRLO (SHT.6)
MRHI (SHT.6)
FMEMR~
MSEL~
74AS02 U242B
SA0,SA(12:23) (SHT.2,10)
444-548
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
SA20
SA21
SA22
SA23
SA0
ROW
S2FREF
Z100EN
FMEMR
LMEG
MSEL
ROM
XRAM
RAM
MX8
20L8B
U266
LMEG~ (SHT.3)
74AS04 U248B
74S05 U229B
M16~ (SHT.5,10)
ROM~ (SHT.9)
XRAM~ (SHT.9)
74AS04 U248F
74S05 U229F
J202
FAST~ (SHT.2,10)
RP202 33
MA8 (SHT.8)
(SHT10) REF~
(SHT.3) GS2F~
74AS08 U259B
(SHT10) Z100EN
T40~
J208
J207
74AS32 U261B
J206
74AS32 U255C
WELO~ (SHT.8)
SA0
FWRT~
74AS32 U254A
WEHI~ (SHT.8)
(SHT.5) WRT~
74AS74 U263A
(SHT.4) PCLK
RP210 1K
J205
74AS32 U262C
MWLO~ (SHT.6)
SBHE~
WRT~
74ALS32 U264A
MWHI~ (SHT.6)
(SHT.3,10) SBHE~
J209
J210
JMEM~
J211
J212
74AS32 U261A
74AS08 U245B
RAS~ (SHT.8)
(SHT.5) MEM~
DELAY
41-31 TTL DELAY LINE
IN
20
30
40
55
102
12
4
10
6
8
U250
T20~
T55~
T102~
74AS04 U248D
74AS27 U243B
74AS02 U242C
CAS_HOLD~
74AS02 U244C
CAS~ (SHT.8)
T40~ (SHT.6)
(SHT10) DISPG~
74AS32 U255B
74AS00 U233A
(SHT.8) PRLO
PARLO
PARHI
PARLO (SHT.6)
PARHI (SHT.6)
(SHT.8) PRHI
74AS00 U233B
FMEMR~
FMEMR~ (SHT.9)
(SHT.2) SA0~
74AS00 U233C
ERRLO~
PWHI
ERROR (SHT.10)
(SHT.6) PWLO~
(SHT.3,10) MEMR~
74AS74 U265B
74F64
&2
&4
&3
&2
=1
U260
74AS74 U265A
ERR
CLK~
(SHT.6) PWHI
(SHT.5) ENPAR~
ENPAR~
RAM~
(SHT.1) CLK~
(SHT.10) ENIOCHK
ENIOCHK

Z248 0WS CPU/MEMORY SCHEMATIC
CPU MEMORY CONTROL LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 7 OF 12	REV: A

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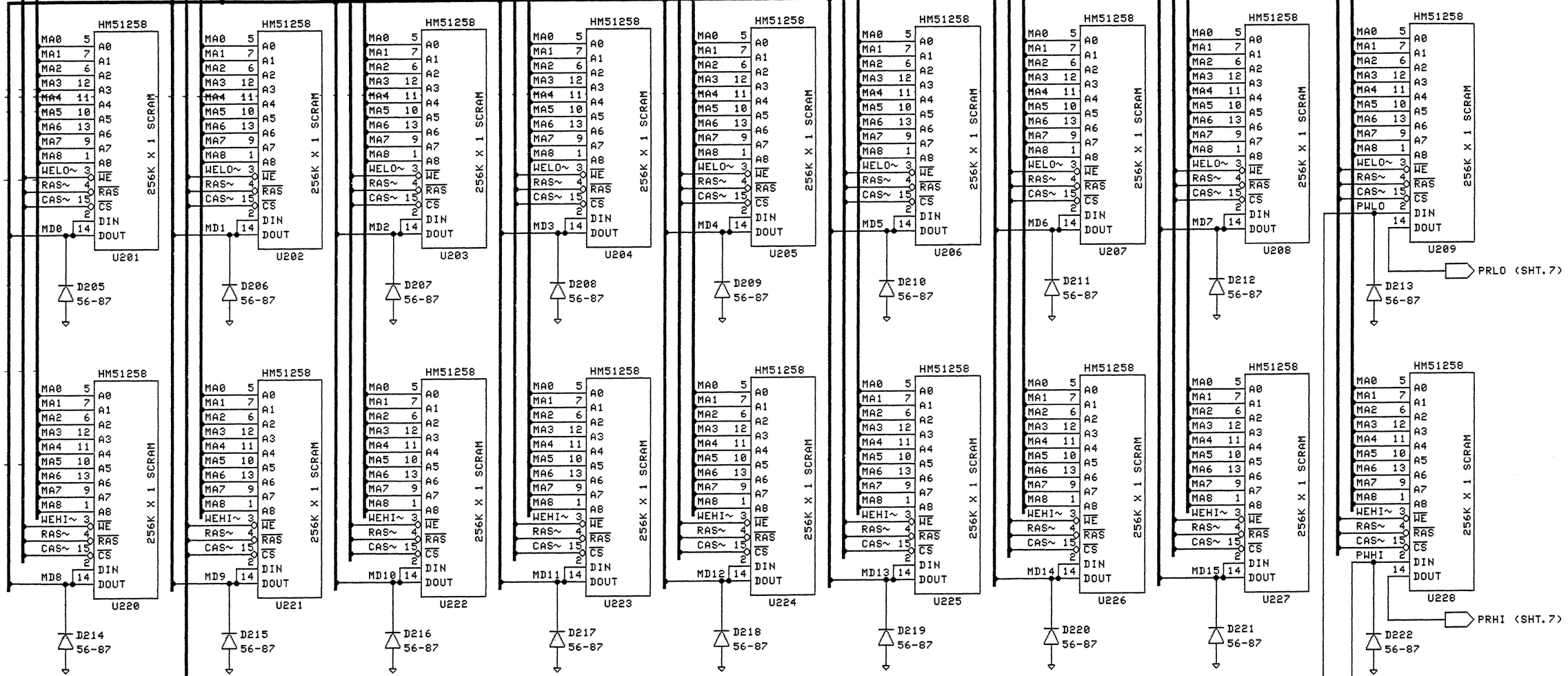
18 AUG 86 13:59 /USER/RMN/0WS248CPU 7.DRAW

(SHT.6) MA(0:8)

(MA8 COMES FROM SHT.7)

(SHT.6) MD(0:15)



(SHT.7) WELO~

(SHT.7) WEHI~

(SHT.7) RAS~

(SHT.7) ~~CAS~~

(SHT.6) PWLO

(SHT.6) PWHI

Z248 0WS CPU/MEMORY SCHEMATIC
512K MEMORY ARRAY LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R. M. NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R. M. N.	SHEET 8 OF 12	REV: A

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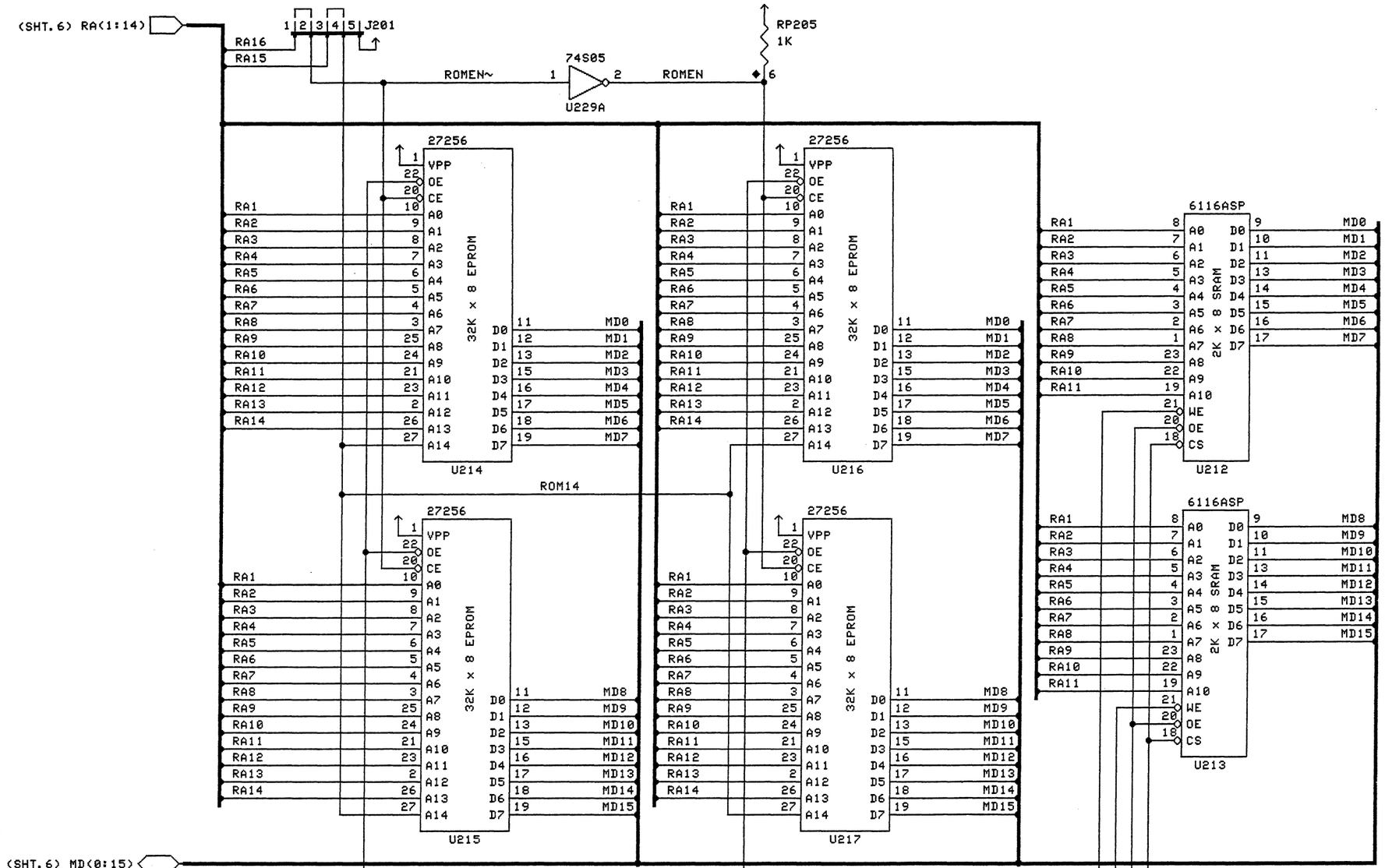
18 AUG 86 15:38 /USER/RMN/0WS248CPU 8.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
ROM/SCRATCH PAD RAM LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI	DATE: 08/18/86	
DRAWN BY: R.M.N.	SHEET 9 OF 12	REV: A

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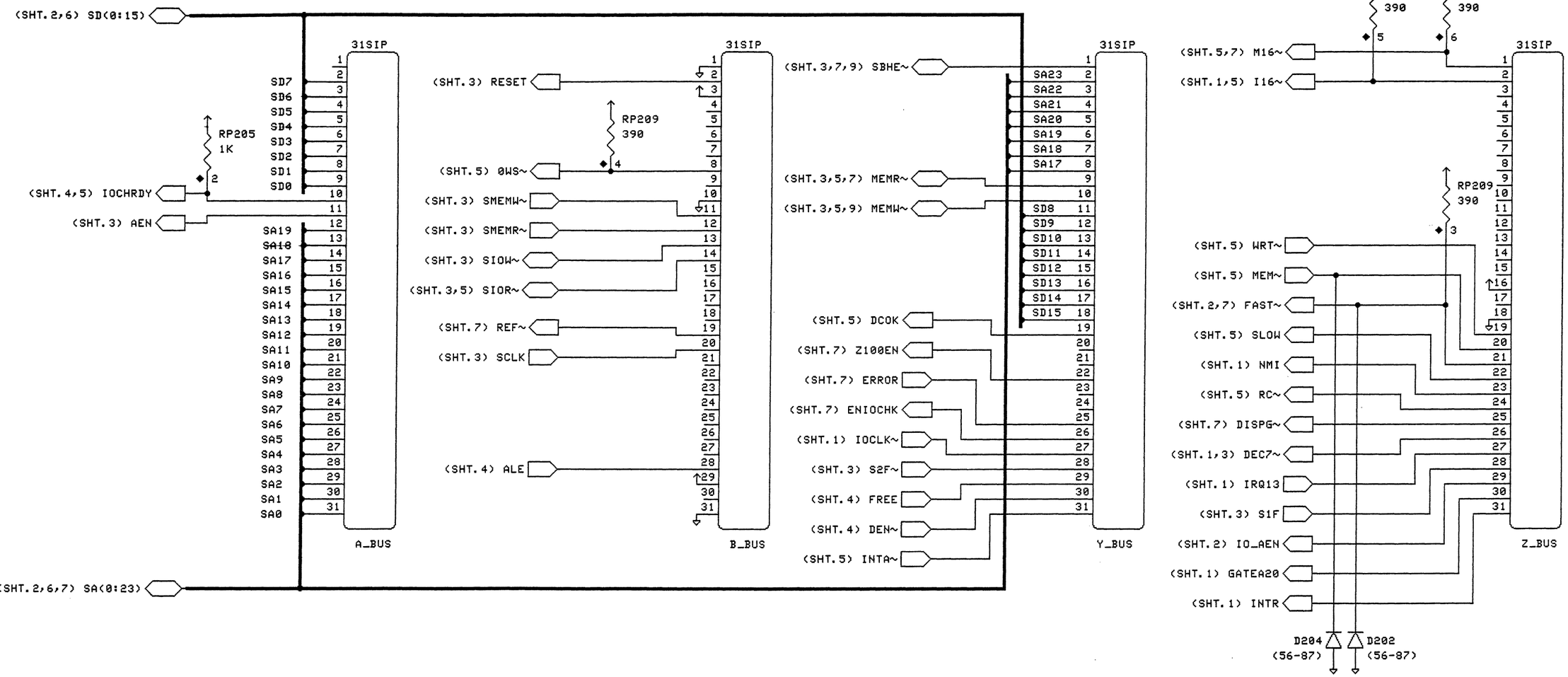
18 AUG 86 15:39 /USER/RMN/0WS248CPU 9.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
CARD EDGE CONNECTOR LOGIC
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 10 OF 12	REV: A

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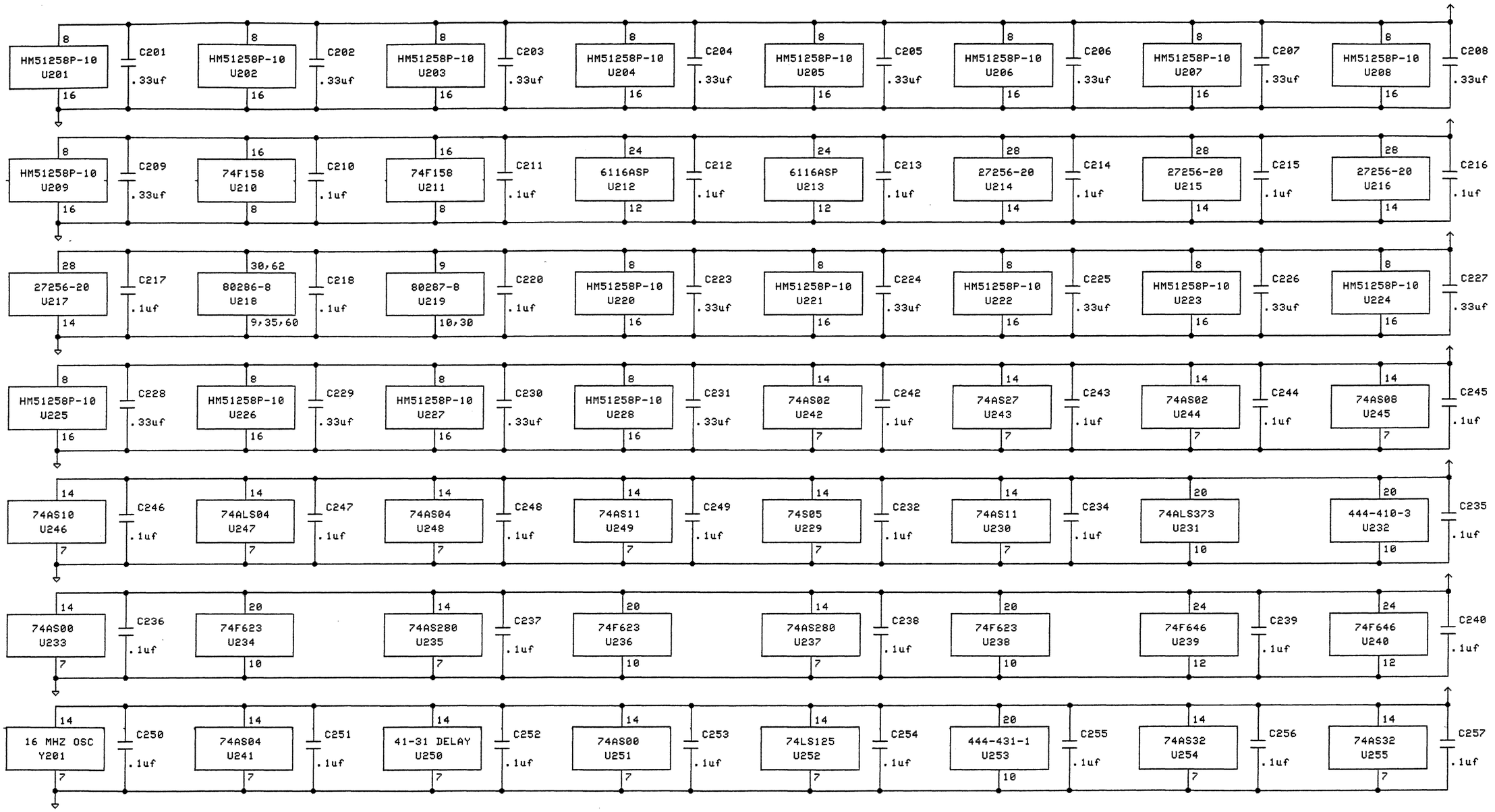
18 AUG 86 15:41 /USER/RMN/0WS248CPU 10.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
POWER SUPPLY RAILS
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 11 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

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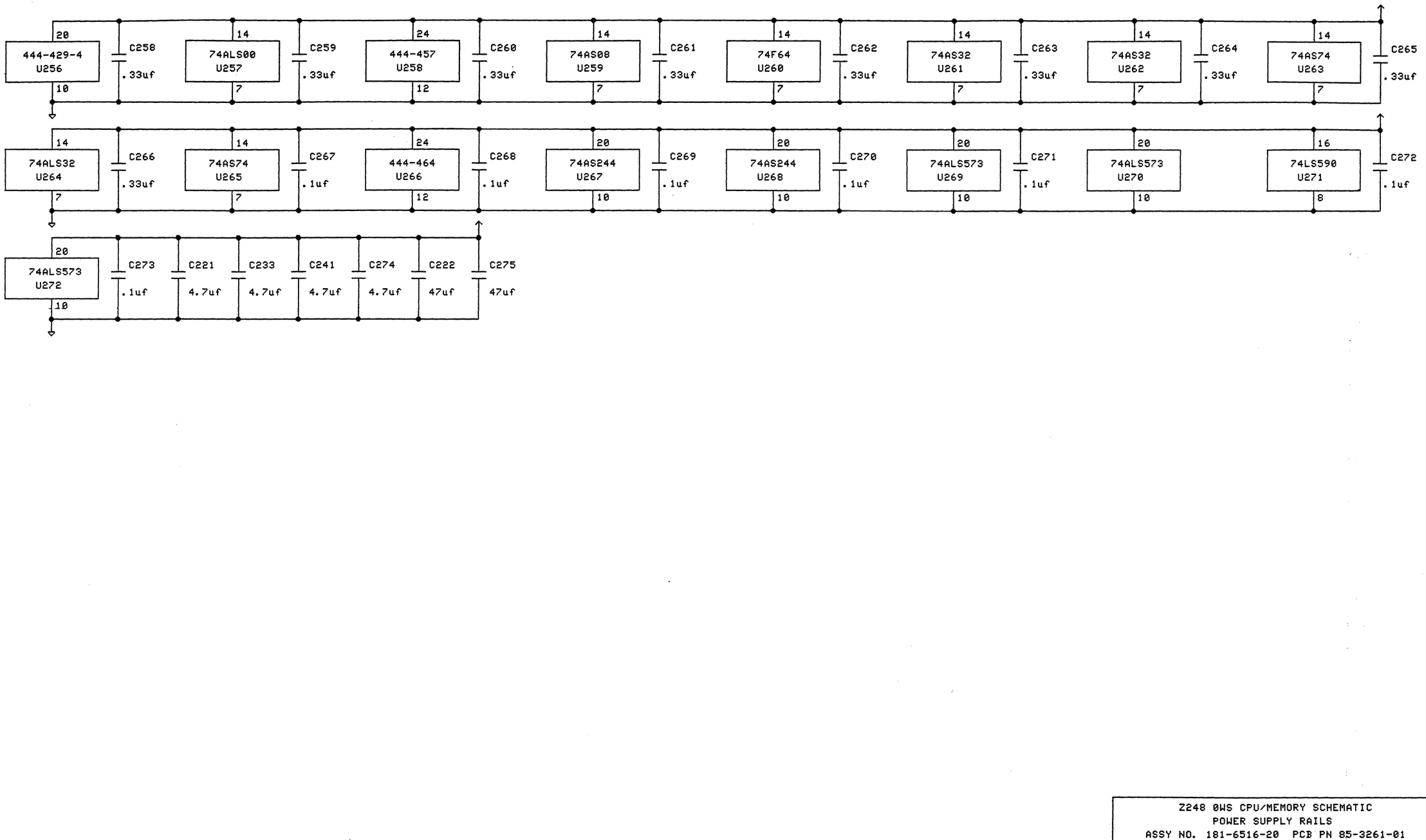
18 AUG 86 15:42 /USER/RMN/0WS248CPU 11.DRAW



Z248 0WS CPU/MEMORY SCHEMATIC
POWER SUPPLY RAILS
ASSY NO. 181-6516-20 PCB PN 85-3261-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 08/18/86
DRAWN BY: R.M.N.	SHEET 12 OF 12	REV: A

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18 AUG 86 15:44 /USER/RMN/0WS248CPU 12.DRAW