Decision 1 Alteration Guide for the Oasis Operating System

Preliminary Edition<br>Rev. $\varnothing-4 / 82$

Morrow Designs
5221 Central Ave. Richmond, CA $948 \varnothing 4$

## Table of Contents

MODIFICATIONS ..... 1
Global Memory ..... 2
Extended Address Memory ..... 5
MPZ8Ø Hardware Modifications ..... 8
MPZ8Ø Firmware Modifications. ..... 8
Mult I/O Switches and Jumpers ..... 9
WB I/O Switches and Jumpers. ..... 10
DJ 2D/B Floppy Controller Settings ..... 11
HDCA Winchester Controller Jumpers and Settings ..... 12
List of Tables
User Memory Maps ..... 1
Switch settings for 16K Superram: ..... 2
Switch settings for l6K Memory Master: ..... 3
MM65KSl6 USER Ø ..... 5
MM65KS16 USER 1 ..... 5
MM65KSI6 USER 2 ..... 6
MM65KSl6 USER 3 ..... 6
MM65KSI6 USER 4 ..... 6
MM65KSI6 USER 5 ..... 7
MM65KSl6 USER 6 ..... 7
MM65KSI6 USER 7 ..... 7
MM65KSl6 Jumpers ..... 8
Mult I/O Switches ..... 9
Mult I/O Jumpers ..... $1 \varnothing$
DJ 2D/B Jumpers. ..... 12
HDCA Jumpers ..... 12
Illustration:Installation of Oasis EPROM ..... 13

## MODIFICATIONS

The Oasis operating system requires that the first 16 K of user memory be global, that is, shared by all the users. For this reason, a non-extended address board (i.e., Morrow Designs Superram l6) is is addressed at XXøøøØh - XX3FFFh, where the operating system will reside. This memory will be common to all tasks running. In addition to this memory, each user will have 48 K of memory at his disposal. In order to minimize the changes to Oasis, the MPZ8Ø will control the upper four address lines (A2ø A23) to simulate a bank select type of system with the extended addressing. This requires that the user memory be extended address memory (a Morrow Designs MM65KSl6 static memory depopulated to 48 K or with two l6K banks overlapping each other). The operating system allows only 16 users and the memory must be addressed to take into account the switching of the upper four address lines when users swap in and out. This would mean the users' memory maps would be as follows:

## User Memory Maps

User $\quad$ Extended Memory Address

| $\emptyset$ | ØØ4ØØø - ØøFFFFH |
| :---: | :---: |
| 1 | 1Ø4ØøØ - 1ØFFFFH |
| 2 | 2ø4øøø - 2ØFFFFH |
| 3 | $3 \varnothing 4 \emptyset \emptyset \emptyset-3 \emptyset F F F F H$ |
| 4 | 404Øøø - 4ØFFFFH |
| 5 | 504øøø - 5øFFFFH |
| 6 | 6ø4øøø - 6øFFFFH |
| 7 | 7ø4øøø - 7ØFFFFH |
| 8 | 8Ø4Øøø - 8ØFFFFH |
| 9 | 9ø4øøØ - 9øFFFFH |
| 10 | Aø4Øøø - AøFFFFH |
| 11 | BØ4Øøø - BØFFFFH |
| 12 | Cø4Øøø - CøFFFFH |
| 13 | DØ4Øøø - DØFFFFH |
| 14 | EØ4ØØØ - EØFFFFH |
| 15 | FØ4ØØø - FØFFFFH |

The global memory part of the system may be composed of any board which does not respond to extended address. This can be any of the following Morrow Design products:

```
16K Superram
l6K Memory Master
24K Memory Master
32K Superram
MM65KSl6Memory Board (setup for bank select)
```

Switch settings for 16 K Superram:
Far Left Switch

| Paddle |  |
| :---: | :---: |
|  |  |
|  | State |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 7 | ON |
| 8 | OFF |

Middle Switch

| Paddle |  |
| :---: | :--- |
|  |  |
|  |  |
| 2 | Otate |
| 3 | ON |
| 4 | OFF |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 8 | OFF |
|  | OFF |

Right Switch

| Paddle | State |
| :---: | :---: |
|  |  |
| 1 | ON |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 8 | ON |

Switch settings for 16 K Memory Master:

| Switch 6A |  |
| :---: | :---: |
| Paddle | State |
| 1 | ON |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 8 | ON |
| Switch | 7A |
| Paddle | State |
| 1 | OFF |
| 2 | OFF |
| 3 | OFF |
| 4 | OFF |
| 5 | OFF |
| 6 | OFF |
| 7 | OFF |
| 8 | ON |

Switch 8A

| Paddle | State |
| :---: | :---: |
| 1 |  |
| 2 | OFF |
| 3 | OFF |
| 4 | ON |
| 5 | OFF |
| 6 | OFF |
| 7 | OFF |
| 8 | ON |
|  | ON |


| Switch |  |
| :---: | :---: |
| Paddle |  |
|  |  |
| 1 | State |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 8 | ON |
|  | OFF |


| Switch |  |
| :---: | :---: |
| Paddle |  |
| 1 | State |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 8 | ON |
|  | ON |

> Switch 7F

| Paddle | State |
| :---: | :---: |
|  |  |
| 1 | ON |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | ON |
| 7 | ON |

The following procedures set up the MM65KSl6 memory board for the Oasis operating system.
I. Depopulate board to 48K. Remove RAM chips at board locations: 1A, 2A, 3A, 4A, 1B, 2B, 1C, 2C

The board now has 48 K of RAM.
II. Addressing the board:

The following are the switch settings for MM65KSl6 for a multi-user Oasis system:

MM65KSl6 USER Ø

| Paddle | Sl | S2 |
| :---: | :--- | :--- |
|  |  | ON |

## MM65KSl6 USER 1

| Paddle |  | Sl |
| :---: | :--- | :--- |
|  |  | S2 |
| 1 | ON | ON |
| 2 | ON | OFF |
| 3 | ON | ON |
| 4 | ON | OFF |
| 5 | OFF | OFF |
| 6 | ON | ON |
| 7 | ON | OFF |
| 8 | ON | OFF |

MM65KSl6 USER 2

| Paddle |  | S1 |
| :---: | :--- | :--- |
|  | ON | S2 |
| 1 | ON | ON |
| 2 | ON | OFF |
| 3 | ON | ON |
| 4 | ON | OFF |
| 5 | ON | OFF |
| 6 | OFF | ON |
| 7 | ON | OFF |
| 8 | ON | OFF |

## MM65KSl6 USER 3

| Paddle |  | Sl | S2 |
| :---: | :--- | :--- | :--- |
|  |  | ON | ON |
| 1 |  | ON | OFF |
| 2 | ON | ON |  |
| 3 | ON | OFF |  |
| 4 | OFF | OFF |  |
| 5 | OFF | ON |  |
| 6 | ON | OFF |  |
| 7 |  |  | OFF |

MM65KSl6 USER 4

| Paddle |  | Sl | S2 |
| :---: | :--- | :--- | :--- |
|  |  | ON | ON |
| 1 | ON | OFF |  |
| 3 | ON | ON |  |
| 4 | ON | OFF |  |
| 5 | ON | OFF |  |
| 6 | ON | ON |  |
| 7 | OFF | OFF |  |
| 8 | ON | OFF |  |

## MM65KSI6 USER 5

| Paddle |  | Sl | S2 |
| :---: | :--- | :--- | :--- |
|  |  |  |  |
| 1 | ON | ON |  |
| 2 | ON | OFF |  |
| 3 | ON | ON |  |
| 4 | ON | OFF |  |
| 5 | OFF | OFF |  |
| 6 | ON | ON |  |
| 7 | OFF | OFF |  |
| 8 | ON | OFF |  |

## MM65KSl6 USER 6

| Paddle |  | Sl | S2 |
| :---: | :--- | :--- | :--- |
|  |  | ON |  |
| 1 |  | ON | ON |
| 2 |  | ON | OFF |
| 3 |  | ON | ON |
| 4 |  | ON | OFF |
| 5 |  | ON | OFF |
| 6 |  | OFF | ON |
| 7 | OFF | OFF |  |
| 8 | ON | OFF |  |

MM65KS16 USER 7

| Paddle |  | Sl | S2 |
| :---: | :--- | :--- | :--- |
|  |  |  |  |
| 1 | ON | ON |  |
| 2 | ON | OFF |  |
| 3 | ON | ON |  |
| 4 | ON | OFF |  |
| 5 | OFF | OFF |  |
| 6 | OFF | ON |  |
| 7 | OFF | OFF |  |
| 8 | ON | OFF |  |

Note the progression of the extended address switch: Sl paddles 5 through 8 form a binary progression. By incrementing these four bits, you will increment the upper four bits of the extended address to which the memory will respond and thus increment users.

The memory board should be set as extended address (not bank select) meaning a 25 LS 2521 should be installed in location $1 D$ and no chip should be installed in location 2D.

| J1 | - | In |
| :--- | :--- | :--- |
| J2 | - | In |
| J3 | - | Out |
| J4 | - | In |
| J5 | - | Out |
| J6 | - | In |
| J7 | - | Out |

No jumpers in area l7D (bank select jumpers).

## MPZ8Ø Hardware Modifications

Normally the Decision $l$ is designed to trap on a 'Halt' instruction (system calls from UNIX) but the Oasis operating system will trap on a 'RST 6' instruction instead. At present, this requires a hardware modification to the MPZ8Ø board. The modification requires four jumpers and is performed as follows:
I. Lift pins 9 and $1 \varnothing$ of $I C 8 D$.
2. Connect pin 9 of chip 8 D to pin 1 of chip 6D.
3. Connect pin 10 of chip 8 D to pin 13 of chip 6D.
4. Connect pin 9 on the socket of 8 D to pins 2 and 3 of chip 6D.
5. Connect pin lø on the socket of 8 D to pins lland 12 of chip 6D.

## MPZ8ø Firmware Modifications

The firmware on the MPZ8ø CPU board has also been changed to accommodate this hardware change and the operating system. Whenever a 'RST 6' instruction is executed in the first 4 K of memory of any task, it is assumed to be an Oasis system call. The EPROM code on the MPZ8Ø will then latch the contents of the upper 4 bits of the 'A' register onto the $\mathrm{S}-1 \emptyset \emptyset$ address line Al9 - A23. The lower 4 bits of the 'A' register are masked off. Operation then resumes at the instruction immediately following the 'RST 6' instruction with all registers preserved.

If a 'RST 6' is executed above the first 4 K by any user, it is assumed to be a user wishing to use a 'RST6' instruction and the program will continue execution at location $3 \varnothing$ in the global memory as though it were actually executing the 'RST 6'. It is in fact interpreting this instruction for the user. Users are warned that the memory location of all the Restart vectors is common to all users and should use care when using these areas.

The switches on the MPZ8Ø are the same as for the standard EPROM:
Switches 1 - 5 control the power on jump address. Normally these switches are all off to boot up a DJ $2 \mathrm{D} / \mathrm{B}$ at F8ØØh. If these switches are all on, the Morrow Designs BOOTHD program is executed to boot up a HDCA hard sectored hard disk. If all switches are on except for 5, the HDC/DMA boot routine is executed.

When ON, switch 6 causes the monitor to be invoked, OFF allows power on jump to the address determined by sl - S5. See MPZ8ø manual for details on the monitor commands.

Switch 7 is unused.

Switch 8 must always be on in systems requiring MWRITE (with DJ 2D/B for instance).

Mult I/O Switches and Jumpers (Revision 3 and 4)

## Mult I/O Switches

Switch 2D
(Address ØFøøøØh)
Paddle
1
State
ON
ON
ON
ON
OFF
OFF
OFF
OFF

Switch 7B

Paddle
State
ON
ON
OFF
ON
ON
OFF
OFF
OFF

| Paddle | State |
| :---: | :---: |
|  |  |
| 1 | OFF |
| 2 | ON |
| 3 | ON |
| 4 | ON |
| 5 | ON |
| 6 | ON |
| 7 | OFF |
| 8 | OFF |



WB I/O Switches and Jumpers

Switch 7C

| Paddle |  | State |
| :---: | :--- | :--- |
|  |  |  |
|  |  | ON |
| 2 |  | ON |
| 3 |  | OFF |
| 4 |  | ON |
| 5 |  | ON |
| 6 |  | OFF |
| 7 |  | OFF |
| 8 |  | OFF |




Parts list:
(1) Decision 1 CPU, MPZ80 rev 2
(1) Oasis EPROM (to be located at 17C)
(4) pieces of 30 gauge insulated (Kynar) wire: $2.5^{\prime \prime}, 2.25^{\prime \prime}, 2^{\prime \prime}$ \& $1.5^{\prime \prime}$
(1) $6^{\prime \prime}$ length of solder ( $60 / 40$ recommended)
(1) solder iron
(1) pair of pliers


* 1 Component Side
\#6 Flip the board over to the solder side and solder the $2.5^{\prime \prime}$ wire from pin \#9 to the pad at pin \#1 of chip 6D.
\#7 Solder the $2.25^{\prime \prime}$ wire from pin \#10 to the pad at pin \#13 of chip 6D.
\#8 Solder one end of the $2^{\prime \prime}$ wire to the pad at pin \#9 of chip 80, and the other end to the pads at pins 2 and 3 of chip 6D.
\#9 Solder one end of the $1.5^{\prime \prime}$ wire to the pad at pin \#10 of chip 80, and the other end to the pads at pins 11 and 12 of chip 60.


