MAINTENANCE MANUAL

MONOSTORE V/PLANAR
PDP-8 Add-In
Semiconductor Memory System

MSC P/N 303-0112-000

MONOLITHIC SYSTEMS
CORPORATION
ENGLEWOOD, COLORADO

MONOSTORE V/PLANAR
PDP-8 Add-In

SEMICONDUCTOR MEMORY SYSTEM

C O N T E N T S

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ENG RELEASE	1-21-75	TSP

MAINTENANCE MANUAL

MONOSTORE V/PLANAR
PDP-8 Add-In
Semiconductor Memory System

MSC P/N 303-0112-000

MONOLITHIC SYSTEMS CORPORATION
14 Inverness Drive East
Englewood, Colorado 80110
303/770-7400

REV																											
SHEET																											
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A												
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14												

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES

MATERIAL

DATE

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SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0023-000

SCALE	REV	SHEET
	A	1

MONOSTORE V/PLANAR
PDP-8 Add-In

SEMICONDUCTOR MEMORY SYSTEM

C O N T E N T S

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information for installing, operating, and maintaining the MONOSTORE V/Planar PDP-8 add-in memory systems. The material is arranged in five sections as follows:

Section I General Description

This section provides the scope, contents, and arrangement of the manual. A general description and a list of system specifications are also given.

Section II Installation and Operation

Instructions are provided for unpacking, inspecting and installing the memory system.

Section III Theory of Operation

An overall description of the memory system is provided along with a timing diagram to aid in understanding the system and to support troubleshooting.

Section IV Maintenance and Troubleshooting

This section gives recommended general maintenance procedures and troubleshooting information for diagnosing and locating a malfunction.

Section V Drawings

This section contains schematics, assembly, and parts list for the memory system.

1.2 GENERAL DESCRIPTION

The MONOSTORE V/Planar PDP-8 Add-In Memory System, P/N 303-0112-000, consists of a single planar 8Kx12 memory assembly. All electronics and semiconductor static N-channel memory storage elements are contained on a single printed circuit board.

All signal interface is made through the DEC OMNIBUS™ Assembly. Data interfacing is provided by 12 bidirectional data bits. Addressing any one of the 8192 words is provided by 13 binary address bits, together with command and control information to define the memory mode required.

The memory system uses the +5V power available on the OMNIBUS assembly.

The maximum capacity of the board is 8192 words by 12 bits. The system can also be configured in 1024 word increments from 1024 up to and including 8192 words.

1.3 MODES OF OPERATION

	MD DIR L
Read Cycle - 1.2 μsec Transfers data from memory to the OMNIBUS.	1
Read/Write Cycle - 1.4 μsec Transfers data from memory to the OMNIBUS during MD DIR L = 1 and then writes data into memory from the OMNIBUS during MD DIR L = 0.	1 → 0

1.4 SYSTEM SPECIFICATIONS

Characteristic	Specification
Storage Capacity	1024 words x 12 bits ↓ 8192 words x 12 bits (1024 word increments)
Cycle Time	
Read	1.2 μsec
Read/Write	1.4 μsec

NOTE: DEC and OMNIBUS are trademarks of Digital Equipment Corporation.

1.4 System Specifications continued ..

Characteristic	Specification
Read Access Time	600 nsec
Input Power	+5V
Operating Environment	
Temperature	0°C to +50°C
Relative Humidity	90% maximum without condensation.
Physical Dimensions	
Height	8.44 inches
Depth	0.5 inches
Width	10.44 inches

SECTION II

INSTALLATION & OPERATION

2.1 INTRODUCTION

This section contains information for installation and operation of the memory system.

2.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container. Remove any packing material from the assembly. Inspect the system for any damage or loose connections.

2.3 INSTALLING MEMORY SYSTEM

Remove the external top cover from the PDP-8 computer. Insert the memory system into the OMNIBUS Assembly. Reassemble the top cover. The memory system is now ready for use.

2.4 I/O SIGNALS

PIN	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+15V	TP	+5V	TP	+5V	TP	+5V
B	TP	-15V	TP	-15V	TP	-15V	TP	-15V
C	GND	GND	GND	GND	GND	GND	SP GND*	GND
D	MA8L	IROL	I/O PAUSE L	TP1H	MA4L	INT STROBE L	MA0L	EMA0L
E	MA9L	IR1L	COL	TP2H	MA5L	BRK IN PROG L	MA1L	EMA1L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA10L	IR2L	C1L	TP3H	MA6L	MA, MS LOAD CONT L	MA2L	EMA2L
J	MA11L	FL	C2L	TP4H	MA7L	OVERFLOW L	MA3L	MEM START L
K	MD8L	DL	BUS STROBE L	TS1L	MD4L	BREAK DATA CONT L	MD0L	MD DIR L
L	MD9L	EL	INTERNAL I/O L	TS2L	MD5L	BREAK CYCLE L	MD1L	SOURCE H
M	MD10L	USER MODE H	NOT LAST XFER L	TS3L	MD6L	LA ENABLE L	MD2L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11L	F SET L	INT ROST L	TS4L	MD7L	INT IN PROG H	MD3L	INHIBIT H
R	DATA 8L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4L	RES 1 H	DATA 0L	RETURN H
S	DATA 9L	STOP L	SKIP L	LINK LOAD L	DATA 5L	RES 2H	DATA 1L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 10L	KEY CONTROL L	CPMA DISABLE L	IND 1L	DATA 6L	RUN L	DATA 2L	ROM ADDRESS L
V	DATA 11L	SW	MS, IR DISABLE L	IND 2L	DATA 7L	POWER OK H	DATA 3L	LINK L

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the overall organization and operation of the MONOSTORE V/Planar PDP-8 Add-in Semiconductor Memory System. The system has a maximum capacity of 8192 words of 12 bits.

This section is organized into the following major parts:

Description	Paragraph
Memory Location Programming	3.2
Address Channel	3.3
Data Channel	3.4
Timing Circuitry	3.5

3.2 MEMORY LOCATION PROGRAMMING

The memory location is programmed via wire jumpers on the board. The user can program the memory to any location according to the following table:

STARTING ADDRESS	0=HI LEVEL EMA			4Kx8K PROGRAM		BOARD CAPACITY	MOD EN PROGRAM	
	0	1	2	C	D		A	B
OK	0	0	0	E	F	4K 8K	1 1	A 2
4K	0	0	1	F	E	4K 8K	2 2	A 3
8K	0	1	0	E	F	4K 8K	3 3	A 4
12K	0	1	1	F	E	4K 8K	4 4	A 5
16K	1	0	0	E	F	4K 8K	5 5	A 6
20K	1	0	1	F	E	4K 8K	6 6	A 7
24K	1	1	0	E	F	4K 8K	7 7	A 8
28K	1	1	1	F	E	4K –	8 –	A –

SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0023-000
SCALE	REV A	SHEET 8

3.2 Memory Location Programming continued ...

The computer generated addresses EMA0, EMA1, and EMA2 are decoded in blocks of 4K with a maximum of two 4K blocks of memory on a single board. If the generated addresses are within the programmed range a memory cycle will be initiated by MEM START L. This circuitry is shown on Sheet 1 of the schematic.

3.3 ADDRESS CHANNEL

When a memory cycle is initiated the information on the address lines MA0L → MA11L is used as follows:

MA2L → MA11L - These address bits are buffered in order to drive the complete memory array.

MA0L, MA1L - These address bits are decoded in conjunction with EMA2 to generate the 1K, 2K...8K cenable pulses required by the memory elements. The cenable pulse then enables only one row of memory elements at any one time thereby preventing interaction of data bits.

The address channel and cenable circuits are shown on Sheet 1 of the schematic.

3.4 DATA CHANNEL

When a memory cycle, READ, is initiated, the information previously stored in the memory elements is accessed and transmitted onto the MD0L → MD11L lines for use by the computer for as long as MD DIR L = 1.

When a memory cycle, READ/WRITE, is initiated the READ cycle is repeated until MD DIR L = 0. At that time the WRITE phase of the memory cycle is performed and the information on the MD0L → MD11L lines is buffered and stored in the memory elements at the same address as the first phase READ portion of the cycle.

The data channel circuit is shown on Sheet 2 of the schematic.

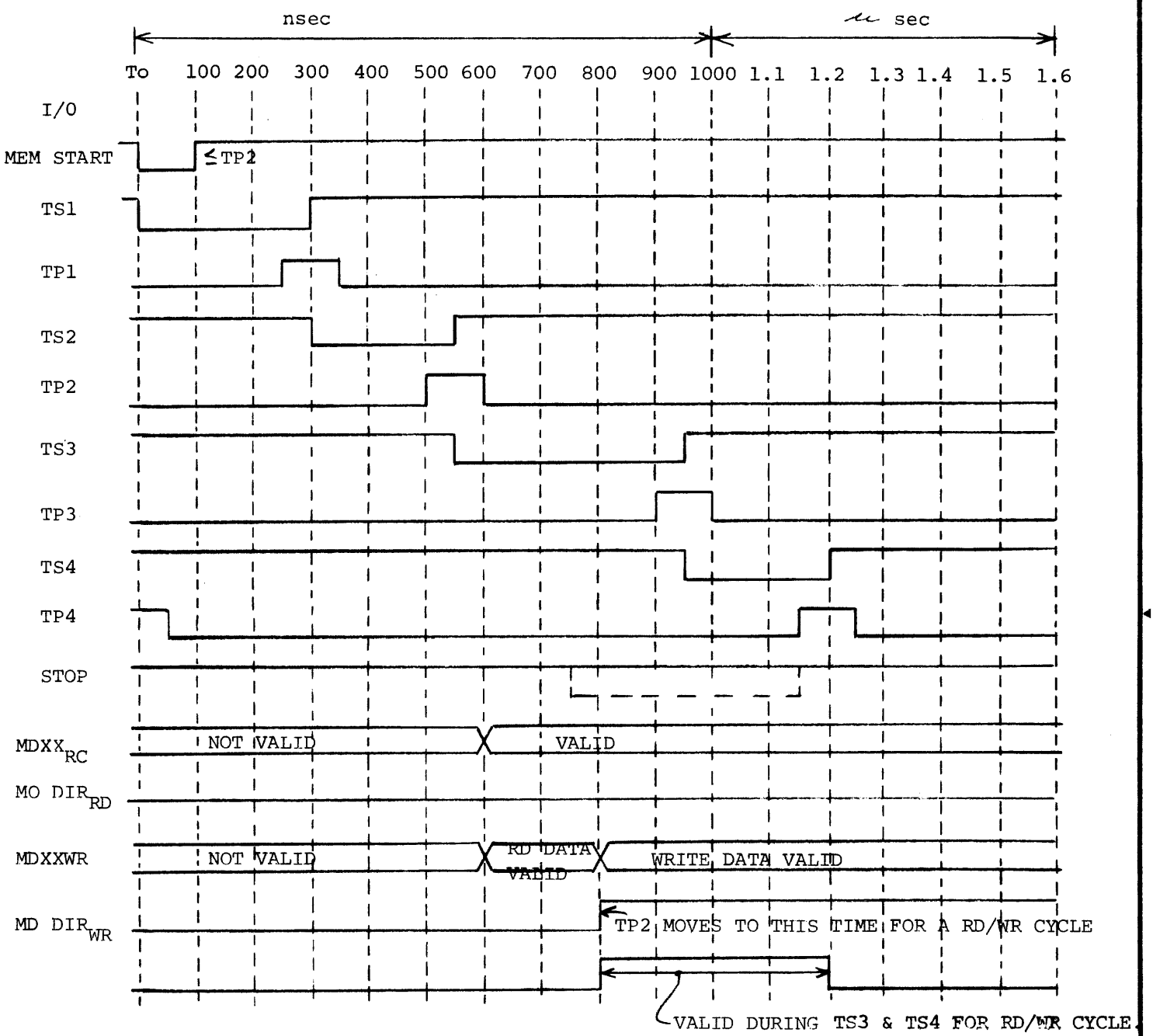
3.5 TIMING CIRCUITRY

All internal and I/O pulses or signals, except the storage element "write" pulse, are generated from timing pulses TS1L → TS4L, TP1H → TP3H, received at the OMNIBUS interface.

The MEM START L signal is received by the memory system and generates a READ or READ/WRITE cycle depending upon whether MD DIR L is a "1" or "1/0" respectively.

The timing pulses and signals at the OMNIBUS interface are generated according to the following timing diagram. The miscellaneous timing and control circuitry is shown on Sheets 1 and 2 of the schematic.

PDP-8



SIZE	CODE IDENT NO.	DWG NO.
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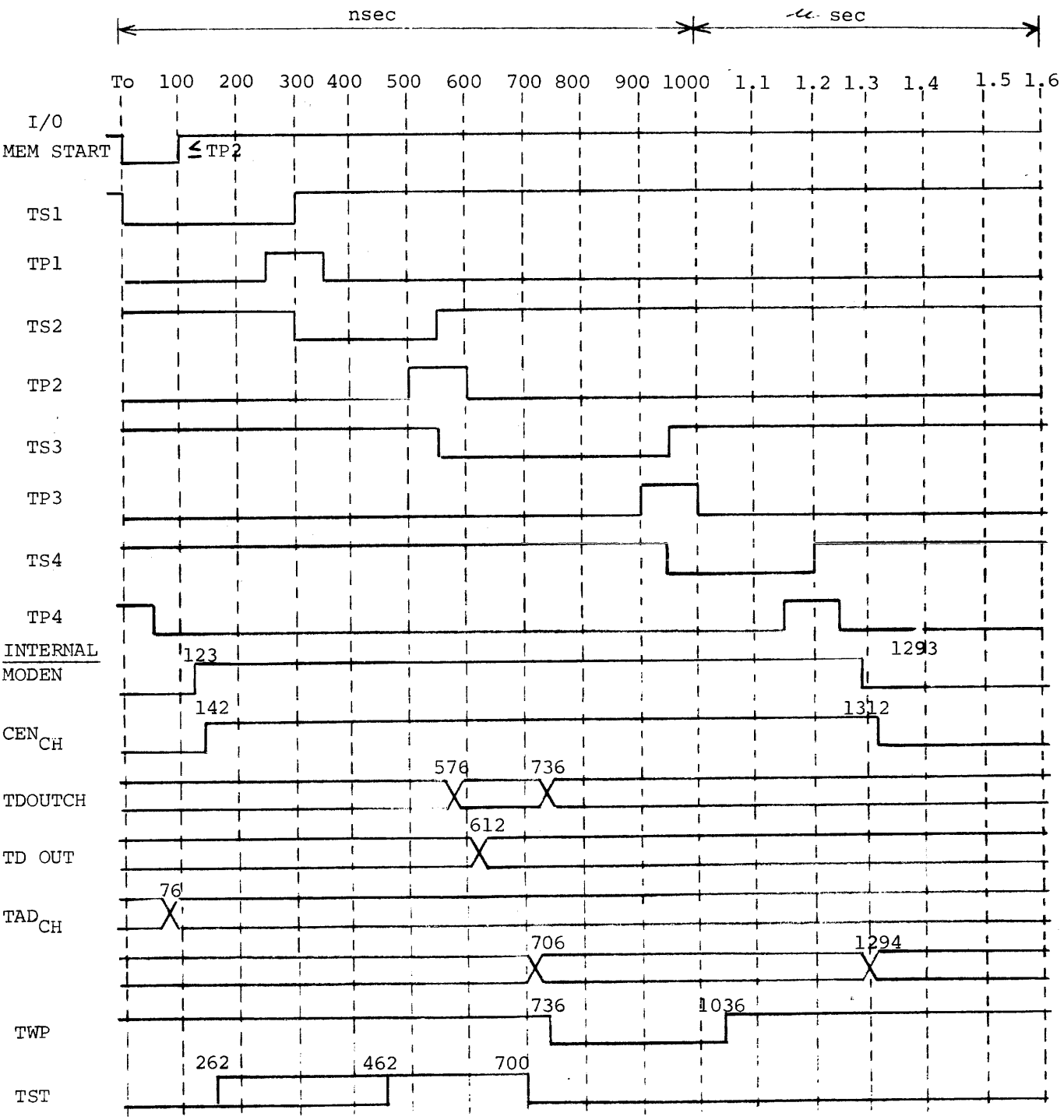
PDP-8



	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0023-000
	SCALE	REV A	SHEET 11

MSE—1005

SECTION IV

MAINTENANCE AND TROUBLESHOOTING

4.1 INTRODUCTION

This section presents troubleshooting instructions for ease of trouble location. Further localization of the trouble is to be found by means of the maintenance drawings in Section V. The theory of operation in Section III should be read and understood, along with a detailed review of the schematics in Section V in order to make effective use of this section.

4.2 PREVENTIVE MAINTENANCE

4.2.1 Visual Inspection

This inspection includes checking for loose programming wires, components, and discoloration of parts. The inspection should be performed with a minimum of prying or moving of parts.

4.2.2 Cleaning

Cleaning should be limited to removal of excess dust or particles. Never use any abrasive on any part of the gold fingers on the edge connectors. Low pressure compressed air can be used for removing dust or dirt and an aerosol cleaner can be used, with light brushing, to do the gold contacts.

4.2.3 DC Voltages

The +5V DC voltage should be maintained at:

$+5V \pm 5\%$

4.3 TROUBLESHOOTING

To facilitate troubleshooting the following information, cause and effect, can be used to isolate the problem to a particular area. From there on the schematics should be used to determine the exact component that is at fault.

Effect	Cause
Single bit failure, all addresses.	Data receiver/driver/read register
Complete word failure, all addresses.	DC voltage/WR pulse/strobe pulse.

4.3 Troubleshooting continued ...

Effect	Cause
Single bit failure, single address.	Memory element
Four bit failure, all addresses	Read register/read data I/O driver.
Complete word failure, a 1K section.	CENABLE driver/CEN programming jumpers/address circuit for MA0L and MA1L.
Complete or major part of word failure, all addresses	Address receiver/address buffer.
Non-retention of data.	DC voltage.

SECTION V

DRAWINGS

PARTS LIST	303-0112-000
ASSEMBLY	303-0112-000
SCHEMATIC	305-0112-000

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	ENG RELEASE ECO 0309	3-21-75	TSP

DASH NO	EQUIP REV LEVEL
002	A
001	A

REV	A	A	A	A																									
SHEET	1	2	3	4																									
REV STATUS OF SHEETS	REV																												
	SHEET																												

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES

MATERIAL

DATE

DRAWN LMG 1/6/75

CHECKED

APPROVED J. Waldenger

APPROVED

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MO-V PL/PDP8 ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0112-000

SCALE	REV	SHEET
	A	1 of 4

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
		002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		1	1	304-0112-001	P.C. Board			1
								2
		3	3	210-0003-10	I.C. SN7475	U1, 4 6		3
		3	3	210-0002-31	I.C. SN7408	U2, 3 5		4
		6	6	210-0002-02	I.C. SN74H04	U7, 9, 10, 12, 13, 18		5
		10	10	210-0015-01	I.C. SP380	U8,15,22,24,25,26,27,28,30,35		6
		3	3	210-0002-05	I.C. SN74H00	U11, 31, 32		7
		3	3	210-0002-08	I.C. SN74H10	U14, 19, 21		8
		2	2	210-0002-33	I.C. SN74H08	U16, 20		9
		3	3	210-0002-35	I.C. SN7438	U17, 33, 34		10
		1	1	210-0008-01	I.C. SN74155	U23		11
		1	1	210-0006-02	I.C. SN74123	U29		12
								13
		-	96	210-0028-002	Array 2102-1	U100-U195		14
		48	-					15
								16
								17
		25	25	201-0018-01	Cap. 6.8 F, 10V	C3-C27		18
		31	31	701-0001-03	Cap. .1 F, 50V	C28-58		19
		1	1	201-0006-006	CAP 15pf	C1.		20
		1	1	201-0006-046	CAP 100pf	C2		21
								22

SIZE A

CODE IDENT NO. 51513

DWG NO. PL 303-0112-000

Rev. A

SHEET 2 of 4

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
		002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		1	1	214-0002-026	RES. 11K 1/4W 5%	R1,		23
		1	1	214-0002-024	RES. 9.1K 1/4W 5%	R2		24
		14	14	208-0060-001	TERMINAL	1-8, A-F		25
								26
		2	2	208-0057-001	CARD PULLS			27
								28
		4	4	208-0011-002	RIVETS			29
								30
								31
								32
								33
								34
								35
								36
								37
								38
								39
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								44

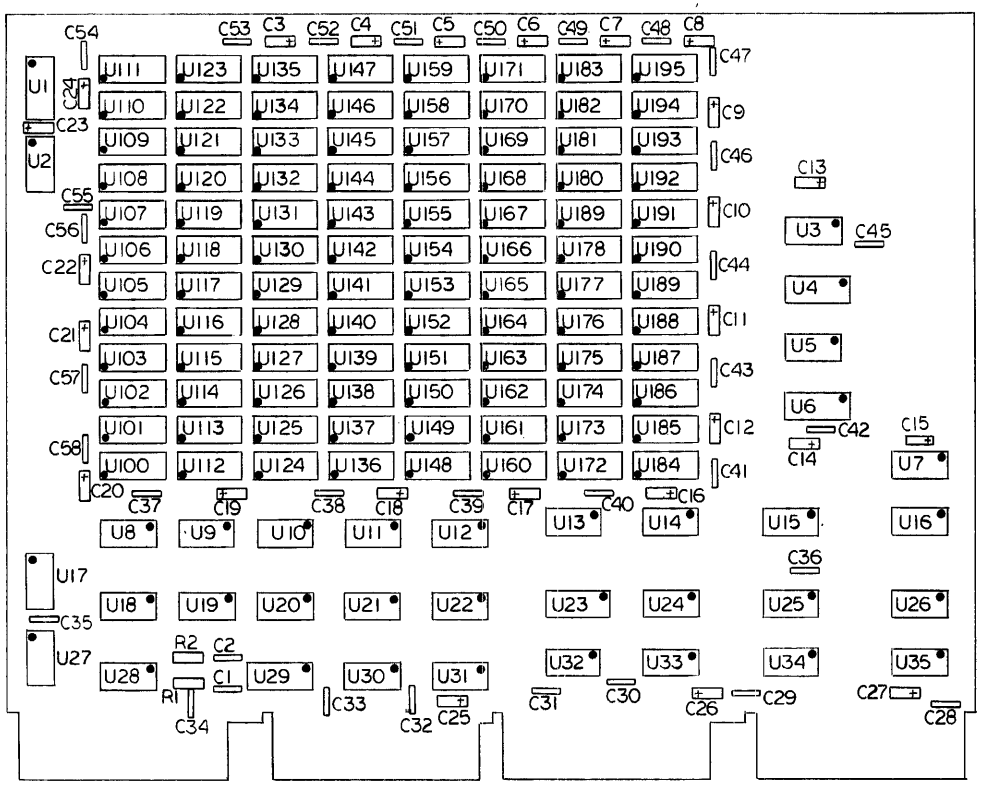
SIZE A

CODE IDENT NO. 51513

DWG NO. PL 303-0112-000

SHEET

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



COMPONENT SIDE

PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	ZONE	ITEM NO.
QTY/DASH NO.	LIST OF MATERIAL				

5 • INDICATES PIN 1 ON ALL I.C'S.

4 WHEN HERMETICALLY SEALED COMPONENTS AND ASSEMBLIES ARE NOT REQUIRED, THE DASH NOS. WILL BEGIN WITH 0XX. WHEN HERMETICALLY SEALED COMPONENTS AND ASSEMBLIES ARE REQUIRED, THE DASH NO. WILL BEGIN WITH 5XX. ASSEMBLIES WILL BE MARKED ACCORDINGLY.

3 FACTORY SERIAL NOS. TO BE MARKED IN A CLEAR AREA WITH NO DUPLICATION.

2 ASSEMBLY DASH NOS. TO BE MARKED PER 313-0003-006.

1 ASSEMBLY WORKMANSHIP PER 313-0001-001.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
AND ARE AFTER PLATING
TOLERANCES ON
FRACTIONS | DECIMALS .X .XX .XXX | ANGLES
± ± ± ± ±

MATERIAL

	DATE
DRAWN CB	3-2-75
CHECKED	
APPROVED	
APPROVED	
APPROVED	
APPROVED	

MONOLITHIC SYSTEMS CORP.

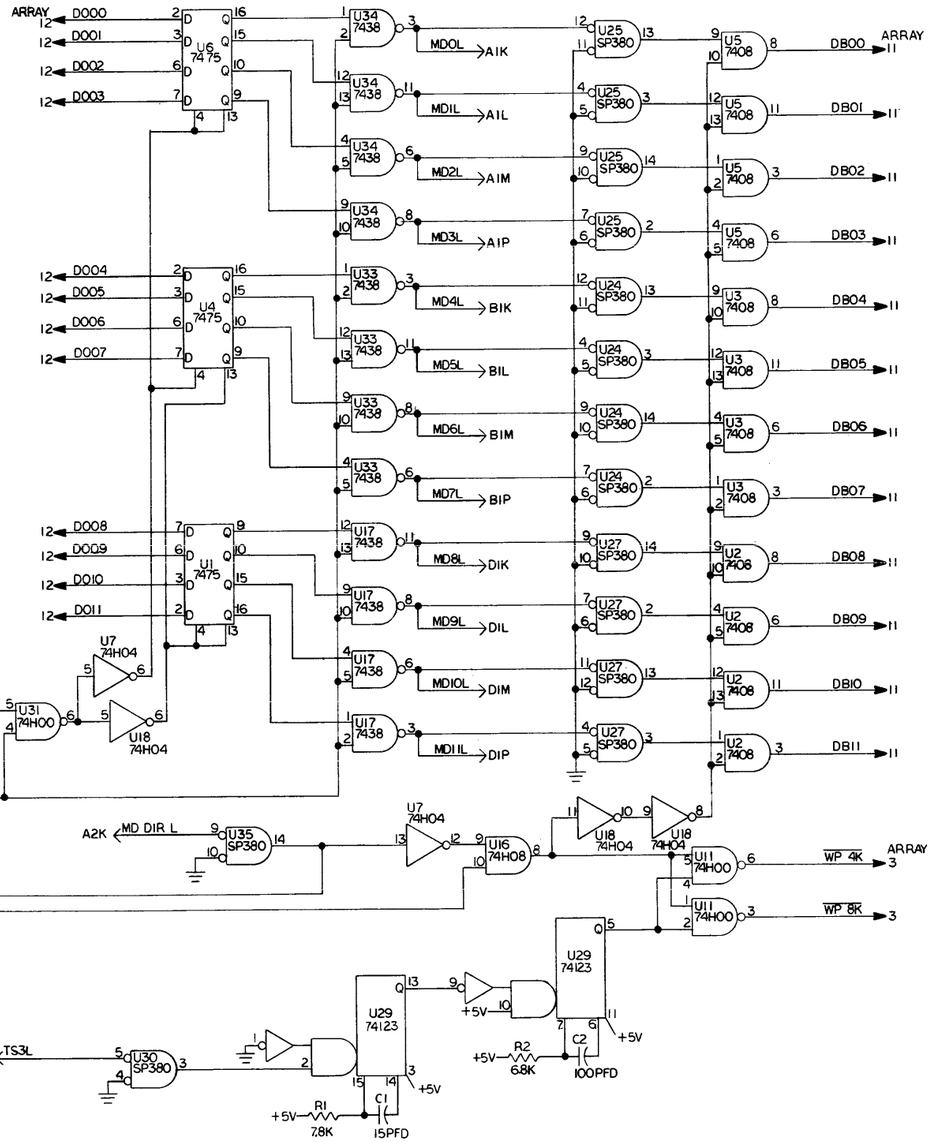
MOV PDP 8
BOARD ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.	REV
C	51513	303-0112-000	A

SCALE 1:1 SHEET 4 OF 4

MSF - 1009

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ENG RELEASE ECO 0309	3-21-75	TSP



NOTES (UNLESS OTHERWISE SPECIFIED)
1 ALL RESISTORS ARE 1/4W, ±5%
2 CAPACITORS ARE IN MICROFARADS.

PARTS LIST

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

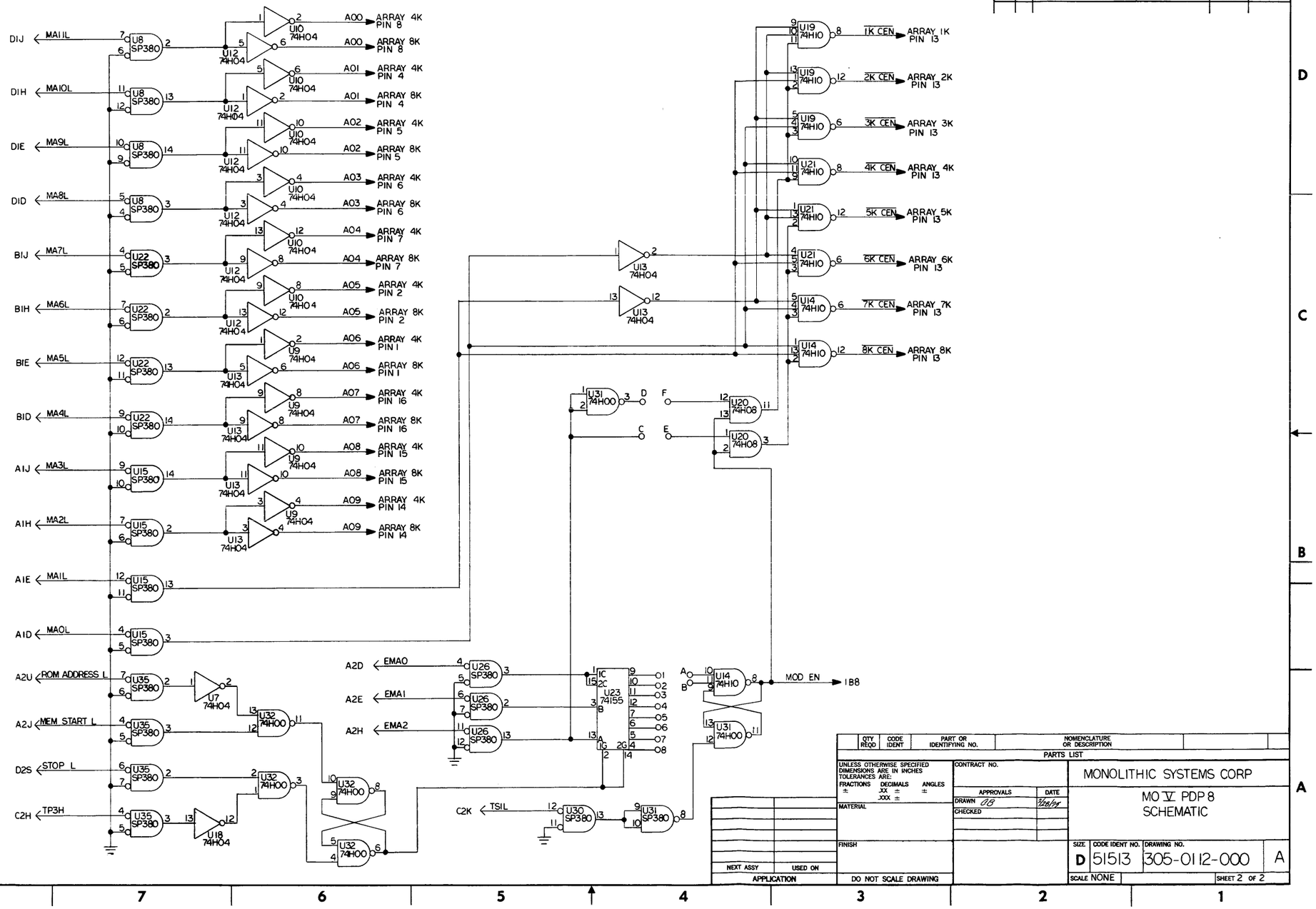
APPROVALS | DATE
DRAWN DB 2/26/75
CHECKED J. Waldinger 2/24/75

MONOLITHIC SYSTEMS CORP.

MOS PDP 8 SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.	
D	51513	305-0112-000	A

SCALE | SHEET 1 OF 2



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN DB	7/28/78
CHECKED	

MONOLITHIC SYSTEMS CORP

MOS PDP 8
SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.	
D	51513	305-0112-000	A

SCALE NONE | SHEET 2 OF 2