

LISPM I/O BOARD

CADRIO: IOB UML
***** DIP MAP *****

18-DEC-80 1049

75118 IOBKBD x	75118 IOBKBD x	74LS374 IOBKBD x	74LS374 IOBKBD x	74LS74 IOBKBD xx	74LS164 IOBKBD x
F30	E30	D30	C30	B30	A30
74LS74 IOBSEr xx	74LS244 IOBSEr x	74LS244 IOBCSR x	74LS374 IOBKBD x	74LS569 IOBMS2 x	74LS164 IOBKBD x
F29	E29	D29	C29	B29	A29
74S374 CLK60H x	74S374 CLK60H x	74LS244 CLKTOD x	74LS10 IOBKBD xxx	74LS569 IOBMS2 x	74LS164 IOBKBD x
F28	E28	D28	C28	B28	A28
74LS244 CLK60H x	74LS244 CLK60H x	74LS175 IOBCSR x	74LS74 IOBCSR xx	74LS569 IOBMS2 x	74LS14 IOBKBD OXXXXX
F27	E27	D27	C27	B27	A27
74LS374 CLKTOD x	74LS374 CLKTOD x	74LS08 IOBKBD xxxx	74LS109 IOBKBD xx	74LS569 IOBMS2 x	74LS86 IOBMS2 xxxo
F26	F26	D26	C26	B26	A26
74LS374 CLKTOD x	74LS374 CLKTOD x	74LS32 IOBCLK xxxx	74 37 IOBCLK xxoo	74LS569 IOBMS2 x	74LS14 IOBMSE xxxxxx
F26	E26	D26	C26	B26	A26
74 393 CLKTOD xx	74 393 CLKTOD xx	74LS163 IOBCLK x	74LS244 IOBMS2 x	74LS569 IOBMS2 x	74LS374 IOBMSE x
F24	E24	D24	C24	B24	A24
74 393 CLKTOD xx	74 393 CLKTOD xx	74 393 CLKTOD xx	74LS74 IOBCLK xx	74LS86 IOBMS2 xxxxx	74LS374 IOBMSE x
F23	E23	D23	C23	B23	A23
74LS163 CLKTIM x	74LS193 CLKTIM x	74 393 CLKTOD xx	74LS13E IOBCLK x	74LS244 CLKTOD x	74LS374 IOBMSE x
F22	E22	D22	C22	B22	A22
74LS193 CLKTIM x	74LS193 CLKTIM x	74LS74 IOBSEr xx	74S163 CLKTIM x	74LS138 CLK60H x	26LS2521 IOBMSE x
F21	F21	D21	C21	B21	A21
DM8838 IOBXCv x	74LS138 IOBADR x	74LS14 CLK60H xxooo	DUMMY20 CLK60H x	74LS174 LMUCOM x	26LS2521 IOBCSR x
F20	E20	D20	C20	B20	A20

LISPM I/O BOARD

***** CADRIO:IOB UML
DIP MAP *****

18-DEC-80 1050

DM8838 IOBXCX x	74S133 IOBADR x	74LS244 LMDATP x	74S133 LMUCON, x	74LS164 LMTURN x	74LS193 LMTURN x
F19	E19	D19	C19	B19	A19
DM8838 IOBXCX x	74LS244 LMDATP x	74LS244 LMDATP x	74LS138 LMUCON x	74LS164 LMTURN x	74LS193 LMTURN x
F18	E18	D18	C18	B18	A18
DM8838 IOBXCX x	74LS244 LMDATP x	74LS244 LMDATP x	74LS244 LMDATP x	MC1488L IOBSER x	74LS193 LMTURN x
F17	E17	D17	C17	B17	A17
74S38 IOBINT xxxx	----- ----- -----	74LS244 LMDATP x	74LS244 LMDATP x	MC1489L IOBSER xxxx	74LS161 LMTURN x
F16	E16	D16	C16	B16	A16
74S38 IOBCSR xxxx	----- ----- -----	74S32 LMRCTL xxxx	74S00 LMTBFC xxxx	74S74 LMMODU xx	EXAR-CL IOBSER x
F15	E15	D15	C15	B15	A15
74S175 IOBINT x	74S260 IOBINT xx	74S112 LMTURN xx	74S00 LMTBFC xxxx	74S04 LMTBFC xxxxxx	----- ----- -----
F14	E14	D14	C14	B14	A14
TD100 IOBINT x	74S04 IOBADR xxxxxx	74S112 LMTBFC xx	25LS193 LMTBUF x	74 165 LMTBUF x	----- ----- -----
F13	E13	D13	C13	B13	A13
74S00 IOBINT xxxx	74LS00 IOBINT xxxx	DUMMY LMYNM x	25LS193 LMTBUF x	74 165 LMTBUF x	2651 IOBSER x
F12	E12	D12	C12	B12	A12
74LS10 IOBINT xxx	74LS02 IOBSER xxxx	P SIP100 LMYNM x	25LS193 LMTBUF x	TD100 LMDETC x	TD25 LMDETC x
F11	E11	D11	C11	B11	A11
DM8838 IOBINT x	74S08 LMRCTL xxxx	DUMMY LMYNM x	2147 LMTBUF x	74S08 LMTBFC xxxx	74S268 LMMODU x
F10	E10	D10	C10	B10	A10
DM8136 IOBADR x	TD260 IOBADR x	74 279 LMRCTL xxox	9401 LMTBUF x	74S04 LMDETC xxxxxx	74S112 LMMODU xx
F09	E09	D09	C09	B09	A09

LISPM I/O BOARD

***** CADRIO:IOB UML
***** DIP MAP *****

18-DEC-80 1062

DM8136 IOBADR x	74S74 IOBADR xx	74S74 LMRCTL xx	74S51 LMRBUF xx	74S02 LMTBFC xxxx	74S374 LMMODU x
F08	E08	D08	C08	B08	A08
DM8837A IOBXCVC x	74S37 IOBADR xxxx	74S00 LMRBUF xxxx	9401 LMRBUF x	74LS164 LMRBUF x	74LS164 LMRBUF x
F07	E07	D07	C07	B07	A07
DM8837A IOBXCVC x	74S251 LMMYNN x	25LS193 LMRBUF x	74S74 LMRCLK xx	74LS161 LMRCLK x	74S112 LMTCLK xx
F06	E06	D06	C06	B06	A06
74S251 LMMYNN x	74S51 LMRBUF xx	25LS193 LMRBUF x	74S37 LMRBUF xxxx	74LS161 LMRCLK x	EXAR-CL LMTCLK x
F05	E05	D05	C05	B05	A05
74LS161 LMMYNN x	74S00 LMUCON xxxx	25LS193 LMRBUF x	2147 LMRBUF x	TD100 LMDETC x	26S02 LMRCTL xx
F04	E04	D04	C04	B04	A04
74LS161 LMMYNN x	74S00 LMRCTL xxxx	74S04 LMTCLK xxxxxx	TD250 LMRCLK x	74S183 LMTCLK x	DUMMY LMLNDR x
F03	E03	D03	C03	B03	A03
74LS161 LMMYNN x	74S158 LMLNDR x	74S10 LMMODU xxx	74S08 LMRBUF xxxx	74S74 LMDETC xx	26LS31 LMLNDR xxxx
F02	E02	D02	C02	B02	A02
74S11 LMMODU 0x0	74S174 LMMYNN x	74S287 LMMYNN x	74S74 LMDETC xx	74S04 LMRCLK xxxxxx	26LS33 LMLNDR xxxx
F01	E01	D01	C01	B01	A01

LISPM I/O BOARD CADRIO:IOB UML 18-DEC-80 1053
 ***** EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *****

-E- -F- -J01- -J02-

A1 GND	# A1	01 GND	# 01
A2 +5.0V+++++	A2 +5.0V+++++	02 INTERFERE+	02
B1	B1	03 INTERFERE-	03
B2 -5.0V	B2 -5.0V	04 GND	04
C1 -A12*	# C1	05 RCVR.DATA+	05
C2 GND-----	C2 GND-----	06 RCVR.DATA-	06
D1 -A17*	D1 -BBSY*	# 07 GND	# 07
D2 -A16*	D2	08 TRANS.DATA+	08
E1 -MSYN*	E1 H SYNC	09 TRANS.DATA-	09
E2 -A16*	E2 V SYNC	10 GND	10
F1 -A2*	F1 NC	# 11	11
F2 -C1*	F2	12	12
H1 -A1*	H1	13	13
H2 -A0*	H2	14	14
J1 -SSYN*	# J1 -NPR*	15	15
J2 -C0*	J2	16	16
K1 -A14*	K1	17	17
K2 -A13*	K2	18	18
L1 -A11*	L1	19	19
L2	L2	20	20
M1	# M1 -INTR*	# 21	21
M2 GND	M2	22	22
N1 GND	# N1 NC	# 23	23
N2 -A8*	N2	24	24
P1 -A10*	P1	25	25
P2 -A7*	P2	26 GND-----	# 26 -----
R1 -A9*	R1	27 GND-----	# 27 -----
R2	R2	28 GND-----	# 28 -----
S1	# S1	29 GND-----	# 29 -----
S2 GND	S2	30 GND-----	# 30 -----
T1 GND-----	# T1 GND-----	# 31 GND-----	# 31 -----
T2	T2 -SACK*	# 32 GND-----	# 32 -----
U1 -A6*	U1	33 GND-----	# 33 -----
U2 -A4*	U2	34 GND-----	# 34 -----
V1 -A5*	V1	35 GND-----	# 35 -----
V2 -A3*	V2 POWER LINE ~↓	36 GND-----	# 36 -----
		37 -----	37 -----
		38 -----	38 -----
		39 -----	39 -----
		40 -----	40 -----
		41 -----	41 -----
		42 -----	42 -----
		43 -----	43 -----
		44 -----	44 -----
		45 -----	45 -----
		46 -----	46 -----
		47 -----	47 -----
		48 -----	48 -----
		49 -----	49 -----
		50 -----	50 -----

LISPM I/O BOARD

CADRIO: IOB UML

18-DEC-80 1053

***** EDGE CONNECTIONS

Flags: (# Output: R Terminator, ---- Dedicated ground, ++++ Dedicated power) *****

-J03-

-J04-

-J05-

-J06-

01 H SYNC	01	01 GPI0	01
02 V SYNC	02	02 GPI1	02
03 FH1	03	03 GPI2	03
04	04	04 GPI3	04
05	05	05 GPI4	05
06	06	06 GPI5	06
07	07	07 GPI6	07
08	08	08 GPI7	08
09	09	09 GPI8	09
10 AUDIO+ *	10	10 GPI9	10
11 KBDCLK+ *	11	11 GPO0	# 11
12 KBDIN+ *	12	12 GPO1	# 12
13 *VERB	13	13 GPO2	# 13
14 *VERA	14	14 GPO3	# 14
15 *HORB	15	15 GPO4	# 15
16 *HORA	16	16 GPO5	# 16
17 *HEADSW	17	17 GPO6	# 17
18 *MIDSW	18	18 GPO7	# 18
19 *TAILSW	19	19 GPO8	# 19
20	20	20 GPO9	# 20
21 -----	21 -----	21	21
22 -----	22 -----	22	22
23 FH2-----	23 -----	23	23
24 -----	24 -----	24	24
25 -----	25 -----	25	25
26 -----	26 -----	26	26
27 -----	27 -----	27	27
28 -----	28 -----	28	28
29 -----	29 -----	29	29
30 AUDIO- *	30 -----	30	30
31 KBDCLK- *	31 -----	31	31
32 KBDIN- *	32 -----	32	32
33 GND-----	# 33 -----	33	33
34 GND-----	# 34 -----	34	34
35 GND-----	# 35 -----	35	35
36 GND-----	# 36 -----	36	36
37 GND-----	# 37 -----	37	37
38 GND-----	# 38 -----	38	38
39 GND-----	# 39 -----	39	39
40 -----	40 -----	40	40
		41 -----	41 -----
		42 -----	42 -----
		43 -----	43 -----
		44 -----	44 -----
		45 -----	45 -----
		46 -----	46 -----
		47 -----	47 -----
		48 -----	48 -----
		49 -----	49 -----
		50 -----	50 -----

LISPM I/O BOARD

CADRIO:IOB UML

18-DEC-80 1054

***** EDGE CONNECTIONS

Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *****

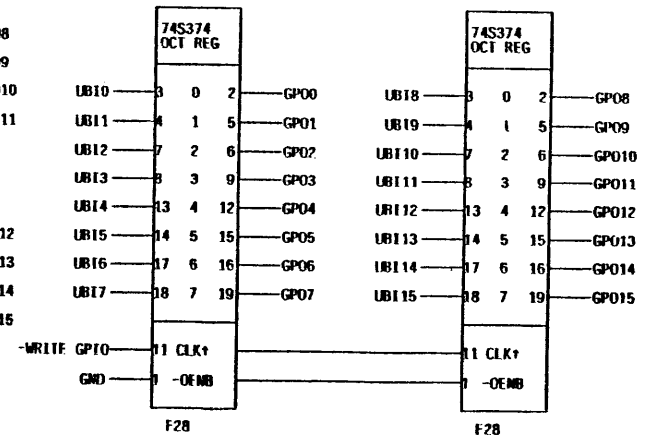
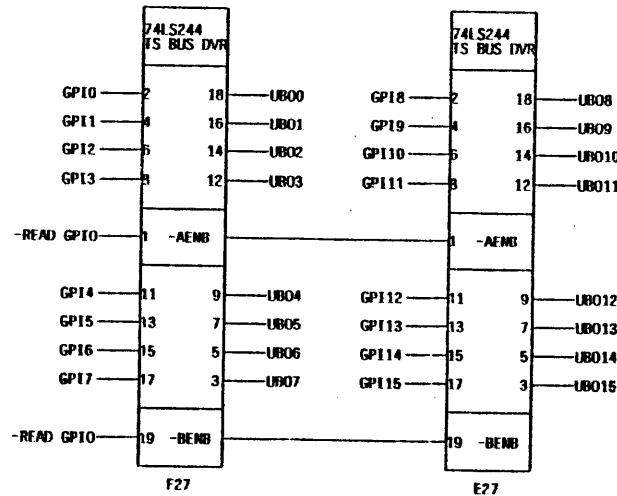
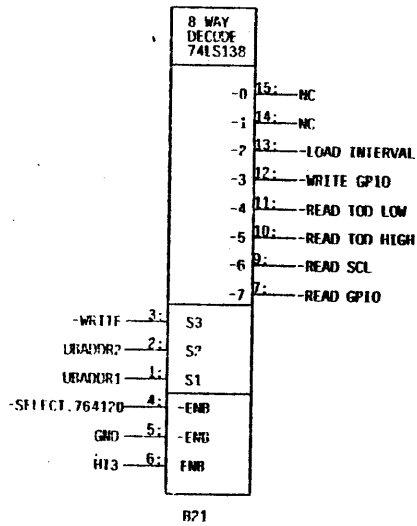
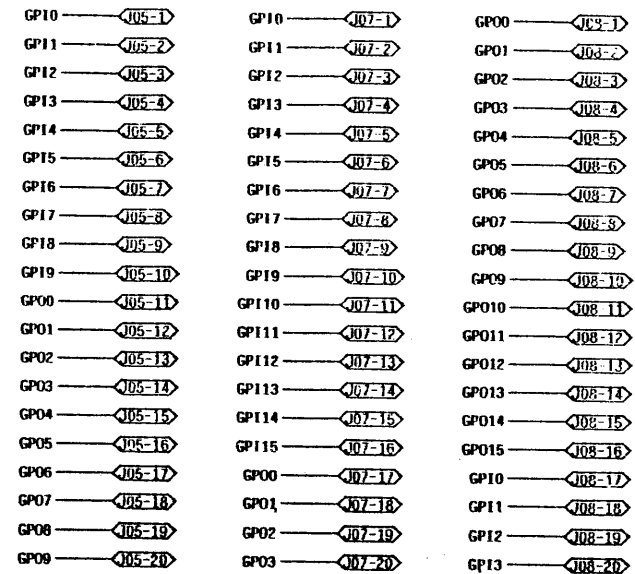
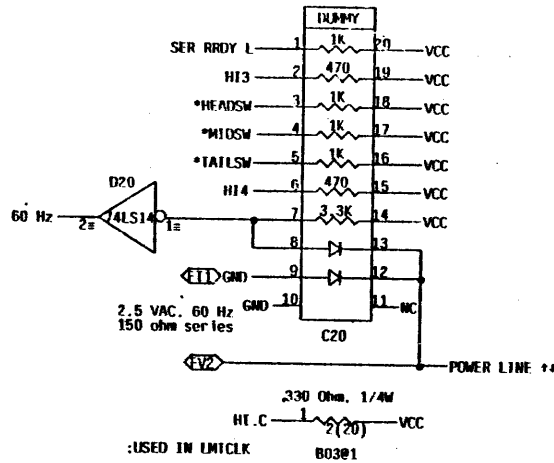
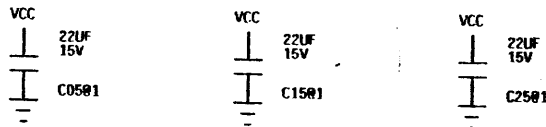
-J07-

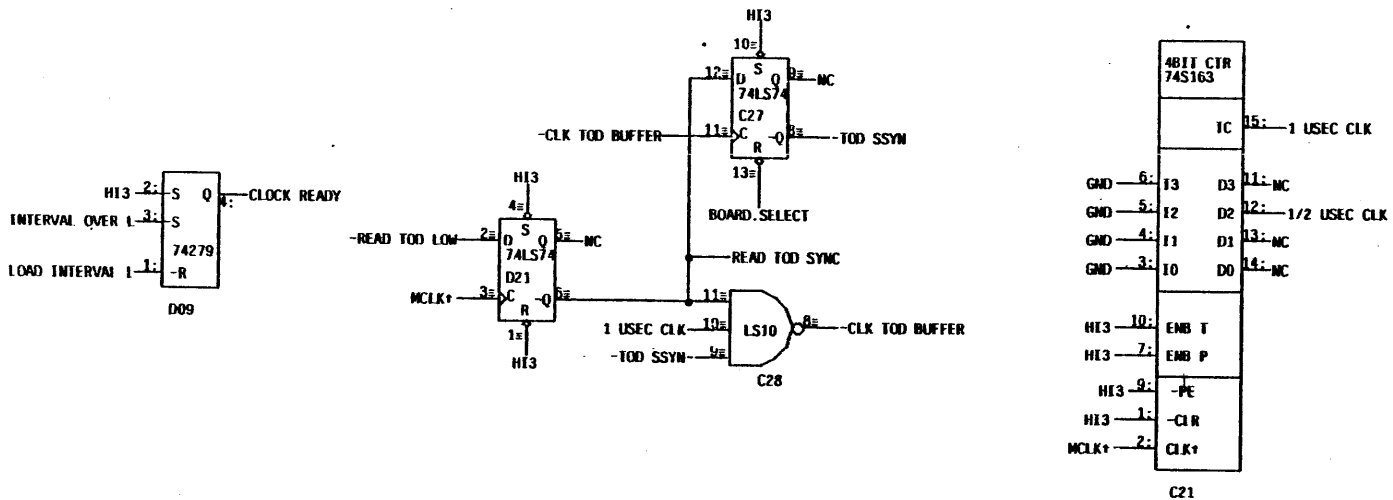
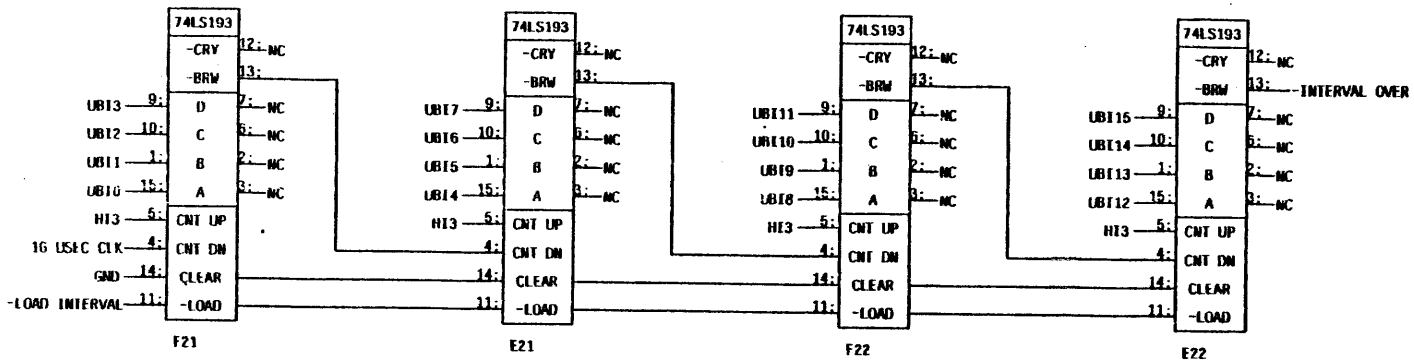
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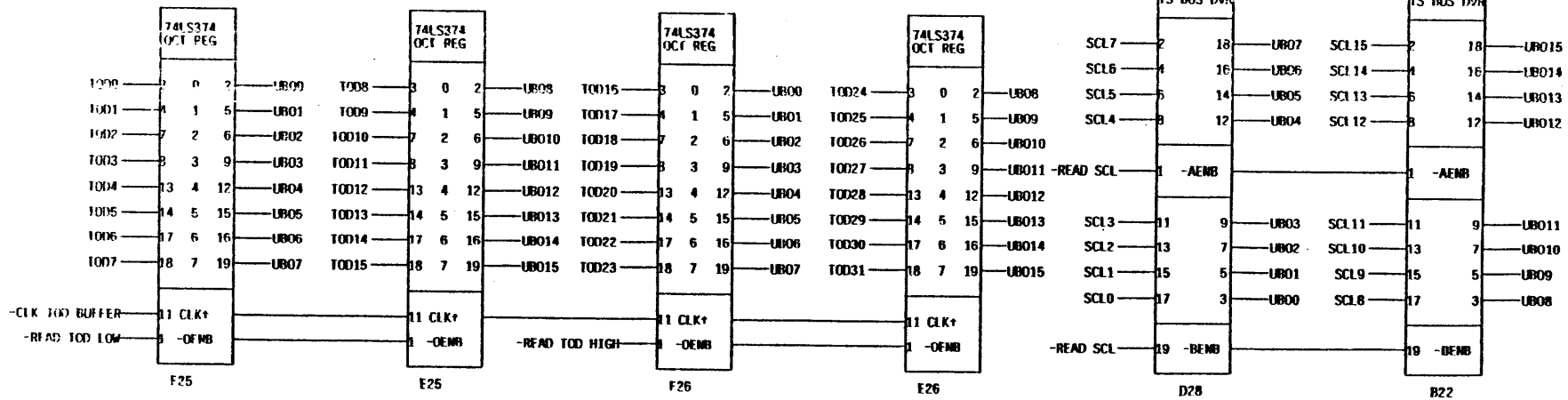
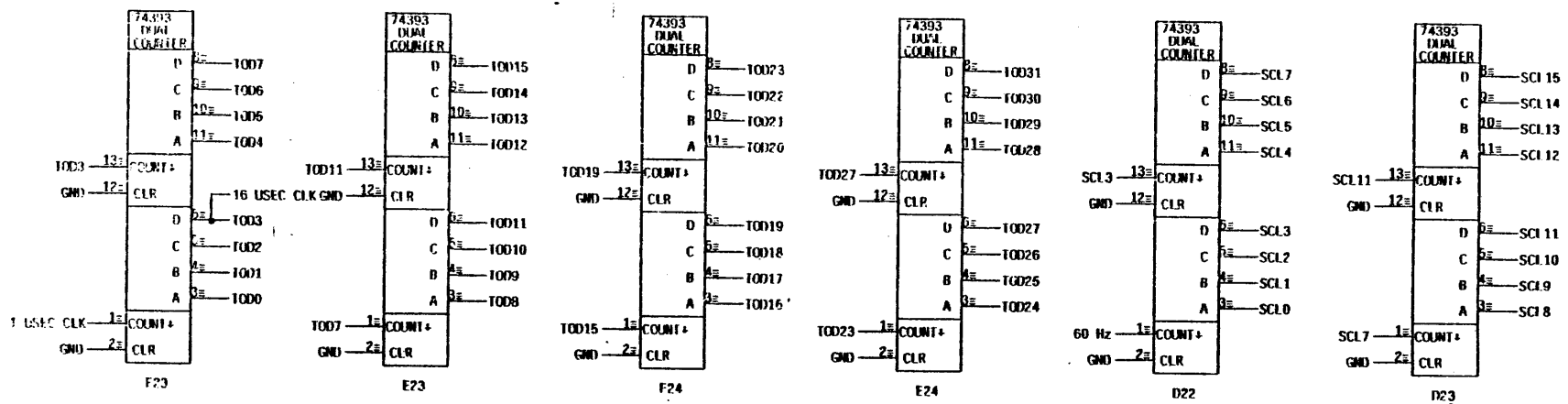
-J09-

-J10-

01 GPI0	01 GPO0	#01 EIA DATA OUT	#01
02 GPI1	02 GPO1	#02 EIA DATA IN	02
03 GPI2	03 GPO2	#03 EIA RTS OUT	#03
04 GPI3	04 GPO3	#04 EIA CTS IN	04
05 GPI4	05 GPO4	#05 EIA DSR IN	05
06 GPI5	06 GPO5	#06 EIA DCD IN	06
07 GPI6	07 GPO6	#07 EIA DTR OUT	#07
08 GPI7	08 GPO7	#08	08
09 GPI8	09 GPO8	#09	09
10 GPI9	10 GPO9	#10	10
11 GPI10	11 GPO10	#11	11
12 GPI11	12 GPO11	#12	12
13 GPI12	13 GPO12	#13	13
14 GPI13	14 GPO13	#14	14
15 GPI14	15 GPO14	#15	15
16 GPI15	16 GPO15	#16	16
17 GPO0	#17 GPI0	17	17
18 GPO1	#18 GPI1	18	18
19 GPO2	#19 GPI2	19	19
20 GPO3	#20 GPI3	20	20
21 -----	21 -----	21	21
22 -----	22 -----	22	22
23 -----	23 -----	23	23
24 -----	24 -----	24	24
25 -----	25 -----	25	25
26 -----	26 -----	26 GND-----	#26 -----
27 -----	27 -----	27 GND-----	#27 -----
28 -----	28 -----	28 -----	28 -----
29 -----	29 -----	29 -----	29 -----
30 -----	30 -----	30 -----	30 -----
31 -----	31 -----	31 -----	31 -----
32 -----	32 -----	32 -----	32 -----
33 -----	33 -----	33 -----	33 -----
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		44 -----	44 -----
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		46 -----	46 -----
		47 -----	47 -----
		48 -----	48 -----
		49 -----	49 -----
		50 -----	50 -----







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 <E1> — NC
 <W1> — NC
 <I1> — GND
 <A2> — GND
 <E1> — NC
 <W1> — NC
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 <E1> — GND
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 <E2> — GND
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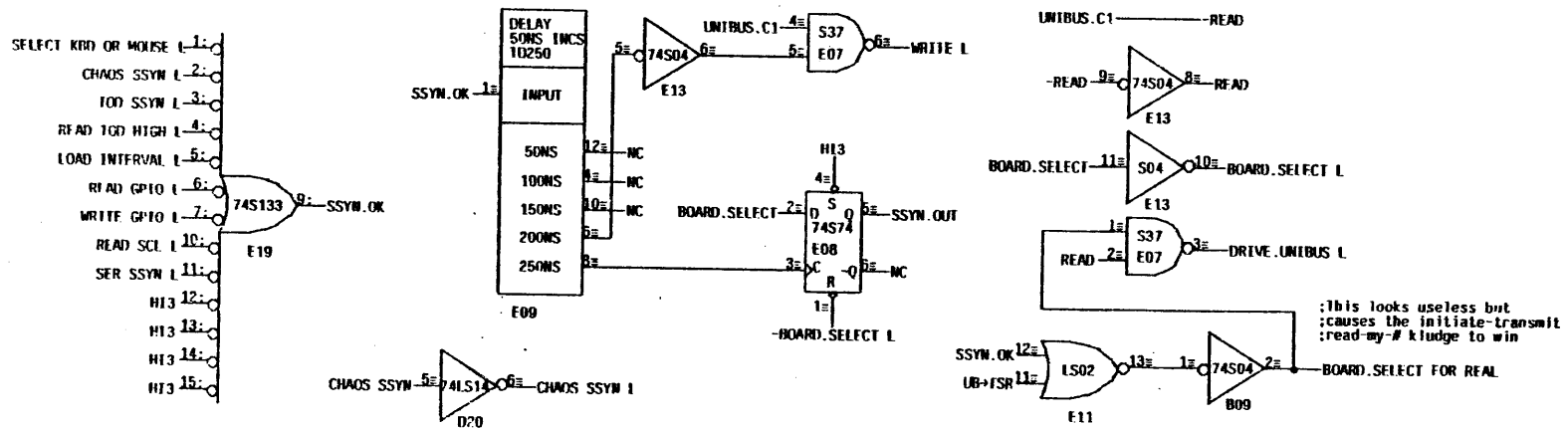
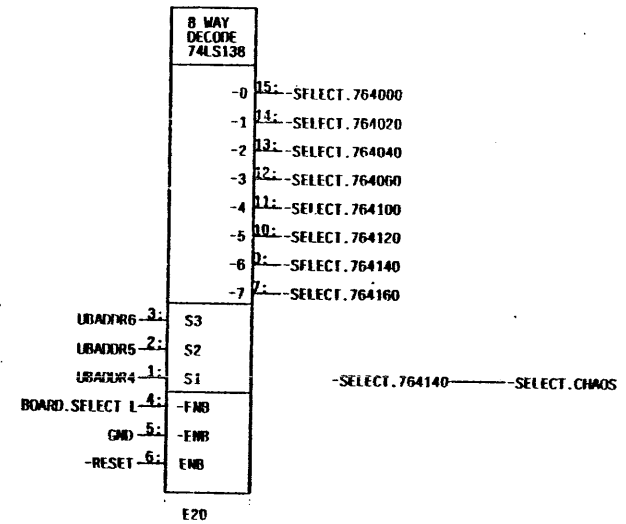
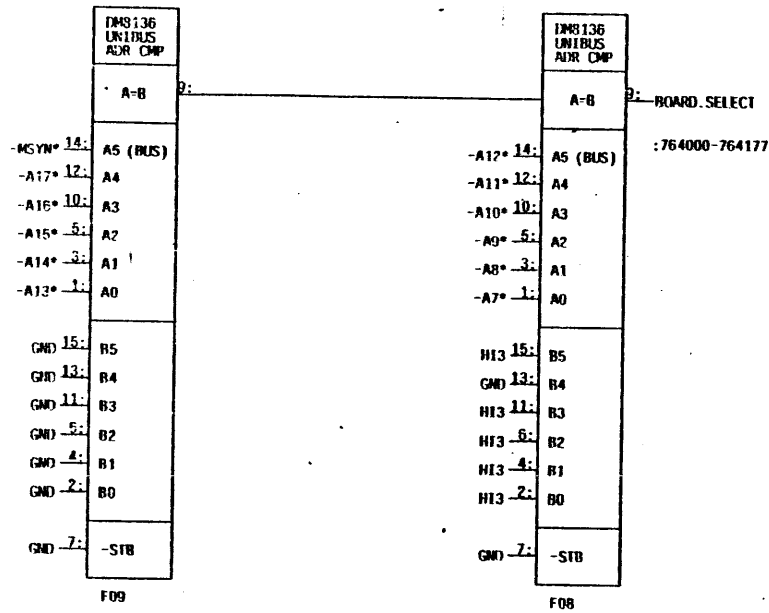
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 <B2> — -5V
 <E2> — -5V
 <E2> — -5V

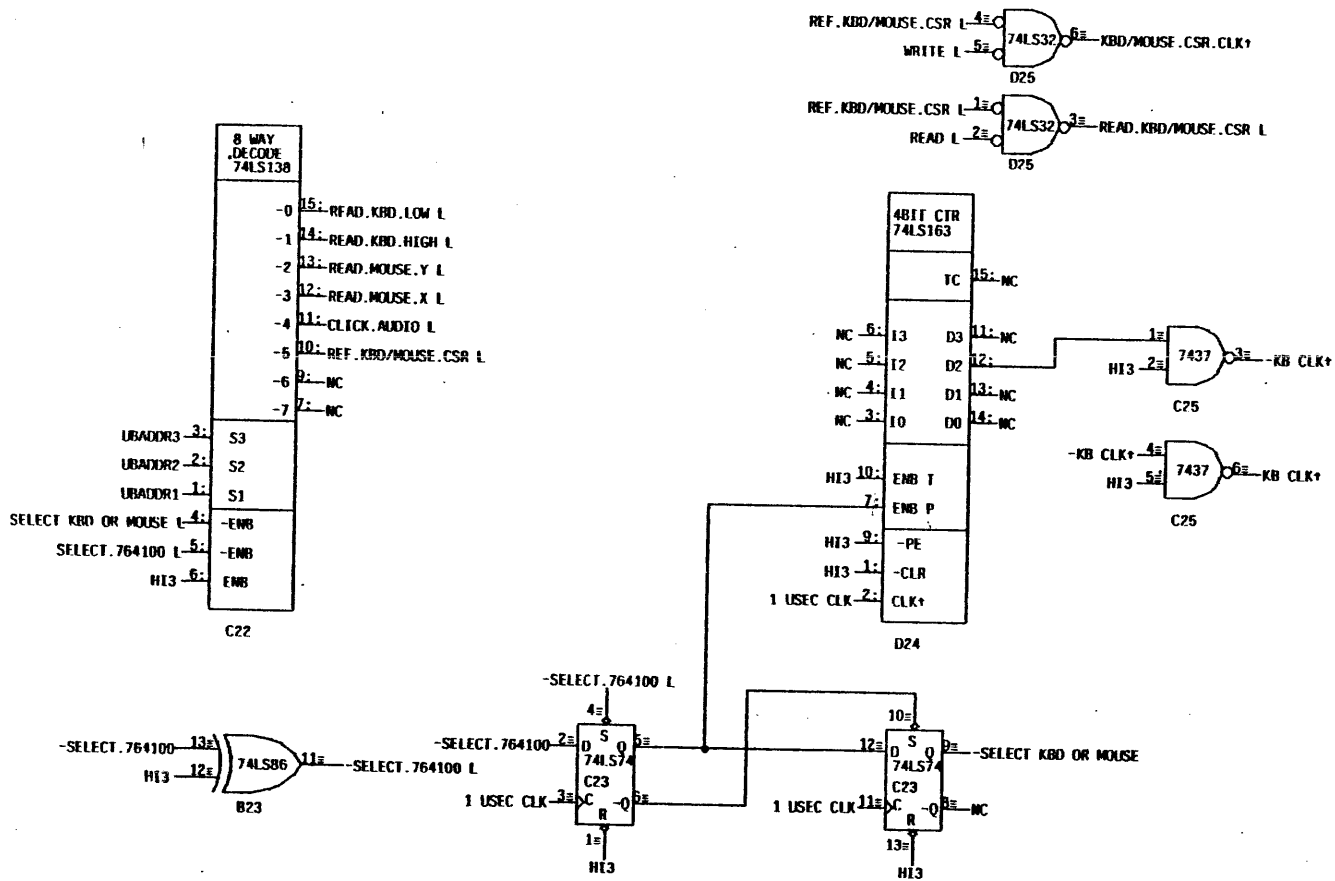
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 <A2> — +5V
 <A2> — +5V
 <A2> — +5V

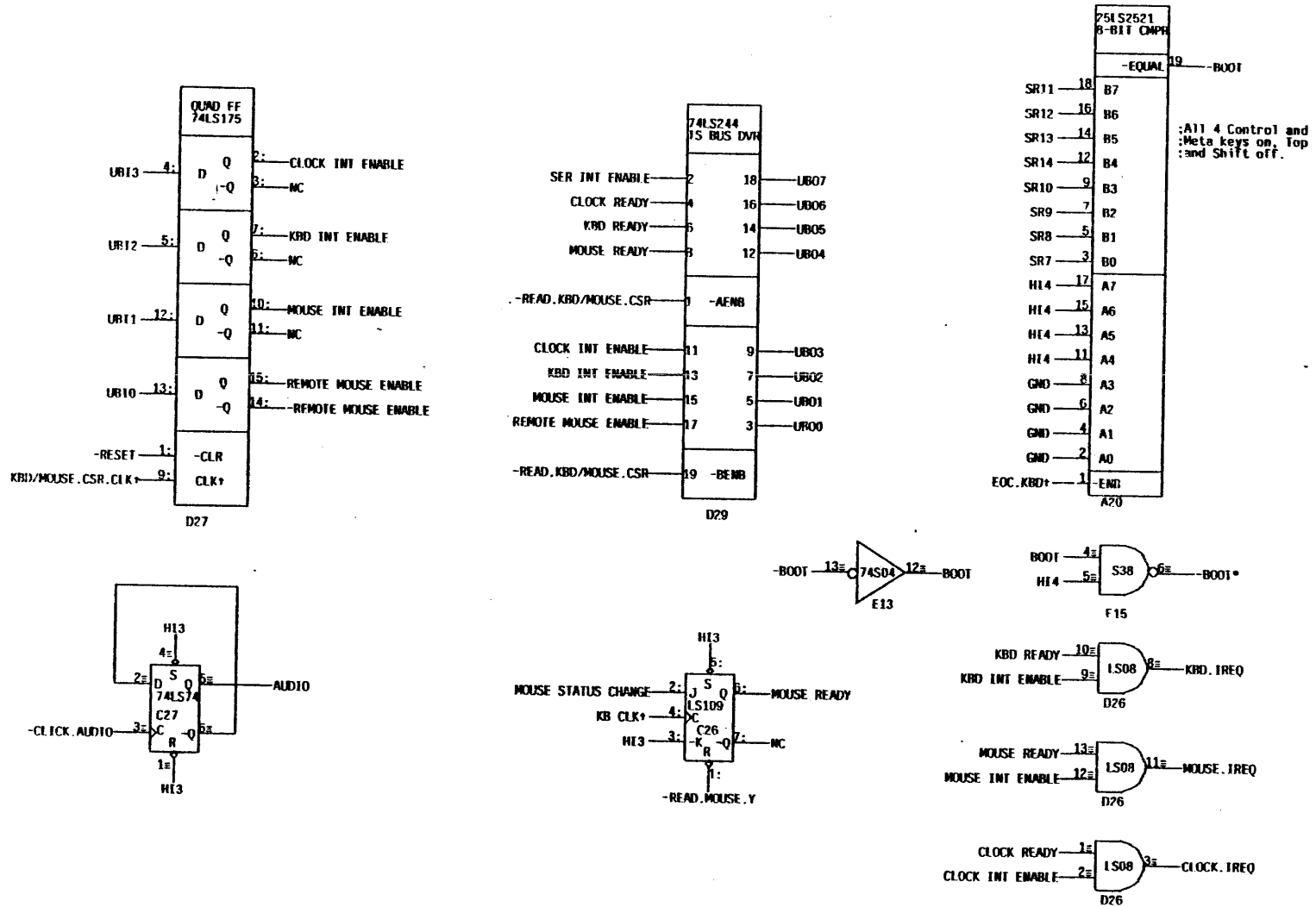
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 <E2> — D1*
 <U2> — D2*
 <I2> — D3*
 <E2> — D4*
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 <E2> — D13*
 <E2> — D14*
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 <E1> — MSYN*
 <E11> — SSM*
 <E2> — C0*
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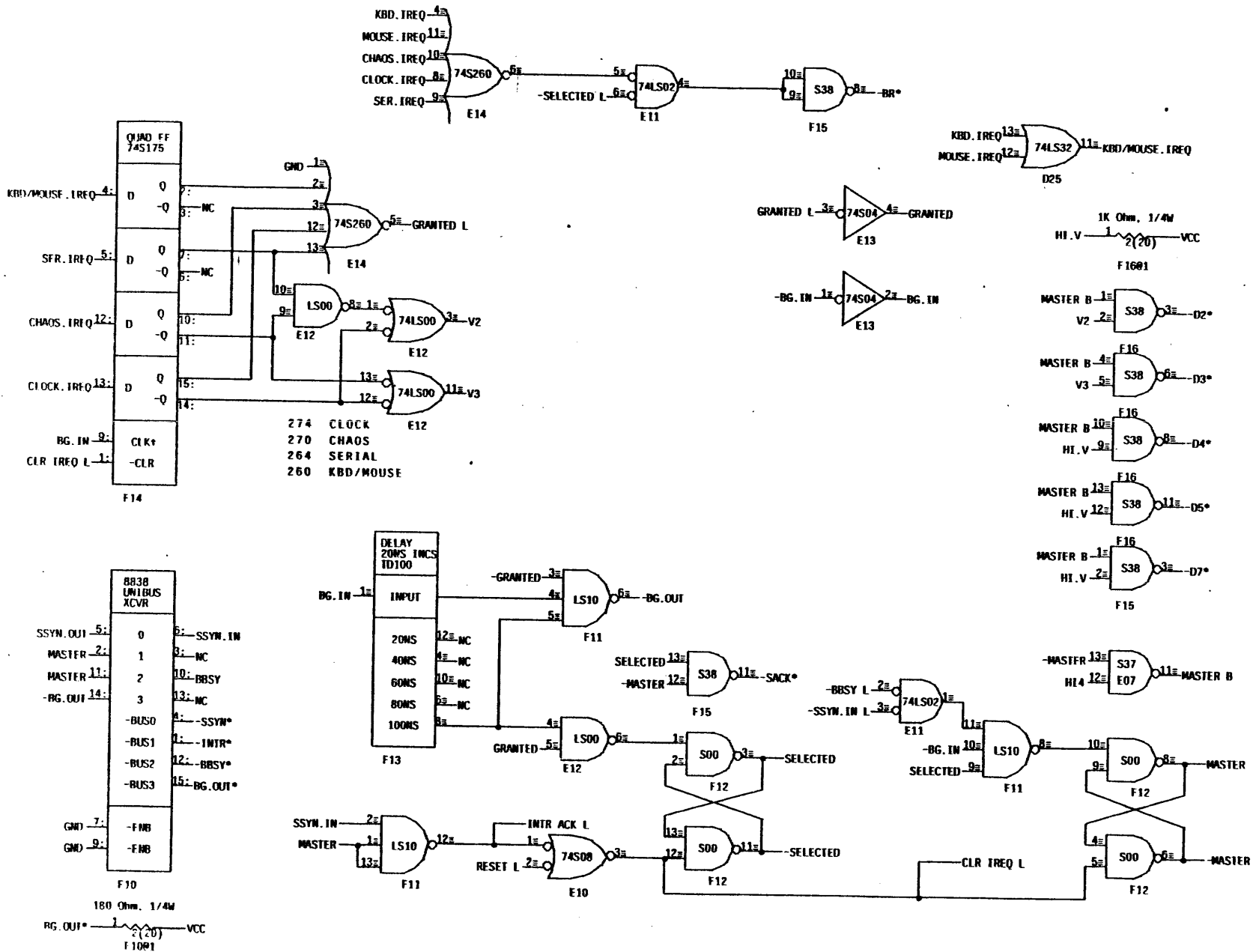
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 <E2> — A13*
 <E11> — A14*
 <E2> — A15*
 <E2> — A16*
 <E11> — A17*
 <E11> — BOOT*

<E11> — NPG.IN*
 <E11> — NPG.OUT*
 <E2> — BR7*
 <E2> — BR6*
 <E2> — BR5*
 <E2> — BR4*
 <E11> — IN11*
 <E2> — BG7.IN*
 <E2> — BG7.OUT*
 <E2> — BG6.IN*
 <E2> — BG6.OUT*
 <E2> — BG5.IN*
 <E2> — BG5.OUT*
 <S2> — BG4.IN*
 <E2> — BG4.OUT*
 <E11> — BBSY*
 <E11> — NPR*
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 <E2> — SACK*





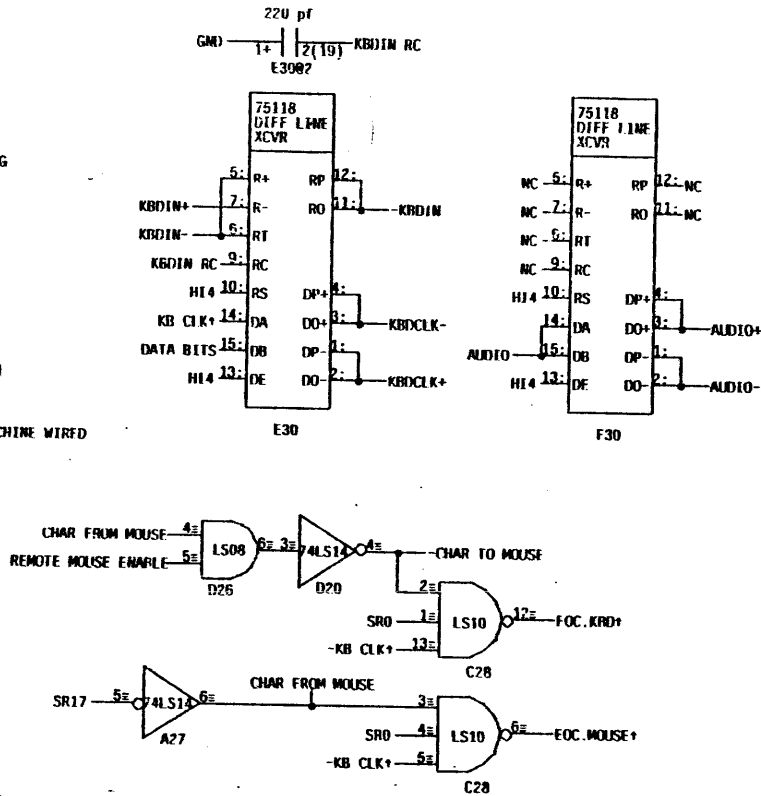
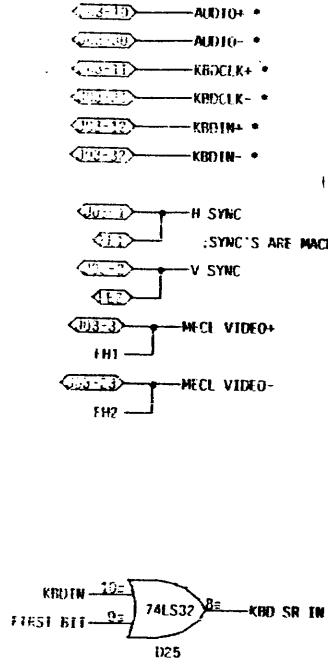




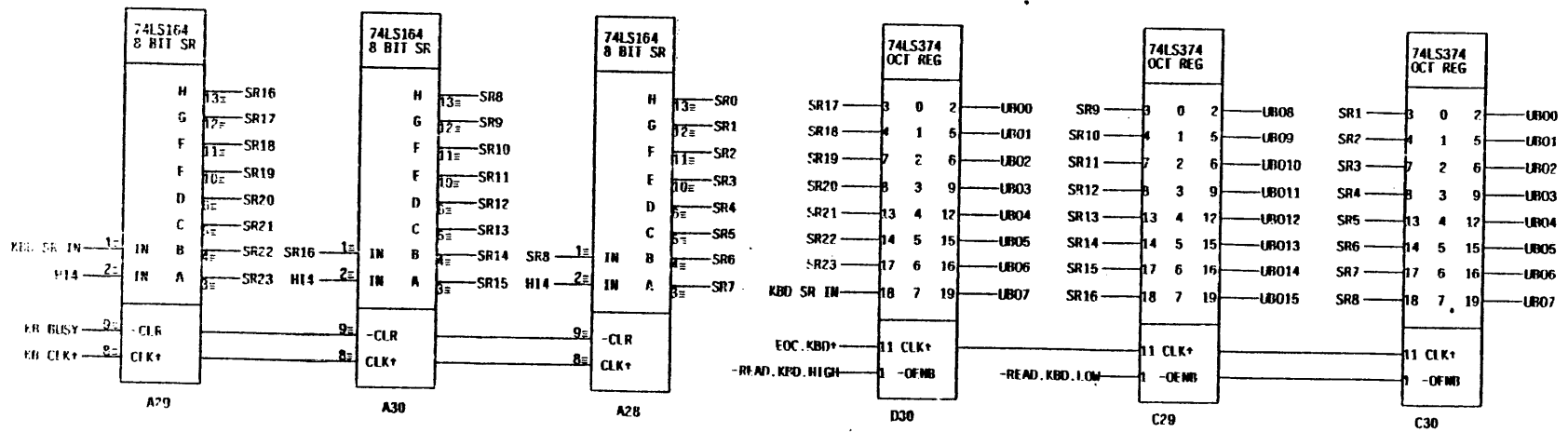
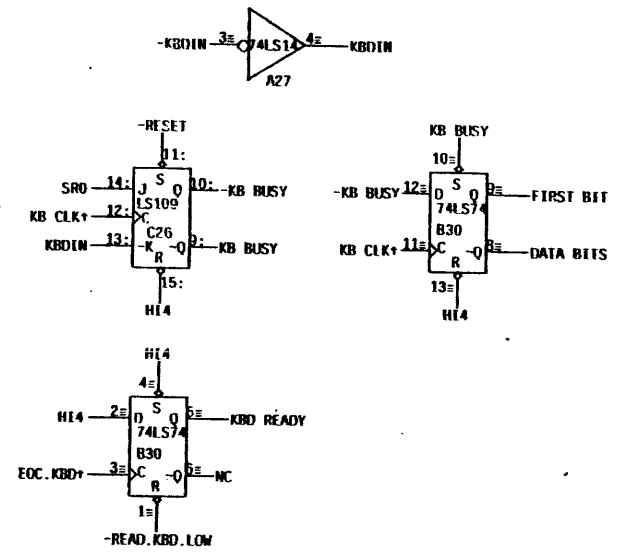
GND	→ J01-1	← J01-26	GND
INTERFERE+	→ J01-2	← J01-27	GND
INTERFERE-	→ J01-3	← J01-28	GND
GND	→ J01-4	← J01-29	GND
RCVR.DATA+	→ J01-5	← J01-30	GND
RCVR.DATA-	→ J01-6	← J01-31	GND
GND	→ J01-7	← J01-32	GND
TRANS.DATA+	→ J01-8	← J01-33	GND
TRANS.DATA-	→ J01-9	← J01-34	GND
GND	→ J01-10	← J01-35	GND

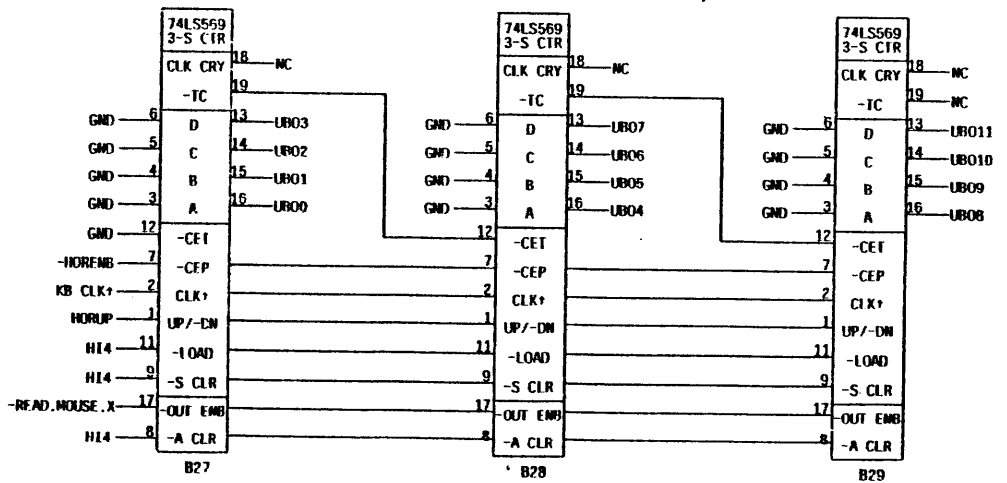
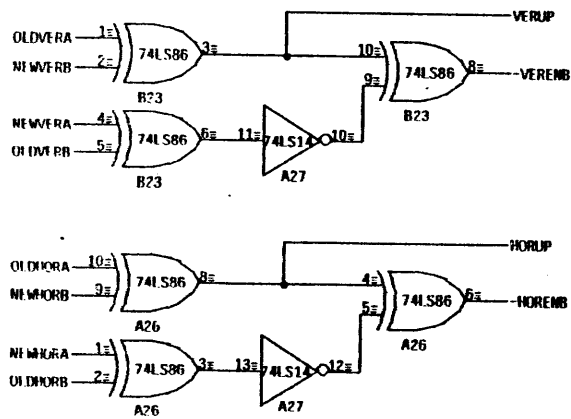
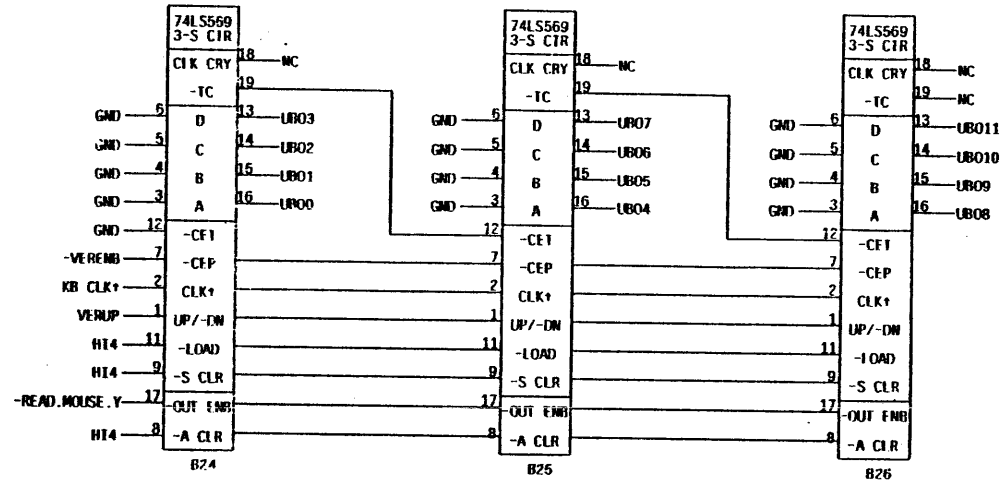
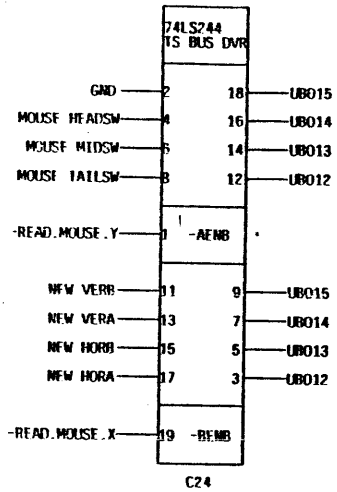
Console Cable

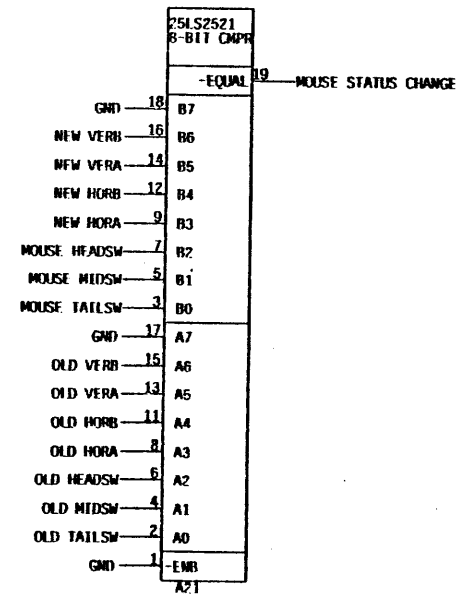
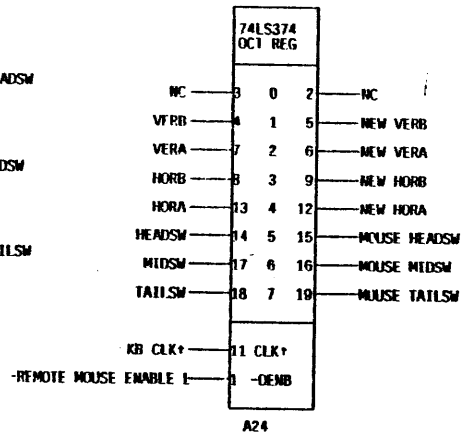
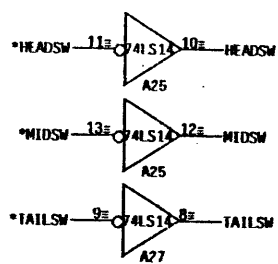
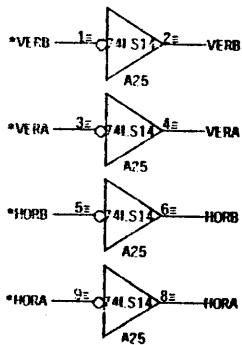
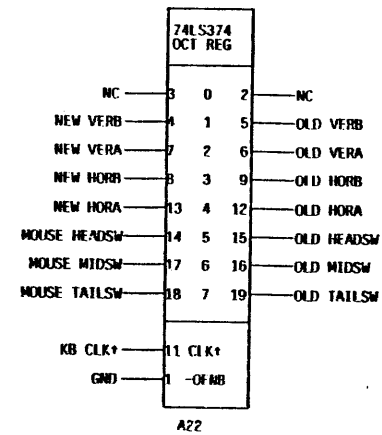
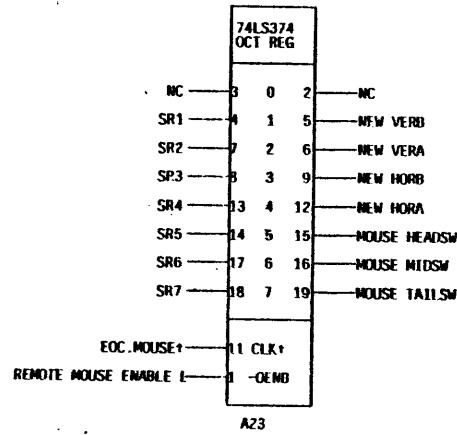
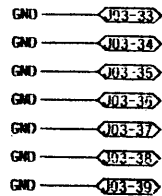
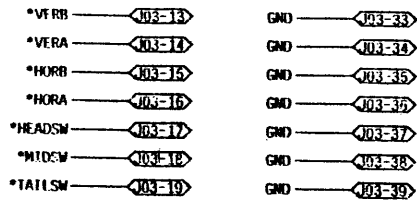
RECOMMET J3-23,30,31,32
 WHEN USE TWISTED-PAIR WIRING

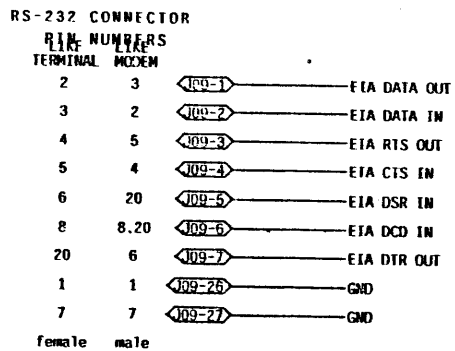
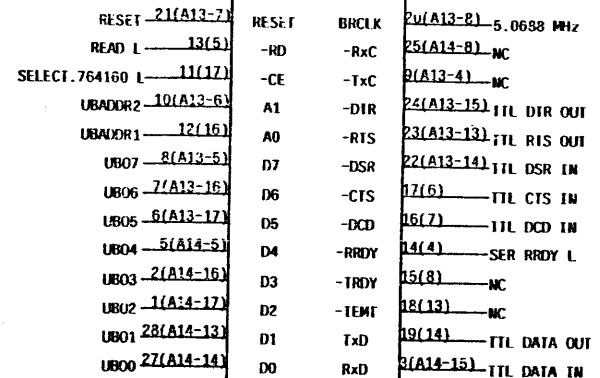
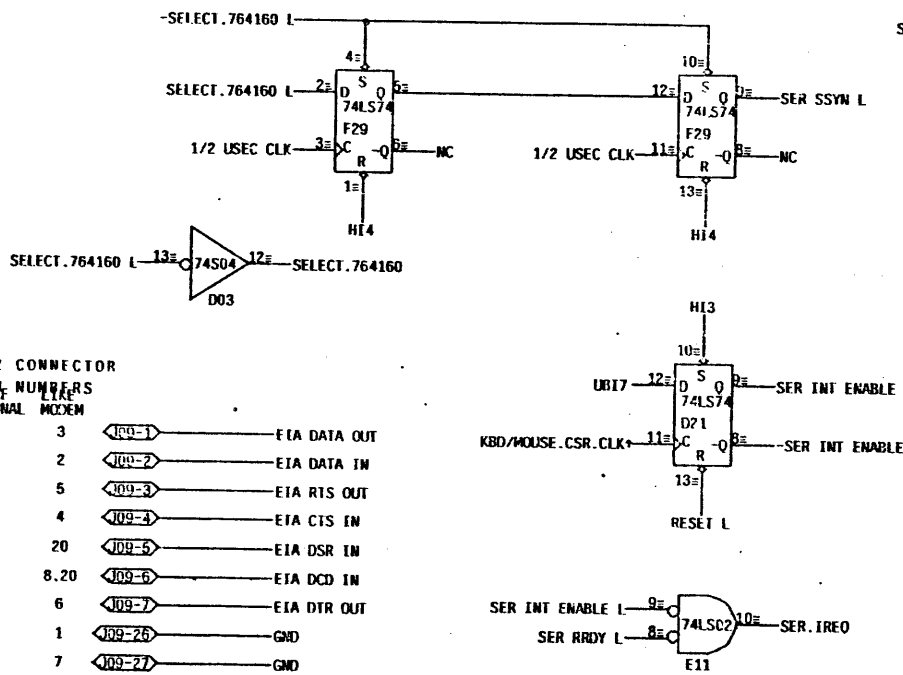
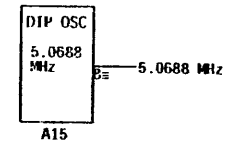
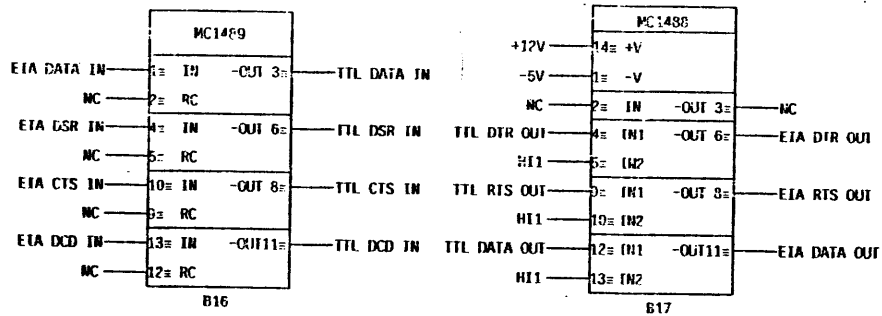


:KBDIN GOES LOW TO START



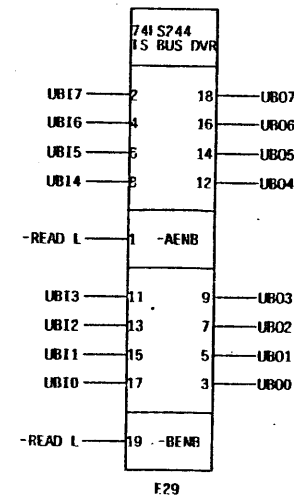
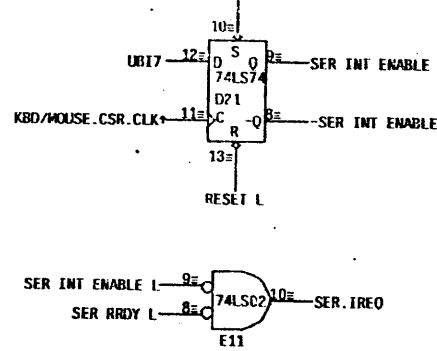


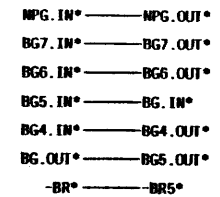
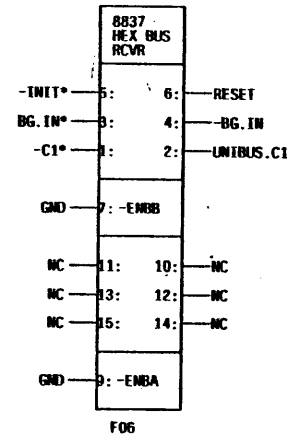
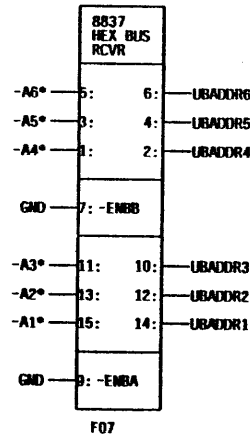
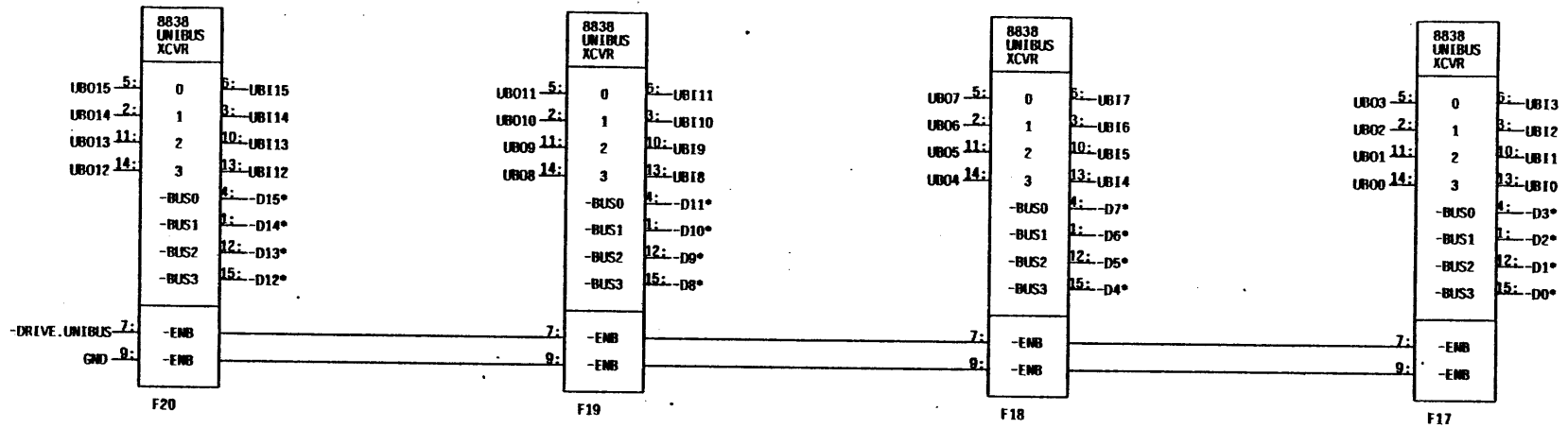


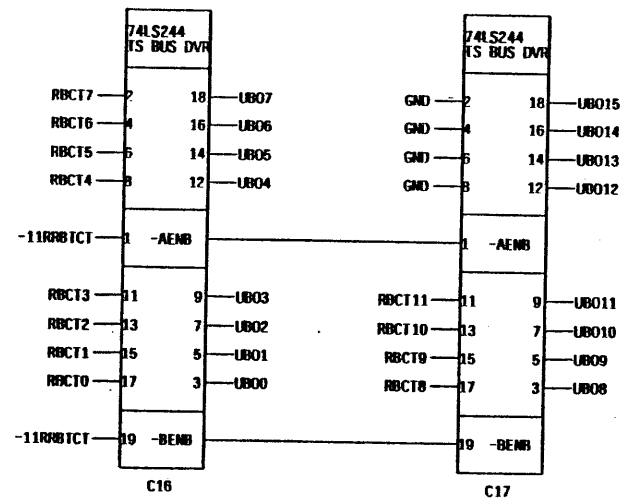
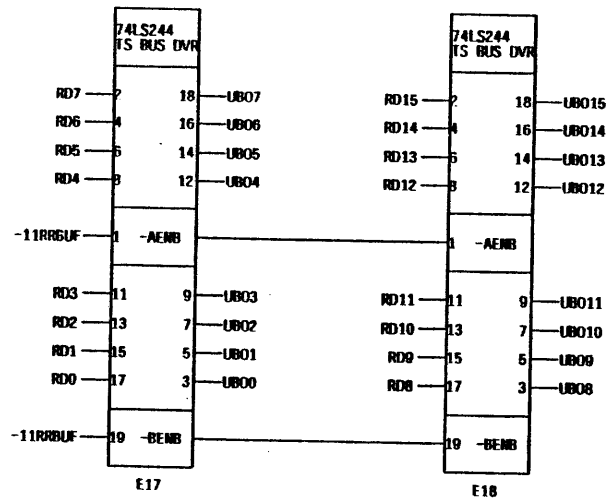
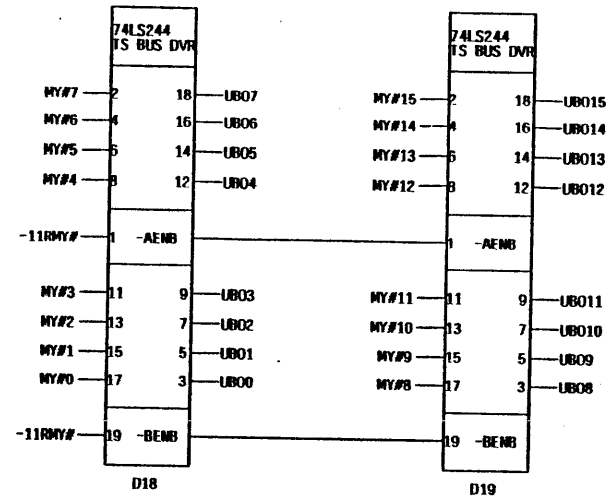
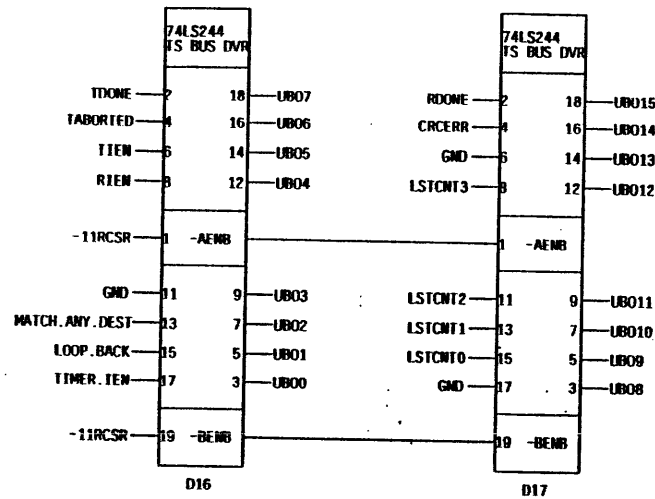


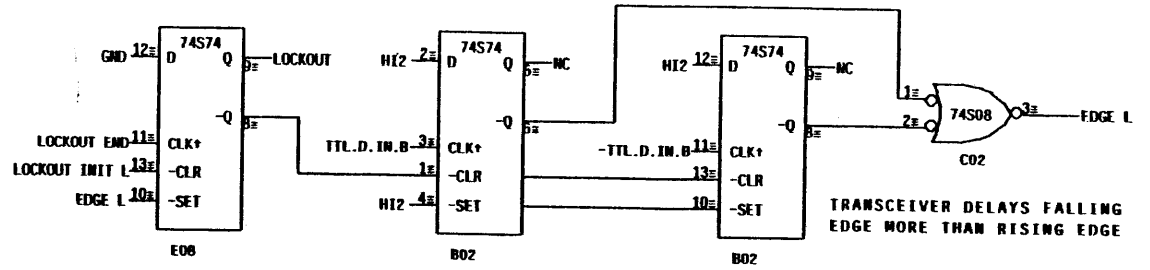
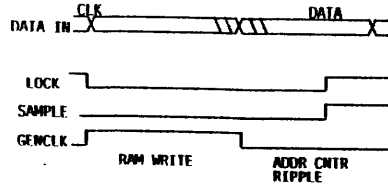
Wire across from Xbus by hand

109-28 +12V

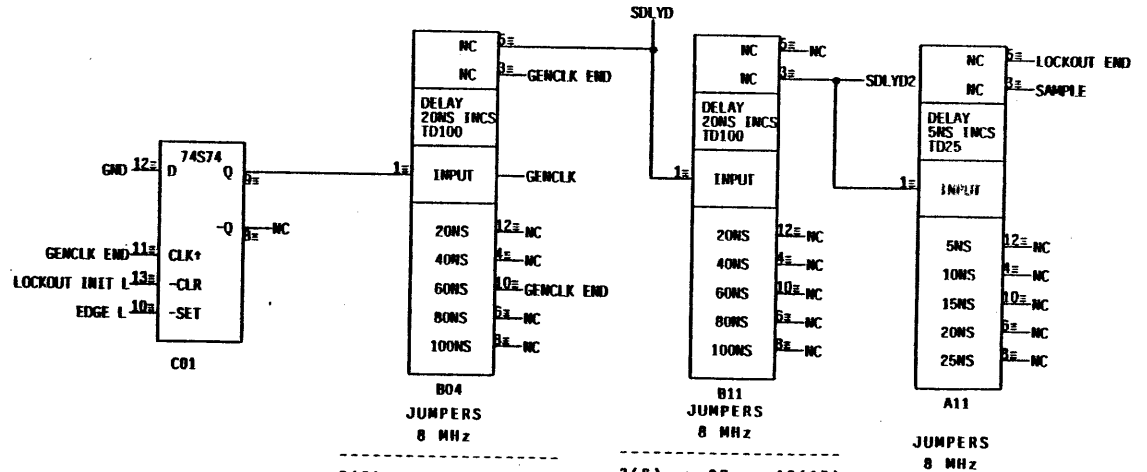
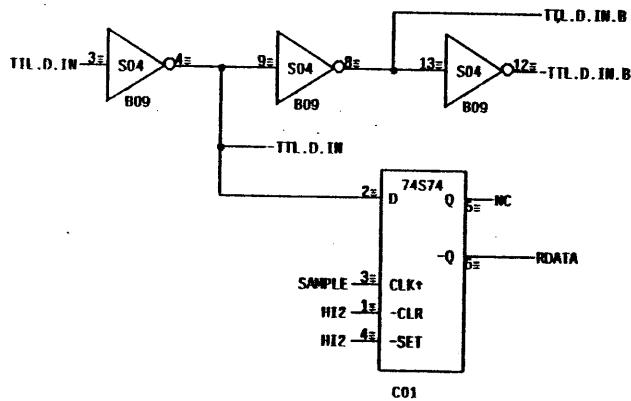
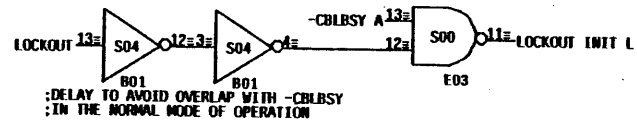








SAMPLE should be timed to occur in the middle of the data part of the cycle. Normally, this will be .75 of the cycle time less 15-25 ns. LOCKOUT END should be 5 ns earlier.

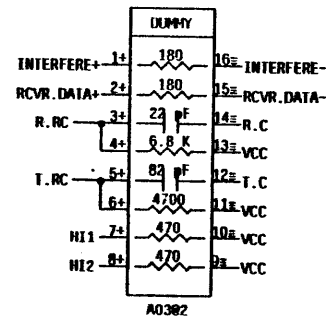
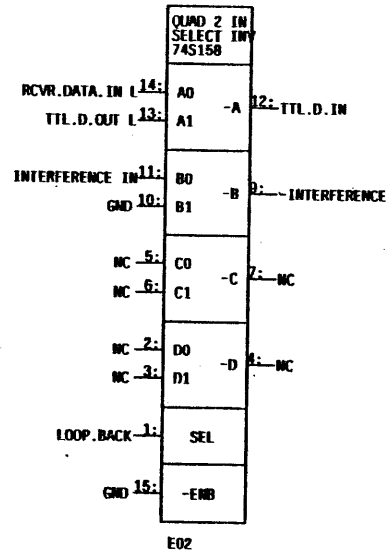
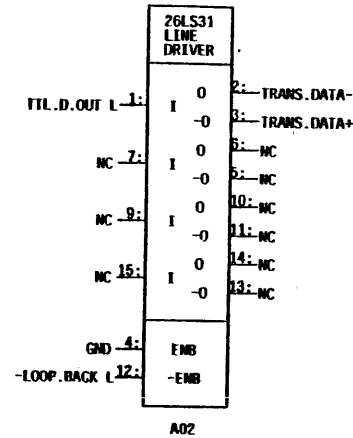
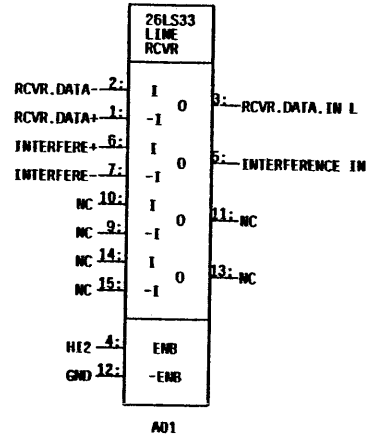


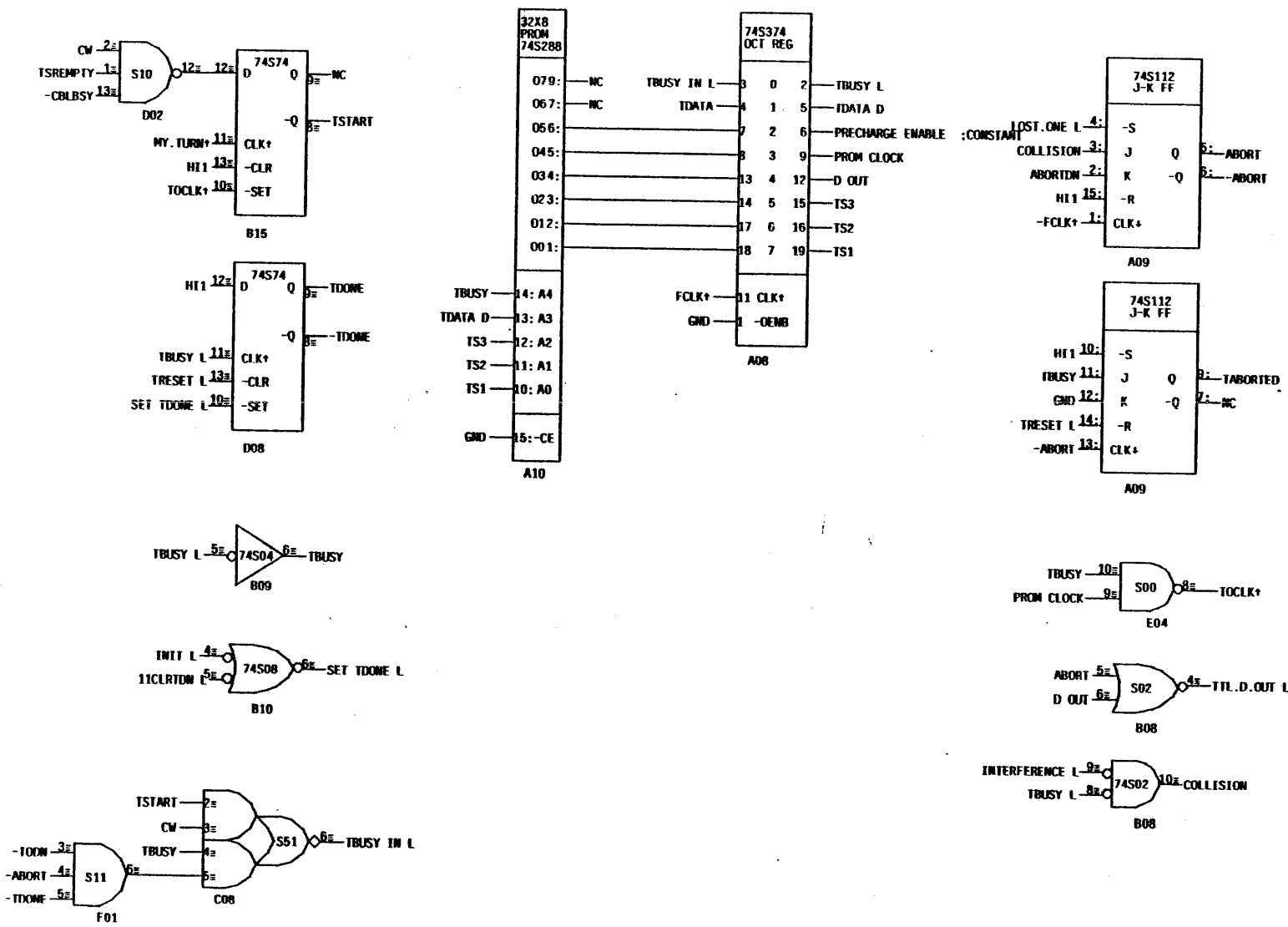
5(8) -> 20 ns 12(15)
3(6) -> 40 ns 4(7)
4 MHz
5(8) -> 100 ns 8(11)
3(6) -> 60 ns 10(13)

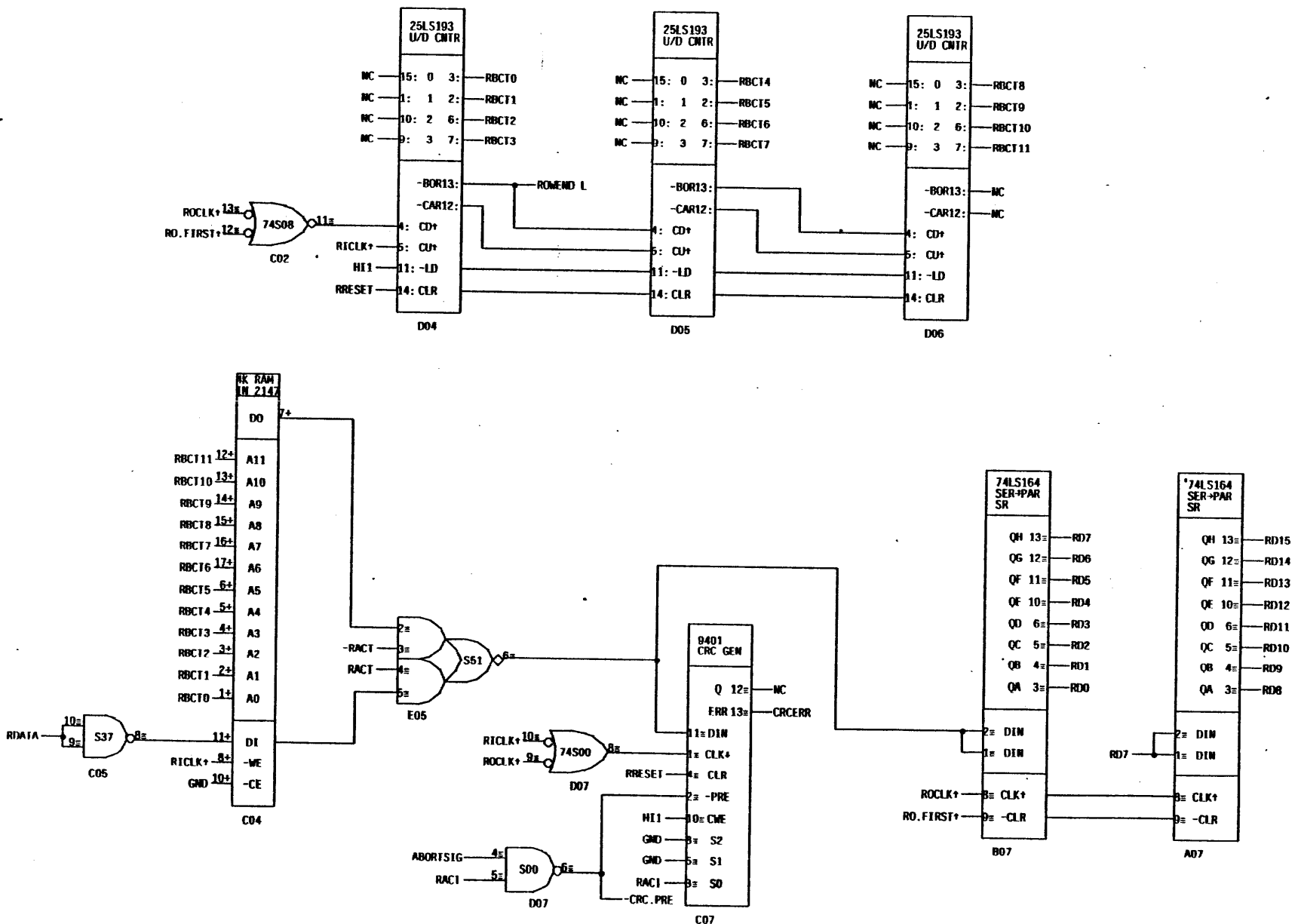
3(6) -> 20 ns 12(15)
4 MHz
3(6) -> 60 ns 10(13)

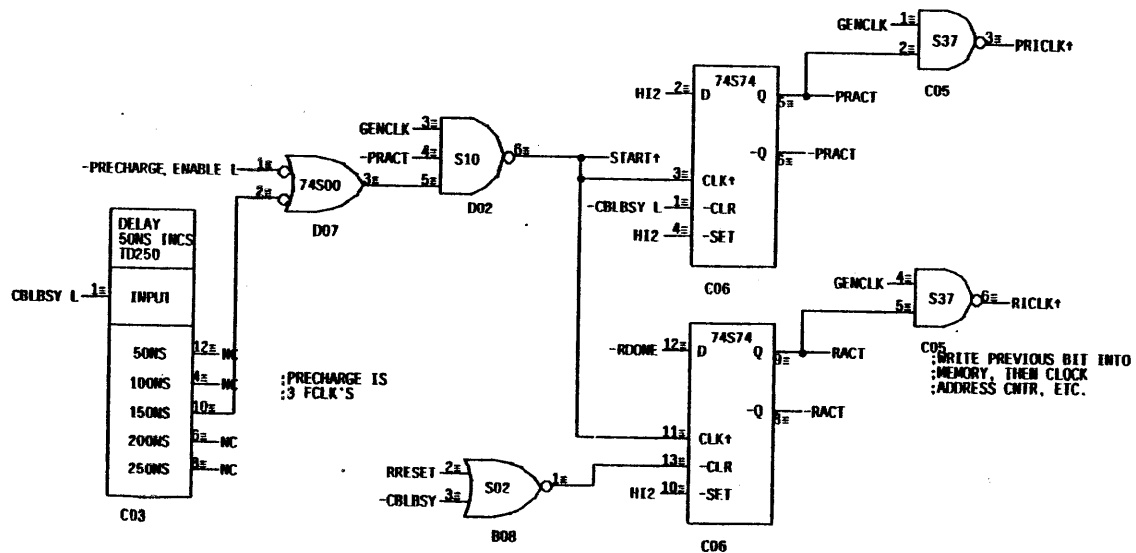
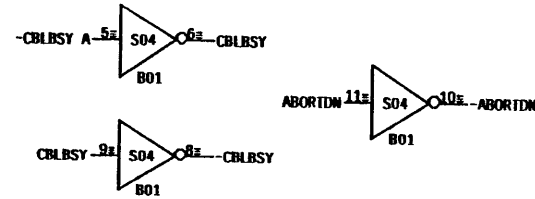
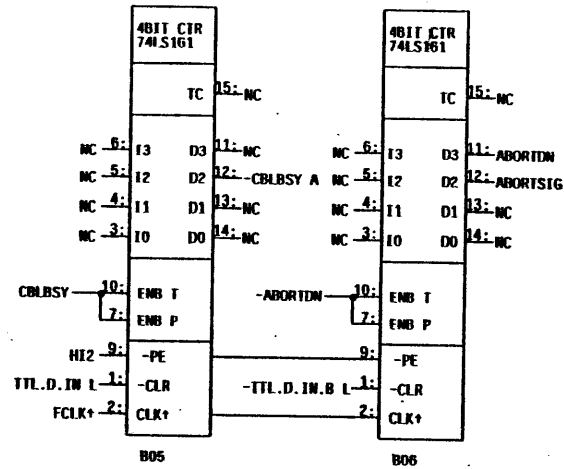
3(6) -> 25 ns 8(11)
5(8) -> 20 ns 6(9)
4 MHz
3(6) -> 15 ns 10(13)
5(8) -> 10 ns 4(7)

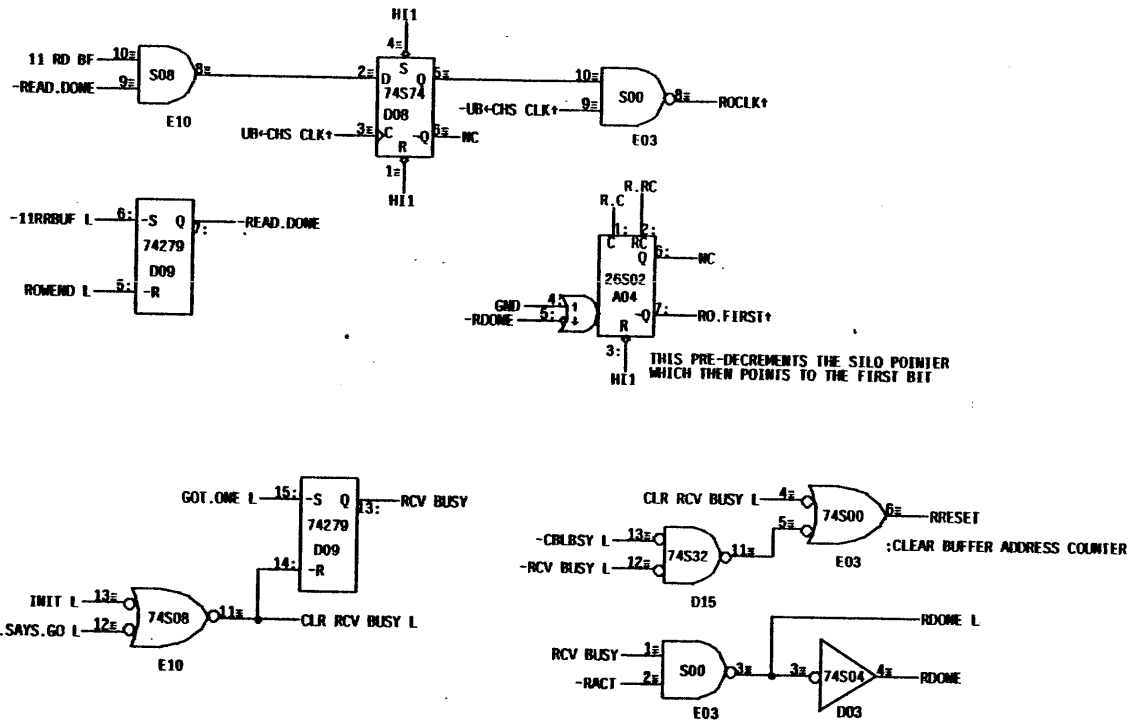
:=26LS32

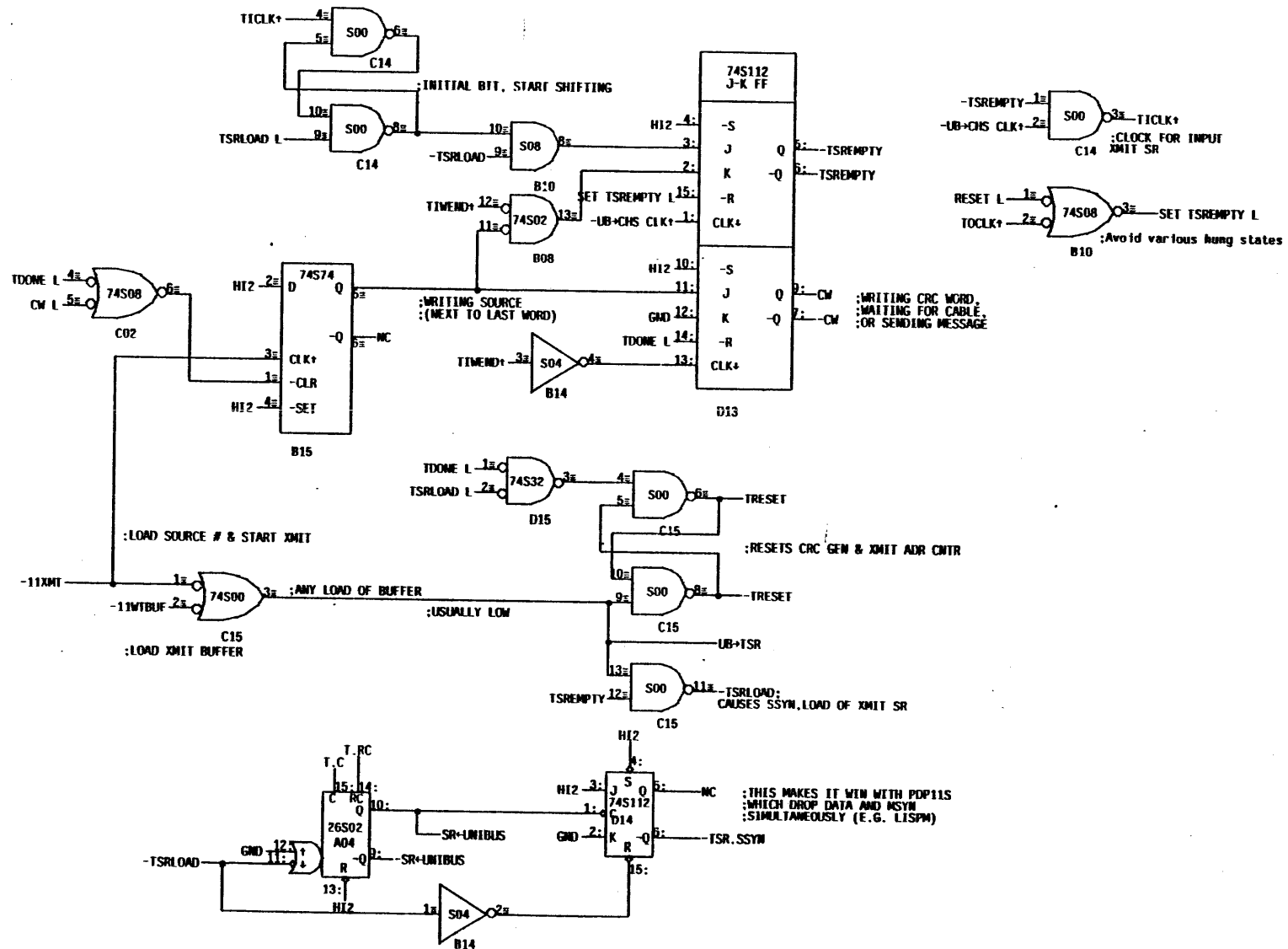


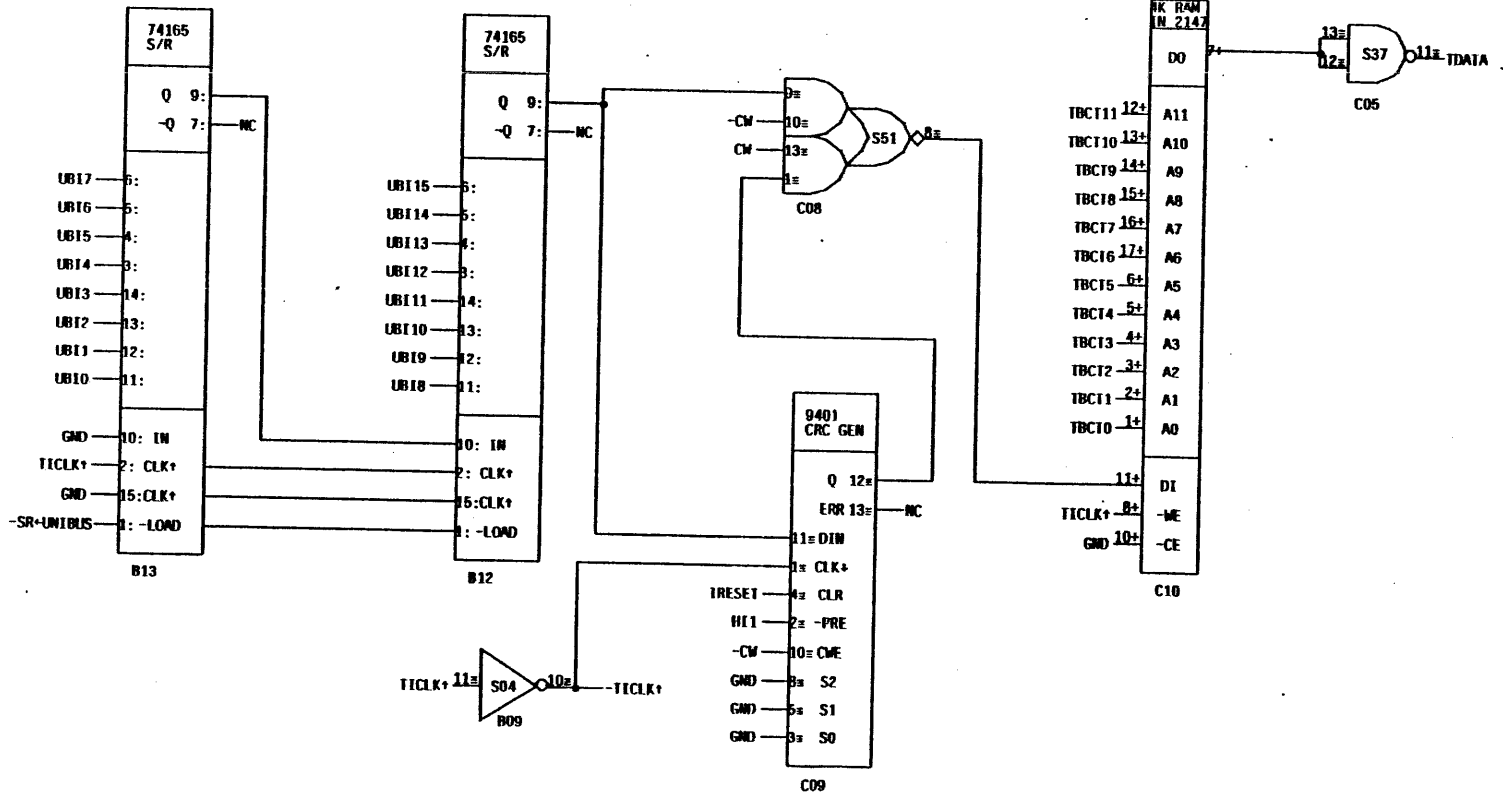
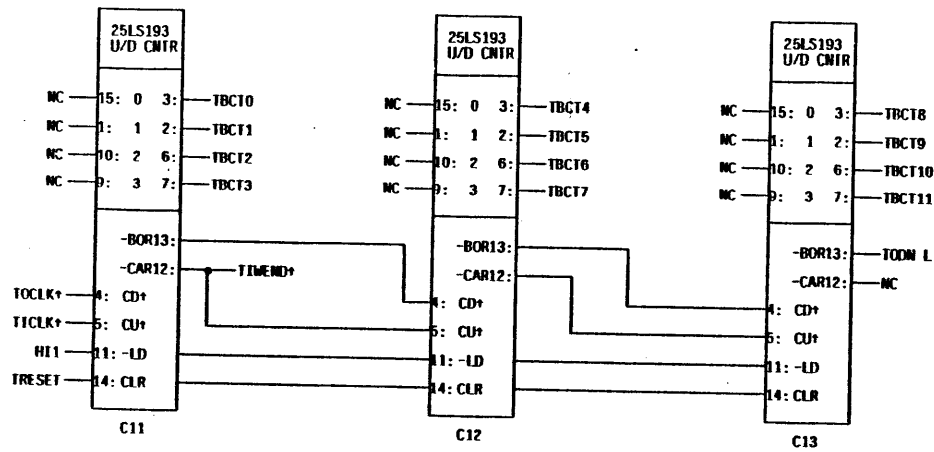


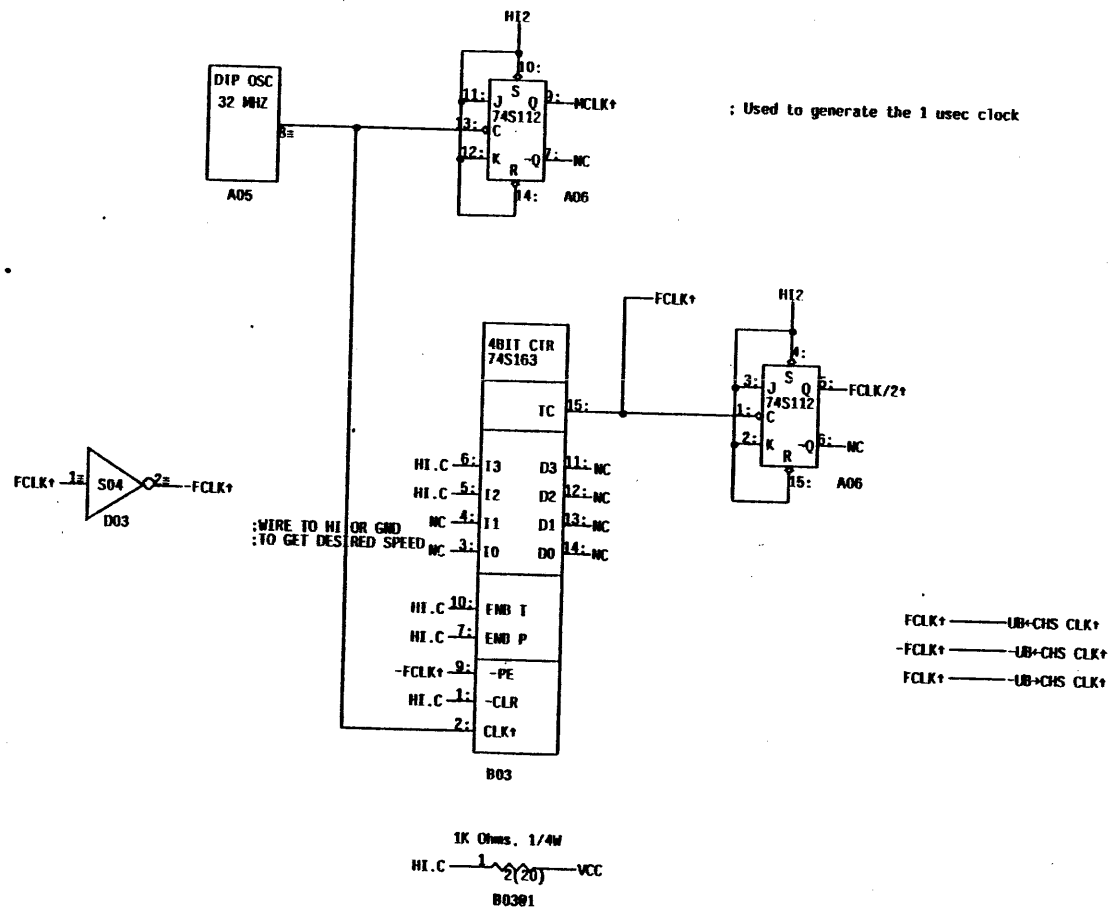




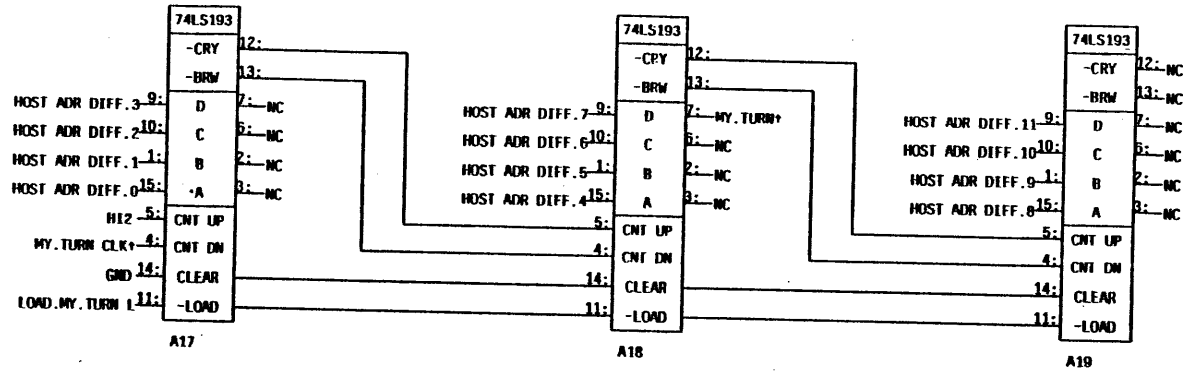








"My Turn" Counter



:DEFAULT IS MYTURN.MOD 2+7 OR 64 USECS

