IMSAI/ALTAIR S-100 COMPATIBLE

JADE Z80 KIT

ASSEMBLY MANUAL AND

OPERATING INSTRUCTIONS

Revised 5/77

Circuit Features

-- On board 2708 EPROM addressable to any 4K boundary above 32K

-- Power-on-jump to any 4K boundary above 32K, or the on-board 2708

-- A wait state may be added to any:

1) M1 cycle
2) Memory Request cycle
3) On-board ROM cycle (for use at 4 MHz)
4) Input cycle
5) Output cycle

-- On-board run-stop flip-flop and optional generation of MEMORY WRITE allow front panel-less operation

-- Selectable IO addressing mode:

1) 8080 mode where peripheral address byte is duplicated on high and low order address bytes
2) Z-80 mode where the peripheral byte appears on the low order address, and the contents of the accumulator appears on the high order byte, allowing simultaneous I/O

-- DMA Grant tri-states all signals from the processor board

-- 8224 clock generator provides 8080 look-alike $\phi 1$ and $\phi 2$ for the S-100 bus

-- Status signals SINP, SOUT, SMEMR, & $\overline{\text{SWO}}$ are latched per S-100 bus specs.

Board Assembly

1) Install sockets for IC 1 thru IC 4, IC 6 thru IC 27, and IC 29 thru IC 40.

2) Install 8 position dip switches (SPST) at locations IC 5 and IC 28.

3) Install .1 uf capacitors at locations C4, C5, and C11 to C24.

4) Install a 50 to 100 uf electrolytic capacitor at locations C1 and C6. Note the polarity orientation on the silkscreen.

5) Install a 10 pf capacitor at location C9.

6) Install a 100 pf mica capacitor at location C10.

7) Install the following resistors:

R1 4.7K
R2 1K
R6 330 ohms

8) Install 7805 regulator and heat sink at location Q1. It is advisable to use heat sink grease between the regulator and the heat sink.

9) If you plan to use the 2708 PROM install:

C2 & C3 50 to 100 uf electrolytic capacitors
R3 51 ohm resistor
R4 240 ohm resistor
D1 12 volt zener diode
D2 5.1 volt zener diode

2 MHz Operation

1) Install an 18 MHz XTAL at location Y1. If the crystal is an overtone type crystal, then install L1, C7 , and C8 . If the crystal is a fundamental type, then these components are not necessary.

2) Install resistor R5 at 3300 ohms.

3) Open all dip switches (off position).

4) Install jumper J2 (adjacent to IC 23) in the 8080 mode by connecting the middle to the lower pads.

Z-80 mode	8080 mode

4 MHz Operation

1) Install a 36 MHz crystal at location Y1. If the crystal is a third overtone type, then install L1, C 7, and C 8 .

2) Install R5 at 1.8K ohms.

3) Open all dip switches except IC 5 position 5. This inserts a wait state into every memory cycle, so that you may test the processor with 500 ns memory.

4) If you are using a 2708 EPROM, close IC 5 position 6.

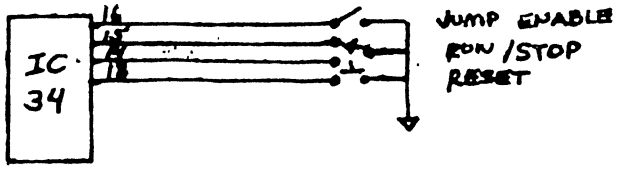
5) Install jumper J2 (adjacent to IC 23) in the 8080 IO mode by connecting the middle to the lower pads.

Front Panel-less Operation

1) On the reverse side of the printed circuit card (not the component side) in the upper left hand corner there are four sets of pads marked A, B, C, and D. Connect each set of pads by carefully soldering a small piece of wire to the two pads of each set.

2) Mount your front panel control switches and attach their terminals to a length of ribbon cable. Attach the other end of the ribbon to a dip header plug, pins 13, 14, 15, and 16 as shown in the schematic. Attach the ground to the ground plane

on the S-100 bus.



3) Close the dip switch at location IC 5 position 1. This allows the processor card to generate its own Memory Write signal (MWRT), normally a front panel function.

Options

1) On-board 2708 EPROM

To use the provision for the on-board 2708, install the components for the plus 12-volt and minus 5-volt power supplies as per step 9 of the board assembly instructions. Connect pad J to pad H of the ROM enable jumper (near IC20).

2) No on-board 2708

Connect pad J to pad K of the ROM enable jumper.

3) Power-on Reset jump

The reset jump feature may be enabled in a number of ways. If you are running front panel-less, the jump enable line is available at the front panel connector by connecting the pads across letter D. When this line is grounded the reset jump is enabled. If you are using a front panel, two options exist:

a) The Reset jump may be permanently enabled by connecting pad F to pad G. This grounds the jump enable line.

b) Tie pad F to any unused S-100 bus pin. When this bus pin is grounded, the reset jump will be enabled. Note that when the jump is enabled the data bus will be blanked during a reset operation. The processor will not be able to read the contents of memory until the jump address is reached. If the processor

is stopped and you hit reset and the jump is enabled, the processor will reset to location 0000, remain stopped, and the data bus will read all zeros, regardless of what is stored at this location. Hitting the run switch will allow the processor to step through memory until the jump address is reached, at which time normal memory operations are resumed, with all memory locations being visible to the processor.

4) PROM and Jump Addressing

The on-board 2708 PROM and the reset jump are addressed by closing the appropriate dip switch at IC 28. They may be addressed at any 4K boundary above 32K. Note that only one dip switch may be closed at a time.

Address (hex)	Close switch at position
8000	8
9000	7
A000	6
B000	5
C000	4
D000	3
E000	1
F000	2

5) Wait State Selection

A wait state may be added to any of the following processor cycles by closing the appropriate dip switch at IC 5.

Wait Added on Cycle	Close switch at position
M1 (instruction fetch)	4
all Memory	5
on-board 2708	6
Input	7
Output	8

6) Address Multiplexing

Jumper J2 has been provided so that you may choose between

8080 and Z-80 IO addressing modes. Unless you have a specific need for using the Z-80 mode, it is recommended that you use the 8080 mode, thereby maintaining S-100 bus compatibility. See step 4 of the section on 2 MHz operation for the proper installation of this jumper.

Checkout Procedure

It is highly recommended that you use static memories during the initial checkout of your processor board. The timing signals necessary to interface dynamic memory are highly critical and checkout is greatly simplified if static memory is used. When handling MOS devices such as the Z-80, be careful to ground your body to both the processor board and the conductive foam in which the devices are stored before handling the chips. Avoid touching the pins of the chips if possible. Do not proceed from any step until the proper results are obtained.

1) If you have installed the jump enable jumper (pad F to pad G), temporarily disconnect it. If you have a jump enable switch, open the switch (jump not enabled).

2) Install the board in the computer, power-up and check the output of of the five-volt regulator (right-most pin). If it is not 5 volts, either the regulator is defective, or a short circuit exists on the board. Power-down and check the board for solder bridges.

3) Power down and install the 8224 clock generator (8224-4 at 4 MHz). Power up and check pin 6 for a 2 MHz (4 MHz) square wave.

4) Power-down and install the remaining TTL and the Z-80. Power up and repeat steps 2 and 3. Ifa front panel is used, plug in the connector.

5) Stop the processor if it is running. Press the reset button and hold down. Examine the following pins of the Z-80 chip:

PIN	NAME	CONDITION EXPECTED
26	RESET	low

PIN	NAME	CONDITION EXPECTED
30-4-* 1-5	AØ- A15	high
7-10* 12-15	DØ- D7	high

*These pins may be examined by checking the front panel lights: A0-A15 and D0-D7 should all be on while reset is held down.

6) Release the RESET button. Examine the following pins on the Z-80 chip:

PIN	NAME	CONDITION EXPECTED
26	RESET	high
25	BUSRQ	high
24	WAIT	low
18	HLTA	high
27	M1	low
16	INT	high
17	NMI	high
23	BUSAK	high
30-40* 1-5	A0-A15	low

*may be examined via front panel lights. A0-A15 should be off.

If there is a front panel, proceed with the following tests:

7) Hit the EXAMINE NEXT switch 3 or 4 times and see if the address lights count up in binary.

8) With all the address switches off, hit EXAMINE The processor should return to location zero, with all address lights off.

9) Power-down and install a memory board at location zero. Power-up and hit STOP and RESET. With all data switches off, hit DEPOSIT. All data lights should go out.

10) Change data switch Ø to a one and hit DEPOSIT NEXT. Check that data light Ø is now on.

11) Change each of the remaining data switches, one at a time, to a one.

Hit DEPOSIT NEXT after each change and check that the corresponding data light is now on.

12) When all of the switches are on and all of the data lights are on, hit RESET. Step through memory hitting EXAMINE NEXT. The data lights should come on one by one until they are all on.

13) Enter the following program at location Ø.

Address	Data	Instruction
0000	D3 18	Out 18(Hex)
0002	C3 00 00	Jmp 0000

Hit RESET. The data lights should contain D3, the MEMR light, the $\overline{SWO}$ light, and the M1 light should be on, INP and OUT should be off. Hit SINGLE STEP. Nothing should change except the address and the data lights. Hit SINGLE STEP. The MEMR and M1 + $\overline{SWO}$ lights should now go off and the OUT light go on. Check to see that both the high and low address bytes contain 18(Hex). This is the 8080 IO mode. After hitting SINGLE STEP 4 times, the processor should return to address zero.

14) Hit RUN. Check to see that the OUT light is partially on. Close the dip switch at location IC 5 position 8, the wait light should come on very dimly. When the dip switch at position 4 is closed, the wait light should come on more strongly. Open position 4 and close position 5; the wait light should come on. Open the switches.

15) Change the contents of location Ø to DB. Hit RESET and RUN. The INP light should now come partially on. Close the dip switch at location IC 5 position 7. The wait light should come on very dimly.

16) Connect a temporary jumper between pads J and K, disconnecting pads J and H if they are connected. Connect a temporary jumper between pads F and G. Deposit 76 (hex) at location COOO. Close the dip switch at location IC 28 position 4. Hit RESET. The data bus at location zero should contain all zeros. Hit RUN. After a fraction of a second the HLTA light should go on. This completes the checkout procedure.

Processor Status

The five primary status lines from the Z-80 chip are Memory Request ($\overline{MREQ}$), Instruction Fetch ($\overline{M1}$), Input-Output Request ($\overline{IORQ}$), Read ($\overline{RD}$), and Write ($\overline{WR}$). They are defined as follows:

$\overline{MREQ}$ when active (low), indicates that the address bus contains a valid address for a Memory Read or Memory Write.

$\overline{IORQ}$ indicates that the address bus contains a valid address for an input or an output device.

$\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed emmory or device uses this signal to gate data onto the data bus.

$\overline{WR}$ indicates the data bus holds valid information to be stored in the addressed memory or I/O device.

$\overline{M1}$ indicates that the current machine cycle is the opcode "fetch" of an instruction cycle.

These signals are inverted and gated together by IC 18 and IC 19 to form the status signals SOUT (output), SINP (input), SMEMR (memory read), and $\overline{SWO}$ (write operation in progress) as follows:

$$SOUT = IORQ \cdot WR \quad (IC\ 18\ pin\ 6)$$

$$SINP = IORQ \cdot RD \quad (IC\ 18\ pin\ 8)$$

$$SMEMR = MREQ \cdot RD \quad (IC\ 18\ pin\ 11)$$

$$SWO = \overline{RD} \cdot \overline{INTA} \quad (IC\ 18\ pin\ 3)$$

The Z-80 does not have an interrupt acknowledge (INTA) pin. Rather, INTA is defined on the Z-80 chip as

$$INTA = M1 \cdot IORQ$$

This signal is generated by IC 15 at pin 11 and is inverted at IC 17 pin 2 for use in the generation of SWO.

These four status signals are then latched by the quad latch IC 13 and SWO is inverted by using the $\overline{Q}$ output from the latch to form $\overline{SWO}$. The latched status signals provide status information for the S-100 bus after gating through the tri-state bus drivers in IC 3.

The Status latch IC 13 is clocked by the PSYNC signal from one-shot IC 8. The Psync signal is true for the first 400 nsec (200 nsec at 4 Mhz) of every IO or memory cycle (except Refresh) and is used by many peripherals to indicate the earliest moment when status and address information may be sampled from the bus. It may also be used by some peripheral cards to sample status information o: the DATA OUT bus. A full description of this signal is given in the section on 8080 PSYNC. The length of the Sync signal is determined by the resistor R5. The one-shot IC 8 is triggered by the SYNCENABLE signal (IC 14 pin 8) which is defined as:

$$SYNCEN = (MRQ \cdot \overline{RFSH}) + IORQ$$

The Memory Write signal MWRT may optionally be generated on the processor card by closing the dip switch at IC 5 position 1. MWRT is defined as; MWRT = MRQ · WR. This signal need only be generated in a front panel-less machine. In a machine with a front panel, the MWRT is generated by the front panel circuitry and defined as processor Memory Write OR Deposit.

Processor Control Bus

The processor write strobe $\overline{PWR}$ i: simply the write strobe of the Z-80 chip delayed slightly by two sections of IC 12 and optionally delayed until the end of the PSYNC signal via jumper J1. This jumper need only be installed if status information is to be ated onto the data bus. See the section on 8080 PSYNC for a complete explanation.

The processor data bus in signal PDBIN is created at IC 10 pin 10 and is defined as:

$$PDBIN = RD + INTA$$

This is inverted at IC 17 pin 8 and gated to the bus by tri-state driver IC 4. PDBIN is also AND-ed with the sense switch disable sig-

nal ($\overline{\text{SSWDSB}}$)from the front panel at IC 14 pin 3. When $\overline{\text{SSWDSB}}$ is active, data is not gated in from the Data-In-bus so that the processor may accept data from the front panel circuitry via the ribbon cable connected to IC 34.

Wait State Generation

A wait state may be added to any processor cycle by closing the appropriate dip switch at location IC 5.

Wait added to cycle	Switch position
M1	4
all Memory	5
on-board 2708	6
Input	7
Output	8

When using marginally slow memory, it may be necessary to add a wait state to the M1 (instruction fetch) cycle since the Z-80 chip makes its most critical timing demands upon the memory during this cycle. If you are using memory with an access time of greater than 500 nsec and a processor clock of 2 MHz or memory with access time greater than 250 nsec and a clock rate of 4 MHz, then you must add a wait state to every memory cycle. The on-board 2708 EPROM will run without wait states at 2 MHz, but a wait state must be added at 4 MHz. If you wish to add a wait state to an input or an output cycle, provision has been made, though this should only be necessary in extreme cases.

Wait states are generated in the following way: The SYNCEN from IC 14 pin 8 is successively clocked through the two flip flop sections of IC 9 by the processor clock Ø. The output of this circuit is a positive-going pulse at pin 8 of IC 15 with a duration of one clock period every time a new processor cycle begins. The wait request signals from the dip switch IC 5 are OR-ed together by IC 6 and inverted at pin 8 of IC 7. This signal may be considered a wait enable signal. If the wait enable signal is active (high) then the pulse

from IC 15 pin 8 is gated through to the NOR gate, IC 6, and then into the Z-80 chip, generating a wait state for one clock period.

Clock Generation

An 8224 clock generator has been used to generate the Ø1 and Ø2 signals for the S-100 bus and the clock for the Z-80 chip. The Z-80 is clocked by the Ø2 signal. This brings the internal timing structure of the Z-80 chip into close emulation of 8080 timing signals, a necessity for interfacing to the S-100 bus. Note that the tank circuit connected to pin 13 of the 8224 need only be installed with a third overtone type crystal. Resistor R1 and capacitor C6 determine the duration of the power-on reset pulse.

Address Multiplexing

The 8080 processor chip provides the peripheral address byte on both the high order and the low order address bytes during an I/O instruction. The Z-80 chip, however, provides the peripheral byte only on the low order address byte. This is done so that the contents of the accumulator may be transferred to the high order address byte during an input instruction, allowing simultaneous input and ouput. Many peripheral cards designed for the S-100 bus decode the high order address byte during an IO instruction, which will cause errors if the Z-80 IO mode is used. Multiplexors IC 24 and IC 25 have been provided so that you may select between 8080 and Z-80 IO modes via jumper J2. It is adviseable to connect the jumper to the ADDMUX line thereby operating the board in 8080 mode unless you specifically need the simultaneous IO feature. If you choose Z-80 mode you may have to extensively modify your existing IO boards to operate correctly in this mode.

ROM Addressing and Power on Jump

Addressing for the on-board 2708 (IC 36) is done via address decoder IC 29 and dip switch IC 28. The ROM and the power-on/reset

jump are addressed together, and may be located at an 4K boundary above 32K. Note that only one switch of the dip switch IC 28 may be closed at a time in order to avoid addressing the ROM at two places in memory. The power-on jump operates in the following way: The processor reset line (RESCLK) clocks the flip flop IC 21 at pin 3. If the jump enable line (JUMPEN) is low at this moment, either by connecting points F and G on the circuit board, or by connection to a front panel switch, (the JUMPEN line is available on the front panel connector IC 34 at pin 16) then flip flop IC 21 is set and the first set of inverting data receivers are tri-stated. This allows the pullup resistors in IC 32 and IC 38 to force the data lines high. The second set of inverting data receivers change all these highs to lows and the processor sees an instruction word of all zeros, which it decodes as a NOP. This had the effect of incrementing the program counter with no other operation being performed. The Program countersteps through memory until the address selected with IC 28 and IC 29 is reached. The ROM select signal is then generated which resets flip flop IC 21 and the processor resumes normal operation.

If you are not using the on-board ROM, but do wish to use the reset jump to go to your own monitor, this may be done by connecting a jumper between pad J and pad K on the circuit board. If the ROM is used, connect the jumper between pad J and pad H. If the jumper is connected between pads J and H, then the data input drivers will be tri-stated when the ROM is being addressed, preventing conflict between the data input drivers and the ROM data lines. If you do not use the ROM, however, and the jumper is connected between J and H, the 1K block of memory beginning at the reset jump address will be "blanked out" by the tri-stating of the input drivers. This is avoided if pad J is tied permanently high by connecting it to pad K. In this configuration, the chip select on the ROM will never tri-state the input drivers and the system memory at the selected jump address is again "visible" to the Z-80.

Direct Memory Access

A Direct Memory Access cycle is initiated by bringing the $\overline{\text{PHOLD}}$ line low (bus pin 74). This is buffered by IC 11 and connected directly to the bus request ($\overline{\text{BUSRQ}}$) pin of the Z-80. The Z-80 samples this line with the rising edge of the last clock period of any processor cycle and if it is active all processor operation is suspended during the next clock cycle and the bus acknowledge pin ($\overline{\text{BUSAK}}$) goes active. This pin is inverted by IC 19 and buffered by IC 20 to drive the DMA grant (DMAG) line on the bus (pin 26). $\overline{\text{BUSAK}}$ is also buffered by IC 20 and drives three sections of IC 22 and one section of IC 7. This has the effect of Tri-stating all data, address, and control signals from the processor card, thereby relinquishing all control to the DMA device. The DMA operation is terminated when the $\overline{\text{PHOLD}}$ line is returned to its inactive (high) state.

Interrupt Handling

Interrupts are handled internally in the Z-80 chip with very little external circuitry required. When the Interrupt line on the S-100 bus is active (low), this low is gated to the processor chip by buffer IC 20. The Z-80 samples its $\overline{\text{INT}}$ pin during the last clock period of each instruction cycle and if it is active AND the internal interrupts enabled flip-flop is set (interrupts are enabled) AND the $\overline{\text{BUSRQ}}$ line is not active, then an interrupt is generated. The processor generates a special M1 cycle (instruction fetch) at this point. During this special cycle the $\overline{\text{IORQ}}$ signal becomes active concurrently with the M1 signal (normally M1 and $\overline{\text{MREQ}}$ are active during an instruction fetch). This special M1 cycle is defined as the interrupt acknowledge signal and an active high signal is generated at IC 15 pin 11 and gated onto the S-100 bus by buffer IC 4. When this signal is active, the interrupting device can place an 8-bit vector on the processor data bus. Refer to the Z-80 technical manual as to how this interrupt vector is utilized by the Z-80 in each of the three interrupt response modes.

On the 8080 processor chip one of the status lines was assigned to the interrupt enable flip-flop, so that its status could be read by

external devices. The pin proved to be of extremely limited usefulness, and was not included on the Z-80 chip. The S-100 bus, however, being essentially a copy of the 8080 pin-out, does include this signal. While it is possible to build circuitry to emulate the function of this pin, its limited usefulness suggests not doing so. Note that the internal interrupt flip-flop operates in the usual way, being set by an EI instruction (ENABLE INTERRUPTS) and reset by a DI instruction (DISABLE INTERRUPTS) OR by a processor reset operation. If you are using any periferal cards that perform interrupts to the processor, check to see if they examine the INTE signal (bus pin 28). If they do, this bus pin may be tied permanently high and the peripheral cards will operate correctly. Note also that if you have a front panel light that indicates interrupts enabled, it will not operate and may be reassigned to another function.

The Non-maskable Interrupt (NMI) line operates in much the same way as the interrupt line, but this line has priority over the normal interrupt line and cannot be disabled under software control. It is extremely useful to provide response to important signals such as impending power failure. CPU response to an NMI signal is similar to a normal interrupt response except that the contents of the data bus is ignored while the processor stores the program counter on the stack and jumps to location 0066H.

8080 PSYNC

The PSYNC signal indicates three things on the 8080 processor chip:

1) PSYNC identifies the first time state in every machine cycle

2) PSYNC And-ed with Ø1 or $\overline{Ø2}$ indicates the earliest moment that address information is stable on the address bus.

3) PSYNC indicates that status information is available on the Data bus. The normal operation of an 8080 processor card is to latch the system status information off the data bus into an on-board 8212, using PSYNC as a strobe. This latched status information is then available to the S-100 bus.

The Z-80 chip, however, does not generate a PSYNC signal, and does not require that status information be latched at the beginning of each machine cycle.

These differences in processor chip architecture have caused some problems in interfacing the Z-80 to the S-100 bus. The PSYNC signal has been created and satisfies the first two conditions of 8080 PSYNC. The third condition, that status information be available on the data bus during the PSYNC signal, has been intentionally ignored. To satisfy the third condition of the 8080 PSYNC signal, status information would have to be gated onto the data-out bus during the PSYNC signal. This is both unnecessary and drastically reduces the time that data is available on the DATA OUT bus during a memory write or output cycle.

If you have peripheral cards that examine the data-out bus during PSYNC, the simple solution is to cut the data line examined at the chip input and to tie the input to the apprpriate status line on the bus.

Data Line Examined	Symbol	Available at bus pin
D0	INTA	96
D1	$\overline{WO}$	97
D3	HLTA	48
D4	OUT	45

Data Line Examined	Symbol	Available at bus pin
D5	M1	44
D6	INP	46
D7	MEMR	47

An Example: IMSAI Front Panel Fix

The IMSAI front panel, for example, examines data line D05 during the PSYNC interval, in order to stop the processor at an M1 cycle. The Z-80 will not necessarily stop on an M1 cycle unless this data line is cut and the line tied to SM1 (pin 44) on the S-100 bus.

When using the Z-80 board, the following differences exist in the assignment of S-100 bus pins:

INTE Interrupt Enable (bus pin 28) is not generated by the CPU as explained in the section on Interrupt handling.

NMI Non-maskable Interrupt is not accepted by 8080 processors but is accepted by Z-80 CPUs. This function has been assigned to the previously unassigned bus pin 12 adjacent to the vectored interrupt lines VI0 to VI7.

STACK Stack operation (bus pin 98) is an 8080 status line that indicates that a stack operation is in progress. This line is not generated by the Z-80 and is not available on the bus. Front panel lights connected to this pin will not operate correctly.

RFSH Refresh is a signal generated by the Z-80 for interfacing the processor to dynamic memories. It has been assigned to previously undefined bus pin 67.

MRQ Memory request is also generated by the Z-80 and is useful in interfacing dynamic memory without slowing the processor. It has been assigned to undefined bus pin 65.

S-100 Bus Definition

SYMBOLS: "P" prefix indicates a processor command/control signal

"S" prefix indicates a processor status signal

LEVELS: All bus signals except the power supply are TTL

No.	SYMBOL	NAME	FUNCTION
1	+8V	+8 volts	Unregulated input to 5v regulators
2	+16V	+16 volts	Positive unregulated voltage
3	$\overline{\text{XRDY}}$	External Ready	For special applications: Pulling this line low will cause the processor to enter a WAIT state and allows the status of the normal Ready line (PRDY) to be examined
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12	NMI	Non masable Interrupt	

No.	SYMBOL	NAME	FUNCTION
18	$\overline{\text{STA DSB}}$	$\overline{\text{STATUS DISABLE}}$	Allows the buffers for the 5 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	$\overline{\text{COMMAND/CONTROL DISABLE}}$	Allows the buffers for the 4 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	Input to the memory protect flip-flop on a given memory board
21	SS	SINGLE STEP	Front panel signal that indicates that the machine is in the process of performing a single step
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSB}}$	$\overline{\text{DATA OUT DISABLE}}$	Allows the buffers for the 8 data output lines to be tri-stated
24	$\phi 2$	Phase 2 Clock	
25	$\phi 1$	Phase 1 Clock	
26	PHLDA	Hold Acknowledge	Processor control output signal which appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state
27	PWAIT	WAIT	Processor command/control output signal which acknowledges that the processor is in a WAIT state
28	PINTE	INTERRUPT ENABLE	This signal not generated by Z-80
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DO1	Data Out Line #1	

No.	SYMBOL	NAME	FUNCTION
36	DO0	Data Out Line #0	
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	
44	SM1	M1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUT	Status output signal which indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{\text{PWR}}$ is active
46	SINP	INP	Status output signal which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMR	Status output signal which indicates that the data bus will be used for memory read data
48	SHLTA	HLTA	Status output signal which acknowledges a HALT instruction
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	Inverted output of the oscillator that generates the 2 phase clock
50	GND	GROUND	
51	+8V	+8 volts	Unregulated input to 5v regulators
52	-16V	-16 volts	Negative unregulated voltage

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23	$\overline{\text{DO DSB}}$	$\overline{\text{DATA OUT DISABLE}}$	Allows the buffers for the 8 data output lines to be tri-stated
24	$\phi 2$	Phase 2 Clock	
25	$\phi 1$	Phase 1 Clock	
26	PHLDA	Hold Acknowledge	Processor command/control output signal which appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state
27	PWAIT	WAIT	Processor command/control output signal which acknowledges that the processor is in a WAIT state
28	PINTE	INTERRUPT ENABLE	This signal not generated by Z-80
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DO1	Data Out Line #1	

No.	SYMBOL	NAME	FUNCTION
36	DO0	Data Out Line #0	
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	
44	SM1	M1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUT	Status output signal which indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{PWR}$ is active
46	SINP	INP	Status output signal which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMR	Status output signal which indicates that the data bus will be used for memory read data
48	SHLTA	HLTA	Status output signal which acknowledges a HALT instruction
49	$\overline{CLOCK}$	$\overline{CLOCK}$	Inverted output of the oscillator that generates the 2 phase clock
50	GND	GROUND	
51	+8V	+8 volts	Unregulated input to 5v regulators
52	-16V	-16 volts	Negative unregulated voltage

No.	SYMBOL	NAME	FUNCTION
53	$\overline{\text{SSW DSB}}$	$\overline{\text{SENSE SWITCH DISABLE}}$	Disables the data input buffers so the input from the sense switches may be strobed onto the bidirectional data bus right at the processor
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	Clear signal for I/O devices (front panel switch closure to ground)
68	MWRT	MEMORY WRITE	Indicates that the current data on the Data Out Bus is to be written into the memory location currently on the address bus
69	$\overline{\text{PS}}$	$\overline{\text{PROJECT STATUS}}$	Indicates the status of the memory protect flip-flop on the memory board currently addressed
70	PROT	PROTECT	Input to the memory protect flip-flop on the memory board currently addressed
71	RUN	RUN	Front panel signal that indicates that the RUN/STOP flip-flop is Reset
72	$\overline{\text{PRDY}}$	READY	Processor command/control input that controls the run state of the processor; if the line is pulled low the processor will enter a wait state until the line is released
73	$\overline{\text{PINT}}$	$\overline{\text{INTERRUPT REQUEST}}$	The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request
74	$\overline{\text{PHOLD}}$	$\overline{\text{HOLD}}$	Processor command/control input signal which requests the processor to enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle

No.	SYMBOL	NAME	FUNCTION
75	$\overline{\text{PRESET}}$	$\overline{\text{RESET}}$	Processor command/control input; while activated the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	Processor command/control output provides a signal to indicate the beginning of each machine cycle
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	Processor command/control output used for memory write or I/O output control: data on the data bus is stable while the $\overline{\text{PWR}}$ is active
78	PDBIN	DATA BUS IN	Processor command/control output signal indicates to external circuits that the data bus is in the input mode
79	A0	Address Line #0	
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DO2	Data Out Line #2	
89	DO3	Data Out Line #3	
90	DO7	Data Out Line #7	
91	DI4	Data In Line #4	
92	DI5	Data In line #5	
93	DI6	Data In Line #6	
94	DI1	Data In Line #1	
95	DI0	Data In Line #0	

No.	SYMBOL	NAME	FUNCTION
96	SINTA	INTA	Status output signal to acknowledge signal for INTERRUPT request
97	$\overline{SWO}$	$\overline{WO}$	Status output signal indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer; not available with Z-80
99	$\overline{POC}$	Power-On Clear	
100	GND	Ground	

Parts List

IC 1 - 8224① (8224-4② at 4 MHz)
IC 2 - Resistor Pak
IC 3 - 8T97
IC 4 - 8T97
IC 5 - 8 position spst Dip Switch
IC 6 - 74LS21
IC 7 - 74LS00
IC 8 - 74121 (Texas Instruments Recommended)
IC 9 - 74LS74
IC 10 - 74LS02
IC 11 - 8T97
IC 12 - 74LS04
IC 13 - 74LS75
IC 14 - 74LS00
IC 15 - 74LS08
IC 16 - Resistor Pak
IC 17 - 74LS04
IC 18 - 74LS08
IC 19 - 74LS04
IC 20 - 8T97
IC 21 - 74LS74
IC 22 - 74LS00
IC 23 - 74LS02
IC 24 - 74LS157
IC 25 - 74LS157
IC 26 - 8T97
IC 27 - 8T97
IC 28 - 8 position SPST Dip Switch
IC 29 - 74LS138
IC 30 - Z-80 (Z-80A at 4 MHz)
IC 31 - 8T98 or 8098
IC 32 - Resistor Pak
IC 33 - 8T97
IC 34 - This is the Front Panel connector
IC 35 - Resistor Pak
IC 36 - 2708 EPROM (optional)
IC 37 - 8T98 or 8098
IC 38 - Resistor Pak
IC 39 - 8T98 or 8098
IC 40 - 8T97

Note: Resistor packs supplied with this kit are 16 pin, 15 resistor, with pin 16 common. Values between 1K and 4.7K may be used.

R1 - 4.7K
R2 - 1K
R3 - 51 ohms
R4 - 240 ohms
R5 - 3.3K(1.8K at 4 MHz)
R6 - 330 ohms
Q1 - 7805 5 volt regulator
Heatsink -
Y1 - 18.000 MHz crystal (36.000 at 4 MHz)
L1 - 1 uhy (needed only with overtone XTAL)
D1 - 12 volt zener diode
D2 - 5.1 volt zener diode
C1 - C3 50-100 uf electrolytic capacitors 25 volt
C4, C5, C7, C11 - C24 - .1 uf ceramic capacitors
C6 - 50 to 100 uf electrolytic
C8 - 56 pf @ 2 MHz 20 pf @ 4 MHz
C9 - 10 pf
C10 - 200pf

① Intel or AMD
② AMD

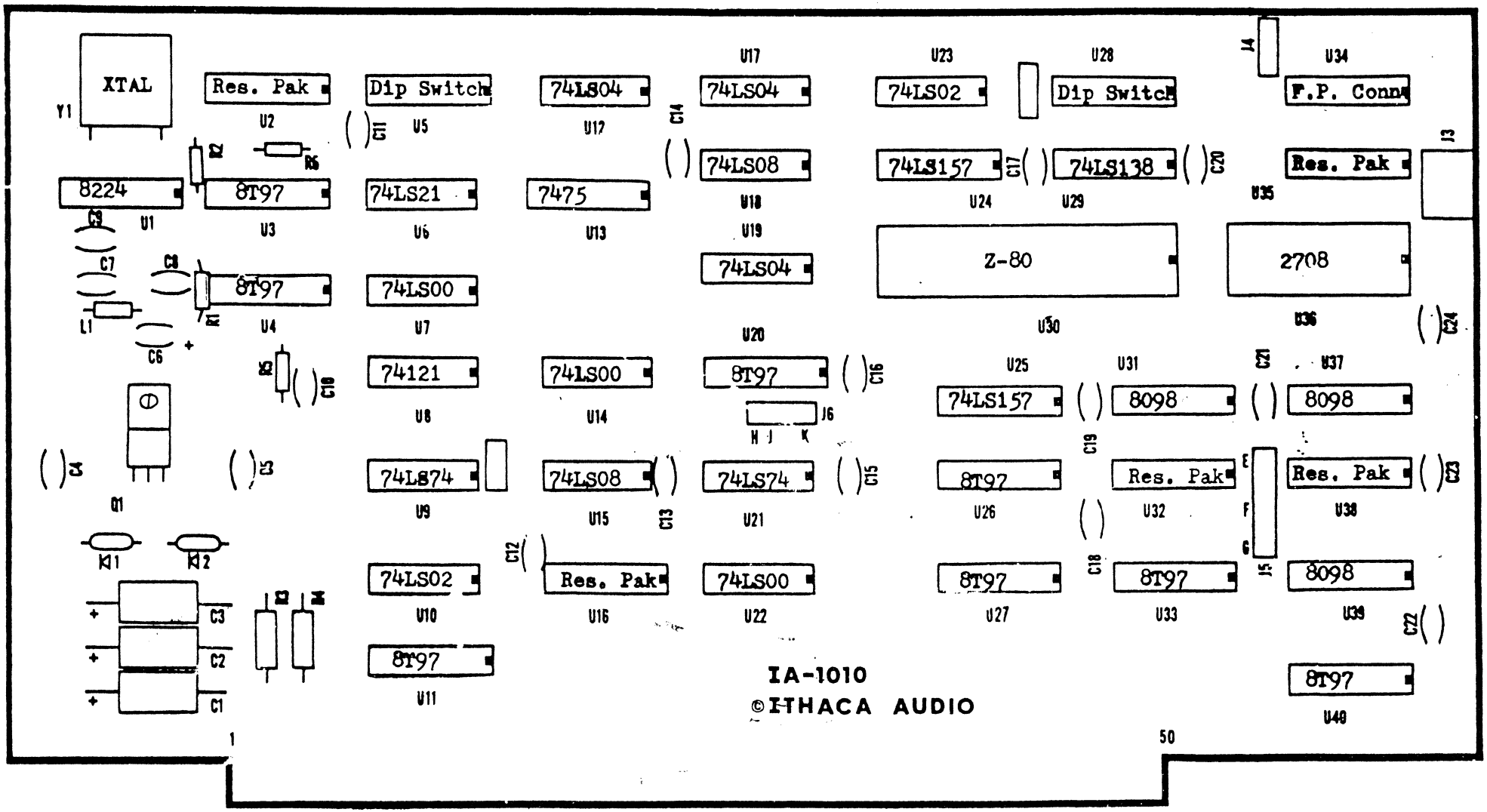
ITHACA AUDIO Z-80 CPU
BOARD

Revisions schedule

Rev. 0 initial release

Rev. 1 edge connectors lines 18 and 19 interchanged. Line 18 corrected to chip 22-9; line 19 to chip 7-1.

REDUCE TO 10.000 S. BOB MKW.

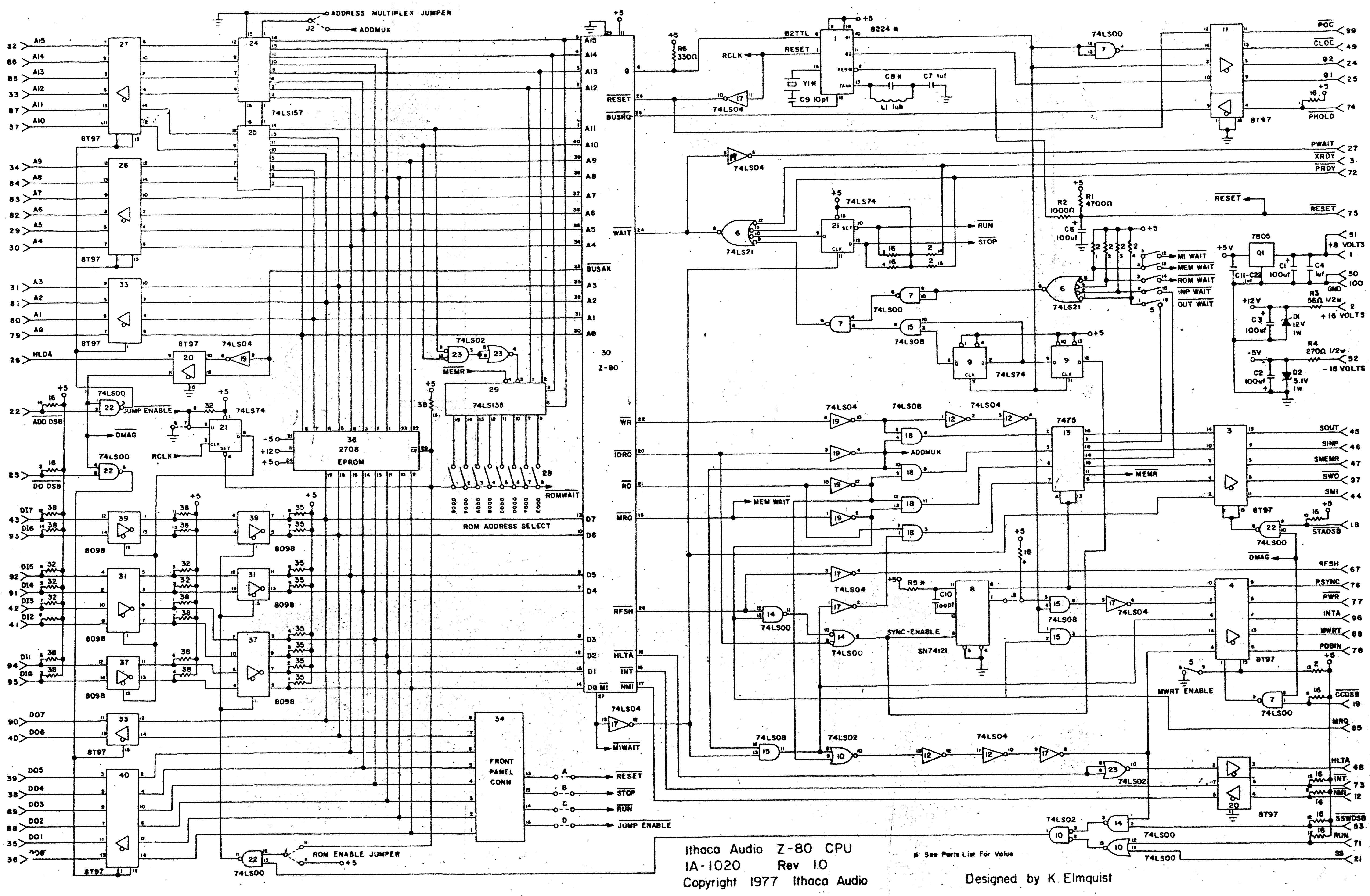


LAYOUT DIAGRAM Z80 BOARD

ITHACA AUDIO Z-80 CPU BOARD

Revisions schedule

Rev. 0	Initial release
Rev. 1	Edge connectors lines 18 and 19 interchanged. Line 18 corrected to chip 22-9; line 19 to chip 7-1.
Rev. 1.1	RClk changed to $\overline{\text{RClk}}$ U17-10 used instead of u17-11. This improves reset jump operation.
Rev. 1.2	Data received on the data in bus is no longer placed on the data out bus. This prevents the possibility of ringing on the data busses caused by crosstalk.
Rev. 1.3	The pins and polarity of refresh have been changed from line 67 to line 66 to correspond with Bus standards.



ADDRESS MULTIPLEX JUMPER
ADDMUX
74LS157
2708
EPROM
74LS138
30
Z-80
ROM ADDRESS SELECT
ROMWAIT
FRONT PANEL CONN
RESET
STOP
RUN
JUMP ENABLE
ROM ENABLE JUMPER
8224 *
MI WAIT
MEM WAIT
ROM WAIT
INP WAIT
OUT WAIT
SYNC-ENABLE
SN74121
MWRT ENABLE
+8 VOLTS
+16 VOLTS
-16 VOLTS
Ithaca Audio Z-80 CPU
IA-1020 Rev 1.0
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* See Parts List For Value
Designed by K. Elmquist

ADDRESS MULTIPLEX JUMPER
J2
ADDMUX
74LS157
8T97
74LS04
74LS00
74LS74
74LS02
74LS138
74LS21
74LS08
2708 EPROM
8098
ADD DSB
DO DSB
JUMP ENABLE
DMAG
RCLK
MEMR
HLDA
ROM ENABLE JUMPER
ROM ADDRESS SELECT
ROMWAIT
FRONT PANEL CONN
Z-80
8224 *
Ø2TTL
RESET
Y1 *
C8 *
C7 1uf
L1 1uh
C9 10pf
R6 330Ω
74LS74
RUN
STOP
R1 4700Ω
R2 1000Ω
C6 100uf
MI WAIT
MEM WAIT
ROM WAIT
INP WAIT
OUT WAIT
7805
Q1
C1 100uf
C4 1uf
C11-C22 1uf
+8 VOLTS
GND
+12V
C3 100uf
D1 12V 1W
R3 56Ω 1/2w
+16 VOLTS
-5V
C2 100uf
D2 5.1V 1W
R4 270Ω 1/2w
-16 VOLTS
7475
SOUT
SINP
SMEMR
SWO
SMI
STADSB
CCDSB
SSWDSB
MWRT ENABLE
MEM WAIT
SYNC ENABLE
SN74121
R5 *
C10 100pf
J1
PWAIT
XRDY
PRDY
PHOLD
POC
CLOC
Ø2
Ø1
RFSH
PSYNC
PWR
INTA
MWRT
PDBIN
MRQ
HLTA
INT
NMI
RUN
SS
MEMR
ADDMUX

* See Parts List For Value

Ithaca Audio Z-80 CPU
IA-1020 Rev 10

Designed by K Elmquist