μSCOPE™820
MICROPROCESSOR SYSTEM CONSOLE

Provides an interface to microcomputer systems for troubleshooting system problems

Monitors, displays, and alters register, memory and I/O values for system under test

Executes diagnostic routines from μScope 820 console overlay memory

Executes instrument resident software patch routines even when microcomputer system is ROM-based

Provides a 32-bit hardware breakpoint with bit masking and a 256-word trace memory

Is a stand-alone, self-contained, rugged portable unit

Human engineered with easy to read 9-segment hexadecimal displays and extensive operator prompting

Gives complete control over microprocessor including single step, run with display, or run real-time capability

Designed to support many different microprocessors

Has built-in, self-test operation

The μScope™ 820 Microprocessor System Console is a portable, self-contained instrument designed to provide the control, monitoring, and interaction necessary to effectively and quickly evaluate and debug 8-bit microcomputer-based systems in the lab, on the production line, or in the field. Connection to the user's system is through a personality probe that is plugged into the microprocessor socket. Each personality probe is unique to each microprocessor type. The instrument features many different operating and control modes which allow the operator to carry out a number of functional checks on the microcomputer System Under Test (SUT).

The unit has been specificially designed to ease the task of microcomputer system check-out for the lab, production line, and field technician. It also provides the more powerful analytical capabilities necessary to troubleshoot difficult problems by the more experienced, sophisticated user. Preprogrammed test routines resident in front panel PROMs, dedicated high level command keys, visual prompting, and simplified data entry sequences all ease the check-out of microcomputer hardware. For more rigorous diagnostic tasks, the unit provides a 32-bit maskable hardware breakpoint with optional course of action after a breakpoint match, a 256 X 32-bit trace memory and a 128 X 8 overlay RAM that allows real-time entry of test routines via the μScope 820 Microprocessor System Console keyboard.

CHARACTERISTICS

COMMANDS

Reset
Self Test
CPU Reset
Run Real Time
Run with Display
Halt
Single Step
Enable/Disable Breakpoint
Enable/Disable Overlay
Enable Trace All Cycles
Enable Trace at Breakpoint
Examine/Modify Value
- Single Registers
- Double Registers
- CPU States
- Breakpoint Pass Count

Examine/Modify Memory
Examine/Modify I/O
Examine/Modify Overlay Memory
Examine/Modify Next Location
Examine/Modify Last Location
Examine/Modify Breakpoint Condition
Examine/Modify Breakpoint Mask
Examine/Modify Breakpoint Action
Examine/Modify Overlay Origin
Display Trace Data
Clear Entry
Continue
End/Execute
Subroutine Select

CPU CONTROLS

User-selectable commands permit one of four possible CPU operating modes:

1. *Run Real Time* — User's CPU runs at full speed set by user clock. No wait states or cycle stealing are required.
2. *Run with Display* — User's CPU runs at full speed, except that 10 times/sec the instrument halts user's CPU temporarily to acquire display data. Worse case throughput is 95% of real time operation.
3. *Halt* — User CPU halted at next opcode fetch. DMA activity is permitted during HALT.
4. *Single Step* — User CPU executes one instruction then halts.

BREAKPOINT

The breakpoint condition is set by a 32-bit word (16-bit address, 8-bit data, 8-bit status). The breakpoint mask is also set by a 32-bit word which is bit-selectable. There are three courses of action following a breakpoint match:

1. Halt on first opcode fetch following breakpoint match.
2. Halt on first opcode fetch following Nth breakpoint match $1 \leq N \leq 256$.
3. Execute subroutine beginning at first opcode fetch following breakpoint match.

All breakpoint actions following a match are controlled by the breakpoint enable/disable switch except for trace recording and the Sync Trigger Output. The Sync Output is a negative true TTL output that occurs whenever a breakpoint match occurs.

Pulse Width = 180 nsec typ
Output High = 2.5 V min, −1.2 mA
Output Low = 0.5 V max, 24.0 mA

TRACE

The trace memory is a 256-word memory with each word consisting of 16 address bits, 8 data bits and 8 status bits. The memory is a circular buffer which records the last 256 cycles (words) prior to a user CPU halt or DISPLAY TRACE command. Trace data can be recorded on all CPU cycles or only when breakpoint matches occur (independent of breakpoint enable/disable status). In addition, the operator can initiate a panel freeze which temporarily stops all trace data recording, and allows display of previously recorded data without halting the user CPU.

DATA ENTRY

All single and double byte items can be entered via the front panel hexadecimal keypad. In addition, all single byte items can be optionally entered via eight binary input keys.

MEMORY OVERLAY

The μScope™ 820 Microprocessor System Console allows memory read/writes of the user CPU in any assigned 1K or 2K block to be made to the instrument's overlay memory. For 1K block assignments, the first 128 bytes reside in the instrument's RAM memory while the remaining 896 bytes reside in the interchangeable front panel ROM/EPROM (either Intel's 2716 EPROM or Intel's 2316E ROM). For 2K block assignments, again the first 128 bytes are from RAM and the remaining 1920 bytes are from the front panel 2716/-2316E.

DATA DISPLAY

Eight hexadecimal 0.5 in. LEDs are provided for the simultaneous display of 4 bytes of information. The displays are physically separated into two groups. The first group displays 2 bytes of address, while the second group displays CPU data, status, single and double byte register values, or single and double byte breakpoint values. In addition, eight binary displays are used to provide quick recognition of single byte binary data patterns.

SELF TEST

The necessary hardware and software have been incorporated into the instrument to facilitate the self-checking of the majority of its operations. Included in these self tests are:

- Bit tests of all breakpoint condition and mask latches.
- Bit tests of all RAM.
- Verifies checksum on all operating system ROMs.
- Clears trace memory and performs bit test on trace RAM.
- Checks miscellaneous I/O ports and peripheral components.
- Lights all front panel displays for user verification.

CONNECTION

Four external connections to the μScope 820 Microprocessor System Console are provided:

- 1.2 m (4 ft), 50 conductor flat cable for connection to the microprocessor probe.
- 20-pin board edge connector for the probe personality PROM.
- 24-pin zero force insertion sockets for overlay EPROM/ROM.
- One recessed pin for breakpoint sync output.

PHYSICAL CHARACTERISTICS

Width:	479 mm	(18-7/8 in.)
Length:	394 mm	(15-1/2 in.)
Height (top closed):	168 mm	(6-5/8 in.)
Height (top removed):	117 mm	(4-5/8 in.)
Weight:	9.1 kg	(20 lb)

ELECTRICAL REQUIREMENTS

Voltage: 100, 120, 220, 240 — 10% +5%, 110VA max
Frequency: 48–63 Hz

ENVIRONMENTAL CONDITIONS

Operating Temperature:	0°C to 55°C (32°F to 130°F)
Storage Temperature:	−40°C to 75°C (−40°F to 167°F)
Humidity:	95% RH, 15°C to 40°C (59°F to 104°F) non condensing

ACCESSORIES SUPPLIED

Two keys
One fuse for 220/240 V operation
One 2.3 m (7.5 ft) power cord
One Operator's Manual
One Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
USC-820	Microprocessor System Console

CPU CONTROL

The instrument provides complete control over the operation of the microprocessor in the System Under Test (SUT). The user CPU can be forced to HALT, SINGLE STEP, RESET, RUN REAL TIME, or RUN WITH DISPLAY. All of the above CPU commands can be issued without impacting other operational parameters or diagnostic sequences that have been set up.

BREAKPOINT CONTROL

The hardware breakpoint of the instrument allows the operator to alter the normal program flow of the SUT. Breakpoint logic is implemented in hardware, thereby eliminating any throughput degradation of the SUT. All bits of the breakpoint condition word are maskable in order to allow the breakpoint condition to be as specific or as general as may be desired.

The occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or the recording of a single cycle of trace data. All of these options are selectable via the EXAM ACTION key prior to enabling the breakpoint.

TRACE MEMORY

The console has a full 32-bit word trace memory that records 256 cycles of SUT operation without causing any delays. The trace memory provides information about CPU operation just prior to a CPU halt or just prior to the initiation of a panel freeze via the trace DISPLAY key.

The operator can alternatively elect to have data recorded on all SUT microprocessor cycles or only when program execution of the SUT microprocessor generates a breakpoint match. Once the data is recorded, sequential examination of the data can be accomplished simply by depressing the EXAM NEXT or EXAM LAST keys.

ADDRESS DISPLAY/SELECT

A dedicated, 4-digit hexadecimal address display allows the following address information to be displayed:

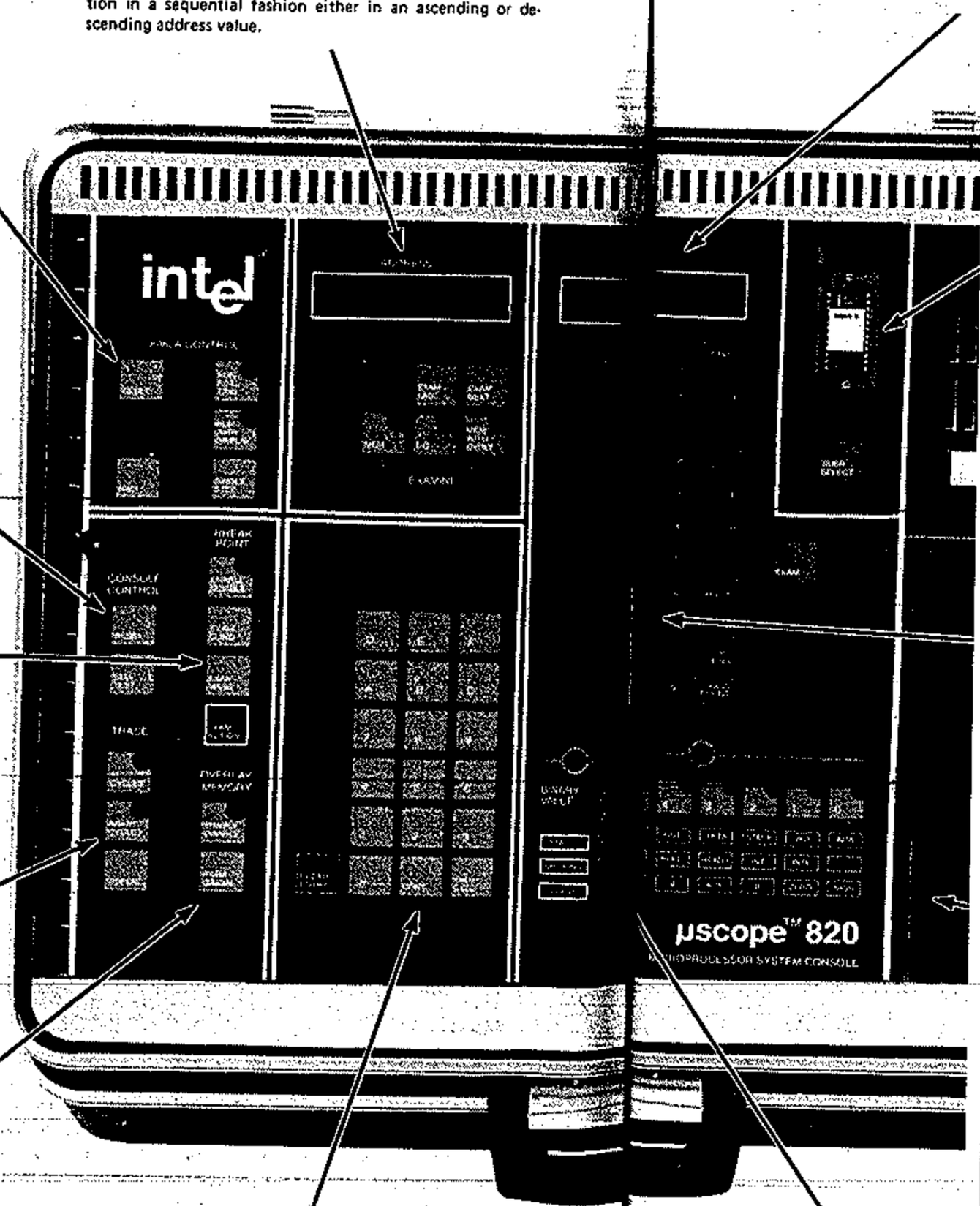
- The address of any memory location.
- The I/O port number of any I/O port.
- The address of any overlay memory location.
- The address of the overlay memory origin assignment.
- The address at which the breakpoint is to occur.
- The address portion of the breakpoint mask.
- The address of the given trace record element.

An additional feature of the address display/select logic is that once the operator has initiated a given memory, trace, or I/O examination, it is possible to continue the examination in a sequential fashion either in an ascending or descending address value.

VALUE DISPLAY/SELECT

The value displays provide
tion. Together with the addr
taneous readout of trace
and breakpoint mask values,
contents. In addition, the
single and double byte regist
and flags, information regar
lowing the occurrence of a
tion regarding the breakpoin

The information displayed b
readouts is selected via the
junction with any of the inst
keys. Further, the informati
or is continually updated 1C
run with display mode.



OVERLAY MEMORY

A unique feature of the unit is the ability to map its memory onto the SUT memory space. Using the overlay memory allows the operator to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. The subroutine can either be entered via the front panel hexadecimal keypad or via the front panel's ROM/PROM socket.

By using the unit's overlay memory, the operator can quickly set up the SUT to execute special maintenance or troubleshooting programs that permit rapid evaluation of system operation.

ADDRESS, DATA, AND CONTROL ENTRY

The address, data, and control variable entry into the instrument is accomplished via the conveniently located hexadecimal keypad.

For selection of the information to be displayed or modified the operator enters the hexadecimal value of the desired address, I/O port number or label assigned to each of the registers. Once this entry is made, the operator can then elect to either CONTINUE data entry if modification is desired or press the END/EXECUTE key if examination only is desired. For all data entry sequences that potentially require multiple value entry, the μScope™ 820 Microprocessor System Console provides operator prompting to indicate the specific information expected.

BINARY DATA DISPLAY/M

All 8-bit values can be displ
instrument. The binary displa
hexadecimal display and it is
where operator recognition is
tion. The selection procedure
identical to that for the hex
the selection has been made
value by means of further
changing the binary state of
8 binary data switches.

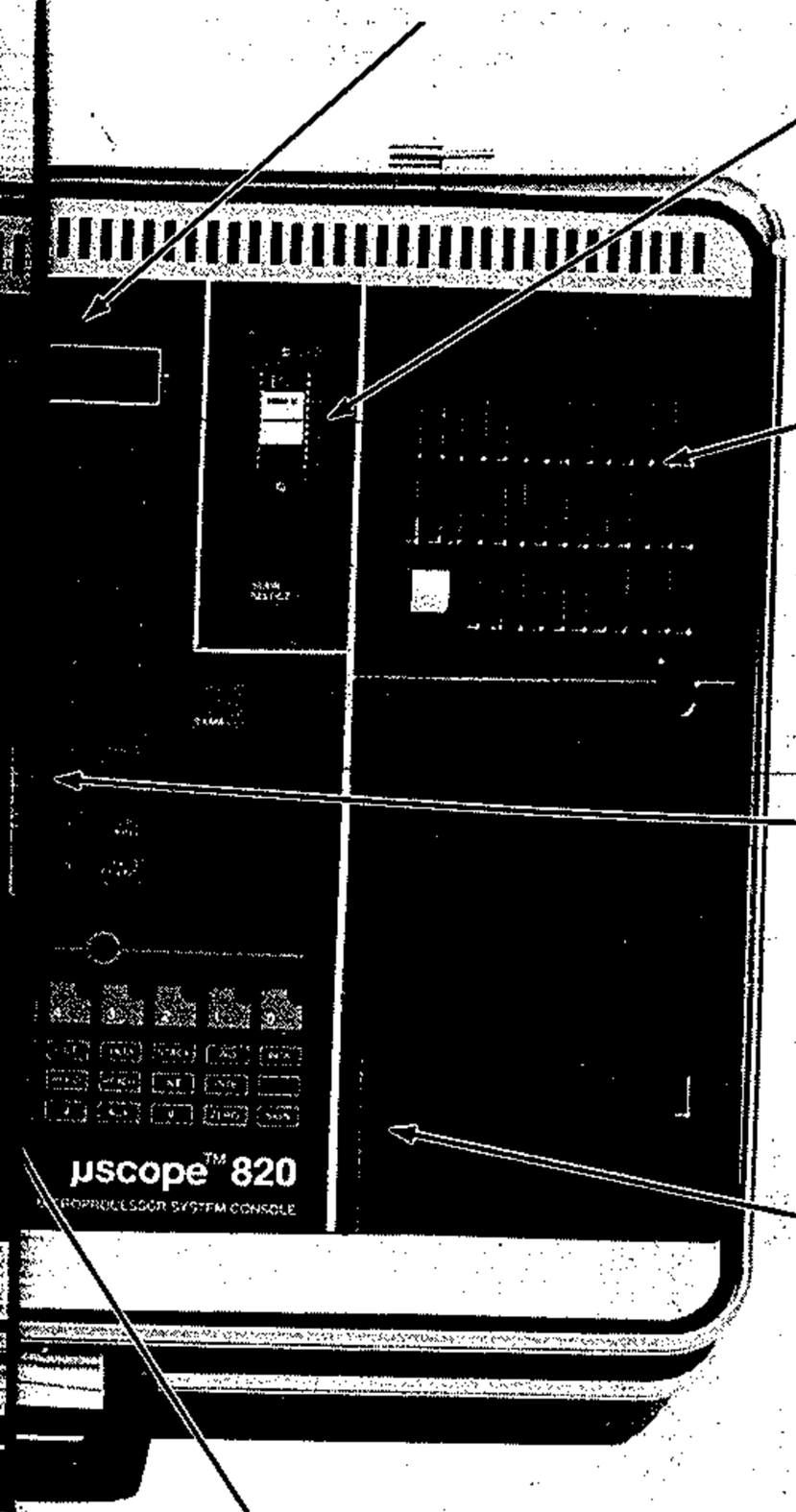
VALUE DISPLAY/SELECT

The value displays provide clear and easy to use information. Together with the address display, they provide simultaneous readout of trace vectors, breakpoint conditions and breakpoint mask values, memory contents and I/O port contents. In addition, the display allows readout of all single and double byte register values, the state of CPU pins and flags, information regarding the course of action following the occurrence of a breakpoint, as well as information regarding the breakpoint pass count.

The information displayed by the 4-digit hexadecimal value readouts is selected via the hexadecimal keypad in conjunction with any of the instrument's 11 dedicated examine keys. Further, the information is either displayed statically or is continually updated 10 times/sec if the unit is in the run with display mode.

PROM/ROM SOCKET

A front panel socket is provided for mounting 2K PROMs or ROMs that serve as storage for preprogrammed test subroutines. The actual useable program space of the PROM/ROM is 1920 bytes. The remaining 128 bytes of storage, shadowed by RAM, are used by the unit to identify up to 16 separate subroutines in the PROM/ROM and to define the specific instrument states and conditions under which the subroutine will be called. Each of the separate subroutines is uniquely enabled by the SUBR SELECT key and the hex keypad.



POWER SUPPLY

The system console is complete with its own fully regulated DC power supply that provides all the DC power required by the unit itself, as well as that which is required by the associated microprocessor probe. The supply is completely self-contained, including its own AC on/off switch, line fuse, line filter and power cord. An additional feature of the power supply is that it has been designed to permit line voltage selection in the field to facilitate operation with a wide range of AC line voltages and frequencies.

BREAKPOINT ACTION

Following the occurrence of a breakpoint match, the operator has the flexibility to execute a number of different diagnostic operations. The selection of these alternate courses of action is accomplished by pushing the EXAM ACTION key and then entering the assigned value of the specific action desired via the hex keypad. Further keypad entries specify the parametric value of the action selected such as the number of breakpoint pass counts or the start address of a subroutine call following a breakpoint.

PROBE CONNECTION

The instrument is intended to work with many of the microprocessors that are available today. This is accomplished by standardized interface logic which transmits and receives various address, data, and control signals between the system console and the circuitry of the particular probe. The interconnect circuitry between the instrument and probe has been designed to drive a 4-foot cable that permits convenient positioning of the panel and the SUT.

In addition, a board edge connector has been provided for a personality ROM that provides front panel definition and interpretation of specific control signals for different types of microprocessors. This personality ROM is supplied with each probe kit.

BINARY DATA DISPLAY/MODIFICATION

All 8-bit values can be displayed in binary format on the instrument. The binary display operates in parallel with the hexadecimal display and it is provided for those instances where operator recognition is enhanced by binary presentation. The selection procedure for the binary data display is identical to that for the hexadecimal value display. Once the selection has been made, the operator can alter the value by means of further hex keypad entries or by changing the binary state of any of the data bits via the 8 binary data switches.

FRONT PANEL

The front panel of the μScope™ 820 Microprocessor System Console has been designed to be rugged and durable as well as easy to use and understand. A plastic overlay that employs membrane switch contacts provides long lasting durability as well as protection from accidental spills. Audio and tactile feedback for the membrane switches is provided for operator convenience.

Ease of use of the front panel has been further enhanced by human engineering with functional grouping of switches as well as LEDs that prompt the operator during data entry sequences. Graphics have also been added to reinforce the functional switch groupings as well as data entry procedures.