HP13195A

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

WRITE FORMATTER ACCESSORY KIT

(FOR THE 7970E DIGITAL MAGNETIC TAPE UNIT)

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(FOR THE 7970E DIGITAL MAGNETIC TAPE UNIT)

Printed-Circuit Assembly:

13195-60000, Series 1415

NOTE

This manual should be retained with the HP 7970E Digital Magnetic Tape Unit Operating and Service Manual.

HEWLETT-PACKARD COMPANY
P.O. BOX 15, BOISE, IDAHO U.S.A.

Publication History

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First Edition ..... AUG 73
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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation, interfacing, maintenance and replaceable parts information for the HP 13195A Write Formatter Accessory Kit.

1-3. GENERAL DESCRIPTION.

1-4. The write formatter is a single, plug-in printed-circuit assembly (PCA) that prescribes the industry-standard 1600-cpi, phase-encoded tape format of records written on HP 7970E Digital Magnetic Tape Units. Format control is attained by performing writing functions that would otherwise be provided by the tape unit interface or controller. The write formatter generates the identification (ID) burst, pre- and postambles, and tape mark. The write formatter also generates the clock synchronization signal with which data are written. The write format of as many as one master and three slave tape units can be controlled by one write formatter PCA.

1-5. IDENTIFICATION.

1-6. Hewlett-Packard uses five digits and a letter (00000A) to identify standard accessories. If the designation of the accessory received does not agree with the designation on the title page of this manual, there are differences between the accessory received and the accessory described in this manual. These differences are described in manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-7. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked below the part number on the PCA. The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the position of the components. If the series code number does not correspond exactly with the code number on the title page of this manual, the PCA differs from the one described in this manual. These differences are explained in manual supplements available at the nearest HP Sales and Service Office.

1-8. SPECIFICATIONS.

1-9. Specifications for the write formatter are listed in table 1-1.

Table 1-1. HP 13195A Write Formatter Specifications

POWER REQUIREMENTS

+5 Vdc @ 900 mA

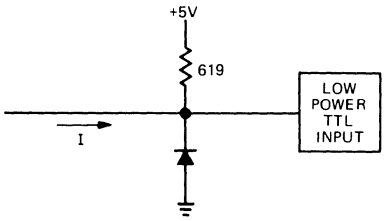
LOGIC LEVELS

Line Receivers (TTL):

D0 through D7

Assertion: $V \leq +0.8V$
$I \geq -7.6$ mA at $V = 0.4V$

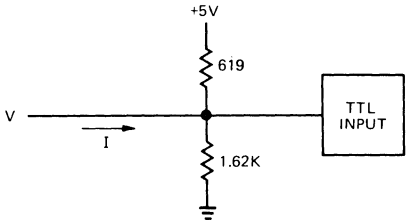
Negation: $V \geq 2.4V$
$V = 5V$ at $I = 0$
$V \geq 2.4V$ at $I = -4.2$ mA



DP, WPA, WID, WTM, EOD and EN

Assertion: $V \leq +0.8V$
$I \geq -9.6$ mA at $V = 0.4V$

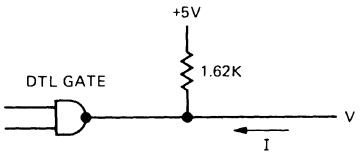
Negation: $V \geq 2.4V$
$V = 3.6V$ at $I = 0$
$V \geq 2.4V$ at $I = -2.6$ mA



Line Transmitters (DTL):

Assertion: $V \leq 0.4V$ at $I = 45$ mA

Negation: $V = 5.0V$ at $I = 0$
$V \geq 2.4V$ at $I = -1.5$ mA



TIMING

- Commands must be asserted a minimum of one-half character period.
- Commands must be removed before RDY is again asserted or multiple execution of the command may result.
- The first data byte must arrive at the interface within 40 character periods of the assertion of WPA.
- DA (Data Accepted) will be asserted for one-half character period.
- New data or EOD must arrive at the interface with one character period less 0.5 μs.
- EOD must be negated before presentation of the first data byte.
- Transmission delays must be included in minimum timing.

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides unpacking, initial inspection, installation, and programming information for the HP 13195A Write Formatter Accessory Kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4. If the write formatter is received separately from the tape unit, inspect the shipping carton before opening. If there is external evidence of damage or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5. Inspect the accessory as it is unpacked. If the PCA is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-6. TAPE-SPEED STRAPPING.

2-7. The write formatter PCA is equipped with strapping connections that modify clock synchronization circuits to permit compatibility with the various tape-speed versions of the tape units. Before installing the write formatter PCA, be sure that the strapping connections are properly configured for the respective tape unit(s). Tape-speed strapping configurations are shown in figure 2-1.

2-8. INSTALLATION.

2-9. Install the write formatter PCA as follows:

a. Set computer and master tape unit power switches to off.

b. Open tape unit for access to write data module assembly.

c. Position the parity jumper on the write formatter PCA (adjacent to U33) on terminal 3 to write nine-bit bytes as transferred by the system interface; or on terminal 4 to write nine-bit bytes, including a parity bit determined by the eight data bits transferred by the system interface.

d. Install the write formatter PCA J2 into tape unit WJ11 above the write data module assembly shown in figure 2-2.

e. Connect write formatter PCA power connector to WJ12 in the tape unit.

f. Thread two number 6-32, 0.75-inch screws with number 6 lockwashers through the holes provided in the write formatter PCA and into the write data module assembly.

g. Connect the WRITE connector of the system interface cable to J1 on the write formatter PCA.

h. Close tape unit and set computer and tape unit power switches to on.

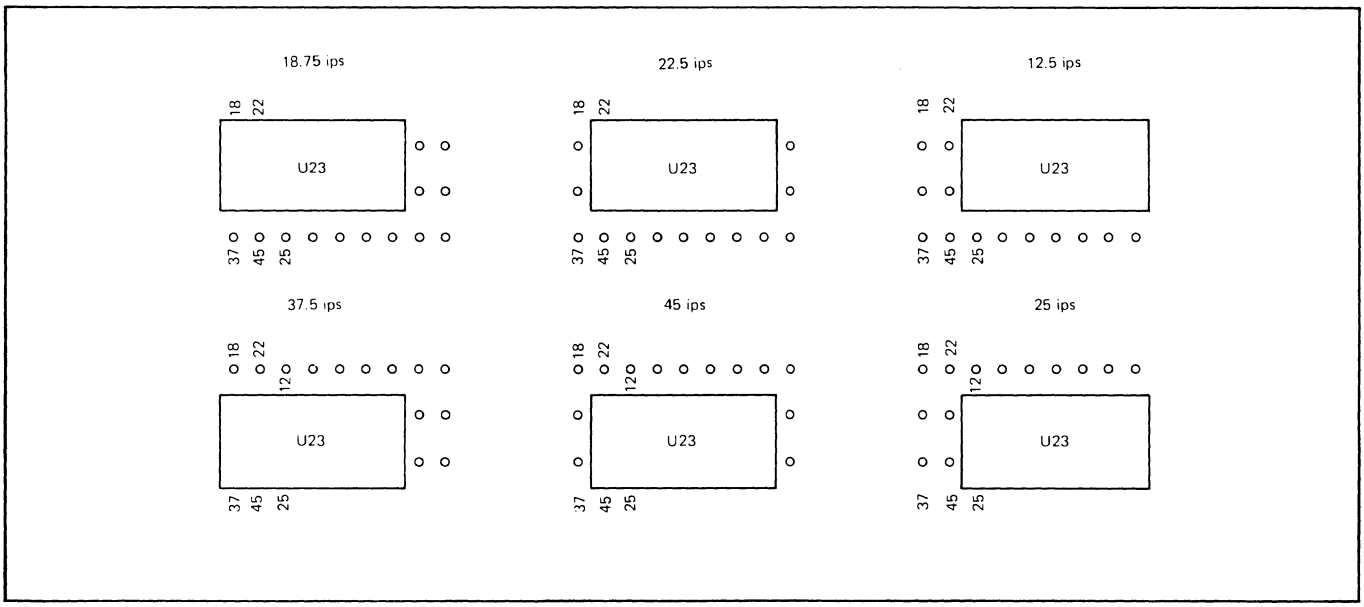


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Figure 2-1. Alternative Tape-Speed Strapping Configurations

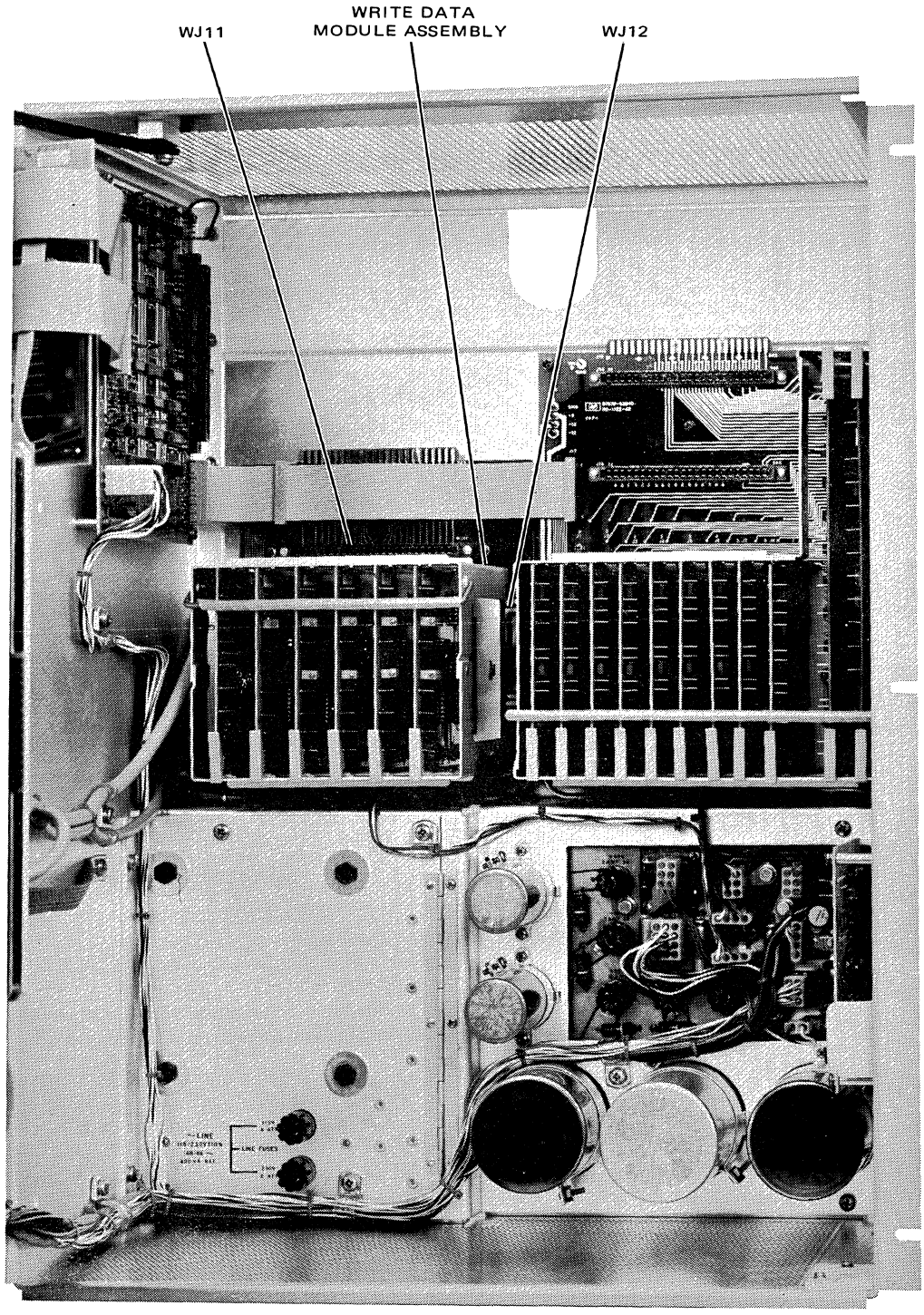

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Figure 2-2. Write Formatter Installation

2-10. PARALLELING TAPE UNITS.

2-11. Each write formatter can provide format control for as many as one master and three slave tape units. Information for connecting tape units for parallel operation is contained in the HP 13194A Multiunit Cable Accessory Kit Operating and Service Manual.

2-12. INTERFACE CONSIDERATIONS.

2-13. WRITE FORMATTER SIGNAL DEFINITIONS.

2-14. The controller or interface of the system in which the write formatter and the associated tape unit(s) are employed must be compatible with the write formatter signals as described in paragraphs 2-15 through 2-22. An interface block diagram for the write formatter is shown in figure 3-1.

2-15. READY. The Ready status line to the interface, when low, indicates that the write formatter will accept a command from the interface. When high, the Ready status line indicates that a command has been accepted and execution of the command is in process.

2-16. WRITE ENABLE. The Write Enable input to the write formatter must be made low by the interface for any write operations to be performed. When the Write Enable input is high, all other write formatter inputs and all outputs except the Twice-Data-Frequency signal are disabled.

2-17. When a write operation is desired, the Write command must be low for at least a half-character time. The tape unit will acknowledge receipt of the Write command by making the Ready status signal high.

2-18. WRITE ID BURST. A Write ID Burst command issued by the interface causes the write formatter to write 5600 characters (in an alternate ones and zeros pattern) in track 4 (ANSI) and to dc erase tracks 1 through 3 and 5 through 9. The Write ID Burst command should be low until the write formatter Ready status signal becomes high. Once Ready status becomes high, the interface may discontinue the Write ID Burst command. When the identification burst is completed, ready status will be low. Refer to table 2-1 for ANSI/IBM track designation cross-references.

Table 2-1. ANSI/IBM Track Designations

ANSI	IBM
1	5
2	7
3	3
4	P
5	2
6	1
7	0
8	6
9	4

2-19. WRITE TAPE MARK. A Write Tape Mark command issued by the interface will cause the write formatter to write 40 zeros in tracks, 1, 2, 4, 5, 7, and 8 (ANSI) and to dc erase tracks 3, 6, and 9. Ready status will be made low when the write tape mark operation is complete.

2-20. DATA ACCEPTED. The Data Accepted signal is generated by the write formatter to indicate to the interface that the data byte just presented or an End-of-Data signal has been accepted. The write formatter should receive the next data byte or End-of-Data signal within one character time less 0.5 microsecond of the Data Accepted signal leading edge. If no new data are presented, the write formatter will write whatever data are present on the write data input lines.

2-21. END-OF-DATA. An End-of-Data signal received by the write formatter indicates the last data byte has been presented. The write formatter will automatically generate a Data Accepted signal and write a postamble in all tracks. The postamble consists of an all-ones character followed by 40 all-zero characters. Ready status will be made low when the postamble is completed.

2-22. WRITE PREAMBLE. A Write Preamble command issued by the interface will cause the write formatter to write 40 all-zero characters followed by an all-ones character in all tracks. The first data byte to be written after the preamble must be presented within 40 character periods after the issuance of the Write Preamble command. If no data are presented, the write formatter will write whatever data are present on the write data input lines.

2-23. WRITE FORMATTER PCA CONNECTOR.

2-24. The controller or interface cable of the system in which the write formatter and the associated tape unit(s) are employed must be compatible with the write formatter PCA connector pin J1 assignments listed in table 2-2.

Table 2-2. Write Formatter PCA Connector J1 Pin Assignments

SIGNAL NAME	MNEMONIC	ACTIVE PIN	GROUND PIN
Write Status	SW	6X	6
Twice Data Frequency	2DF	7X	7
Data P	WDP	9X	9
Data 0	WD0	10X	10
Data 1	WD1	11X	11
Data 2	WD2	12X	12
Data 3	WD3	13X	13
Data 4	WD4	14X	14
Data 5	WD5	15X	15
Data 6	WD6	16X	16
Data 7	WD7	17X	17
Ready	RDY	18X	18
Data Accepted	DA	19X	19
Write Enable	EN	20X	20
Write Preamble	WPA	21X	21
End-of-Data	EOD	22X	22
Write Tape Mark	WTM	23X	23
Write ID Burst	WID	24X	24

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section describes the theory of operation of the write formatter. See the foldout schematic diagram in the maintenance section (figure 4-1) for an illustration of the circuits described in this section.

3-3. INTERFACE DESCRIPTION.

3-4. Figure 3-1 contains an interface block diagram for the write formatter. As shown in figure 3-1, the write formatter provides synchronization timing signals for the controller and tape unit, provides data transfer paths between the controller and tape unit, accepts write commands from the controller, generates identification bursts, pre- and postambles, and tape marks on command, and provides write formatter status signals for the controller. The synchronization timing signals consists of Write Clock (WC) timing signals for the tape unit and Twice Data Frequency (2DF) timing signals for the controller. The write command signals from the controller consist of Write Enable signals, Write Identification Burst signals, Write Tape Mark signals, Write Preamble signals, and End-of-Data signals. The status signals applied to the controller consist of Ready signals and Data Accepted signals. Detailed definitions of these signals are contained in paragraphs 2-13 through 2-22.

3-5. BLOCK DIAGRAM DISCUSSION.

3-6. Paragraphs 3-7 through 3-23 contain a discussion of the write formatter at the block diagram level. Figure 3-2 contains a block diagram of the write formatter and figure 3-3 contains an associated timing diagram illustrating a typical phase encoded write operation.

3-7. SYSTEM CLOCK.

3-8. The system clock supplies a Twice Data Frequency (2DF) pulse train to the external system interface, the phase encoded (PE) write sequencer logic, and the sequence control logic for signal synchronization. It also supplies a delayed 2DF for generating the Write Clock (WC) pulse train applied to the tape unit. The system clock uses a crystal oscillator to supply a base frequency from which the synchronization frequencies are derived. To be compatible with the six tape-speed versions of the tape unit, a dummy plug (U23) is supplied to establish coordination between 2DF and the density of recorded data. The 2DF rate for each tape speed is shown in figure 4-1.

3-9. System clock oscillator Y1 operates at 7.2 MHz which is reduced to 720 kHz by divide-by-ten counter U22. Depending on the position of dummy plug U23, this frequency is again reduced by programmable counter (divide-by-5, 6, or 9) U12 to 2DF rates of either 144, 120 or 80 kHz. For the slower tape speeds, these frequencies are further reduced by divide-by-two flip-flop U24 to 2DF rates of 72, 60, and 40 kHz. The 2DF pulse train applied through delay and shaping circuit U14 is delayed to compensate for the propagation delay of the write formatter circuits and applied to "nand" gate U54 along with the Write Clock Enable (WCEN) pulse train from the PE write sequencer logic decode gates to generate the WC pulse train for the tape unit.

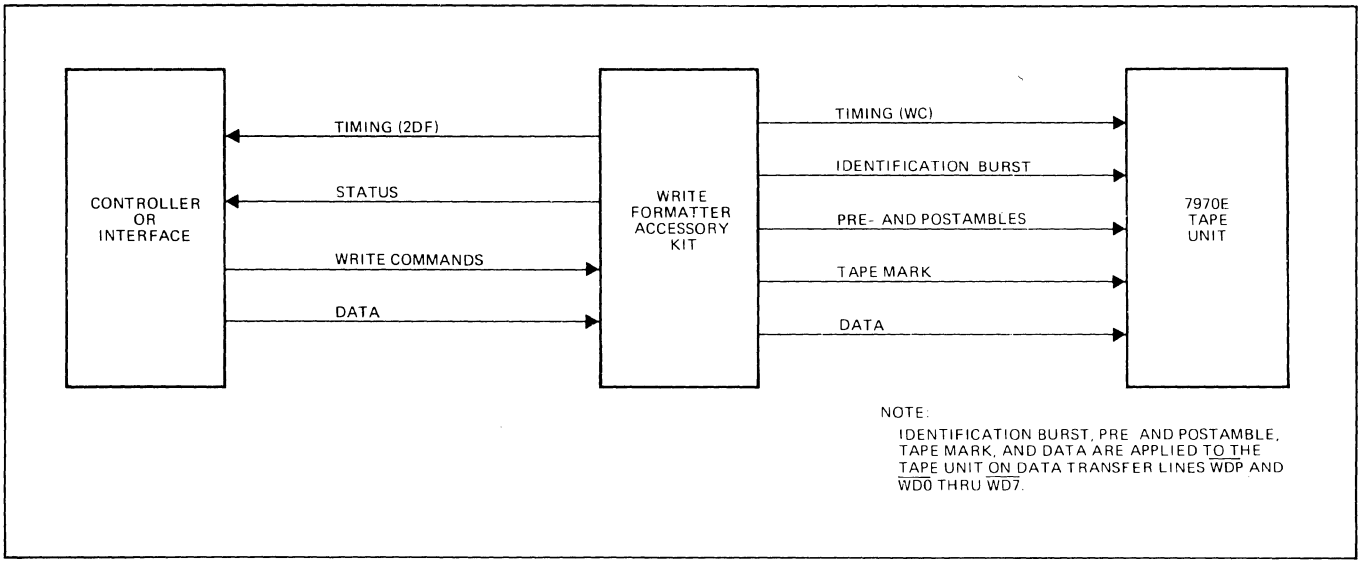

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Figure 3-1. Interface Block Diagram

3-10. SEQUENCE CONTROL LOGIC.

3-11. The sequence control logic, in conjunction with the write commands from the system interface, controls the sequence of the write functions. Control of the write functions is performed by sequencing control signals to activate various logic functions at the appropriate times. Since each logic circuit group depends on control signals from the other for some of its operations, the sequence control logic and PE write sequencer logic may operate at the same time.

3-12. The Enable (EN), Write Identification Burst (WID), Write Preamble (WPA), Write Tape Mark (WTM), and End-Of-Data (EOD) write commands are applied through the complex of state control input gates to initiate the specific write functions. These signals are combined with control signals from the state decoder logic, byte counter, and PE write sequencer logic to provide the Sequence Control Clock (SCC), set, and reset signals required to sequence the state control flip-flops (CTL A, B, and C) which select the specific write functions at specific times. The state decoder logic decodes the write function signals from the state control flip-flops and generates the signals required to enable the appropriate groups of logic for each write function. In addition, the sequence control logic generates a Ready (RDY) status signal during its clear state for the external system interface. During its data transfer state, the sequence control logic generates an Enable Flag (ENF) signal that is applied to "nand" gate U74 along with the Data Frequency (DF) pulse train from the PE write sequencer logic to generate the Data Accepted (DA) status signal for the external system interface.

3-13. PE WRITE SEQUENCER LOGIC.

3-14. The PE write sequencer logic controls the format of the write functions and, in conjunction with the true/complement logic, performs the functions required to convert data into PE format. Once the sequence control logic has initiated a specific write function, a Start signal (any state except clear) is applied to the PE write sequencer logic start and data frequency flip-flops (SWS FF and DF FF) which generate the sequenced Write Control (WRT CTL) pulse trains required by the decode gates and sequence control logic. The decode gates use the WRT CTL pulse trains to generate WCEN signals at data frequency for the generation of the tape units WC pulse train (refer to paragraph 3-9) and to generate the Load Data Buffer (LDB) pulse train required by the sequence control logic, byte counter, data buffer, and parity buffer. The decode gates also combine write ID state signals from the sequence control logic and the odd bit count pulse train from the byte counter with the WRT CTL pulse trains to generate the Invert Data (INV) and Invert Parity (INVP) pulse trains required by the true/complement logic.

3-15. BYTE COUNTER.

3-16. The byte counter provides the bit counts required by the write formatter to generate the write functions in their prescribed byte formats. The counter is clocked by the LDB pulse train from the PE write sequencer logic and receives its Count Control (CNT CTL) signals from the sequence control logic. When enabled, the counter provides the odd count of bits required by the PE write sequencer logic to generate INV and INVP pulse trains and the counts of 40 and 5600 bits required by the sequence control logic to signal the completion of writing tape marks (TMD), pre- and postambles (PAD), and identification burst (IDD).

3-17. DATA BUFFER AND PARITY GENERATOR.

3-18. The data buffer accepts and stores 16 bits of data (eight bits from the external system interface and eight bits from the sequence control logic) and, under control of the sequence control logic and PE write sequencer logic, transfers the appropriate eight-bit byte to its output lines. Selection of internal or external data transfer is controlled by an Internal/External Select (I/E SLT) signal from the sequence control logic. Transfer of the selected data bits from storage to the output lines is controlled by the LDB pulse train from the PE write sequencer logic.

3-19. If the parity jumper is connected between terminals 1 and 4, the eight data output lines (D0 thru D7) are monitored by the parity generator which adds the parity bit (DP) to the output lines. If the parity jumper is connected between terminals 1 and 3, the parity bit is determined by a data bit applied to the parity buffer logic from either the external system interface or the sequence control logic. Storage and transfer control of DP through the parity buffer logic is the same as control of the data bits through the data buffer.

3-20. TRUE/COMPLEMENT LOGIC.

3-21. The true/complement logic combines the nine-bit output byte with the INV and INVP pulse trains from the PE write sequencer logic to generate alternate ones and zeros when writing an ID burst or to generate a complement signal of a specific data bit when a phase transition of that bit is required for PE format. Figure 3-4 illustrates a typical write timing sequence of a partial data block for one output data line applied to the tape unit and shows the relationship between the tape units write head current and the write formatters phase transition pulses.

3-22. DATA BLOCK DECODER LOGIC.

3-23. The data block decoder logic receives the PE formatted, nine-bit output byte from the true/complement logic, inverts each data bit, and transmits the data signals to the tape unit. The data block decoder logic, under control of the sequence control logic, also applies a d-c erase level to the appropriate data lines when the write formatter is generating ID bursts or tape marks.

3-24. DETAILED DISCUSSION.

3-25. The detailed functional operation of the write formatter is described by the hardware flowchart and associated annotations shown in figure 3-5. Table 3-1 contains a list of definitions for the mnemonics used in figure 3-5. Input/output signal name mnemonics are defined in table 2-2.

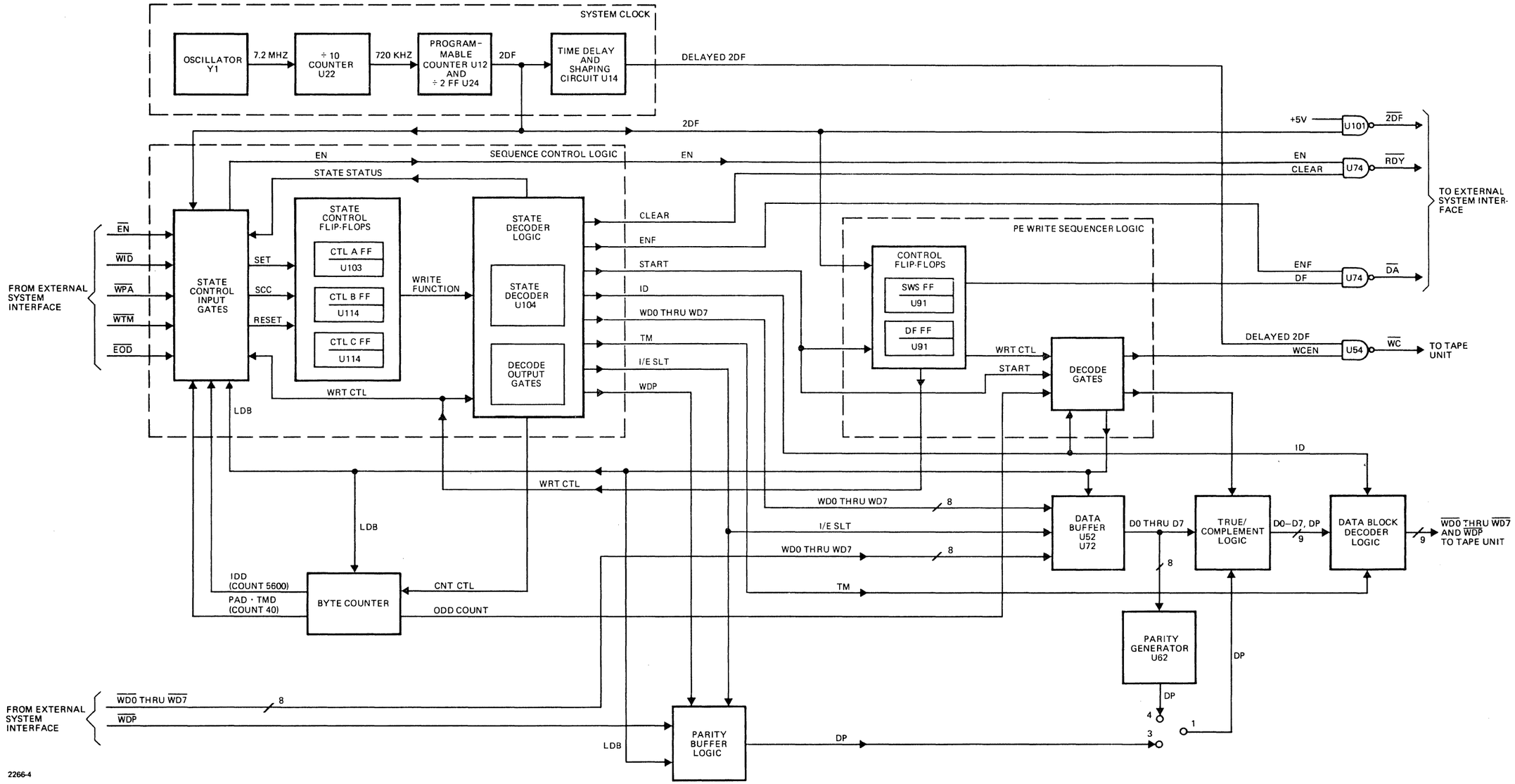

Figure 3-2. Write Formatter Block Diagram

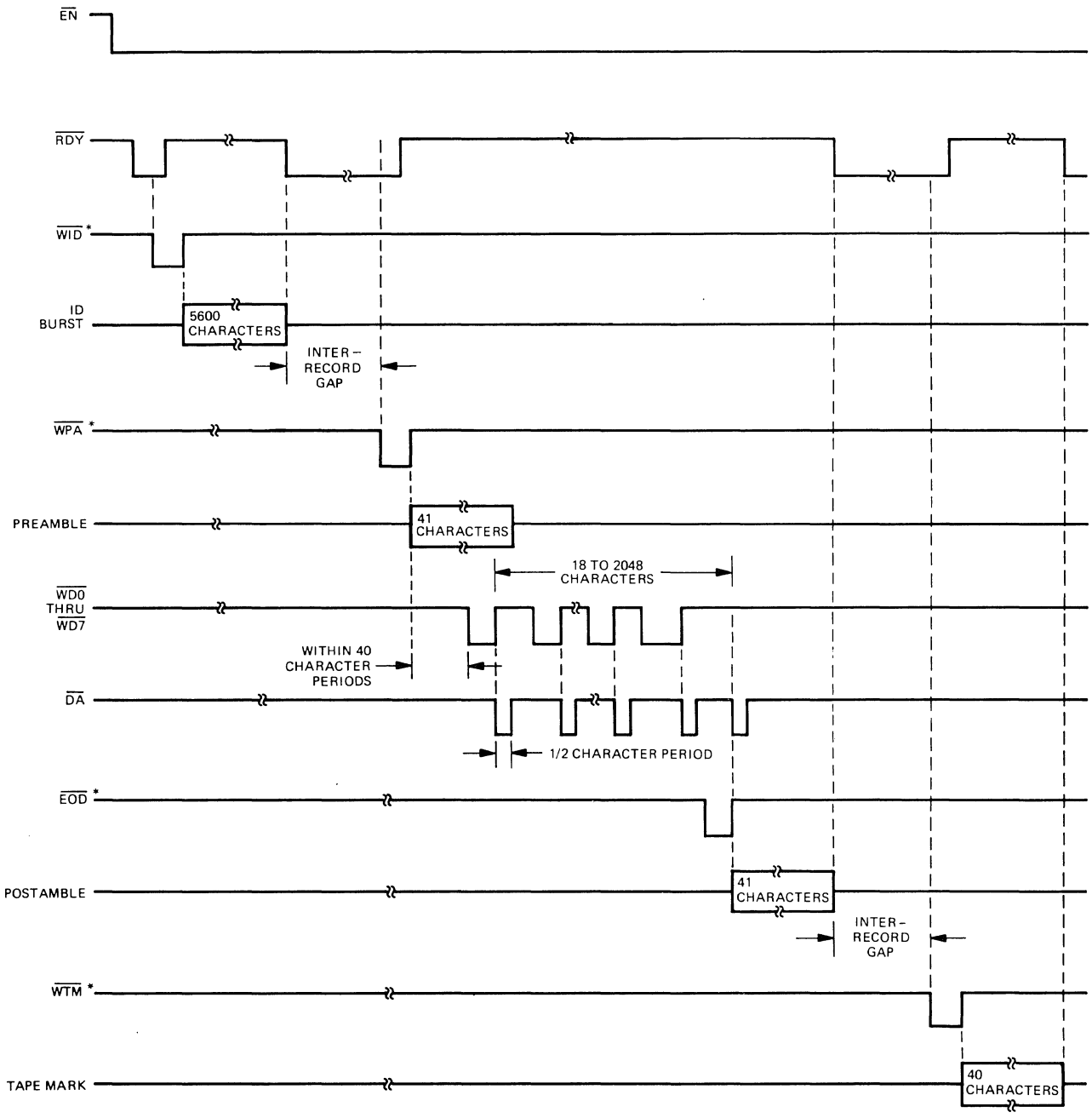

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Figure 3-3. Typical PE Write Format Operation Timing Diagram

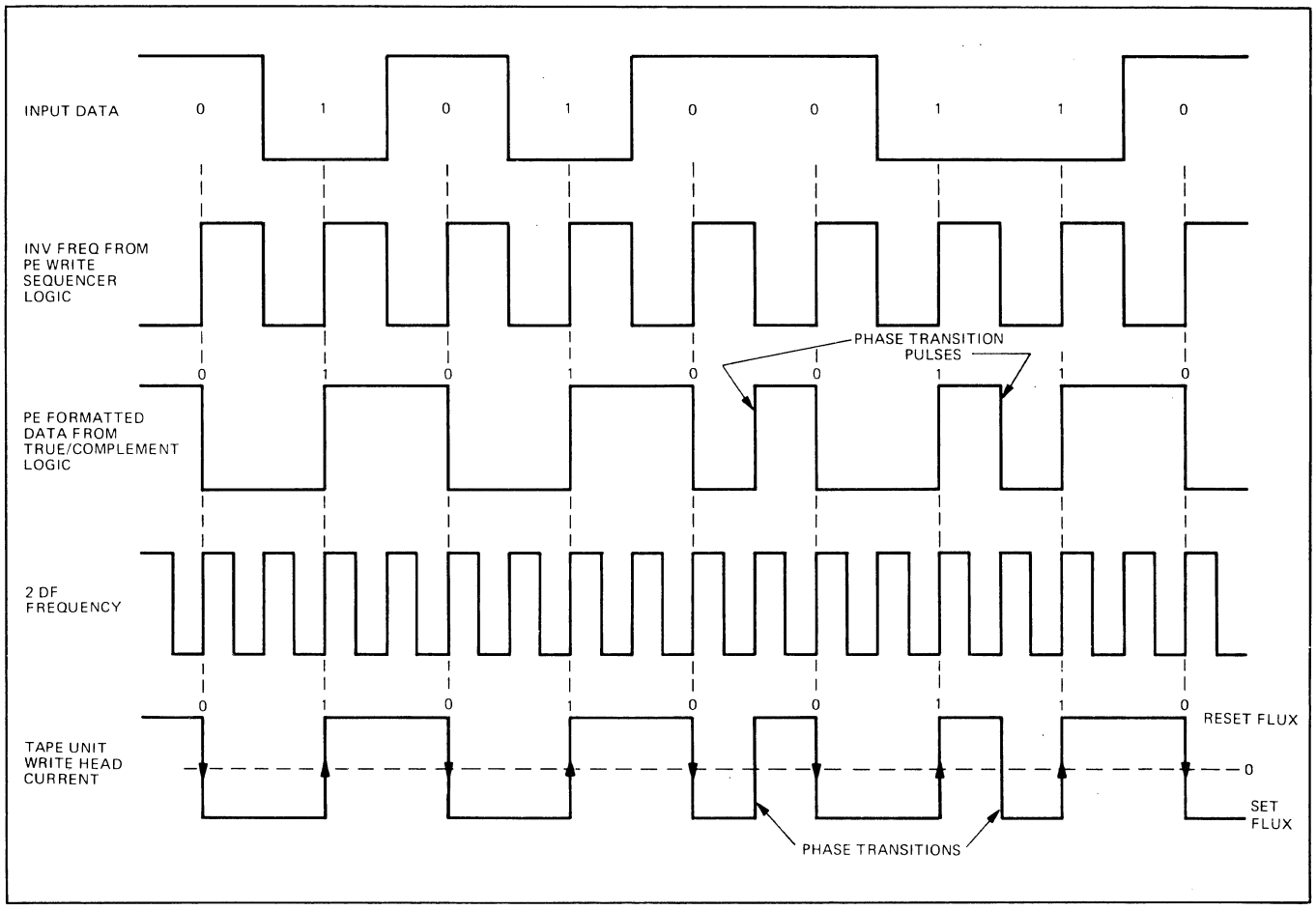

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Figure 3-4. PE Write Timing Diagram

Table 3-1. Flowchart Mnemonic Definitions

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
CLCNT	Clear byte counter to zero	INVP	Invert parity bit (WDP)
CNTEN	Enable byte counter	LDB	Load data buffer
CTL FF	Control flip-flops	ODD	Odd bit count
DB	Data block being written	PA	Pre- or postamble being written
DF	Data frequency	PAD	Pre- or postamble done (40 count)
D OS	Delay one-shot	SCC	Sequence control clock
ENF	Enable flag	S OS	Shaping one-shot
ID	ID burst being written	STCNT	Set byte counter to one
IDD	ID burst done (5600 count)	SWS	Start write sequence
IDRFS	ID burst reset flux state	TM	Tape mark being written
I/E SLT	Internal/external data select	TMD	Tape mark done (40 count)
INV	Invert data bits (WD0 through WD7)	TMRFS	Tape mark reset flux state
		WCEN	Write clock enable

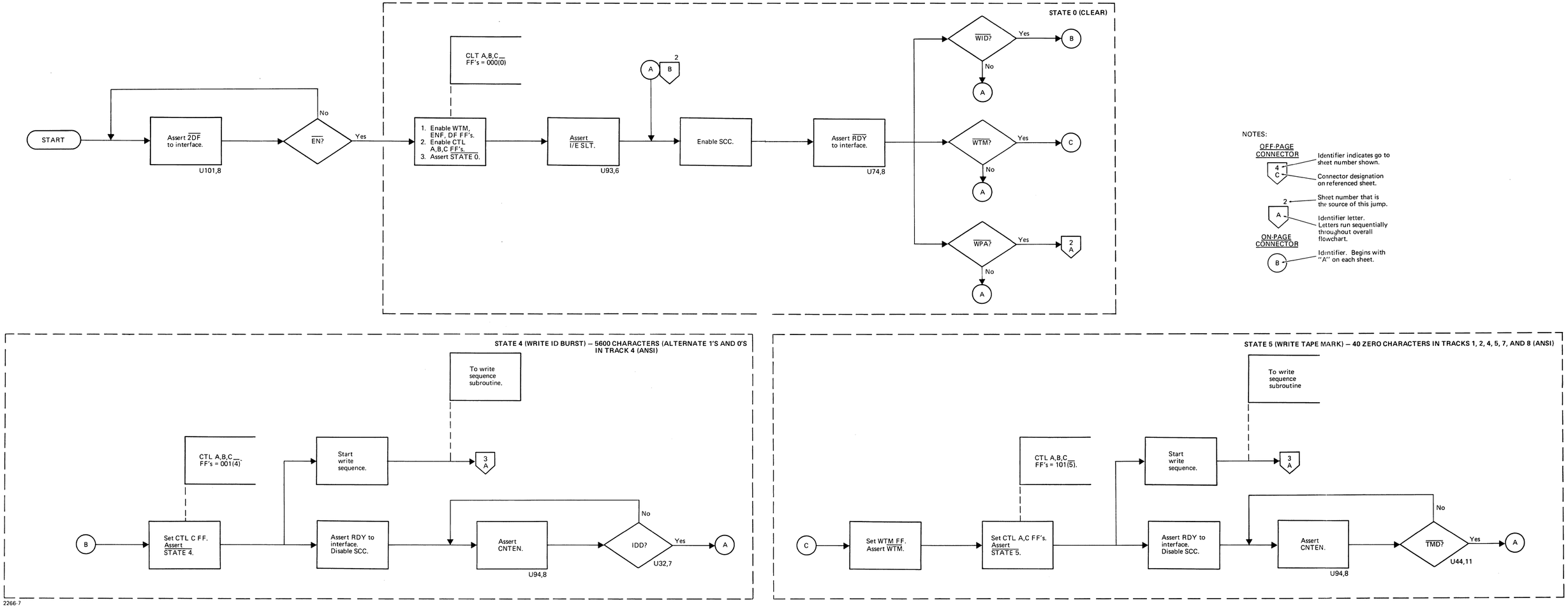

Figure 3-5. Write Formatter Flowchart (Sheet 1 of 3)

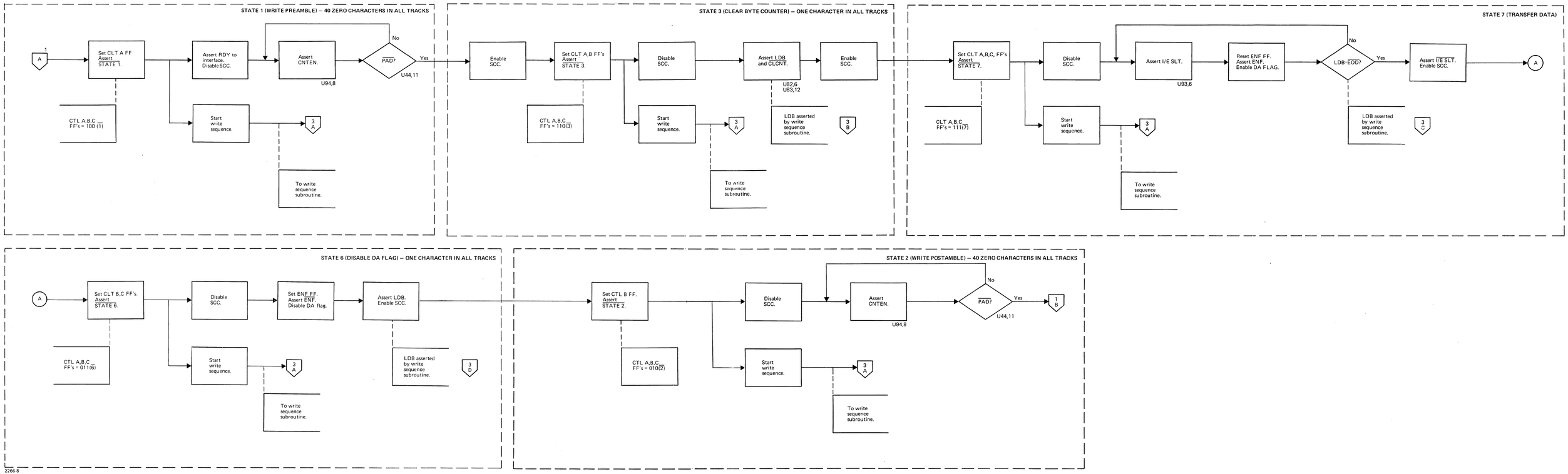

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Figure 3-5. Write Formatter Flowchart (Sheet 2 of 3)

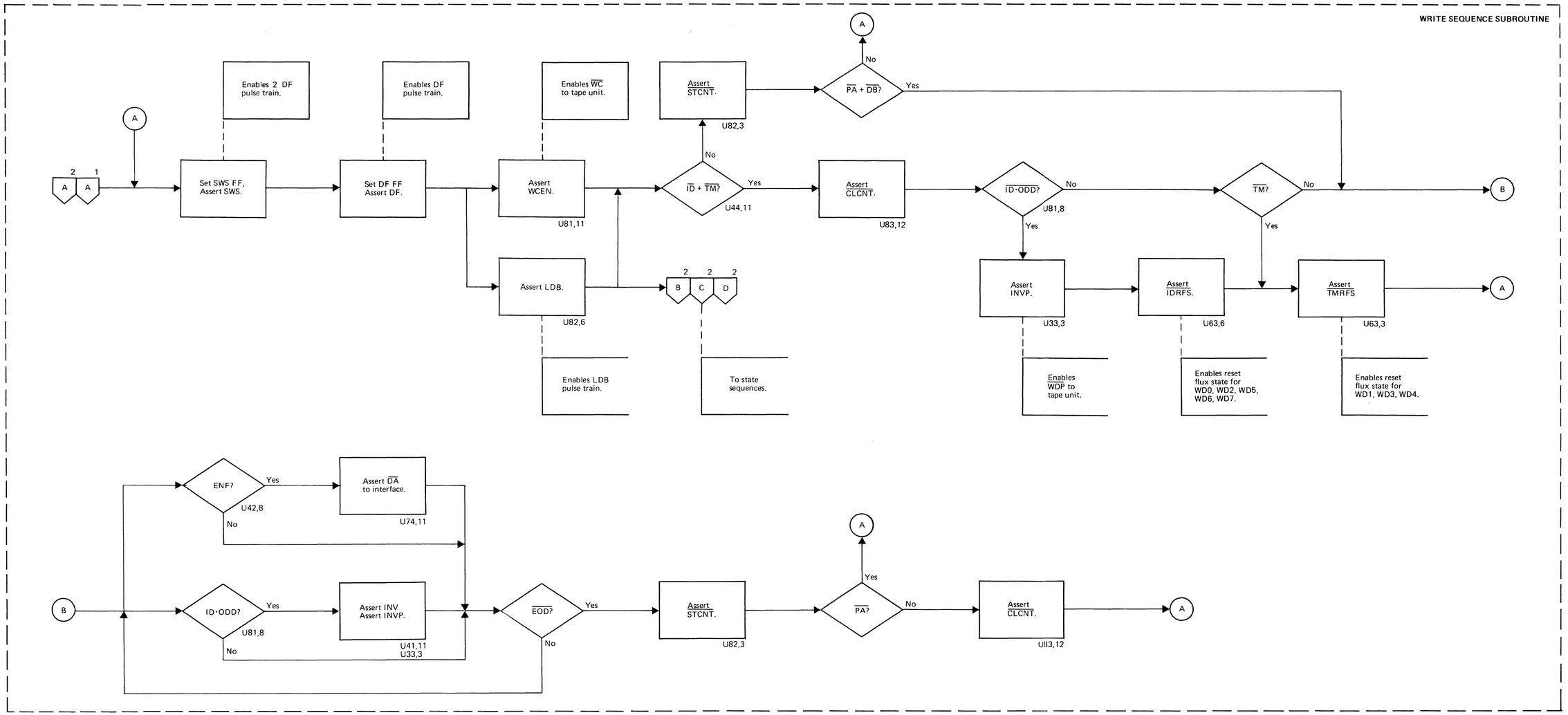


Figure 3-5. Write Formatter Flowchart (Sheet 3 of 3)

4-1. INTRODUCTION.

4-2. This section contains maintenance information for the HP 13195A Write Formatter Accessory Kit. Included are preventive maintenance and troubleshooting information. Parts lists and parts location and schematic diagrams are provided as an aid to troubleshooting.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are provided in the HP tape unit documentation. There are no separate preventive maintenance procedures to be performed on the write formatter.

4-5. TROUBLESHOOTING.

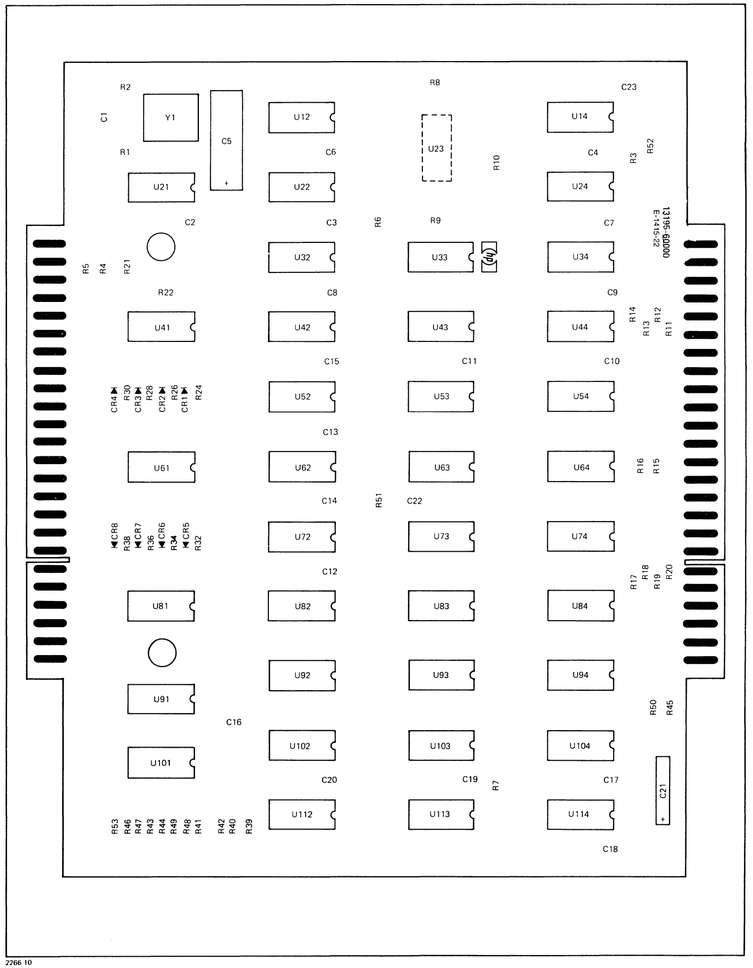
4-6. Troubleshooting the write formatter is accomplished by performing the tape unit write module performance tests using the write formatter test PCA given in the tape unit documentation and analyzing any performance deficiencies. If any malfunction is isolated to the write formatter, further isolation of trouble can be accomplished by referring to the theory of operation section and to the parts location and schematic diagram in figure 4-1.

4-7. Figure 4-2 contains logic diagrams and pin locations for the integrated circuits used on the write formatter. Table 4-1 gives the integrated-circuit input levels, output levels, and delay times that correspond to the characteristic number shown below each diagram in figure 4-2. Table 4-2 is the parts list for the write formatter. The parts are listed in alphanumeric order by reference designation.

Table 4-1. Integrated Circuit Characteristics

CHARACTERISTIC NUMBER	INPUT VOLTAGE		OUTPUT VOLTAGE		OPEN INPUT ACTS AS	MAX. PROPAGATION DELAY	
	MINIMUM HIGH LEVEL	MAXIMUM LOW LEVEL	MINIMUM HIGH LEVEL	MAXIMUM LOW LEVEL		TO HIGH LEVEL (NS)	TO LOW LEVEL (NS)
2	2.0	0.8	2.4	0.4	Logic 1	29	15
3	2.0	0.8	2.4	0.4	Logic 1	12	10
5	2.0	0.8	(1)	0.4	Logic 1	45	15
7	2.0	0.8	2.4	0.4	Logic 1	50(2)	50
8	2.0(3)	0.8	2.4	0.4	Logic 1	35	50
12	2.0	0.7	2.4	0.3	Logic 1	35	35
29	2.0	0.7	2.4	0.3	Logic 1	200	200
34	2.0(4)	0.8	2.4	0.4	Logic 1	30	45
44	1.8	1.1	2.5	0.4	Logic 1	15	15
49	1.8	1.1	2.5	0.4	Logic 1	10	10
50	1.8	1.1	2.5	0.4	Logic 1	25	25
53	2.0	0.8	2.5	0.4	Logic 1	60	68
61	2.0	0.8	2.4	0.4	Logic 1	22	15
63	2.0	0.8	2.4	0.4	Logic 1	30	22
72	1.9	1.1	2.6	0.45	Logic 1	60	35

NOTES:
(1) Level depends on load.
(2) Required clock pulse width 20 ns min; set-clear 25 ns min.
(3) Required pulse widths 30 ns min.
(4) Required clock pulse widths 20 ns min.



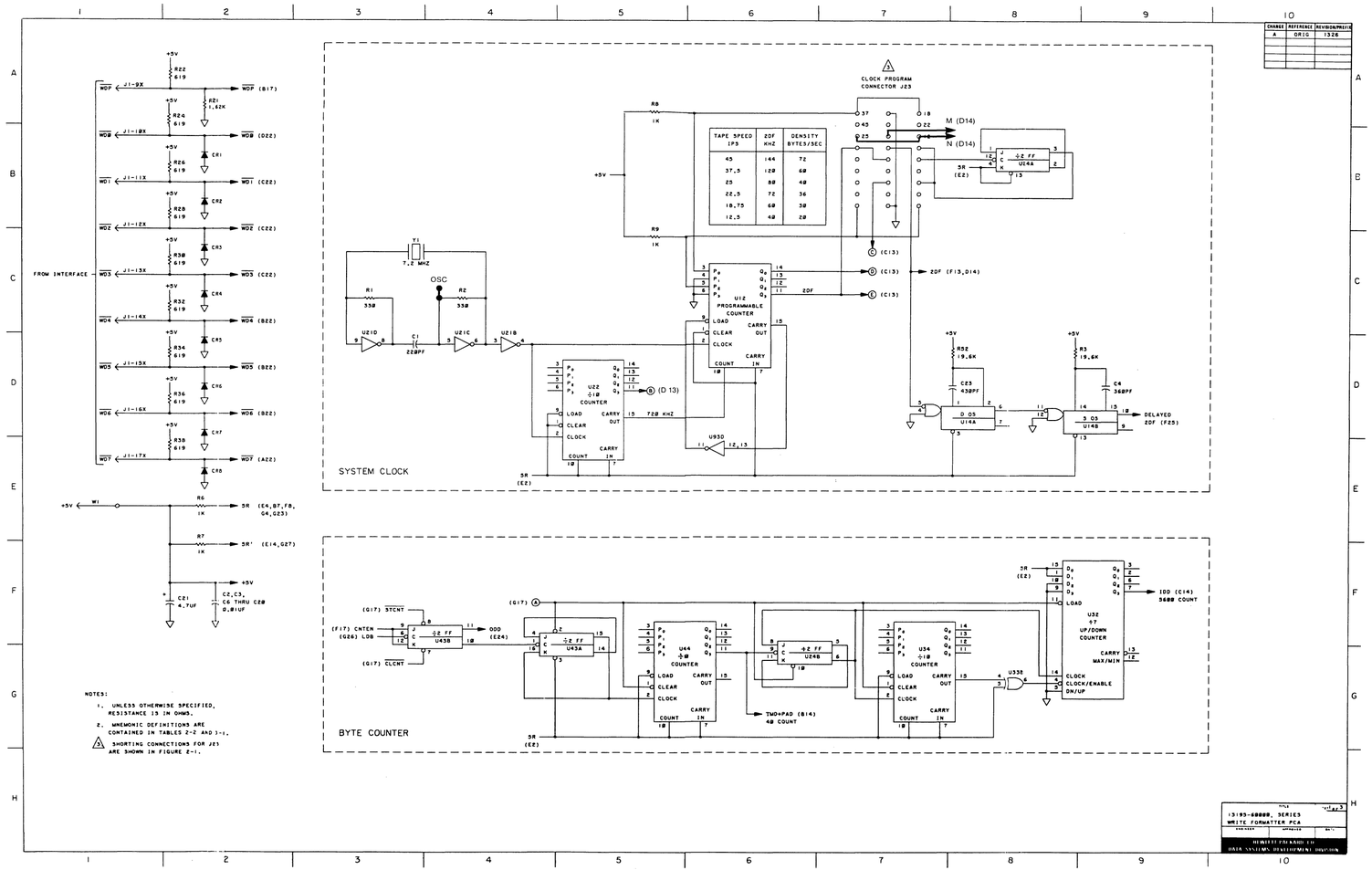


Figure 4-1. Write Formatter Schematic and Parts Location Diagram (Sheet 1 of 3)

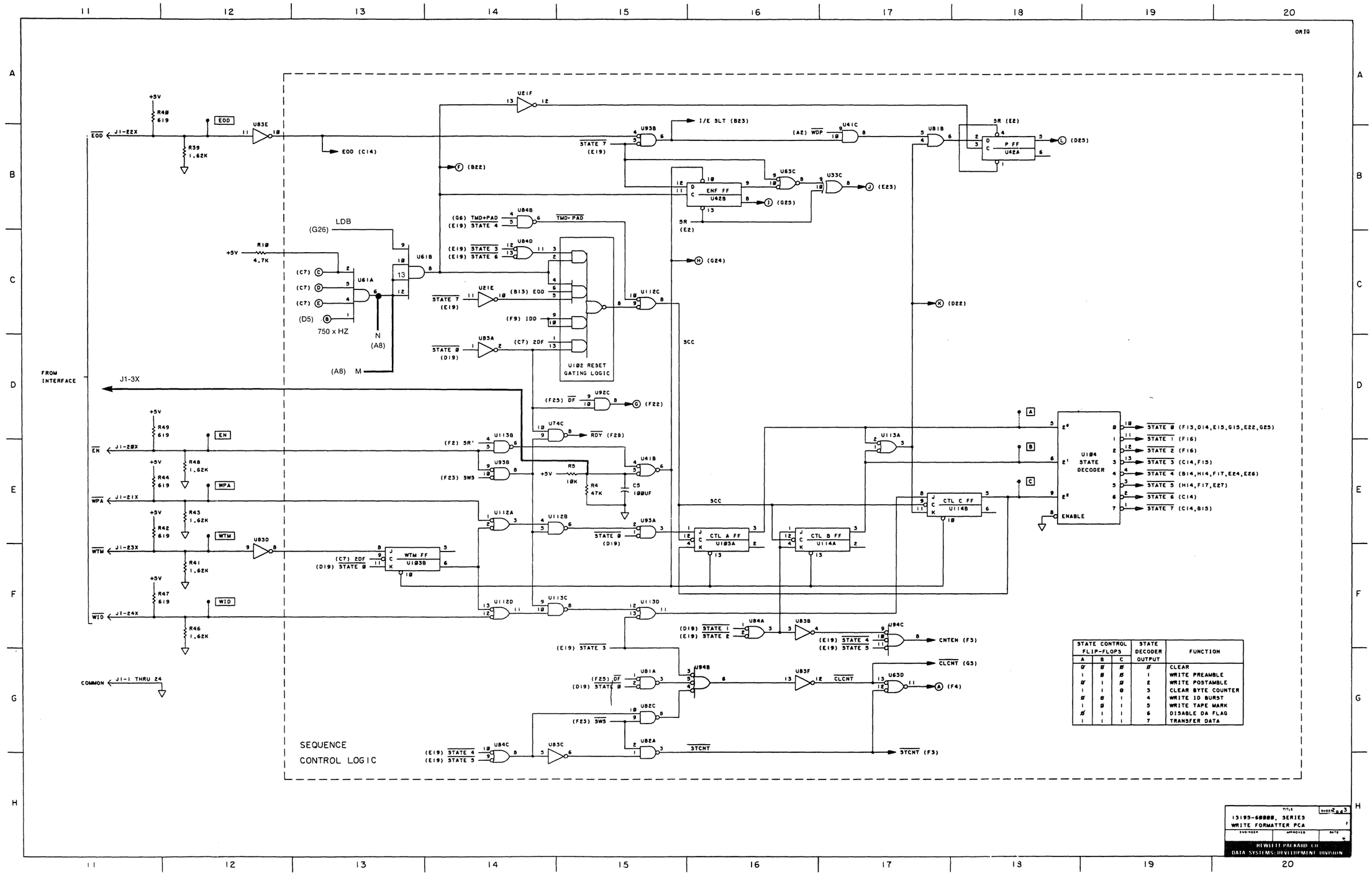


Figure 4-1. Write Formatter Schematic and Parts Location Diagram (Sheet 2 of 3)

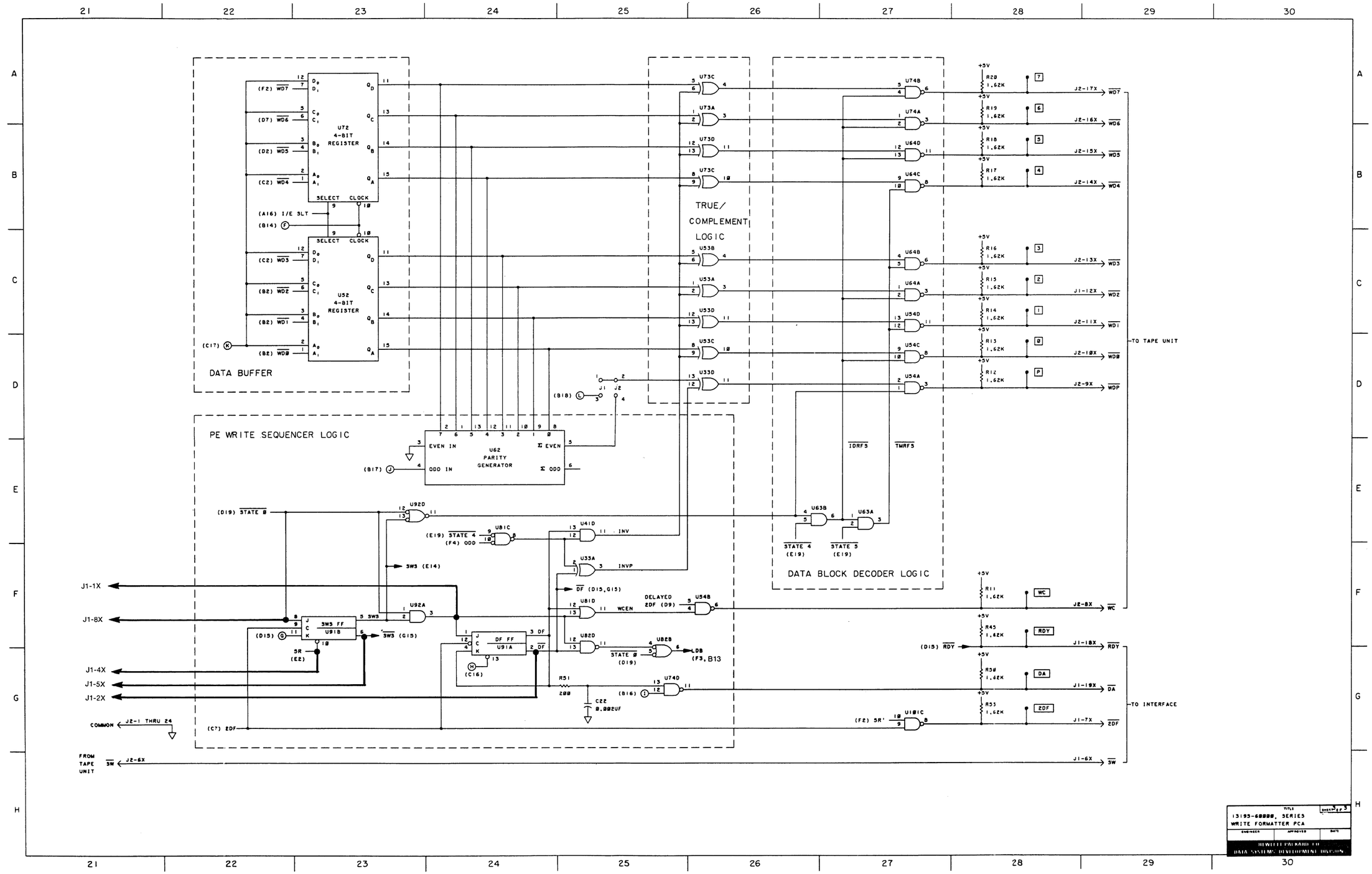


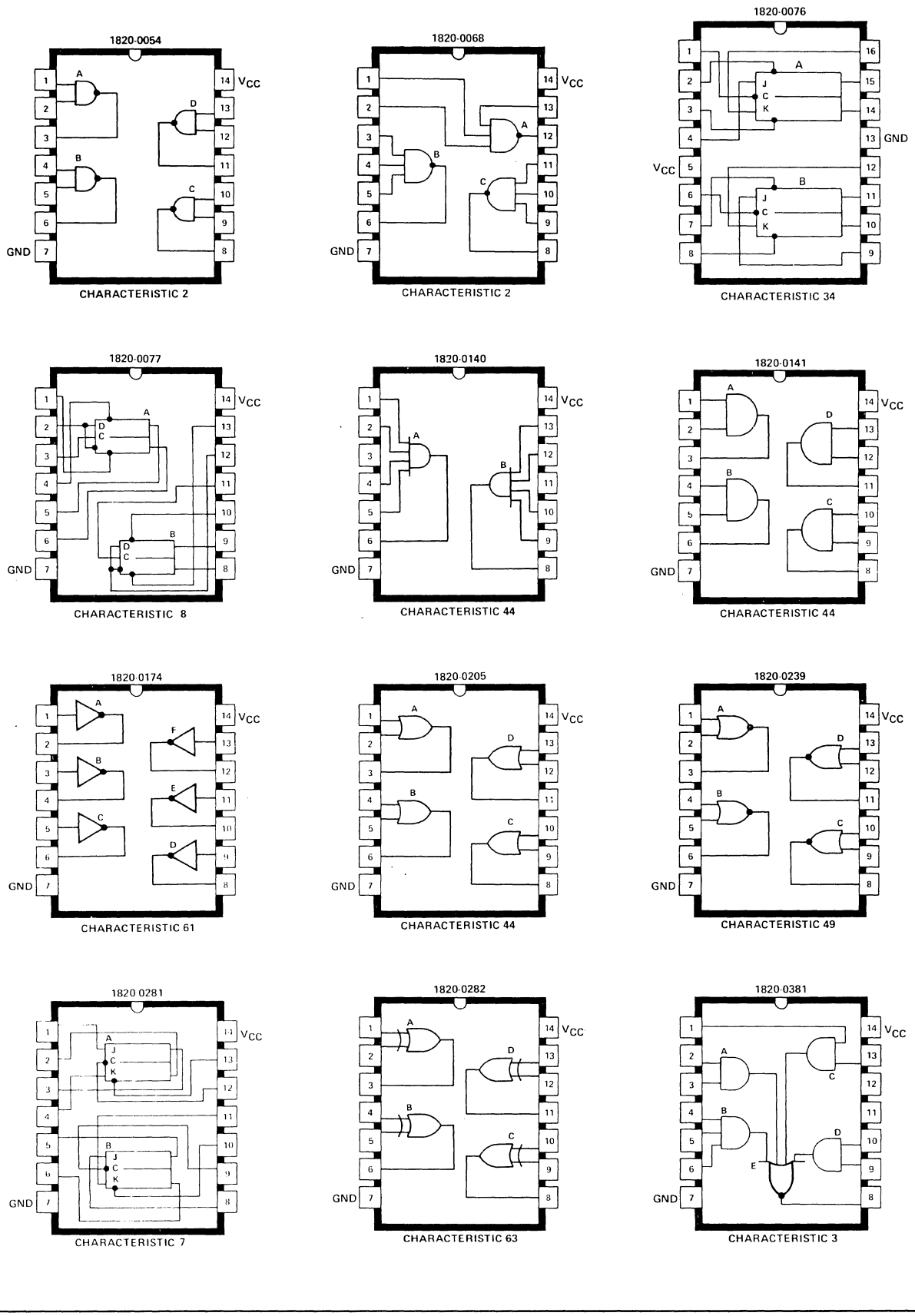
Figure 4-1. Write Formatter Schematic and Parts Location Diagram (Sheet 3 of 3)

Table 4-2. Write Formatter Replaceable Parts

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.	TQ
C1	CAPACITOR, fxd, mica, 220 pF, 5%, 300 Vdcw	0160-0134	1
C2	CAPACITOR, fxd, cer, 0.01 uF, +80 -2%, 100 Vdcw	0160-2055	2
C3	CAPACITOR, fxd, cer, 0.01 uF, +80 -2%, 100 Vdcw	0160-2055	
C4	CAPACITOR, fxd, mica, 360 pF	0160-2209	1
C5	CAPACITOR, fxd, elect, Ta, 100 uF, 10 Vdcw	0180-2207	1
C6-20	CAPACITOR, fxd, cer, 0.01 uF, +80 -2%, 100 Vdcw	0160-2055	15
C21	CAPACITOR, fxd, elect 4.7 uF, 10%, 35 Vdcw	0180-0100	1
C22	CAPACITOR, fxd, cer, 0.002 uF	0160-3457	1
C23	CAPACITOR, fxd, cer, 430 pF, 5%, 300 Vdcw	0160-0939	1
CR1-8	DIODE, Si, 30 ma, 30 wv	1901-0040	8
J1	POWER CONNECTOR, multi-contact	1251-2512	1
R1	RESISTOR, fxd, comp, 330 ohms, 5%, 1/4W	0683-3315	2
R2	RESISTOR, fxd, comp, 330 ohms, 5%, 1/4W	0683-3315	
R3	RESISTOR, fxd, metal flm, 19.6k, 1%, 1/8W	0698-3157	1
R4	RESISTOR, fxd, comp, 47k, 5%, 1/4W	0683-4735	1
R5	RESISTOR, fxd, comp, 10k, 5%, 1/4W	0683-1035	1
R6	RESISTOR, fxd, flm, 1k, 5%, 1/4W	0683-1025	4
R7	RESISTOR, fxd, flm, 1k, 5%, 1/4W	0683-1025	
R8	RESISTOR, fxd, flm, 1k, 5%, 1/4W	0683-1025	
R9	RESISTOR, fxd, flm, 1k, 5%, 1/4W	0683-1025	
R10	RESISTOR, fxd, comp, 4.7k, 5%, 1/4W	0683-4725	1
R11-21	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	11
R22,24,26,28,30, 32,34,36,38	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	9
R39	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
R40	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	1
R41	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
R42	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	1
R43	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
R44	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	1
R45	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	2
R46	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	
R47	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	1
R48	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
R49	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	0683-6215	1
R50	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
R51	RESISTOR, fxd, comp, 196 ohms, 5%, 1/4W	0698-3440	1
R52	RESISTOR, fxd, metal flm, 19.6k, 1%, 1/8W	0698-3157	1
R53	RESISTOR, fxd, metal flm, 1.62k, 1%, 1/8W	0757-0428	1
U12	IC, decade counter w/asynchro clear, TTL	1820-0899	1
U14	IC, dual re-trig one shot with re-set, TTL	1820-0515	1
U21	IC, hex inverter, TTL	1820-0174	1
U22	IC, decade counter, synchro, presettable, TTL	1820-0705	1
U23	JUMPER ASSEMBLY	7970-62120	1
U24	IC, dual J-K m-s flip-flop w/sep clk inputs, TTL	1820-0281	1
U32	IC, decade up/dn counter, synchro, 20 MHzin, TTL	1820-0734	1
U33	IC, quad 2-input exclusive or gate, TTL	1820-0282	1
U34	IC, decade counter, synchro, presettable, TTL	1820-0705	1
U41	IC, quad 2-input and gate, TTL	1820-0141	1
U42	IC, dual D flip-flop, TTL	1820-0077	1
U43	IC, dual J-K flip-flop w/preset and clock, TTL	1820-0076	1
U44	IC, decade counter, synchro, presettable, TTL	1820-0705	1
U52	IC, lp 2-input 4-bit multiplexer, TTL	1820-0656	1
U53	IC, lp quad 2-input exclusive or gate, TTL	1820-0598	1
U54	IC, quad 2-input nand buffer, open collector, TTL	1820-0621	1
U61	IC, dual 4-input and buffer, TTL	1820-0140	1
U62	IC, 8-bit odd/even parity generator/checker, TTL	1820-0435	1
U63	IC, quad 2-input and gate, TTL	1820-0141	1
U64	IC, quad 2-input nand buffer, open collector, TTL	1820-0621	1
U72	IC, lp 2-input 4-bit multiplexer, TTL	1820-0656	1
U73	IC, lp quad 2-input exclusive or gate, TTL	1820-0598	1
U74	IC, quad 2-input nand buffer, open collector, TTL	1820-0621	1

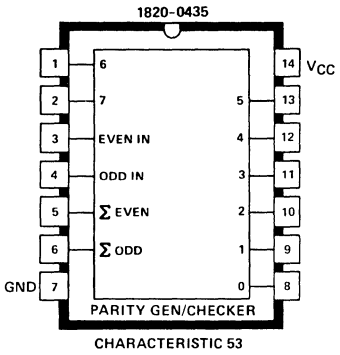
Table 4-2. Write Formatter Replaceable Parts (Continued)

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.	TQ
U81	IC, quad 2-input or gate, TTL	1820-0205	1
U82	IC, quad 2-input nand gate, TTL	1820-0054	1
U83	IC, hex inverter, TTL	1820-0174	1
U84	IC, quad 2-input nand gate, TTL	1820-0054	1
U91	IC, dual J-K m-s flip-flop w/sep clk inputs, TTL	1820-0281	1
U92	IC, quad 2-input and gate, TTL	1820-0141	1
U93	IC, quad 2-input nor gate, TTL	1820-0239	1
U94	IC, triple 3-input nand gate, TTL	1820-0068	1
U101	IC, quad 2-input nand buffer, open collector, TTL	1820-0621	1
U102	IC, hs 4-wide 2-2-2-3-input and-or inverter gate, TTL	1820-0381	1
U103	IC, dual J-K m-s flip-flop w/sep clk inputs, TTL	1820-0281	1
U104	IC, 1-of-8 decoder, TTL	1820-0608	1
U112	IC, quad 2-input nand gate, TTL	1820-0054	2
U113	IC, quad 2-input nand gate, TTL	1820-0054	
U114	IC, dual J-K m-s flip-flop w/sep clk inputs, TTL	1820-0281	1
W1	CABLE ASSEMBLY, power	13195-60001	1
Y1	XTAL-quartz, 7.2 MHz .005%	0410-0449	1



2266-12

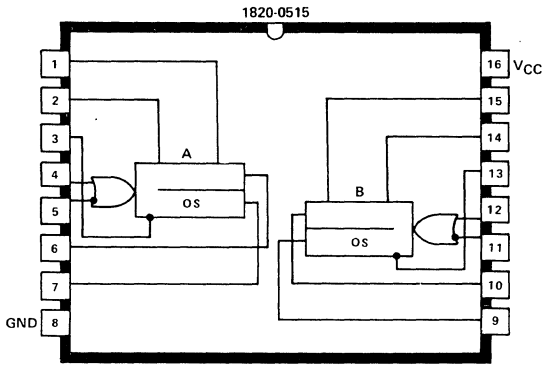
Figure 4-2. Integrated Circuit Pack Diagrams (Sheet 1 of 3)



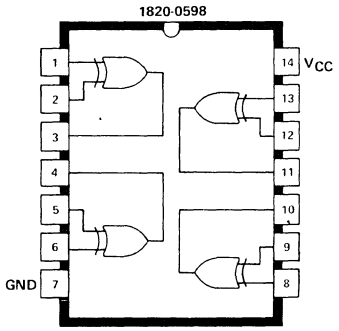
CHARACTERISTIC 53

0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
—	1	1	0	0
—	0	0	1	1

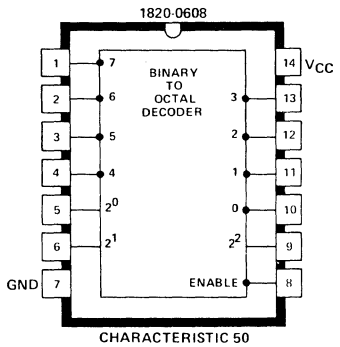
The eight data lines are tested to determine whether the true bits are even or odd. The EVEN and ODD inputs are interpreted as parity from another parity checker. (Note: the EVEN and ODD lines may also be interpreted as the expected parity.) The SUM EVEN and SUM ODD outputs are the combined parity of the two sets of data. Refer to the table above. If the parity check mode is used the output of the SUM ODD line will indicate a parity error.



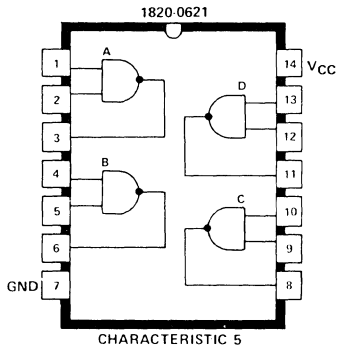
CHARACTERISTIC 72



CHARACTERISTIC 12



CHARACTERISTIC 50

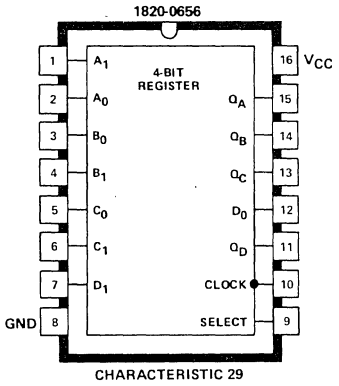


CHARACTERISTIC 5

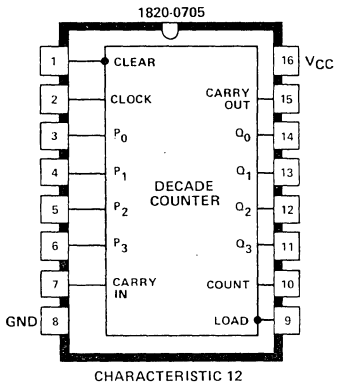
Binary data is decoded to octal when the ENABLE input is low. For a given input, only one output line will be low.

2266-13

Figure 4-2. Integrated Circuit Pack Diagrams (Sheet 2 of 3)

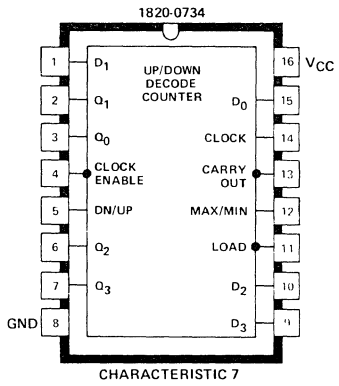


One of two four-bit data words (A_0 through D_0 or A_1 through D_1) is transferred to output lines Q_A through Q_D on the negative-going edge of the CLOCK pulse. The SELECT line determines which data word is transferred to the output lines. When the SELECT line is low, data word A_0 through D_0 is transferred to the output lines. When the SELECT line is high, data word A_1 through D_1 is transferred to the output lines.

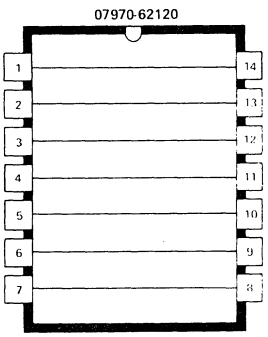


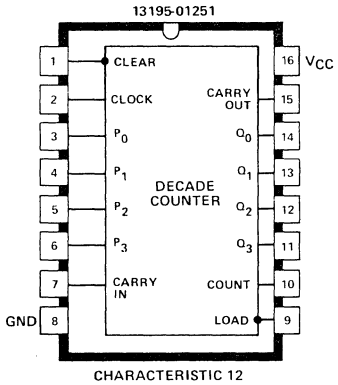
When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

The CARRY OUT line will be high if the output lines Q_0-Q_3 equal nine (1001) and the CARRY IN line is high. The counter will be set to 0000 when the CLOCK line goes low.



The counter is clocked by a low to high transition of the CLOCK line. The clock is effective only if the CLOCK ENABLE line is low. The CLOCK ENABLE line may only be changed while the CLOCK line is high. The direction of count is determined by the DN/UP line. If the DN/UP line is low the count is up. If the line is high the count is down. The counter may be preset with a low signal on the LOAD line. This will cause the data present on the input lines (D_0-D_3) to be stored. A low output signal is generated on the CARRY line if either a carry or borrow condition occurs. The MAX/MIN line outputs a high signal when the above conditions occur, but for a full clock cycle. This signal is used in "look-ahead carry" applications.





(See 1820-0705)

2266-14

Figure 4-2. Integrated Circuit Pack Diagrams (Sheet 3 of 3)

REPLACEABLE PARTS

SECTION V

5-1. INTRODUCTION.

5-2. This section contains information pertaining to replaceable parts for the HP 13195A Write Formatter Accessory Kit. Included are replaceable parts lists and ordering information.

5-3. REPLACEABLE PARTS LISTS.

5-4. Table 5-1 lists the replaceable parts for the write formatter. It lists the parts in numerical order by part number and the total quantity of each part is specified. Table 5-1 gives the following information for each part.

a. Hewlett-Packard part number.

b. Description of the part. (Refer to table 5-2 for an explanation of abbreviations used in the DESCRIPTION column.)

c. Manufacturer of the part, as a five digit code. Refer to table 5-3 for a listing of the manufacturers that correspond to the codes.

d. Manufacturer's part number.

e. Total quantity of parts.

5-5. ORDERING INFORMATION.

5-6. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Model number of the accessory kit.

b. HP part number for each part.

c. Description of each part.

d. Circuit reference designation, if applicable, for each part. (Refer to table 4-2 for reference designations.)

Table 5-1. Write Formatter Accessory Kit, Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0134	CAPACITOR, fxd, mica, 220 pF, 5%, 300 Vdcw	14655	RDM1SF221J3C	1
0160-0939	CAPACITOR, fxd, cer, 430 pF, 5%, 300 Vdcw	72136	OBD	1
0160-2055	CAPACITOR, fxd, cer, 0.01 uF, +80 -20%, 100 Vdcw	28480	0160-2055	17
0160-2209	CAPACITOR, fxd, mica, 360 pF	72136	OBD	1
0160-3457	CAPACITOR, fxd, cer, 0.002 uF	56289	C067F251F202K522-CDH	1
0180-0100	CAPACITOR, fxd, elect, 4.7 uF, 10%, 35 Vdcw	56289	150D475X9035B2-DYS	1
0180-2207	CAPACITOR, fxd, elect, ta, 100 uF, 10 Vdcw	56289	150D107X9010R2-DYS	1
0410-0449	XTAL-QUARTZ, 7.2 MHz .005%	00809	OBD	1
0683-1025	RESISTOR, fxd, flm, 1K, 5%, 1/4W	01121	CB1025	4
0683-1035	RESISTOR, fxd, comp, 10K, 5%, 1/4W	01121	CB1035	1
0683-3315	RESISTOR, fxd, comp, 330 ohms, 5%, 1/4W	01121	CB3315	2
0683-4725	RESISTOR, fxd, comp, 4.7K, 5%, 1/4W	01121	CB4725	1
0683-4735	RESISTOR, fxd, comp, 47K, 5%, 1/4W	01121	CB4735	1
0683-6215	RESISTOR, fxd, comp, 620 ohms, 5%, 1/4W	01121	CB6215	14
0698-3157	RESISTOR, fxd, metal flm, 19.6K, 1%, 1/8W	30983	MF4C,TO	2
0698-3440	RESISTOR, fxd, comp, 196 ohms, 5%, 1/4W	30983	MF4C,TO	1
0757-0428	RESISTOR, fxd, metal flm, 1.62K, 1%, 1/8W	30983	MF4C,TO	19
1820-0054	IC, quad 2-input nand gate, TTL	01295	SN7400N	4
1820-0068	IC, triple 3-input nand gate, TTL	56289	USN7410A	1
1820-0076	IC, dual J-K flip-flop w/preset and clock, TTL	01295	SN4355	1
1820-0077	IC, dual D flip-flop, TTL	01295	SN7474N	1
1820-0140	IC, dual 4-input and buffer, TTL	04713	SC7513PK	1
1820-0141	IC, quad 2-input and gate, TTL	04713	MC3001P	3
1820-0174	IC, hex inverter, TTL	01295	SN7404N	2
1820-0205	IC, quad 2-input or gate, TTL	04713	MC3003P	1
1820-0239	IC, quad 2-input nor gate, TTL	04713	MC3002P	1
1820-0281	IC, dual J-K M-S flip-flop w/sep clk inputs, TTL	01295	SN13618	4
1820-0282	IC, quad 2-input exclusive or gate, TTL	01295	SN13603	1
1820-0381	IC, hs 4-wide 2-2-2-3-input and-or invert gate, TTL	01295	SN4489	1
1820-0435	IC, 8-bit odd/even parity generator/checker, TTL	01295	SN14656	1
1820-0515	IC, dual re-trig one shot with re-set, TTL	07263	U6B960259X	1
1820-0598	IC, lp quad 2-input exclusive or gate, TTL	27014	DM74L86N	2
1820-0608	IC, 1-of-8 decoder, TTL	04713	MC4006P	1
1820-0621	IC, quad 2-input nand buffer, open collector, TTL	01295	SN7438N	4
1820-0656	IC, lp 2-input 4-bit multiplexer, TTL	01295	SN74L98N	2
1820-0705	IC, decade counter, synchro, presettable, TTL	07263	U7B931059X	3
1820-0734	IC, decade up/dn counter, synchro, 20 MHzin, TTL	01295	SN74190N	1
1820-0899	IC, decade counter w/asynchro clear, TTL	01295	SN74160N	1
1901-0040	DIODE, Si, 30 ma, 30 WV	07263	FDG1088	8
7970-62120	JUMPER ASSEMBLY	28480	07970-62120	1
13195-60001	CABLE ASSY, pwr	28480	13195-60001	1

Table 5-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or integrated circuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= jumper wire
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
Ag	= silver			phh	= phillips head
Al	= aluminum	H	= henries	pk	= peak
ar	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	prv	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
b	= base	hex	= hexagon, hexagonal	pwv	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rms	= root-mean-square
Be Cu	= beryllium copper	insul	= insulation, insulated	rwv	= reverse working voltage
		impgrg	= impregnated	rect	= rectifier
cpi	= characters per inch	incand	= incandescent	r/min	= revolutions per minute
coll	= collector	ips	= inches per second	RTL	= resistor-transistor logic
cw	= clockwise				
ccw	= counterclockwise	k	= kilo (10^3), kilohm	s	= second
cer	= ceramic			SB, TT	= slow blow
com	= common	lp	= low pass	Se	= selenium
crt	= cathode-ray tube			Si	= silicon
CTL	= complementary-transistor logic	m	= milli (10^{-3})	scr	= silicon controlled rectifier
		M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
Cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous		
		met. ox.	= metal oxide		
dc	= direct current	mintr	= miniature		
dr	= drive			Ta	= tantalum
DTL	= diode-transistor logic	n	= nano (10^{-9})	td	= time delay
depc	= deposited carbon	nc	= normally closed or no connection	Ti	= titanium
dpdt	= double-pole, double-throw			tgl	= toggle
dpst	= double-pole, single-throw	Ne	= neon	thd	= thread
		no.	= number	tol	= tolerance
em	= emitter	n.o.	= normally open	TTL	= transistor transistor logic
ECL	= emitter-coupled logic	np	= nickel plated		
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	U(μ)	= micro (10^{-6})
elctlt	= electrolytic				
		NSR	= not separately replaceable	V	= volt(s)
F	= farads	NRFR	= not recommended for field replacement	var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head			Vdcw	= direct current working volts
flm	= film	OD	= outside diameter		
fxd	= fixed	OBD	= order by description	W	= watts
filh	= fillister head	orn	= orange	ww	= wirewound
		ovh	= oval head	wht	= white
G	= giga (10^9)	oxd	= oxide	WIV	= working inverse voltage
Ge	= germanium				
gl	= glass	p	= pico (10^{-12})	yel	= yellow
gnd	= ground(ed)	PC	= printed circuit		

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wis.
01295	Texas Instruments Inc., Semiconductor Components Division	Dallas, Texas
04713	Motorola Semiconductor Products Inc.	Phoenix, Arizona
07263	Fairchild Camera & Inst. Corp., Semiconductor Div.	Mountain View, Cal.
12040	National Semiconductor Corp.	Danbury, Conn.
19701	Electra Manufacturing Co.	Mineral Wells, Texas
28480	Hewlett-Packard Co.	Palo Alto, Cal.
56289	Sprague Electric Co.	N. Adams, Mass.

HEWLETT PACKARD

13195A

WRITE FORMATTER ACCESSORY KIT

OPERATING AND SERVICE MANUAL

UPDATING SUPPLEMENT

23 OCT 1975

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

Manual Printed: August 1973

Manual Part No.: 13195-90000

Microfiche Part No.: 13195-90002

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to equipment containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left. For any given instrument serial number prefix, all change steps noted for prior serial number prefixes must be incorporated in addition to those for the given prefix.

INSTRUMENT CHANGES

Serial No. Prefix	Change
All (Errata)	4 thru 6

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Series	Changes
	Write Formatter PCA	13195-60000	1415	1 thru 3
	Write Formatter PCA	13195-60000	1536	1 thru 3

Changes 1 through 6 dated 7 March 1974.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221

Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

Printed in U.S.A.

CHANGE	DESCRIPTION
1	Title page, Add 1415 to the series code effectivity for PCA 13195-60000.
2	Pages 4-3/4-4, 4-5/4-6, 4-7/4-8, figure 4-1. In the parts location and schematic diagrams, change the series code from 1326 to 1415.
3	Pages 4-3/4-4, 4-5/4-6, 4-7/4-8, figure 4-1. Make the following changes in the schematic diagram. a. Sheet 1 of 3, System Clock circuit; add a test point labeled "OSC" at U21C pin 5. b. Sheet 1 of 3, System Clock circuit; change the destination zone for index "B" at U22 pin 11 from C13 to D13. c. Sheet 1 of 3, System Clock circuit; at Clock Program Connector J23 indicate a connection from pin 25 to pin 12 to an index letter "N" with zone destination (D14). Also show a connection from the pin immediately to the right of pin 25 to an index letter "M" with zone destination (D14). d. Sheet 2 of 3, Sequence Control logic; indicate a connection from U41B pin 5 to connector J1 pin 3X. e. Sheet 2 of 3, Sequence Control logic; delete the destination and signal information presently at U61B pin 9 (zone D5, index letter "B", 720 kHz) and show U61B pin 9 going to the "LDB" signal at zone (G26). Correct the remaining input pin numbers on U61B to read 10, 13, 12. Delete the trace from U61A pin 6 to U61B pins 10, 13, 12. Add a trace from U61B pins 10, 13, 12 to an index letter "M" going to zone (A8). Add a trace from U61A pin 6 to an index letter "N" going to zone (A8). Delete the zone and signal information (zone G26, LDB) presently at U61A pin 1 and show U61A pin 1 with index letter "B" going to zone (D5), signal 720 kHz. f. Sheet 3 of 3, PE Write Sequencer logic; add the following traces: FROM — TO U91B pin 8 — J1 pin 8X U91A pin 1 — J1 pin 1X U91B pin 10 — J1 pin 4X U91B pin 6 — J1 pin 5X U91A pin 2 — J1 pin 2X g. Sheet 3 of 3, PE Write Sequencer logic; at U82B pin 6 (the LDB signal) change destination indicator (C13) to (B13).
4	Page 4-9, table 4-2. Correct Reference Designation R22-38 to read; R22, 24, 26, 28, 30, 32, 34, 36 and 38.
5	Page 4-10, table 4-2. HP part number for W1 cable assembly should be 13195-60001.
6	Page 5-2, table 5-1. Delete the entry for part number 1251-2512. Change part number 13195-01251 to read 13195-60001 in the HP PART NO. and MFR PART NO. columns.

13195-90000
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