Honeywell DPS 90 Series

MANAGEMENT SUMMARY

Honeywell Information Systems remains a serious contender within the high-end mainframe world with the March 1985 announcement of the new top-end DPS 90 Series. The announcement came just one month after the annoucement of IBM's new top-of-the-line processor family, the 3090. From a technology standpoint, the DPS 90 is competitive with the 3090 and the several other 3090-class systems introduced earlier this year. The new Honeywell line consists of five processors models: the single-processor DPS 90/91; the dual-processor DPS 90/92; the three-processor DPS 90/93; the four-processor DPS 90/94; and the DPS 90/92T, a fully-redundant version of the DPS 90/92. The new series features the new 256K-bit memory chips, current mode logic chips, integrated vector-processing capabilities, and high-capacity main memories. DPS 90 memory capacity ranges from 32 to 256 megabytes. The 256-megabyte maximum capacity now exceeds the 128 memory capacity available with the DPS 88 line.

The new series is designed to handle high-volume workloads in commercial, interactive, and engineering/scientific environments. Besides addressing the large-computer capacity needs of big *Fortune 500* and government customers, the built-in vector capabilities of the DPS 90 Series allow these same customers access to a number cruncher without having to purchase a much more expensive supercomputer. Honeywell shipped the first models during the spring of this year. Volume shipments will begin by the first quarter of 1986. The DPS 90 Series offers more memory capacity and delivers up to three times the processor performance of Honeywell's previously most powerful computer series, the DPS 88. DPS 90 models are designed to serve at the center of communications networks that could typically involve other Honeywell systems ranging from the DPS 6 to the DPS 88 Series.

Like the other newly announced processor lines in its class, (IBM 3090, Burroughs A 15, NAS Alliance Series), the

The new (Distributed Processing System) DPS 90, now the most powerful processor series in the Honeywell lineup, was developed through a joint agreement between Honeywell and NEC Corporation of Japan, and is largely based on NEC S-1000 processor technology. The DPS 90 can be the host processor in a vast computer network, and is well-suited for batch, interactive, transaction processing, and some engineering/scientific applications.

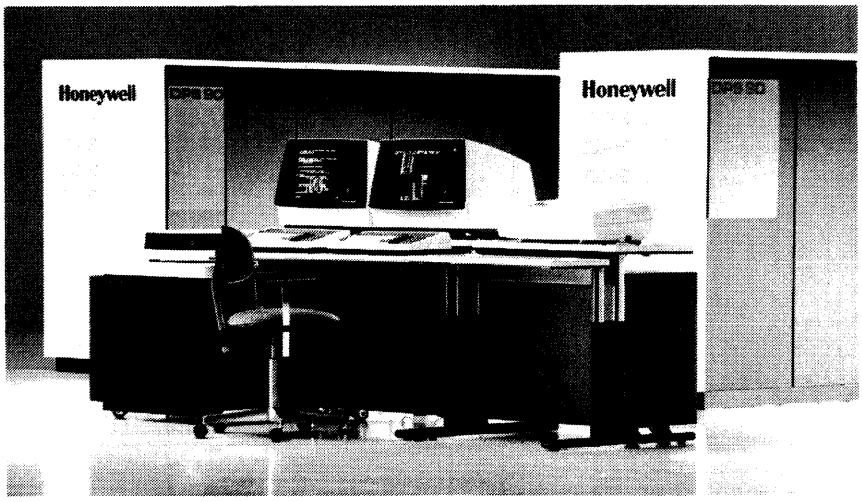
MODELS: The five models in the series consist of the single-processor DPS 90/91, the dual-processor DPS 90/92, the three-processor DPS 90/93, the four-processor DPS 90/94, and the DPS 90/92T, a fully-redundant version of the DPS 90/92.
CONFIGURATION: 1 to 4 CPUs, 32 to 256 megabytes of main memory, 1 to 4 input/output processors, and 16 to 64 channels.
COMPETITION: IBM 3090 Series, NAS AS/XL Series, Control Data Cyber 180, Burroughs A-15.
PRICING: Base purchase prices range from $3,950,000 for a DPS 90/91 to $8,350,000 for a DPS 90/94.

CHARACTERISTICS

MANUFACTURER: Honeywell Information Systems, 200 Smith Street, Waltham, MA 02154. Telephone (617) 895-6000. In Canada: 155 Gordon Baker Road, Willowdale, Ontario M2H 3N7. Telephone (416) 499-6111.

MODELS: Honeywell DPS 90 single-processor 90/91, dual-processor 90/92, fully-redundant 90/92T, three-processor 90/93, and four-processor 90/94.

DATE ANNOUNCED: See Table 1.



Honeywell's new top-of-the-line DPS 90 mainframe family includes one-, two-, three-, and four-processor models, plus a fully-redundant dual system. The top-end DPS 90/94 can be configured with up to 256 megabytes of main memory and delivers three times the processing power of the DPS 88, Honeywell's previous top-end series.

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DPS 90 Series is designed to meet the needs of organizations with workloads growing at a rate of 20 to 50 percent annually. The DPS 90 Series is positioned to provide a growth path for Honeywell large-system users who have outgrown the capabilities of Honeywell's DPS 8 and DPS 88 product line. The DPS 90/91 single-processor mainframe is said to deliver 30 to 70 percent greater performance than the single-processor DPS 88/81, depending on work load and application, while the top-end DPS 90/94 four-processor model provides up to 3.4 times the power of the DPS 90/91.

Besides addressing the growth needs of its customers, Honeywell also wanted to protect its considerable investments. To accomplish this, Honeywell modified the NEC S-1000-based processor that the DPS 90 is based on to make it compatible with the GCOS 8 operating system, with other Honeywell peripherals, and with its communications system. Honeywell systems operating under GCOS 8 can readily migrate to the DPS 90.

The DPS 90 Series represents something of a new direction for Honeywell. The processors are the product of agreements and collaborative efforts with other vendors outside the Honeywell organization. Honeywell and NEC Corporation of Japan entered into a cross-licensing agreement last year to develop a processor series based largely on NEC S-1000 technology. The new MSU3380 disk units offered with the processors were obtained from IBM under the terms of a third-party OEM agreement worked out in 1984.

The peripheral equipment introduced along with the new series includes a new mass storage subsystem, magnetic tape processors, and enhanced high-speed belt printers. As already alluded to, the mass storage subsystem incorporates the IBM-based MSU3380 head-of-string mass storage unit. The MSU3380 consists of two string controllers, two Head Disk Assemblies, and four actuators. The disk unit provides up to 1.8 gigabytes of formatted capacity, which exceeds the 1.1-gigabyte capacity of the MSU0501, Honeywell's previous maximum-capacity disk unit.

The new processor line operates under an enhanced version of GCOS 8, and is software compatible with the DPS 8 and DPS 88 Series. This makes it possible for DPS 8 or DPS 88 users to upgrade to the more powerful processors without major difficulties. DPS 8 users, in fact, can upgrade directly to the DPS 90 Series should their capacity requirements exceed the capabilities of the DPS 88. All the DPS 90 processors, except for the top-end DPS 90/94, are also field upgradable to progressively more powerful processors within the series.

COMPETITIVE POSITION

The DPS 90 specifically focuses on two markets: interactive processing, an established Honeywell market niche, and engineering/scientific processing, a new Honeywell market. Honeywell has strongly addressed the interactive processing market throughout its large system line with strong emphasis on fault-tolerant capabilities, high availability, and high throughput. The DPS 90 is no exception in

DATE OF FIRST DELIVERY: See Table 1.

DATA FORMATS

BASIC UNIT: 9-bit bytes organized functionally to process 36-bit word groupings of information. Special features are also included for ease in manipulating 4-bit groups, 6-bit groups, 9-bit groups, and 18-bit groups, 72-bit double-precision groups, and 144-bit quadruple-precision, floating-point groups.

FIXED-POINT OPERANDS: Binary fixed-point numbers are represented with 18-bit half word, 36-bit single word, and 72-bit double-precision operands.

Decimal numbers used directly in hardware arithmetic commands are expressed as decimal digits in either the four-bit or nine-bit character format. They are expressed as unsigned numbers or as signed numbers using a separate sign character.

Alphanumeric data is represented by nine-bit, six-bit, or four-bit characters. A machine word contains either four, six, or eight characters, respectively.

FLOATING-POINT OPERANDS: There are two floating-point formats—binary and hexadecimal. Binary floating-point numbers are represented with 36-bit single-word and 72-bit double-word precision. In both operands, 0 represents the sign of the exponent, bits 1 to 7 the exponent, and bit 8 the sign of the fraction. The rest of the operand starting with bit 9 represents the rest of the fraction. Quadruple-precision floating point operands, introduced with the DPS 90 Series, automatically use a hexadecimal exponent. The reason for two floating-point formats is to expand the exponent range of the floating-point operand.

INSTRUCTIONS: All basic instructions use one 36-bit word. The processor performs operations using 6-, 9-, 18-, 36-, and 72-bit operands. All single-word instructions use bits 0 through 17 for the address field, bits 18 through 27 for the op code, bit 28 as the interrupt inhibit bit, bit 29 as the address register bit, and bits 30 through 35 as the instruction address modifier. Multiword instructions use bits 0 through 17 for various functions as required, bits 18 through 27 as the op code, bit 28 as the interrupt inhibit bit, and bits 29 through 36 as the operand descriptor 1 modification field. Words 2, 3, and 4 contain the operand descriptor or indirect pointer for operands 1, 2, and 3, respectively.

INSTRUCTION REPERTOIRE: The DPS 90 processor models have a comprehensive instruction set for performing data movement, binary arithmetic, shifting, logic, and control operations. The instruction set includes arithmetic facilities for performing variable-length fixed- and floating-point decimal arithmetic, and bit and byte string manipulation for processing bytes, BCD characters, packed decimal data, and bit strings. Additional instructions introduced with the DPS 90 include general instructions for fixed- and floating-point random number operations, vector instructions for fixed-, floating-point, and, logical operations on vectors with up to 256K elements each, and finally, a set of register-to-register instructions.

The basic instruction set of the DPS 90 contains more than 400 instructions, exceeding the instruction complement of the DPS 8 which is more than 300 instructions.

INTERNAL CODE: 9-bit ASCII code is standard.

MAIN STORAGE

STORAGE TYPE: 256K-bit metallic oxide semiconductor (MOS) chips.

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TABLE 1. SYSTEM COMPARISON

MODEL	DPS 90/91	DPS 90/92	DPS 90/92T	DPS 90/93	DPS 90/94
SYSTEM CHARACTERISTICS					
Date announced	March 1985	March 1985	March 1985	March 1985	March 1985
Date first delivered	June 1985	April 1985	—	—	—
Field upgradable to	DPS 90/92	DPS 90/92T	DPS 90/93	DPS 90/94	—
Relative performance	—	—	—	—	—
Number of processors	1	2	2	3	4
Cycle time, nanoseconds	—	—	—	—	—
Word size, bits	36	36	36	36	36
Operating systems	GCOS 8	GCOS 8	GCOS 8	GCOS 8	GCOS 8
MAIN MEMORY					
Type	256K-bit MOS	256K-bit MOS	256K-bit MOS	256K-bit MOS	256K-bit MOS
Minimum capacity, bytes	32MB	32MB	64MB	64MB	64MB
Maximum capacity, bytes	128MB	128MB	256MB	256MB	256MB
Increment size	32MB	32MB	32MB	32MB	32MB
Cycle time, nanoseconds	—	—	—	—	—
BUFFER STORAGE					
Minimum capacity	128KB	128KB	128KB	128KB	128KB
Maximum capacity	128KB	128KB	128KB	128KB	128KB
Increment size	—	—	—	—	—
INPUT/OUTPUT CONTROL					
Number of channels:					
Byte multiplexer	—	—	—	—	—
Block multiplexer	—	—	—	—	—
Word	—	—	—	—	—
Other	16-32	16-32	16-64	16-64	16-64

these respects. Most of the processors come with some degree of built-in redundancy to minimize downtime, while the DPS 90/92T comes as a fully-redundant system featuring two of each major system component. Honeywell believes its interactive processing and fault-tolerant capabilities give its large system products a clear edge over comparable IBM systems. By Honeywell estimations, the DPS 90 is superior to the new IBM 3090 Series in interactive processing and at least competitive to IBM in commercial batch processing capabilities.

The built-in vector processing capabilities for engineering and scientific work places the DPS 90 in direct competition with CDC Cyber 180 and Digital's VAX systems. Other vendors now finding this market exploitable include IBM and NAS, which have both built number crunching capabilities into their respective systems, the IBM 3090 and the NAS Alliance Series.

The DPS 90 contains most of the current state-of-the-art features to keep Honeywell in the same advanced technology league with IBM and the other vendors responding to the IBM announcements. Other vendors launching new high-end product lines include NAS with its AS/XL Alliance Series and Burroughs with its A 15 Series. All the new processor products are featuring high-capacity main memories and the new 256K-bit memory chips, except for IBM, which is using higher density 288K-bit chips. All the new high-end processor lines offer main memories of up to 256 megabytes, except for the Burroughs A 15 system which goes up to 192 megabytes.

Of all the remaining high-end mainframe vendors tailoring big systems to equally big *Fortune 500* customers, IBM continues to be the vendor Honeywell needs to outgun. Whether the DPS 90 is indeed superior to the IBM 3090 in interactive processing environments, as Honeywell claims, is difficult to accurately gauge, since the vendor does not

CAPACITY: See Table 1.

CYCLE TIME: Honeywell does not release information about machine cycle times.

CHECKING: An 8-bit error-correcting Hamming code is appended to each 72-bit word pair. Single-bit errors are corrected automatically, and multiple-bit errors are detected and flagged for subsequent error recovery routines. Odd parity is utilized throughout the processor.

STORAGE PROTECTION: The DPS 90 has read, write, and execute permission bits in the Segment Descriptor. Within the DPS 90 Series additional segment descriptors are implemented to describe very large data segments essential for vector operations. The Page Table Word (PTW) contains a write permit bit. Hardware also checks that data addresses generated during program execution do not exceed specified boundaries.

CENTRAL PROCESSORS

The DPS 90 central system includes the following modular components:

- **Central Processing Unit (CPU)**
- **Main Memory Unit (MMU)**
- **System Control Unit (SCU)**
- **Input/Output Processor (IOP)**
- **Power Sequencer (PSQ)**
- **System Control Center (SCC)**
- **Interface Adapter Unit (IAU)**

The DPS 90 Series, composed of modular processing components, makes use of a pipeline-type processing architecture, some parallel processing techniques, cache memory, and a high-speed address translation mechanism to enhance system throughput. In addition, the central processing system comes with built-in vector processing capabilities for engineering/scientific applications. The system supports

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disclose standard performance measurements such as MIPS and processor cycle time. Honeywell and other mainframe vendors have been backing away from such handy benchmarks in recent years, claiming variations in system architectures and applications make MIPS and cycle time comparisons between competing processors misleading.

It is possible to make some comparisons between Honeywell and IBM based on price and main memory size. A basic IBM 3090 Model 200 with a minimum of 64 megabytes of memory sells for approximately $5 million, roughly equal to the cost of the Honeywell two-processor DPS 90/92 which comes minimally configured with 32 megabytes of memory. Adding an additional 32 megabytes of memory to the DPS 90/92 to make it equal the basic 64 megabytes of the Model 200 brings the price to $5,400,000. The top-end IBM Model 400, a four-way processor minimally configured with 128 megabytes of main memory, costs roughly $9,100,185, while the top-end Honeywell DPS 90/94, also a four-processor system that comes minimally configured with 64 megabytes, sells for $8,350,000. When configured with 128 megabytes to equal the Model 400 main memory, the price comes to $9,150,000.

Aside from price/performance factors, Honeywell may have one small competitive edge over IBM. Honeywell processors are scheduled to be delivered more than a year before IBM said it could deliver its top-end processor, the 3090 Model 400, which features up to 256 megabytes of shared expanded storage. Of course, whether IBM keeps to that delivery schedule or delivers the Model 400 sooner remains to be seen.

ADVANTAGES AND RESTRICTIONS

In many ways, the DPS 90 looks like a souped-up version of the DPS 88. Both processor lines use a pipeline-processing architecture, a technique that makes it possible to simultaneously process five CPU instructions in various stages of execution for enhanced throughput. Both systems also make use of current mode logic, a computer logic said to be similar to the emitter-coupled logic now used on such competing systems as the IBM 3090. These new logic chips achieve faster switching speeds and consume less power.

Major differences between the DPS 88 and DPS 90 center around memory capacity, throughput enhancement techniques, and scientific processing capabilities. The differences between the DPS 88, a fairly new processor family announced only three years ago, and the new DPS 90 line announced earlier this year, give testimony to the rate at which computer technology continues to advance. The DPS 90 uses the new 256K-bit MOS chips and can be configured with 256 megabytes of memory rather than the 128 maximum memory on the DPS 88 Series. DPS 90 main memory units also make use of eight-way interlacing that helps speed up memory accesses and increase throughput. The DPS 88 processors use four-way interlacing.

Another major DPS 90 feature is vector processing. The processor line uses 63 new vector instructions that can be vectorized processing on multiple data arrays of up to four gigabytes.

On the circuitry level, the processors make extensive use of Current Mode Logic (CML) logic chips and 256K-bit MOS memory chips. CML circuitry is used in the CPU, SCU, MMU, IOP, and high-speed channel processors. CML achieves faster switching speeds at a lower power consumption. It uses a higher density of logic gates per chip than transistor-to-transistor logic. Multichip carriers, called micropackages, incorporate a large number of densely packed large-scale integrated chips in one air-cooled assembly. The micropackage ceramic substrate has high-dissipation heat sinks and makes use of forced-air cooling.

The Central Processing Unit (CPU) executes instructions from both application and system programs. The unit contains five elements: A memory buffer unit; a prefetch unit and pipeline control; control store unit; execution unit, and diagnostic control unit. Functions include the decoding of instructions from the main memory unit, executing arithmetic, logic and vector operations, and processing interrupts.

The memory buffer unit contains a 64K-byte operand cache and a 64K-byte instruction cache for a total of 128K bytes. Each cache is organized in 16-word blocks with set associative mapping. To maintain a high cache hit ratio, the buffer uses a least-recently-used algorithm. The high-speed address translator uses the buffer to convert virtual addresses to real addresses. The address translation buffer contains two sets of 256 conversion pairs for the instruction cache and two sets of 256 conversion pairs for the operand cache. This retains virtual to real address translations and minimizes page table accesses. Virtual-to-real translations and cache accesses are executed in parallel to boost system speed. Eight-byte transfers from memory can move in parallel.

The Prefetch Unit and Pipeline Control implement the pipeline processing mechanism. The unit can process five instructions in various stages of execution simultaneously. Processed instructions moving through the pipeline may be in a decode cycle, address development cycle, page cycle, cache access cycle, execute cycle, or write cycle. Each stage is executed in one machine cycle. The prefetch unit, using the pipeline control mechanism, transfers an instruction read request to the memory buffer unit and decodes it. It also transfers operand read requests to the memory buffer. Additionally, the unit presents prefetched instructions and data to the execution unit and processes branch instructions.

The Control Store Unit controls the execution of the remainder of the pipeline, while also maintaining the integrity of all control stores, using error checking and correction.

The Execution Unit contains program registers and four arithmetic units. These include a basic arithmetic unit, a floating-point arithmetic unit, a high-speed multiplier, and a variable-length arithmetic unit. To reduce execution time, some frequently used instructions may be processed in parallel with preceding instructions. Furthermore, various arithmetic units can be used in parallel, providing an overlapped instruction sequence.

The Diagnostic Control Unit supports a number of operational, maintenance, and diagnostic functions. The unit controls CPU status logout, testing and diagnostics, display functions through keyboard operations of the system control center, and the reporting of scan-path testing.

MAIN MEMORY UNIT: The MMU uses metal oxide semiconductor (MOS) 256K-bit chips. A single MMU can be configured to contain 32 to 128 megabytes of main memory. Larger systems configured with two MMUs can contain up to 256 megabytes of main memory. To enhance throughput, the MMU employs eight-way interlacing.

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invoked using Fortran programs adapted to vector processing. This built-in, high-speed arithmetic ability is ideal for users whose occasional number crunching needs are not enough to justify the purchase of an expensive supercomputer. Honeywell believes organizations using CAD/CAM applications and engineering simulation could find the engineering/scientific capabilities beneficial.

Besides scientific work, Honeywell continues to offer a product that could appeal to the transaction processing market. The firm offers a fully-redundant DPS 90/92T and builds redundancy features into its other processors to insure system availability.

Like most competing vendors trying to protect their customer base, Honeywell has made it possible for existing Honeywell customers to migrate from the DPS 8 and DPS 88 to the DPS 90 without having to make major changes to operating system and applications software. Most peripherals used on previous Honeywell systems are also compatible with the DPS 90.

A peripheral product Honeywell has recently made available to its customers is the MSU3380 disk unit/controller and the MSU3382 slave disk unit, which were obtained from IBM under an OEM agreement. Both units can hold 1.8 gigabytes of information and achieve a transfer rate of three megabytes per second. Previously, Honeywell's highest capacity unit was the MSU0501, featuring 1.1 gigabytes of capacity and a transfer rate of 1065K bytes per second. Although the new IBM-based units offer users more capacity per unit, they still fall far short of the new high-capacity units offered from IBM and NAS. Both the IBM 3380 DASD Model AE4 and the NAS 7380-AE have capacities of 5.04 gigabytes. □

MMU uses Error Checking and Correction logic for single-bit error correction and double-bit error detection. Should part of the MMU fail, the affected part is released by the IOP Maintenance System Operating Supervisor program to insure operating system continuity.

SYSTEM CONTROL UNIT: The System Control Unit (SCU), packaged with the MMU, handles data, commands and interrupt traffic among the various central components, and provides system availability, maintenance, and diagnostic functions. A System Interface Unit, contained in the SCU, carries out the main functions of the SCU. The interface unit accepts requests and assigns data paths according to priorities and the configurations maintained by the configuration management unit. The SCU has interfaces for two CPUs, two IOPs and two MMUs, and has a direct connection to the service processor contained in the SCC from the SCU Diagnostic Control Unit.

SYSTEM CONTROL CENTER: The System Control Center (SCC) controls the entire DPS 90 system, simplifies system interaction, monitors activities under the control of the operating system, initializes the system, and provides an interface to maintenance and diagnostic functions for Honeywell maintenance contract customers. The SCC consists of a control unit, an operator panel, an operator display with keyboard, a status display with keyboard, two diskette drives, a fixed disk, an activity monitor, a timer feature, a serial printer, and a service processor. Built-in redundancy features ensure system availability.

INTERFACE ADAPTER UNIT: The Interface Adapter Unit (IAU) contains two backpanels which each support four general-purpose adapters. The adapters permit attachment of peripheral equipment complying with Federal Information Processing Standards. With additional backpanels, the IAU may be configured with up to 16 general-purpose adapters.

POWER SEQUENCER: The Power Sequencer (PSU), packaged in a separate cabinet, is a required component that controls the power sequencing of central system units for either a motor-generator or an uninterruptible power system. The PSQ provides single-switch, power-on/power-off control for all central system components through the System Control Center.

I/O PROCESSOR: The Input/Output Processor (IOP) handles data transfers between peripheral equipment and the MMU. Each IOP has four high-speed channel processors (HCPs) that each, in turn, support four physical channels. In total, a maximum of 16 channels per IOP can be configured. In systems using a maximum of four IOPs up to 64 channels can be configured. The four HCP high-speed I/O channel ports can achieve transfer rates of up to 3 megabytes per second. Channel types supported include high- and low-speed Peripheral Subsystem Interface channels, Direct Interface channels, and Data Streaming channels. All peripherals, except for System Control Centers, are connected through the HCPs. System Control Centers connect to a separate multiplexer.

The Input/Output Processor (IOP), itself a computer, has a one-megabyte local memory containing peripheral control and maintenance system software. The IOP, connected to the system control unit, performs system start-up, initiates system reconfiguration, handles errors, and controls system test and diagnosis. Software residing in the IOP, the IOP Maintenance and Peripheral Supervisor, has two distinct parts. These are the IOP Software and the Maintenance System Operating Supervisor. IOP Software (IOPSOS) processes connects and interrupts, dispatch to other IOP software modules, logical-to-physical channel mapping, report status. Maintenance System Operating Supervisor, (MSOS), the other software component, handles system initialization and bootloading, maintenance chores, and error logging.

PROCESSOR MODES: The central processor has six modes of operation: master mode, privileged master mode, slave mode, hypermode, nonextended segment mode, and extended segment mode. The first three modes are standard, while hypermode is actually part of the privileged master mode, and extended and nonextended segment modes are superimposed on the basic processor modes. The privileged master mode permits unrestricted access to all memory, permits the initiation of data transfer operations through the Input/Output Transfer Unit, and the setting of control registers. Master mode allows access to certain authorized portions of memory, while the slave mode is utilized by the operating system, when appropriate, and for execution of all user programs. These modes provide operating control and security in a multiprogramming environment. Hypermode is used to share CPU resources when diagnosing the health of the system. Hypermode allows direct access to reserved memory through a special base register. Extended segment mode is setable during a CLIMB instruction. In this mode, new four-gigabyte data segments are allowed, the index and address registers are expanded to 36 bits, and the 21 new register-to-register instructions are enabled. Since registers are larger, the Safe Store Stack is expanded and instructions which load or store the registers operate differently to accommodate the expanded number of bits. It should be noted, however, that GCOS 8 operating system currently limits the address space of a program to a working space of 64 megabytes.

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TABLE 2. MASS STORAGE

MODEL	MSU0451	MUS0500	MSU0501	MSU3380	MSU3382
Cabinets per subsystem	16	8-15	8-15	8	8
Disk packs/HDAs per cabinet	1	2	2	2	2
Capacity	156MB	626MB	1.1GB	1.8GB	1.8GB
Tracks/segments per drive unit	815	1630 per surface	1686 per surface	13,275	13,275
Average seek time, msec.	30	25	25	16	16
Average access time, msec.	38.3	33.3	33.3	24.3	24.3
Average rotational delay, msec.	8.3	8.3	8.3	8.3	8.3
Data transfer rate	716KB/sec.	1065KB/sec.	1065KB/sec.	3MB/sec.	3MB/sec.
Controller model	MSP8021/8022/ 8023	MSP8021/8022/ 8023	MSP8021/8022/ 8023	MSP3881/3885	MSP3881/3885
Comments	Removable	Fixed	Fixed	Fixed HDAs	Fixed HDAs

PHYSICAL SPECIFICATIONS: DPS 90 systems must be located on a raised floor providing at least 12 inches of space beneath the equipment. The room ceiling must be eight feet above the raised floor. Power requirements must meet the following specifications: Central System components require 208 VAC, +12 VAC, −28 VAC nominal; 3 phase at 50 or 60 Hz ±1 percent. A neutral is not needed. Peripherals require 208Y/120 V, ±10 percent; 60 Hz, or 380Y/220 V, +10 percent/−15 percent; 50 Hz, five wire which includes ground with a maximum phase variation of ±0.5 Hz maximum variation. Harmonic content is 6 percent or less of nominal frequency. Maximum phase variation is six degrees from 120 V nominal.

A design temperature between 68 and 78 degrees Fahrenheit with a relative humidity between 40 and 60 percent noncondensing is an acceptable range.

CONFIGURATION RULES

The five models operate under an enhanced version of GCOS 8, and are based on NEC Corporation large systems technology.

The DPS 90/91 single processor consists of one Central Processing Unit (CPU), two Input/Output Processors (IOP), with four high-speed channel processors each, one Main Memory Unit with 32 megabytes of main memory, one System Control Unit (SCU), one Power Supply Unit (PSU), one System Control Center with serial printer, and one Interface Adapter Unit (IAU). Options include an additional IOP and up to 96 megabytes of additional memory in 32-megabyte increments.

The DPS 90/92 dual-processor system consists of two CPUs, one IOP with four high-speed channel processors each, one MMU with 32 megabytes of main memory, one SCU, one PSU, one SCC with serial printer, and one IAU. Options include an additional IOP and up to 96 megabytes of additional memory in 32-megabyte increments.

The DPS 90/92T tandem processor system consists of two of each central system component. The fully-redundant version may be operated either as a single system or as two separate systems. Options include one or two additional IOPs and up to 224 megabytes of additional memory in 32-megabyte increments.

The DPS 90/93 three-processor system consists of three CPUs, three IOPs with four high-speed channel processors each, two MMUs with 32 megabytes of memory each, two SCUs, two PSUs, two SCCs with serial printer, and two IAUs. Options include an additional IOP and up to 224 megabytes of additional memory in 32-megabyte increments.

The DPS 90/94 four-processor system consists of four CPUs, four IOPs with four high-speed channel processors each, two MMUs with 32 megabytes of memory each, two SCUs, two PSUs, two SCCs, and two IAUs. Options include up to 224 megabytes of additional memory in 32-megabyte increments.

PERIPHERALS

Peripherals that can be connected to the DPS 90 include network processors, terminals, peripheral processors, disk and tape units, card readers and punches, and on-line and off-line printers. Disk, tape, and unit record devices are attached to various peripheral processors that control the transfer of information between the device and the Input/Output Processor. The various peripheral processor families are described below.

MASS STORAGE

The MSP3880 Series includes two mass storage processors which comply with the Federal Information Processor Standards, the MSP3881 and the MSP3885. The processors and the MSU3380/3882 mass storage units are purchased on an OEM basis from IBM.

The MSP3881 includes two storage directors and two IAU attachment channels. The MSP3885 includes two storage directors and four IAU attachment channels. The storage directors attach to the controller in the head-of-string mass storage units. The IAUs, in turn, attach to channels in the Input/Output Processor on the central system.

The MSP8021/22/23 mass storage processors are designed to work with the MSU0451, 0500, and 0501 mass storage units. To make more efficient use of floor space, the processor series lets users configure selectable combinations of the MSP8021 storage processor line and the MTP8021 magnetic tape line in single compact cabinets. The MSP8021 freestanding single-channel processor supports up to 16 MSU spindles. The MSP8022 secondary single-channel processor supports up to 16 MSU spindles. The MSP8023 primary single-channel processor also supports up to 16 MSU spindles, and is used when an MTP8021 magnetic tape processor is already installed. All the MSPs can be field upgraded with optional dual-channel capabilities to provide redundancy and greater simultaneous access to mass storage units. MSPs can be configured with up to 16 removable-disk MSUs, eight fixed-disk MSUs, or else a mixed combination of removable and fixed-disk units.

Disk storage units available for the DPS 90 are listed in Table 2.

INPUT/OUTPUT UNITS

The MTP8021/22/23 are designed to work with the MTU0500, 0610, and 0630 magnetic tape drives. As described above, the magnetic tape processors can be housed in selectable combinations with the new MSPs to make more efficient use of floor space. The tape processors provide

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TABLE 3. INPUT/OUTPUT UNITS

Magnetic Tape Units	Number of Tracks	Recording Density, Bits/Inch	Encoding	Tape Speed Inches/Sec.	Transfer Rate, Bytes/Sec.
MTU0500	7	556/800	NRZI	125	52K/75K
MTU0500	9	556/800/1600	NRZI/NRZI/PE	125	70K/100K/200K
MTU0610	9	800/1600/6250	NRZI/PE/GCR	200	100K/200K/1250K
MTU0630	9	800/1600/6250	NRZI/PE/GCR	75 or 125	60-100K/120-200K/468.7-7781.2K
Printers	**Printing Speed**	**Print Positions**	**Horizontal Spacing, Chars./Inch**	**Vertical Spacing, Lines/Inch**	**Form Size, Inches**
PRU0908	900 lpm	136	10	6 or 8	4 in. to 19 in. width x 3 in. to 11 in. length
PRU1208	1200 lpm	136	10	6 or 8	4 in. to 19 in. width x 3 in. to 11 in. length
PRU1600	1325 lpm	136 or 160	10	6 or 8	4 in. to 22 in. width to 3 in. to 220 in. length

control for a string of tape units and connect to the bidirectional input/output data transfer paths of central systems.

The MTP8021 is a freestanding primary single channel tape processor that includes 1600/6250 bpi capability and the first MTU addressing feature. It can support up to eight tape units.

The MTP8022 secondary single-channel processor also includes 1600/6250 bpi capability and the first MTU addressing feature. The processor can support up to eight tape units.

The MTP8023 primary single-channel processor includes 1600/6250 bpi capability and the first MTU addressing feature. The MTP8023 is used when an MSP8021 is already installed. It can support up to eight tape units. Tape processors can be field upgraded with optional dual channel capabilities to provide system redundancy and greater access to tape units. A single-channel tape processor can support up to eight tape units in a single-channel subsystem. The dual channel option provides two separate channels in a tape processor, allowing the two channels to be interconnected. Both could support up to 16 tape units in dual simultaneous channel configuration.

UNIT RECORD SUBSYSTEM: The URP0600 or URP8901 Unit Record Processors can control up to eight unit record devices simultaneously. Unit record devices include card readers, a card punch that handles 100 to 400 cards per minute, a card reader/punch unit that reads at 400 cards per minute and punches at 100 cards per minute, and on-line, high-speed printers.

Magnetic tape subsystems and printers available for the DPS 90 are listed in Table 3.

TERMINALS: Terminals available for the DPS 90 are listed in Table 4. Card equipment is described in the price list.

COMMUNICATIONS CONTROL

The DPS 90 Series uses Datanet 8 and Datanet 666X network processors to carry large-volume communications loads, allowing central processors to concentrate on information processing. Datanet 8 operates under Distributive Network Supervisor software. Datanet 666X can operate under either General Remote Terminal Supervisor-II (GRTS-II) or the Network Processing Supervisor (NPS).

DATANET 6661 FRONT-END NETWORK PROCESSOR (FNP): This processor provides large-volume network communications capabilities for DPS 90 systems. The Datanet 6661 incorporates an independently programmable computer with an instruction repertoire of 98 single-address instructions. The CPU in the Datanet 6661 is a solidstate, interrupt-driven 18-bit unit operating asynchronously under firmware control. The DCU6661 comes standard with 64K bytes of memory and is expandable to 512K bytes. The DCP6661 has two performance enhancement packages rated at 47 and 82 percent. Multiple FNPs can be configured.

A high-speed cache memory is optional in the DCU6661, which provides an execution rate of up to 1,000,000 instructions per second given the appropriate configuration and optimum instruction mix.

The FNP input/output multiplexer (IOM) performs all operations required for the transfer of data between I/O devices and the FNP memory. A data transfer rate of up to 2,000,000 bytes per second is possible. The IOM is connected to the I/O bus, to which various devices are attached. These units are the System Support Controller for the console and network processor diskette; the Direct Interface Adapter, which connects to the host; and the Peripheral Interface Adapter (optional) for access to the host's mass storage processor, when required. The remaining I/O connections are for the Channel Interface Bases, through which the network devices enter the system.

The Channel Interface Base (CIB) provides the line interfacing arrangements necessary to accommodate terminals with various data transfer rates, bit orders, bits per character, information codes, character sets, message formats, and communications control procedures. Terminals in the low-, medium-, and high-speed ranges can be supported, with a maximum of 72,000 bps possible. In addition, synchronous, bisynchronous, and asynchronous transmissions and any combination of half- and full-duplex modes are supported. Each Channel Interface Base can handle up to eight communications lines, in various configurations. The DCU6661 can accommodate up to 12 CIBs.

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TABLE 4. TERMINALS

MODEL	VIP 7814	VIP 7815-7817 and 7824-7827	VIP 7823/7831	VIP 7201	VIP 7301/ 7303/7307	VIP 7305
DISPLAY PARAMETERS						
Max. chars./screen	2000	2000	2000	1920	2000	2000
Screen size (lines x chars.)	24 x 80	24 x 80	24 x 80	24 x 80	25 x 80	25 x 80
Symbol formation	7 x 9 dot matrix	7 x 8 upper/ 7 x 9 lower	7 x 8 dot matrix/ 7 x 9 lower	7 x 11 dot matrix	7 x 9 dot matrix	7 x 8 upper/ 7 x 9 lower
Character phosphor	P31 green std.	P31 green	P31 green	P31 green std.	P31 green std.	P31 green std.
Total colors/no. simult. displayed	—	—	—	—	—	—
KEYBOARD PARAMETERS						
Style	Typewriter	Typewriter	Typewriter	Typewriter	Typewriter	Typewriter
Character/code set	128 ASCII	128 ASCII	128 ASCII	128 ASCII	128 ASCII	128 ASCII
Detachable	Std.	Std.	Std.	Std.	Std.	Std.
Program function keys	12 std.	12 std.	12 dual std.	7 std.	12 std.	12 dual std.
OTHER FEATURES						
Buffer capacity	3 pages	3 pages	3 pages	1 page	1 page	1 page
Tilt/swivel	Tilt opt.	Tilt opt.	Tilt opt.	Tilt opt.	No	Tilt opt.
Graphics capability	—	Std.	Std.	—	—	Std.
TERMINAL INTERFACE	RS-232-C	RS-232-C or RS-442A	RS-232-C or RS-422A	RS-232-C or RS-442A	RS-232-C, RS-422A, 20 ma, or MIL-188-C	RS-232-C or RS-422

DATANET 8 FRONT-END NETWORK PROCESSOR (FNP): This system is designed for use in communication networks conforming to the Distributed Systems Architecture (DSA) and operates under the control of the Distributed Network Supervisor (DNS) and GCOS 8. The Datanet 8 (DCU8010) is not compatible with the Datanet 6661, but can coexist with it on the same system. A maximum of four DPS 90 host connections can be configured enabling the Datanet 8 to be shared by four DPS 88 host systems.

The base Datanet 8 includes 512K bytes of memory (expandable to 1536K) and a 512K-byte diskette (a second 512K diskette is optional). It can accommodate from 16 to 128 communication lines. The DPS 90 Host connection (DCE8018) and the 100-cps Console (DCF8001) are required additions.

The Datanet 8 can be configured with 2, 8, or 16 DCF8007 Channel Interface Bases (CIB) depending on the line configuration. Each CIB supports up to four channel interfaces, each of which in turn supports either one or two communication lines, depending on the specific type of Channel Interface chosen. The following options are available on Datanet 8 systems and can be field-installed:

- **Dual Asynchronous Channel Package, EIA RS-422-C, to 9600 bps each (DCF8009)**
- **Dual Bisynchronous Channel Package, EIA RS-232-C, to 9600 bps (DCF8018)**
- **Dual Asynchronous Channel Package, MIL-188-C, to 9600 bps (DCF8015)**
- **Single Synchronous Channel Package, MIL-188-C, to 9600 bps (DCF8014)**
- **Single Synchronous HDLC Channel Package, MIL-188-C, to 9600 bps (DCF8017)**
- **Single Synchronous HDLC Wideband Channel Package, MIL-188-C, to 56K bps (DCF8016)**
- **Channel Interface Base (DCF8007); accommodates up to four Channel Interface Options**
- **Dual Synchronous EIA RS-232-C Channel, to 9600 bps (DCF8011)**
- **Dual Asynchronous EIA RS-232-C Channel, to 9600 bps (DCH8012)**
- **Single HDLC EIA RS-232-C Channel, to 9600 bps (DCF8020)**
- **Single HDLC Wideband Channel, to 56K bps (DCF8022)**
- **Single HDLC Wideband Channel, CCITT-V.25, to 56K bps (DCF8023)**
- **Direct Connect Capability (DCF8024) for one Asynchronous or one Synchronous Line, to 9600 bps**
- **Universal Modem By-Pass (DCF8026), Synchronous to 20.8K bps or Asynchronous to 1800 bps**
- **Two Asynchronous Current Loop Ports, to 9600 bps (DCF8036)**

SOFTWARE

The Honeywell GCOS 8 (General Comprehensive Operating Supervisor 8) is the only operating system available on the DPS 90 processor line. GCOS 8 is a multidimensional operating system common to all large-scale Honeywell systems from the DPS 8 processor family, to the DPS 88 family and, of course, now available on the DPS 90. Under the latest release of GCOS 8, Release 2500, substantial changes were implemented that permits the DPS 90 Series to accommodate the Input/Output Processor (IOP) and other DPS 90 hardware characteristics. The operating system will dynamically adjust to the hardware configuration it serves. A single copy of the operating system is developed and maintained.

Many of the significant operating system differences implemented with the DPS 90 involve reliability, availability and serviceability tools, and facilities that were incorporated into GCOS 8 software, the IOP's resident MSOS software, and in firmware. A major software feature unique to the DPS 90 is the integrated vector processing and the large program and date structures the system supports. These features are readily visible to the end user.

Introduced in 1979 with the DPS 8 systems, GCOS 8 is a product with a genesis dating back to the early 1960s. GCOS 8 is a multiprocessing, multiprogramming, communications-oriented operating system that supports distributed systems requirements. Honeywell's objective is to keep the operating system dynamic by a series of planned releases which capitalize on new technology while preserving the user's investment in software. Honeywell's direction for distributed systems is toward the eventual linking of an organization's entire complex of physically separate data processing systems into a single logical network system regardless of physical boundaries.

According to Honeywell, current GCOS users can upgrade to GCOS 8, and user programs (with few exceptions) that have been running under GCOS will run unchanged under GCOS 8.

GCOS 8 is user-defined and user-oriented, with multidimensional capabilities. It is a batch system, a time-sharing

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system, and a transaction processing system. GCOS 8 balances the use of system resources, and gives multiple options for customizing the system for each user's needs. GCOS 8 concurrently supports 1) batch processing, 2) remote job entry (RJE), 3) interactive remote job entry (IRJE), 4) time-sharing, 5) transaction processing, 6) direct program access, 7) on-line test and diagnostics, 8) on-line program test and development, and 9) electronic mail.

GCOS 8 is a flexible operating system that features hardware transparency, meaning that the user has no need to know the particular architecture of the system, its hardware, I/O devices, or processor types. All processors can access all of memory and can execute any program. GCOS 8 can address real memory up to memory-capacity limits. Up to 477 user programs of up to one megabyte each can be executed concurrently. GCOS 8 can use up to 128 megabytes of memory for time-sharing. It provides high throughput by efficient and rapid scheduling of all activities, which reduces operator intervention.

MEMORY MANAGEMENT: The system architecture with GCOS 8 provides dynamic memory management, descriptor-controlled access, and shared access (to both data and procedures). Each of these functions is based on a hardware-protected memory segment. The memory segment is defined by a segment descriptor that contains the logical address of the beginning of the segment, the size of the segment, and the permissions that control its use.

Dynamic memory management permits programmers to develop software as if there were an unlimited logical memory. The available physical memory, on the other hand, depends on the system configuration and the workload.

Real physical memory is limited to a maximum of 256 megabytes or 64,000 pages. Virtual memory can consume up to 8 gigabytes or 2 million 4K-byte pages divided into 512 work spaces. Out of the 512 spaces, up to 477 are available for user programs.

Any available page of main memory can be used for any page-sized block of logical memory. Although pages may be located anywhere in memory, they can be accessed as if they were physically contiguous. With memory access, segment descriptors and page table words translate the virtual address to a main memory address.

DIMENSIONS: GCOS 8 is a virtual operating system, with multiprogramming, multiprocessing, and flexible job entry capabilities. GCOS 8 also has file protection and file sharing, testing and diagnostics, communications, time-sharing, data management facilities, language processors, diagnostic and system protection facilities, and various system utilities. Batch, time-sharing, transaction processing, and other activities can be individually tailored and dynamically varied throughout the day. Peripherals are allocated before memory so that processing is not delayed by operator or mechanical delays.

SYSTEM SECURITY: GCOS 8 provides security of hardware and software in several ways. It will abort an activity if an illegal operation is received. The File Management Supervisor provides a common file system for all processor operating dimensions as well as protective and restorative functions to ensure file integrity. Access to files is controlled through several levels. Files are grouped in a hierarchical order by user name, access restrictions, and resource control. File names are qualified by comparing them to the user names under which they are cataloged. Passwords may be required as an additional form of user identification. Access to files is under the originator's discretion and control. Each user can have a multilevel hierarchical subcatalog structure, with the ability to assign access controls and passwords at each subcatalog level. Another safeguard is a hardware implementation that controls access to sets of memory segments called domains. This structure protects programs and files from intentional access by unauthorized personnel and unintentional access during debugging procedures.

NETWORKING AND COMMUNICATIONS SOFTWARE

DISTRIBUTED NETWORK SUPERVISOR (DNS): DNS has been designed specifically for use in the Datanet 8 Front-End Processor, and is part of a set of communication software products based on Honeywell's Distributed Systems Architecture (DSA). DNS supports up to four DPS 90 Host connections enabling one Datanet 8 to serve multiple hosts.

DNS operates in the Datanet 8 in conjunction with a DPS 90 host running the GCOS 8 or GCOS operating system to provide support for transaction processing, distributed transaction processing, distributed terminal concentration, time-sharing, remote job entry, direct program access, and networks made up of DPS 90s, DPS 88s, DPS 8s, DPS 7s, and DPS 6s in any combination. DNS supports private networks, Public Data Networks (PDNs), and Value Added Networks (VANs), including X.25 packet switched and X.21 circuit switched networks.

The administrative functions distributed throughout the various systems that make up the DSA network include network monitoring, cross-network software loading, dumping, data logging for statistics, billing and maintenance, in-line tests, and software generation.

DNS supports a variety of terminals such as the Honeywell TWU/PRU 1003, 1005, and 1901, VIP 7100/7200/7201/7700/7700R/7800 and VTS7710. Also supported is the DPS 6-DSA software package that allows a DPS 6 or Level 6 system to function as a distributed processor and to communicate with a DPS 90 host in a DSA network.

NETWORK PROCESSING SUPERVISOR: The DPS 90 and NPS support five types of remote processing in any combination: remote job entry (RJE), transaction processing, time-sharing, message switching, and direct program access. RJE is supported by four standard interfaces for remote computers: remote computer interface, remote network processor multimessage interface, BSC interface, and HDLC interface.

The information network is controlled by a combination of the Datanet 6600 Front-End Network Processor and the NPS software, and can range in size from several terminals to a comprehensive, distributed information network with multiple host processing facilities.

NPS supports a wide variety of remote terminals, computers, and communications facilities, such as the Honeywell TWU/PRU 1003 and 1005, Teletype Models 28/33/35/37/38, GE TermiNet 300/1200, Hazeltine 2000, IBM 2741 and 2780, and Honeywell VIP 765/776/786, VIP 7100/7200, VIP 7700/7700R/7760/7800, RNP 702/707, and RNP 6/DPS 6 minicomputers. NPS also provides customization and parameterization facilities to facilitate implementation of additional terminal types and network protocols into the system, journalization of message traffic on mass storage, restart/recovery capability, supervisory control through one or more Network Control Supervisory Stations, statistical recording and reporting, and a high level of line/terminal control through parameterization.

REMOTE TERMINAL SUPERVISOR-II (GRTS-II): Provides controls for five types of remote processing: remote job entry, transaction processing, time-sharing, message concentration, and direct program access. RJE supports the same standard interfaces as NPS. Programming subsystems

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supported under time-sharing are the same as for NPS. GRTS-II does not support the direct program access communications-queued (DAC-queued) mode provided in NPS, nor does it support any host interface which makes use of the DAC-queued method.

GRTS-II includes a Communication On-Line Test System (COLTS) and support for remote terminals and devices with speeds from 75 to 56,000 bps. GRTS-II may coexist with NPS or DNS, each residing and executing in a different network processor. Host-to-host file transmission is supported through the Data Link System.

TRANSACTION PROCESSING SYSTEM (TPS): This facility invokes the loading and execution of the appropriate application programs for processing transactions received from remote terminals. The Transaction Processing System requires a front-end network processor and can accept transactions from various terminals.

TPS is modular in design and consists of the Transaction Processing Executive (TPE), user-written Transaction Processing Applications Programs, the Transaction Input Interface at each remote terminal, and the Interslave Communication (INTERCOM) Facility. Transaction Processing Applications Programs (TPAPs) can be written in any language processor supported by GCOS 8 including Cobol, Fortran, or GMAP, and are stored in the GCOS file system for activation as required.

The Transaction Input Interface provides simplified procedures for entering transactions from either teletypewriter or keyboard/display consoles. The INTERCOM facility permits data to be exchanged between the Transaction Processing Executive and applications programs through direct buffer-to-buffer transfers. The Transaction Processing Executive operates as a privileged slave program under the GCOS 8 operating system and is activated by an operator command.

TRANSACTION DRIVEN SYSTEM (TDS): Designed for high-volume, on-line transaction processing, TDS differs substantially in internal architecture from the GCOS Transaction Processing System (TPS), but it complements TPS by giving a total DPS 90 transaction processing capability. The TDS internal design is optimized for high-volume transaction processing where extremely fast response and fast, automatic restart/recovery are required.

The TDS Executive program executes under GCOS 8 much like the Time-Sharing System Executive. It is an executive operating under GCOS 8 with the major responsibilities of scheduling and coordination of all TDS activities and tasks. TDS manages the allocation of system resources for transaction processing and handles all communications between TDS and GCOS 8.

TIME-SHARING: The DPS 90 Time-Sharing System (TSS), in connection with a Datanet front-end processor, provides time-sharing computing services to multiple users at remote terminals. The system resources allocated to time-sharing can be dynamically varied under operator control. The time-sharing executive, operating as a slave activity under GCOS 8, suballocates storage and dispatches the processor to the programs of individual time-sharing users. Time-sharing on GCOS 8 utilizes the GCOS 8 memory architecture to permit any desired amount of system memory to be allocated to time-sharing. A single copy of TSS can support up to 600 users, assuming enough memory, I/O, and communications facilities are provided. In multiple-processor systems, the time-sharing users' programs can simultaneously use as many processors as desired by the site. A separately priced Multicopy Support Option allows from two to four copies of the time-sharing executive to run on one DPS 90 system, thereby increasing the number of users that can be supported.

DPS 90 GCOS Time-sharing users have a choice of six major programming languages: Cobol-74, Extended Basic, Pascal, Time-Sharing Fortran-66, Fortran-77, and APL. Time-sharing users can communicate directly with batch-mode facilities, permitting the development and testing of programs, data entry, control of batch program execution, and manipulation of results from remote terminals.

The Text Editor permits terminal users to create a body of text, edit it, save it, and print it in a specified format. TEX is an interpretive language that integrates the capabilities of the Text Editor with text processing, providing additional verbs and subroutine calls. Interactive Integrated Data Store/II (I-D-S/II) provides the ability to interactively update and retrieve information from an I-D-S/II data base. Access is a conversational file management system for creating, deleting, and maintaining catalogs and files and for assigning passwords and accessing criteria. The FDUMP facility can be used for inspection and maintenance of permanent files. The LODT routine permits execution of experimental user subsystems, including trace analysis and debugging of user programs from remote terminals. The Time-Sharing Activity Report provides reports on the accumulated utilization of the time-sharing system resources. Personal Computing Facility is now available under time-sharing offering spreadsheet capability.

LANGUAGES

The language processors available for use on the DPS 90 systems under GCOS 8 are Cobol-74, Cobol-68, Fortran-66, Fortran-77, PL/1, GMAP, GPSS, Basic, data Basic, Simscript, Pascal, Compiler "B," Lisp, APL, and RPG II.

The Cobol-74 compiler provides the functional modules specified for ANS Cobol-74, including the Debug, Sort/Merge, and Report Writer facilities. All modules are implemented at the highest level (Level 2) defined in the ANSI X3.23-1974 standard.

Syntax Directed Editor (SDE) is a productivity tool designed to support the creation or modification of Cobol-74 programs. SDE reduces the amount of code that a programmer must enter and immediately checks for format and syntax errors.

System-80 is designed to reduce the time and effort of coding, maintenance, and documentation normally associated with Cobol program development. It includes several functional programs and associated files that interact with the user to acquire needed information about files, fields, screen formats, and validations and edits.

Softool is a set of software tools designed for cost-effective management, development, and maintenance of application software. The Softool Development Environment Product Set offered by Honeywell consists of the Cobol Programming Environment (Cobol-74) and the Change and Configuration Control.

Both Fortran-66 and Fortran-77 operate in the batch and time-sharing environments. Fortran-66 is a full implementation of Fortran IV and the 1966 ANSI standard with extensions. Fortran-77 complies with the 1978 ANSI standard and MIL-STD-1753 (Department of Defense supplement to 1978 ANSI standard), plus numerous extensions. Fortran-77 extensions include code optimization, a DO WHILE plus optional loop incrementation statement, full subscript range checking, passed argument type verification, DOUBLE precision COMPLEX data type and extrinsics, upper-, lowercase ASCII character intrinsics, graphics character set, the INCLUDE statement, binary/octal/hexadecimal constants, and bit processing and intrinsics. Other Fortran-77 extensions are pretty printer (reformatting of source code), upper-/lowercase source code, optional flagging of unde-

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cleared variables/called functions and subroutines/intrinsics, optional flagging of implicit type conversions, and subdivision of compile time error messages into seven categories. Interactive and batch symbolic debugging of source programs through the Debug Support System (DSS) is available to the Fortran-77 user. There is also a compatibility mode which allows compilation of Fortran-66 programs without source modification. Both Fortran-77 and Fortran-66 processors compile programs in local, remote job entry, or time-sharing environments and ensure compatibility between source programs developed in one environment and used in another. Executable programs that have been developed in one environment may be run in another. Data Manipulation Language (DML) verbs for accessing DM-IV and I-D-S/II data bases are available in the Fortran-77 and Fortran-66 processors.

PL/1 is a block-structured language that allows both internal and external names. This feature facilitates the development and maintenance of modular PL/1 programs. All procedures are recursive and sharable. PL/1 utilizes the full ASCII character set defined in American National Standards Institute standard X3.4-1968.

Basic is a one-pass conversational compiler that operates under the GCOS 8 Time-Sharing System. It implements the Basic language as defined by the ANSI minimal Basic standard plus several Honeywell extensions.

DataBasic is a version of Basic employing the I-D-S/I file management system. DataBasic is supported by both time-sharing and batch component subsystems.

APL Level II is a superset version of the APL programming language. APL is an interactive system for use with large-scale Honeywell computers.

The Pascal compiler runs under TSS and provides these extensions to standard Pascal: constant-valued expressions may be used wherever a constant is legal in Standard Pascal, and are evaluated at compile time; files may be opened dynamically; and extended file handling is available.

Lisp is an interpreter/compiler system designed to assist in the symbolic computations common to language translation, theorem proving, symbolic mathematics, and artificial intelligence. It is a compatible superset of Lisp 1.5.

Simscript provides the user with a simulation-oriented language that permits the translation of complex mathematical and logical models into meaningful simulation sequences. It is an event-oriented language with a timing routine that allows the analysis of activities in a controlled sequence in simulated time.

Compiler "B" is a high-level language which operates in the batch or time-sharing mode. It is used for systems programming and for teaching compiler programming and design.

"C" is a general-purpose programming language featuring economy of expression, modern control flow and data structures, strong data typing, and a set of language operators. Its lack of restrictions and its generality make it more convenient to use for many tasks, including realtime applications, than the more powerful languages. "C" is useful for writing operating systems and for writing numerical, text-processing, and data base programs.

RPG II is Honeywell's implementation of the IBM-developed report program generator, and is very similar to the IBM System/3 version of the language. RPG II supports UFAS sequential, relative, and indexed sequential files, all compatible with Cobol-74.

The General-Purpose Simulator System (GPSS) is a simplified, simulation-oriented language that establishes mathematical models in order to provide results for further analysis.

The General Macro Assembler Program (GMAP) enables the programmer to code either in an open-ended macro language or directly in machine-oriented symbolic instructions.

The Debug Support System (DSS) supports batch or on-line debugging of user programs, and can trace programs, display memory contents, and modify memory locations. Object-level debug can be performed with any language. Symbolic debug is supported by Cobol-74, Fortran-77, and PL/1.

DATA MANAGEMENT

Honeywell offers a number of software packages in this category, including Data Management-IV, File Management Supervisor, Indexed Sequential Processor, Unified File Access System, Integrated Data Store I and II, Management Data Query System, TOTAL Central, and Common Files Facility.

The latest Honeywell data management, transaction processing, query and reporting, batch and interactive data base capabilities are provided by Data Management-IV (DM-IV). DM-IV has evolved from earlier software systems such as Integrated Data Store-I, Transaction Processing System, Transaction Driven System and Management Query System. DM-IV is a fully operational on-line, integrated data base management system. Data extraction and updating from data bases with various file organizations and data structures can be directly performed by non-data processing professionals. DM-IV consists of the following functional modules: the Data Manager, the Transaction Processor, the Query and Reporting Processor, and the Procedural Language Processor. It also supports batch and time-sharing programs.

The DM-IV Data Manager administers the creation of the physical and logical structures of the data base and controls the creation of the application-specific views of that data base which are used in processing. It further serves as the interface between the data base and the various DM-IV processors that access the data base and perform operations upon it.

The DM-IV Transaction Processor (TP) provides the facility for rapid, efficient, on-line data base processing. It is most effectively used in applications where the end user has little or no knowledge of the operating system or storage structure, or data processing in general. Its internal design is optimized for high-volume transaction processing where extremely fast response and fast, automatic restart/recovery are required. The TP system includes both on-line software components for processing the actual transaction and a wide variety of support software products for program testing, library updating, and TP system generation. Within DM-IV/TP, there are five major functional components: Transaction Manager, Data Base Manager, Integrity Manager, Message Manager, and Executive Manager.

The Executive Manager schedules and coordinates all Transaction Processor activities. It manages the allocation of system resources for transaction processing.

The Transaction Manager controls and coordinates all activities during the processing of a transaction. It initiates each transaction control task which TP processes and controls the communication between application routines.

The Data Base Manager controls all data base activities for on-line files assigned to TP. The executive software also

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provides for dynamic allocation and deallocation of data base files to TP for uninterrupted continuous operation.

The Integrity Manager provides for fast, automatic recovery and restart after any type of application or system failure. This includes everything from rollback of the data base after an application program abort to the complete reconstruction of a destroyed data base.

The Message Manager is the executive software component that actually handles the communication interface with the terminal network supported by the Front-End Network Processor (FNP). The Message Manager provides both the physical and logical interface to the on-line network of terminals and handles the acceptance and delivery of input and output messages.

The DM-IV Query and Reporting Processor (QRP) provides the user with several different subsystems which act to access the defined data base and its structure and to generate reports on the results of the requested access. The DM-IV QRP end-user facilities provide access to the data base by noncomputer-oriented personnel. Within QRP, simple, straight-line procedures may be written to explicitly retrieve the desired data and process exception conditions such as no data qualifier and end of retrieval conditions. The optional DM-IV Procedural Language Processor (PLP) is an extension of QRP which provides a high-level, procedure-oriented language for use by application and system programmers. When using the QRP end-user facilities, the user need not be concerned with the data base structure or access methods.

The Personal Computing Facility (PCF) is a screen-oriented, interactive system that provides a user-friendly application environment. A person without knowledge of conventional computer programming can use PCF to create any type of VDU or CRT form as a basis for interactive problem solving.

Example Query (EQ) is an end-user facility consisting of an easy-to-learn language and support program. EQ aids application-oriented users in the queuing of data through the Relational Access Manager, which is included. User interface is through CRT devices (VIP7800), and alternatives to CRT display include printed output and file output. The interactive language facilities are designed for fast and simple formulation of requests which provide answers to application questions. The language has minimal syntax which is easily constructed into graphic representation of user processing requests.

Interactive Query (IQ) is an end-user facility that allows users to interface in nonforms mode with any type of terminal. Included with IQ is the Relational Access Manager, which allows interface to many standard file types.

The Comprehensive Report Examination/Display Option (CREDO) is an optional Personal Data Query (PDQ) facility that can format report data generated through the EQ and IQ facilities into refined, individualized reports. CREDO reports are defined, created, examined, and distributed according to user-specified or system-default options.

The Transaction Application Test System (TATS) is a software tool that provides an interactive time-sharing environment for writing, compiling, testing, and debugging Transaction Processing Routines (TPRs) using a DM-IV (IDS-II) data base. TATS also provides a TPR program skeleton generator, and forms mode support is currently provided for the DM-IV TP Forms Option (TPFO). The TATS package can also be used to interactively verify data base updates and to integrate completed TPRs into the production system.

The Transaction Screen Management System (TSM) is a set of tools designed to enhance the development of application programs in a DM-IV TP environment. This system enables the developer to design, develop, test, and implement screen formats for application systems. Little or no knowledge of the communications network or the DM-IV TP operating environment is required.

The File Management Supervisor (FMS) provides powerful file management capabilities, including multilevel user catalogs, file sharing, and access control. The system employs a hierarchical, "tree-structured" design. A System Master Catalog lists the various user Master Catalogs, and each user may in turn define one or more levels of subcatalogs. Users may permit general sharing of their files or specify individual users who may access them on either a read/write or read-only basis. Password access control can be imposed at any or all levels of the file structure. Security is also provided by the optional logging of file access attempts and by a time-sharing command allowing a user to encrypt his or her file using a predefined algorithm.

The Indexed-Sequential Processor (ISP) supports the widely used indexed-sequential file organization and access method, which permits mass storage files to be accessed in either random or sequential fashion. For each logical file, ISP maintains a data file and an independent key file, which serves as an index. The key file can be placed on a faster random-access device to speed up the access process.

The Data Dictionary/Directory System (DD/DS) is a comprehensive set of software modules that can implement a centralized data dictionary/directory. Data is entered into the dictionary data base via either batch or interactive operations. The DD/DS supports up to 19 entity-types such as fields, records, files, programs, procedures, jobs, schemas, reports, etc. Multiple versions and status of each entity-type, alias names, narrative, and attributes unique to the entity type are also supported.

Several report generation facilities are available to the DD/DS user. The reporting system extracts information from the date dictionary and presents it to the user in various formats. Included is an extensive cross-reference (where used) reporting capability for all entity-type occurrences and an Impact Analysis Report which analyzes and reports the effect of change to an entity-type occurrence. A complete set of utilities is provided to assist in the maintenance of the data dictionary system and its data base.

The Unified File Access System (UFAS) provides automatic management for file processing, including record location and automatic blocking and deblocking. File organizations supported include sequential, relative, indexed, and integrated files. UFAS also includes facilities for error checking and initiation of error processing as defined by ANSI Cobol-74, and file integrity protection for normal and abort processing.

The Integrated Data Store (I-D-S/I and I-D-S/II) systems are enhanced versions of I-D-S, a data base management system originally developed by GE. I-D-S/II is based on the CODASYL Data Base Facility specifications. I-D-S/II is fully integrated with Honeywell's Cobol-74 compiler, and user interfaces are also implemented for Fortran.

The Management Data Query System (MDQS) is a data management system that permits interrogation of sequential, indexed sequential, or I-D-S/I file organizations. MDQS operates as a subsystem to GCOS in both batch and time-sharing environments, and is available in two versions: MDQS/II, a databased retrieval and report generation system, and MDQS/IV, a system that offers all MDQS/II capabilities plus data base creation and maintenance features.

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The Common Files Facility (CFF) controls the sharing of user program and data files between GCOS III and GCOS 8 as well as between GCOS 8 hosts without requiring manual partitioning of data or mass storage devices. The CFF allows a Level 66 or DPS 8 system(s) and a DPS 88 system(s) and DPS 90 systems(s) to share disk files on a single common group of disk drives.

CFF allows up to four computer systems, in any mix, to share common disk drives. Concurrent access to files is controlled by lock bytes in the mass storage processor that supervises disk drive operation. Locking occurs at the single file level, which ensures that only one computer system in the cluster can update a file at one time. CFF clusters can also exist within communications networks based on Honeywell's Distributed Systems Architecture.

The Honeywell Error Logging and Analysis (ELAN) system is a software system concentrated mostly within the Input/Output Processor and its resident MSOS software. The DPS 90 is capable of storing cabinet status the instant an error is detected. A fault dictionary is then used to locate the failure if it is solid or recurring. MSOS communicates with GCOS 8 through MSOS Extension Execution Program (MEEP), a GCOS 8 module.

APPLICATION PROGRAMS AND UTILITIES

Honeywell offers the following utility routines and application programs for the DPS 90 systems.

Utilities

- HONEYEDIT
- TEXT Editor
- Text Executive Processor (TEX)
- Slave Program Activity Monitor (SPM)
- Time-sharing Debug/Trace (TSD/T)
- Collection and Plot of System Usage Levels (CAPSUL)
- Data Dictionary IDS I
- Mass Storage Utility
- Tape Testing
- Peripherals Resource Monitor
- Time-Sharing Dump Analysis
- Load Generator System-II
- SOLOMAN (Source & Library On-Line Manager)

Banking Applications

- Check Handling Executive Control Systems (CHECS)
- Document Entry Subsystem
- Proof and Transit Subsystem
- FUNDS System Administrative and Control Module
- FUNDS System Customer Profile Module
- FUNDS System Savings Account Module
- FUNDS System Loan Account Module
- FUNDS System General Ledger Module

Manufacturing Applications

- Honeywell Manufacturing System (HMS)
- Inventory Record Management Module
- Manufacturing Data Control Module
- Material Requirements Planning Module
- Master Production Scheduling Module
- Statistical Forecasting Module
- Capacity Requirements Planning Module
- Automatically Programmed Tools (APT)

Distribution Applications

- PROFIT (Inventory Control)
- Point-of-Sale System

Management Science Application Programs

- Mathematical Programming System (MPS)
- BMDP Statistical Programs
- SPSS Statistical Package
- IMSL Math/Statistics Library
- Project Management and Control System (PMCS)
- GPSS Simulation System
- Numerically Integrated Elements for Systems Analysis—(NISA) (Structural Analysis)
- Polo Finite (Structural Analysis)
- Coordinate Geometry (COGO)
- Concordance Generator Program

Financial Management Systems

- General Ledger
- Accounts Payable
- Accounts Receivable
- Payroll

MSA/Honeywell Applications

- Financial—General Ledger, Fixed Assets
- Cash Management—Accounts Receivable, Accounts Payable, Inventory and Purchasing
- Human Resources—Payroll, Personnel

Health Care Applications

- HHS (Honeywell Hospital System) Foundation System—Patient Profile/Master Index, Admission/Discharge/Transfer, Patient Accounting
- Fiscal/Administrative System—General Ledger/Responsibility Reporting, Accounts Payable, Property Ledger, Preventive Maintenance, Cost Allocation, Medical Records

Miscellaneous Application Programs

- Individualized Mathematics Instruction/66 (IMS/66)
- SCRIBE/66 Scheduling System
- ROLIN (Rapid On-Line Information Network)
- Employment Security Application Packages

Education Support

- Large Systems Marketing Education Support

PRICING

EQUIPMENT: What follows is estimated pricing and leasing cost for a possible basic configuration involving a DPS 90/92 dual-processor system and a maximum configuration involving a DPS 90/94 four-processor system:

TYPICAL DPS 90/92 SYSTEM: Consists of CPS8992 processor group with two CPUs, 32 megabytes of memory, a System Control Unit, a System Control Center, an Input/Output Processor, an Interface Adapter Unit, a Power Unit, a Network Processor Channel, a Low-Speed Channel, a Data-Streaming Channel, 90 VIP 7815 Display Units, a DCU8010 Network Processor and host connection, a Communications Console, three MTP8021 Magnetic Tape Processors, 24 MTU0610 Tape Drives, four MSP3885 Storage Processors, eight MSU3380 Storage Unit/Controllers, 24 MSU3382 Mass Storage Units, three PRU1600 1325 lpm Printers, and one URP0600 Unit Record Processor. Total purchase price comes to $8,758,123, and total one-year lease price comes to $501,991.

TYPICAL DPS 90/94 SYSTEM FOR A MAXIMUM CONFIGURATION: Consists of CPS8983 processor group with four CPUs, 256 megabytes of main memory, two

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System Control Units, two System Control Centers, four Input/Output Processors, two Interface Adapter Units, two Power Units, and the same complement of peripheral devices described in the DPS 90/92 configuration. Total purchase price comes to $15,808,123 and a total one-year lease price comes to $792,616.

SUPPORT: Honeywell offers five categories of support products for DPS 90 systems. These products include technical engineering, software, education, publications, and supplies.

System engineering falls into one of five billable support categories, as described in the following table.

	Hourly Rates ($)	Monthly Rates ($)
Principal or senior technical consultant	138	19,174
Project supervisor or technical consultant	112	15,653
Technical specialist	100	14,088
Systems analyst/senior programmer	85	11,739
Programmer	59	8,218

Hourly charges are for a four-hour minimum. The monthly rates do not include supplies.

The GCOS 8 operating system executive (OSE) is provided to DPS 88 users at no additional cost. All other facilities, such as job management, file systems, conversion aids, language processors, utilities, applications packages, communications software, system maintenance, and system performance analysis are separately priced.

Education services include standard courses, advanced professional training, multimedia self-instruction courses so that customers can self-train as often as needed, site surveys to determine educational requirements, on-site classes, and clustered on-site classes to accommodate a group of users from an area.

CONTRACT TERMS: DPS 90 equipment is available for purchase or for rental under a one-year or four-year lease. The basic monthly rentals entitle the user to unlimited central processor usage per month with on-call remedial maintenance between the hours of 8 a.m. and 6 p.m. on Mondays through Fridays, except for local Honeywell holidays. For maintenance beyond this period, the user pays an additional charge which is a fixed percentage of the base maintenance charge. For scheduled extended maintenance service (24 hours, 7 days per week), the additional charge is 40 percent of the base maintenance charge. Hourly rates for unscheduled maintenance outside of the daily 8 a.m. to 6 p.m. period are listed in the above chart.

Honeywell's TotalCare Program provides support services for hardware and software. These services include Basic and Extended Hardware Maintenance Site Preparation, Installation, On-site Dedicated Maintenance, Basic and Expanded Software Support, On-site Software Support, and Software Installation. Remote testing and diagnostic facilities include the National Response Center for toll-free, 24-hour-a-day contact with Honeywell; the Technical Assistance Center (which provides remote support); the Logistics Inventory Data System for rapid location of parts; and the ELAN software system for troubleshooting.

EQUIPMENT PRICES

		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)
PROCESSORS					
CPS8990	DPS 90/91 Central System includes a single CPU and 32 megabytes of main memory	3,950,000	6,250	246,875	183,721
CPS8992	DPS 90/92 Central System includes two CPUs and 32 megabytes of main memory	5,000,000	7,500	312,500	232,558
CPS8996	DPS 90/92T fully-redundant version contains two of each central system component and 64 megabytes of main memory	6,250,000	9,250	390,625	290,698
CPS8993	DPS 90/93 Central System includes three CPUs and 64 megabytes of main memory	7,300,000	10,500	456,250	339,535
CPS8994	DPS 90/94 Central System includes four CPUs and 64 megabytes of main memory	8,350,000	11,750	521,875	388,372
ADDITIONAL MEMORY					
CMM8932	Additional 32-megabyte memory module	400,000	800	25,000	18,605
SYSTEM UPGRADES					
CPK8991	DPS 90/91 to DPS 90/92	1,200,000	950	75,000	55,814
CPK8992	DPS 90/92 to DPS 90/93	2,000,000	2,700	125,000	93,023
CPK8993	DPS 90/93 to DPS 90/94	1,000,000	950	62,500	46,512
CPK8996	DPS 90/92 to DPS 90/92T	950,000	1,450	59,375	44,186
CPK8997	DPS 90/92T to DPS 90/93	1,000,000	950	62,500	46,512
CPK8981	DPS 90/91 to DPS 90/92 with second IOP	1,550,000	1,250	96,875	72,093
CPK8982	DPS 90/92 to DPS 90/93 with second and third IOP	2,350,000	3,000	146,875	109,302
CPK8983	DPS 90/93 to DPS 90/94 with fourth IOP	1,300,000	1,250	81,250	60,465
CPK8984	DPS 90/92 to DPS 90/92T with second IOP	1,300,000	1,750	81,250	60,465
CPK8985	DPS 90/92T to DPS 90/93 with third IOP	1,300,000	1,250	81,250	60,465

Five-Year Lease

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		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)
CHANNEL OPTIONS					
MXU8902	Additional Input/Output Processor with four high-speed channel processors	500,000	300	31,250	23,256
MXF8903	Exchange Feature, high-speed channel	2,500	—	156	116
MXF8904	Exchange Feature; network processor channel	1,500	—	94	70
MXF8905	Exchange Feature; low-speed channel	2,500	—	156	116
MXF8906	Exchange Feature; data streaming channel	2,500	—	156	116
MXF8909	Exchange Feature; Federal Information Processing Standard tape channel	2,500	—	156	116
MXF8913	High-speed channel attachment feature	8,000	12	500	372
MXF8914	Network processor attachment feature	8,000	12	500	372
MXF8915	Low-speed attachment feature	8,000	12	500	372
MXF8916	Data streaming channel attachment feature	8,000	12	500	372
INTERFACE ADAPTER UNIT AND OPTIONS					
MXU8910	Basic IAU; supports up to 8 GPA channels	52,650	150	3,291	2,449
MXF8921	Channel expansion for MXU8910; provides support for 9 to 16 channels	2,800	10	175	130
MXF8923	Power Expansion for MXU8910	5,200	5	325	242
MXF8927	Power Sequencer for MXU8910; 1 to 8 GPA channels	3,200	5	200	149
MSF8928	Power Sequencer Expansion for MXU8910; 9 to 16 GPA channels	2,600	5	162	121
MXF8023	General Purpose Adapter for tape	18,500	15	850	700
MXF8023	General Purpose Adapter for disk	18,500	15	850	700
MASS STORAGE SUBSYSTEM					
Processors and Features:					
MSP3881	Mass Storage Processor includes two storage directors and two attachment channels	74,270	200	4,400	3,745
MSP3885	Mass Storage Processor includes two storage directors and four attachment channels	90,270	226	5,350	4,550
MSP8021	Freestanding Primary Single-Channel Mass Storage Processor, which includes first MSU addressing feature; requires one channel connection feature	39,000	110	2,311	1,965
MSP8022	Integrated Secondary Single-Channel Mass Storage Processor	29,000	82	1,720	1,460
MSP8023	Integrated Secondary Single-Channel Mass Storage Processor	32,000	90	1,900	1,615
MSF8021	Dual Channel Option for MSP8021 and MSP8023	16,300	54	965	820
MSF8022	Dual Channel Option for MSP8022	16,300	54	965	820
MSA8011	Addressing capability for four MSU0451s or for two MSU0500/0501s	NC	NC	NC	NC
MSF8018	Primary Host Channel Connection to DPS 90 high speed channel	3,500	6	175	145
MSF8019	Switched Host Channel Connection for DPS 90 high speed channel	4,600	7	230	195
MSF3881	MSP3881 upgrade to MSP3885	16,000	26	890	755
MXF8916	Data Streaming Channel attachment feature	8,000	12	500	372
MSK0501	Upgrade Kit; MSU0500 to MSU0501	10,800	25	361	*297
MSK0502	MSU0500 Upgrade Kit for additional head disk assembly	3,468	—	—	—
MSF0011	MSU0501 Dual Access Feature	4,140	23	163	*136
MSF0501	MSU0501 Additional Head Disk Assembly	15,808	—	—	—
Disk Drives:					
MSU3380	Head-of-String Mass Storage Disk Drive includes a built-in controller and two HDAs	88,800	325	4,780	4,070
MSU3382	Slave Mass Storage Disk Drive includes two HDAs and attaches to the MSU3380	64,450	240	3,470	2,960
MSU0451	Removable Disk Mass Storage Unit, 156 megabytes	27,047	122	1,140	*950
MSF0006	Dual Access Feature for MSU0451	2,070	14	89	*76
MSF0007	Remote Position Sensing Option for MSU0451	2,025	14	87	*76
MSU0500	Dual Fixed Disk Mass Storage Unit; 626 megabytes	38,850	172	1,386	*1,154
MSU0501	Dual Fixed Disk Mass Storage Unit; 1101 megabytes	49,650	197	1,747	*1,452
MSK0501	Upgrade kit; MSU0500 to MSU0501	10,800	25	361	*297
MAGNETIC TAPE PROCESSORS					
MTP8021	Freestanding Primary Magnetic Tape Processor, which includes 1600/6250 bpi capability and first MTU addressing feature; requires a minimum of one channel connection feature	29,000	180	1,620	1,355
MTP8022	Integrated Secondary Magnetic Tape Processor	29,000	180	1,620	1,355
MTP8023	Integrated Secondary Magnetic Tape Processor	22,000	137	1,230	1,030
MTU0500	Magnetic Tape Unit	12,128	175	725	*613
MTU0610	Magnetic Tape Unit; includes cartridge load	21,000	175	801	*677
MTU0630	Magnetic Tape Unit	14,815	130	593	*505
Features for the MTU0500:					
MTF0018	Cartridge Load Capability	735	3	28	*24
MTF0540	75 ips, 9-Track	1,029	121	138	*132
MTF0541	75 ips, 7-Track	1,029	121	138	132
MTF0542	125 ips, 9-Track; includes cartridge load	4,872	77	218	*189
MTF0543	125 ips, 7-Track; includes cartridge load	5,523	123	324	*279

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		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)
Features for the MTU0610:					
MTF0607	800/1600 bpi feature	6,090	75	300	*260
MTF0608	1600/6250 bpi feature	13,319	115	511	*432
MTK0678	Upgrade Kit; MTF0607 to MTF0608 performance	10,784	48	211	*172
Features for the MTU0630:					
MTF0634	75 ips, 800/1600 bpi	4,725	140	286	*257
MTF0635	75 ips, 1600/6250 bpi	7,110	120	342	*300
MTF0636	125 ips, 800/1600 bpi	9,805	158	460	*398
MTF0637	125 ips, 1600/6250 bpi	10,330	150	460	*398
MTK0630	Performance upgrade MTF0634 to MTF0635	2,385	20	75	*60
MTK0631	Performance upgrade MTF0636 to MTF0637	1,700	25	55	*45
MTK0632	Performance upgrade MTF0634 to MTF0636	5,080	20	175	*145
MTK0633	Performance upgrade MTF0635 to MTF0637	3,220	20	120	*100
MTK0634	High Altitude Adapter	240	—	8	*6
PRINTERS					
PRU908	High-Speed Belt Printer; 900 lpm	34,975	421	2,065	*1,720
PRU1208	High-Speed Belt Printer; 1200 lpm	38,275	468	2,340	*1,920
PRU1600	High-Speed Belt Printer; 1325 lpm	64,940	538	2,910	*2,472
PRU1600 Options:					
PRB0500	OCR-B Print Belt	2,460	90	179	*164
PRB0524	OCR A/B Print Belt	2,460	90	179	*164
PRB0532	Puerto Rico Print Belt	2,460	94	179	*164
PRB0549	OCR-A Alphanumeric Print Belt	2,460	90	179	*164
PRB0600	ASCII Belt; upper-/lowercase	2,567	90	184	*166
PRF0022	24 Additional Print Positions; 136 to 160	2,610	16	112	*93
PUNCH CARD EQUIPMENT					
URP0600	Freestanding Unit Record Processor	26,585	42	940	*791
URP8901	DPS 90 Unit Record Processor	20,000	30	1,250	930
MXF8915	Low Speed Channel Attachment Feature for URP8901	8,000	12	500	372
URA0050	URP0600 Addressing Capability for PCU0121 and CCU0401	4,253	4	151	*123
URA0056	URP0600 Addressing Capability for CRU0501	265	—	9	*6
CRU0501	Card Reader; 500 cpm	19,500	119	684	*568
CCU0401	Card Reader/Punch; 400 cpm (read); 100 to 400 cpm (punch)	29,594	219	1,228	*1,032
PCU0121	Card Punch; 100 to 400 cpm	20,032	153	900	*698
CCK0401	Upgrade Kit; PCU0121 to CCU0401	9,562	79	328	*334
TERMINALS					
VIP7201	Asynchronous, Multipurpose Keyboard Display Terminal	795	20	—	—
VIP7301	Standard Keyboard Display Terminal with RS-422-A interface and 25-foot cable; includes optional RS-232-C interface	1,900	20	—	—
VIP7303	Word Processing Keyboard Display Terminal with RS-422-A interface and 25-foot cable; includes optional RS-232-C interface	1,900	20	—	—
VIP7307	Data Entry Keyboard Display Terminal with RS-422-A interface and 25-foot cable; includes optional RS-232-C interface	1,900	20	—	—
VIP7305	Multifunction Keyboard Display Terminal with RS-232-C/RS-422-A interface and 25-foot cable	1,900	20	—	—
VIP7814	Synchronous/Asynchronous Keyboard Display Terminal with 12-inch diagonal CRT, 1,920-character display positions	2,700	25	—	123
VIP7815	Synchronous/Asynchronous Keyboard Display Terminal with 15-inch CRT green phosphor, RS-232-C, and RS-422-A interfaces	3,095	30	—	138
VIP7823	Asynchronous Keyboard Display Terminal with Multifunction Keyboard; includes a 72-line scroll feature, buffered print adapter, and 25-foot RS-422-A cable	2,350	25	—	—
DATANET 6661 FRONT-END NETWORK PROCESSOR					
DCU6661	Processor; includes 64K bytes of memory, system support controller, direct interface adapter; up to 12 channel interface bases	36,605	261	1,990	*1,669
DATANET 6661 Options:					
DCF6607	Channel Interface Base	1,651	9	70	*58
DCF6611	Dual Synchronous Channel Package, to 9600 bps	1,450	7	60	*50
DCF6612	Dual Asynchronous Channel Package, to 9600 bps	590	4	26	*23
DCF6613	Automatic Call Unit, Dual Channel	1,180	4	46	*39

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		Purchase Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)
DCF6614	MIL STD 188C Synchronous Channel, to 9600 bps	1,501	8	63	*53
DCF6618	Dual Binary Synchronous Channel Package, to 9600 bps	1,450	7	60	*50
DCF6619	Broadband Channel, to 72K bps	3,056	12	125	*104
DCF6620	HDLC Voice-Grade Channel; to 9600 bps	2,573	11	106	*89
DCF6621	Bisynchronous Broadband Single Channel; to 72K bps	3,056	12	125	*104
DCF6626	Direct Connect Capability	350	2	15	*13
DCF6627	Broadband Channel, CCITT V.35 to 72K bps	3,430	12	139	*114
DCF6927	Universal Modem Bypass	415	11	30	*24
DCF6610	Dual Channel Package, to 9600 bps	1,180	4	46	*39
DCF6615	Asynchronous Dual Channel, to 9600 bps	1,501	8	63	*53
DCF6616	MIL-STD 188C Broadband Channel to 72K bps	1,501	8	63	*53
DCF6617	MIL-STD 188C HDLC Channel	2,573	11	106	*89
DCF6622	HDLC Broadband Channel to 72K bps	3,056	12	125	*104
DCF6623	HDLC Channel, CCITT-V.35 to 72K bps	3,430	12	139	*114
DATANET 8 FRONT-END NETWORK PROCESSOR					
DCU8010	Processor; includes 512K bytes of memory, system support controller, 512K bytes diskette drive, up to 16 channel interface bases	29,000	135	1,123	*937
DATANET 8 Options:					
DCE8003	Processor Power Module Enhancement	7,400	40	293	*245
DCE8002	Communications Line Expansion from 16 to 64 lines	3,000	5	106	*86
DCE8004	Communications Line Expansion from 64 to 128 lines; requires DEC8002/8003	5,000	10	179	*147
DCP8010	Extended Processor Performance Enhancement	18,500	86	644	*554
DCE8005	Additional 512K-byte diskette unit	1,785	18	79	*68
DCF8007	Channel Interface Base	2,500	14	99	*83
DCF8001	Communications Console; 100 cps	2,065	40	105	*92
DCF8009	Dual Asynchronous Channel; EIA RS-422-A; to 9600 bps each	1,000	7	41	*35
DCF8011	Dual Synchronous Channel; EIA RS-232-C; to 9600 bps	1,500	8	58	*49
DCF8012	Dual Asynchronous Channel; EIA RS-232-C; to 9600 bps	1,000	5	39	*32
DCF8014	Single Synchronous Channel; MIL-188-C; to 9600 bps	1,000	6	40	*33
DCF8015	Dual Asynchronous Channel; MIL-188-C; to 9600 bps	1,000	7	41	*35
DCF8016	Single Synchronous HDLC Wideband Channel; MIL-188-C; to 56K bps	1,995	15	83	*70
DCF8017	Single Synchronous HDLC Channel Package; MIL-188-C; to 9600 bps	2,500	12	99	*82
DCF8018	Dual Bi-Synchronous HDLC Channel Package; EIA RS-232-C; to 9600 bps	1,500	7	58	*49
DCF8019	Cross-Net Load/Dump Feature	1,000	6	40	*33
DCF8020	Single Synchronous HDLC EIA RS-232-C Channel; to 9600 bps	1,500	8	58	*49
DCF8022	Single Synchronous HDLC Wideband Channel; to 56K bps	3,000	16	118	*98
DCF8023	Single Synchronous HDLC Wideband Channel; CCITT V.35; to 56K bps	3,000	16	118	*98
DCF8024	Direct Connect Capability; to 9600 bps	350	2	14	*12
DCF8026	Universal Modem Bypass	415	2	16	*13
DCF8036	Dual Asynchronous Current Loop Channel; to 9600 bps	1,000	6	41	*35
DCM8005	Additional 512K bytes of memory; 512-1024KB	6,000	21	622	*534
DCM8008	Additional 512K bytes of memory; 1,024-1536KB	6,000	21	622	*534

**Five-Year Lease*

SOFTWARE PRICES

		Monthly License Fee ($)	Optional Support Charge ($)
GCOS 8 SYSTEM			
SVS8000	GCOS 8 Operating System EXEC	NSC	—
SVP8000	System Maintenance Facility	87	44
SVP8001	Software Management Facility	79	13
SVP8002	System Performance Analysis Facility	281	25
SVE8000	FMS Catalog Cache Facility	69	13
SVE8001	FMS Test Access Mode Facility	70	8
SVE8002	Password Encryption Facility	58	5
SVJ8000	Parametric JCL	36	5
Utilities:			
SNU0471	PPS Utilities	25	—
SNU0472	PPS Off-line	NSC	—
SNU0473	PPS On-line	NSC	—

NA—Not available.
NSC—No separate charge.

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		Monthly License Fee ($)	Optional Support Charge ($)
SVU8012	File Management System Utilities	316	45
SVU8000	Systems Utilities Facility	52	5
SVU8001	File Generation Facility	49	5
SVU8002	Sort/Merge Facility	107	17
Data Management:			
SVD8000	DM-IV Standard Facility	1,041	183
SVD8001	DM-IV Fortran Subschema Translator Option	120	10
SVD8002	I-D-S/I Facility	1,041	110
SVD8003	Indexed Sequential Processing Facility	28	6
SVD8006	Data Dictionary/Batch	281	35
SVD8007	Data Dictionary/Online	125	15
Languages and Compilers:			
SVL8000	Cobol-74 Compiler & Runtime Facility	262	26
SVL8001	Fortran Compiler & Runtime Facility	354	50
SVL8002	PL/1 Compiler & Runtime Facility	285	50
SVR8002	PL/1 Runtime Facility	77	11
SVL8003	RPG-II Facility	133	5
SVL8010	Fortran-77 Compiler & Runtime Facility	213	15
SVL8011	Fortran-77 Hex Option	NC	NC
SVL8012	Fortran-66 Compatibility Option for Fortran-77	NC	NC
SVL8013	Cobol-74 Relational Query (RQ)	90	10
SVR8000	Cobol-74 Runtime Facility	86	9
SVR8004	Fortran-77 Runtime Facility	63	5
SVP8008	Debug Support Option	104	20
SVP8009	Cobol-74 Debug Support Option	190	27
SVP8010	Fortran-77 Debug Support Option	229	10
SVL8008	Cobol-68 Compiler & Runtime	306	39
Transaction Processing:			
SVS8006	TDS Facility	1,601	210
SVS8007	TPE Facility	561	55
SVS8002	DM-IV TP Facility	1,389	167
SVU8003	DM-IV TP Forms Option	250	50
Time-Sharing:			
SVE8020	Multicopy Times-sharing Option	557	110
SVS8005	TSS Facility	84	22
SVE8019	TSS Administration Option	118	16
SVE8008	TSS File Management Option	112	11
SVE8009	TSS Advanced Application Support Option	167	33
SVE8010	TSS Media Input Option	55	11
SVL8007	TSS Basic Language Option	202	38
SVE8011	TSS Cobol-74 Option	55	11
SVE8012	TSS Fortran Option	55	11
SVE8013	TSS Text Processing Option (TEX)	320	66
SVE8014	TSS Editing Option (EDIT)	101	22
SVE8015	TSS Document Formatting Option	51	11
SVE8016	TSS Electronic Mail Option	167	33
SVE8017	TSS Sort Interface Option	70	11
SVE8022	TSS Fortran-77 option	55	11
SVD8004	TSS Data Basic	139	22
SVE8018	TSS DM-IV Option	82	14
Communications Software:			
SVC8000	GRTS-II Facility	273	44
SVC8001	GRTS-II HDLC Support Option	129	11
SVC8002	NPS Facility	974	209
SVC8003	NPS HDLC Support Option	129	11
SVC8006	Host File Transceiver Facility for L6	16	6
SVC8004	Extended FNP Support Facility	139	28
SVC8048	GRTS-I Facility	450	110
Query and End-User Facilities:			
SVD8005	I-D-S/I Data Query Option	167	33
SVP8003	DM-IV QRP Option	375	59
SVH8000	Personal Computing Facility	170	30
SVP8004	DM-IV PLP Option	263	45
SVH8001	PDQ Example Query (EQ)	350	40

NA—Not available.
NSC—No separate charge.

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		Monthly License Fee ($)	Optional Support Charge ($)
SVH8002	PDQ Interactive Query (IQ)	270	30
SVH8003	PDQ Comprehensive Report Examination & Display Option (CREDO)	210	25
SVP8006	MDQS/II Facility	612	117
SVP8007	MDQS/IV Facility	1,058	212
Other:			
SVS8003	DM-IV TP Comprehensive Facility	2,755	286
SVR8003	TSS Text Processing (TEX) Library Option	36	5
SVD8024	DDE Basic System	1,373	226
SVD8028	DDE Comprehensive Package for TDS	3,575	506
SVD8031	DDE Comprehensive Package for TPE	3,360	474
SVD8033	DDE System Management Facility for TDS	1,484	244
SVD8034	DDE System Management Facility for TPE	1,385	228
SPECIAL SYSTEMS SOFTWARE			
SVL8015	C Programming Language	340	800
SVL8016	C Programming Language Cross Compiler	70	160
SVP8013	Transaction Application Test System (TATS)	500	1,620
SVP8014	Softool Cobol Programming Environment	1,400	8,375
SVP8015	Softool Change & Config. Control	1,500	7,500
SVP8016	Complete Softool	2,500	15,500
SVP8017	Transaction Screen Mgmt. System (TSM)	980	1,920
SVP8018	System-80 Automatic Cobol Program Generator	780	1,840
SVP8019	System-80 Cobol Report Generator	480	1,000
SVU8016	MPCD Disk I/O Performance Analyzer	NA	100
SVU8019	BUSINESS-GRAF	NA	2,700
SVU8020	GRAFMASTER	NA	1,650
SVU8021	Scientific/Engineering Option	NA	1,575
DISTRIBUTED NETWORK SUPERVISOR (DNS) SOFTWARE			
SNC8020	Distributed Network Supervisor	490	86
SNC8021	Network Operator Interface (NOI)	10	5
SNC8022	Cross-Net Load/Dump Facility	10	5
SNC8023	Accommodation Mode, Host Conn. (DPS 8)	42	7
SNC8024	Host Connection (DPS 7)	42	7
SNC8028	Multiple Host Connection	20	8
SNC8031	HDLC Primary Network Support	82	15
SNC8033	Primary Network Private Virtual Circuit (Endpoint)	166	29
SNC8034	Primary Network Private Virtual Circuit (Switching)	170	30
SNC8035	TRANSPAC Connection (France) Limited	166	29
SNC8036	TRANSPAC Conn. (France) Extended	20	5
SNC8037	TELENET Connection (USA)	166	29
SNC8038	TYMNET Connection (USA)	166	29
SNC8039	DATAPAC Connection (Canada)	166	29
SNC8040	DDX-P Connection (Japan)	166	29
SNC8041	AUSTPAC Connection (Australia)	166	29
SNC8044	EDWP Connection (Switzerland)	166	29
SNC8045	DN-1 Connection (Netherlands)	166	29
SNC8046	EURONET Conn. (European Economic Community)	166	29
SNC8047	DATEX-P Conn. (West Germany) X.25	166	29
SNC8052	PSS Connection (United Kingdom)	166	29
SNC8053	NPDN Conn. (Scandanavia) X.21 Basic	166	29
SNC8054	NPDN Conn. (Scandanavia) X.21 Ext.	20	5
SNC8056	Extended X.25 Public Network (Greater than 16 Virtual Circuits)	20	5
SNC8057	Asynchronous Terminal Support	NSC	—
SNC8058	VIP Synchronous Terminal Support	NSC	—
SNC8060	Interactive Bisync (3270) Terminal Support	76	14
SNC8061	Remote Batch Bisync (2780) Terminal Support	52	9
SNC8062	Remote Computer Interface Terminal Support	20	5
SNC8065	TRANSPAC Anync Pad Support (France)	20	5
SNC8067	TELENET Anync Pad Support (USA)	20	5
SNC8068	TYMNET Anync Pad Support (USA)	20	5
SNC8069	DATAPAC Anync Pad Support (Canada)	20	5
SNC8070	DDX-P Anync Pad Support (Japan)	20	5
SNC8071	AUSTPAC Anync Pad Support (Australia)	20	5
SNC8072	PSS Anync Pad Support (United King.)	20	5
SNC8073	Logical HDLC	85	15
SNC8074	EDWP Anync Pad Support (Switzerland)	20	5
SNC8075	DN-1 Anync Pad Support (Netherlands)	20	5
SNC8076	EURONET Anync Pad Support (European Economic Community)	20	5
SNC8077	DATEX-P Anync Pad Support (West Germany)	20	5
SNC8090	GCOS Administration	136	24

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NSC—No separate charge.

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		Monthly License Fee ($)	Optional Support Charge ($)
SNC8091	GCOS 8 Administration (8MIN)	136	24
SNC8093	Log File Formatter (GCOS/GCOS 8)	NSC	—
SNC8094	DPS 8 Host to Host File Transfer	15	5
SNC8095	DNS for DPS 8/20 to 8/49	396	70
SNC8096	DNS for DPS 7 (Entry Level)	396	70
SCC1220	GCOS 64 FNP Support	15	5
SCU1618	GCOS 64 Distributed File Transfer	15	5

NA—Not available.
NSC—No separate charge. ■