CONNER
PERIPHERALS

CP3024
PRODUCT MANUAL

THE INSIGHT AND THE DRIVE.

PART NUMBER 00501-012

Conner Peripherals, Inc.

CP3024

Product Manual

Revision I.1

October, 1989

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Part Number: 00501-012

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1.0 Scope of Manual

This manual is intended for integrators of Conner Peripheral's line of OEM 3.5 inch disk drives. It covers the CP3024, a high performance 3.5 inch low-profile (1.00") 21.4 megabyte (formatted) disk drive with a 27 ms average seek time. It is designed to operate on an IBM PC/AT or equivalent in translate mode.

This manual describes the key features of the CP3024 and summarizes the specifications. It provides a description of the environmental and functional characteristics, the electrical interface of the disk drive, and the recommended mounting configuration. The timing requirements for data and register transfers are described, followed by sections on Host Address Decoding and Register Description. Operations that span several commands and the errors that are valid for each command are summarized in the concluding sections of the manual.

Conner Peripherals has developed an adapter board to be used in conjunction with the drive on an AT or equivalent system. The logic and a description of this adapter board can be found in Appendix A.

2.0 Key Features

Key features of the CP3024 include:

- Low power requirements enabling battery operation in portable environments
- High performance rotary voice coil actuator with embedded servo system
- Two of seven run length limited code
- High shock resistance
- Internal air filtration system
- Sealed HDA
- Automatic actuator latch against inner stop upon power down
- Microprocessor-controlled diagnostic routines that are automatically executed at start-up
- Automatic error correction and retries
- Block size: 512 bytes
- Emulates IBM Task File and supports additional commands
- Up to two drives may be daisy-chained on this interface
- Translate mode (17 sectors, 4 heads, 615 cylinders) is supported
- 1:1 interleave
- Look Ahead Read Capability
- AC Hysteresis on interface
- 8K Buffer

3.0 Specification Summary

3.1 Capacity

Model	CP3024
Formatted Mbytes	21.4

3.2 Physical Configuration

Model	CP3024
Actuator Type	Rotary Voice-Coil
Number of Disks	1
Data Surfaces	2
Data Heads	2
Servo	Embedded
Tracks per Surface	636
Track Density (TPI)	1150
Formatted Track Capacity (Bytes)	16,896
Bytes per Block	512
Blocks per Drive	41,976
Sectors per Track	34 physical, 33 user

3.3 Performance

Seek Times [1]	Track to Track: 8.0 ms Average: 27.0 ms [2] Maximum: 50.0 ms
Average Latency	8.4 ms
Rotation Speed (+0.1%)	3575 RPM
Controller Overhead	1.0 ms
Data Transfer Rate (To/From Media)	1.25 MByte/second
Data Transfer Rate (To/From Buffer)	4.5 MByte/second
Start Time (Power Up)	
(0-3557 r p m)	Typical: 5 seconds Maximum: 10 seconds
(0 r p m - Ready)	Typical: 7 seconds Maximum: 15
Stop Time (Power Down)	Typical: 5 seconds Maximum: 10
Start/Stop Cycles	10,000 minimum
Interleave	1:1 ratio
Buffer Size	8K

1 *At nominal D.C. input voltages.*

2 *Average seek time is determined by dividing the total time required to seek between all possible ordered pairs of track addresses, by the total number of these ordered pairs.*

3.4 Read/Write

Interface	Task File
Recording Method	2 of 7 RLL code
Recording Density (ID)	21,594 bits per inch
Flux Density (ID)	14,396 flux reversals per inch

3.5 Power Requirements (Typical)

	+12V DC ±5%	+5V DC ±5%	POWER
Read/Write Mode	230 mA	275 mA	4.2 W
Seek Mode	140 mA	180 mA	2.8 W
Idle Mode	120 mA	120 mA	2.0 W
Standby Mode	1 mA	90 mA	0.5 W
Spin-Up Mode	700 mA	180 mA	n/a

Read/Write Mode: Occurs when data is being read from or written to the disk.

Seeking Mode: Occurs while the actuator is in motion.

Idle Mode: Occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.

Standby Mode: Occurs when the motor is stopped, actuator parked and all electronics except interface control is in sleep state. STANDBY MODE will occur after a programmable timeout since last host access occurs. Drive ready and seek

complete status exist. The drive will leave STANDBY MODE upon receipt of a command which requires disk access or upon receipt of a spin up command.

Spin-Up Mode: Occurs while the spindle motor is accelerating from its rest state to its operational speed. During the typical spin-up cycle, current on the 12 volt line may reach up to 900 mA for up to 500 microseconds. The specified current is the averaged value over the spin-up cycle.

Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load):

+12V DC	1 %
+5V DC	2 %

3.6 Physical Characteristics

Outline Dimensions ± .010"	1.00" x 4.00" x 5.75"
Weight	1.1 pounds
Mounting Dimensions	See Figure 1

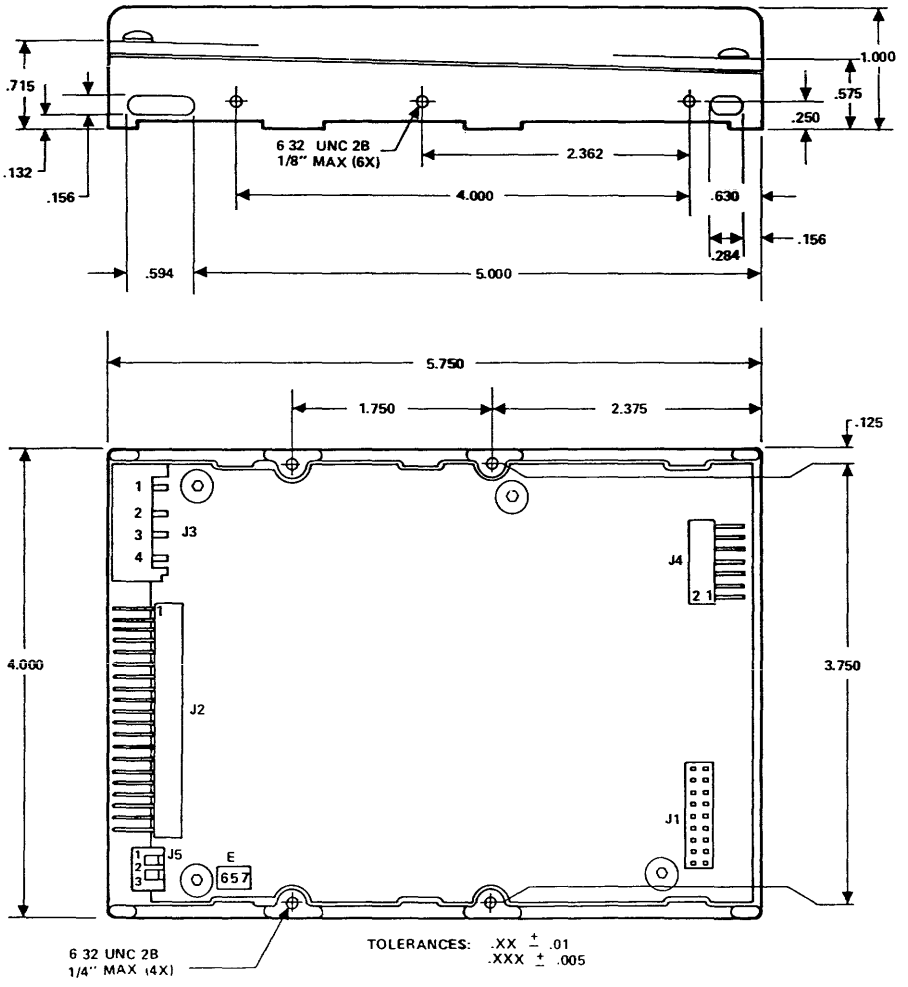


Figure 1. Mounting Configuration

4.0 Environmental Characteristics

4.1 Temperature

Operating	5°C to 55°C
Nonoperating	-40°C to 60°C
Thermal Gradient	20°C per hour maximum

4.2 Humidity

Operating	8% to 80% noncondensing
Nonoperating	8% to 80% noncondensing
Maximum Wet Bulb	26°C

4.3 Altitude (relative to sea level)

Operating	-200 to 10,000 feet
Nonoperating (maximum)	40,000 feet

4.4 Reliability and Maintenance

MTBF	20,000 hours (POH)[1]
MTTR	10 minutes typical
Preventative Maintenance	None
Component Design Life	5 years
Data Reliability	<1 nonrecoverable error in 10^{12} bits read

[1] *population is minimum of 100 units*

4.5 Shock and Vibration

Shock	1/2 sine pulse
Vibration (measured without shock isolation)	Swept sine, 1 octave per minute
Nonoperating shock[1]	75 G's, 11 ms
Nonoperating vibration[1]	
5-62 Hz	.020" (double amplitude)
63-500 Hz	4 G's (0 peak)
Operating Shock[1]	5 G's, 11 ms
Operating Vibration[1]	
5-27 Hz	.010" double amplitude
28-500 Hz	.5 G's

[1] *Without nonrecoverable errors*

4.6 Magnetic Field

The externally induced magnetic flux density may not exceed six gauss as measured at the disk surface.

4.7 Acoustic Noise

40 dBA maximum at one meter.

4.8 Safety Standards

The CP3024 disk drive is designed to comply with relevant product safety standards such as:

- UL 478 Electronic Data Processing Units and Systems
- CSA C22.2 No. 154 Data Processing Equipment
- VDE 0804 Regulations for Telecommunications Apparatuses including Information Processing Equipment
- IEC 435 Safety Requirements for Data Processing Equipment.

5.0 Functional Description

The CP3024 contains all mechanical and electronic parts necessary to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

5.1 Read/Write and Control Electronics

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is to provide one of two head selections, read pre-amplification, and write data circuitry.

The single microprocessor controlled circuit card provides the remaining electronic functions which include:

- Read/Write Circuitry
- Rotary Actuator Control
- Interface Control
- Spin Speed Control
- Dynamic Braking
- Power Management

At power down or the start of STANDBY MODE, the heads are automatically retracted to the inner diameter of the disk. There they are latched and parked on a landing zone that is inside the data tracks.

5.2 Drive Mechanism

A brushless DC direct drive motor rotates the spindle at 3575 rpm. The motor/spindle assembly is balanced to provide minimal mechanical runout to the disks and to reduce vibration of the HDA. A dynamic brake is used to provide a fast stop to the spindle motor when power is removed, or upon initiation of STANDBY MODE.

5.3 Air Filtration System

Within the sealed enclosure, a .3 micron filter provides a clean environment to the heads and disks.

5.4 Head Positioning Mechanism

The two read/write heads are supported by a mechanism coupled to the voice coil actuator.

5.5 Read/Write Heads and Disks

Data is recorded on one 95 mm diameter disk through two 3370 type composite ferrite heads.

5.6 Error Correction

The CP3024 performs internal error correction. The error correction polynomial is capable of correcting one error burst with a maximum of 8 bits per 512 byte block. The following polynomial is used:

$$\text{Forward: } P(X) = (X^{32}+X^{28}+X^{26}+X^{19}+X^{17}+X^{10}+X^{6}+X^{2}+1)$$

5.7 Customer Options

There are four jumper options available for configuration: HSP, C/D, DSP, and ACT.

HSP, when jumpered, connects the -HOST SLV/ACT signal on the interface to ground for systems that require the slave drive to provide -SLAVE PRESENT signal in a two-drive system.

C/D is the address jumper. When jumpered, the master (or C drive), is selected. When open, the slave (or D drive), is selected.

DSP, when jumpered, indicates to the master drive that a slave is present. In a two-drive system, this jumper option must be installed in the master, or C drive.

The last jumper, ACT, connects the -ACTIVE signal to the - HOST SLV/ACT signal on the interface. This signal provides the capability to drive an external LED. An external current limiting resistor is required.

As an alternative, an LED may be connected between J4, pins 1 and 2. This would provide both an open collector drive signal and a current limiting resistor connected to +5V respectively.

The following table shows what the jumper settings should be for various system configurations.

Jumper Configuration	1 Drive	2 Drive Master	2 Drive Slave
ACT	J	Note 1	Note 1
C/D	J	J	NJ
HSP	NJ	NJ	Note 2
DSP	NJ	J	NJ

Note 1: In a two drive system, it is possible to drive one LED with both drives. An external current limiting resistor is required.

Note 2: If the drive is connected to a host that requires that the signal -DRIVE SLAVE PRESENT be supplied from the slave drive, via the interface signal -HOST SLV/ACT, then this jumper must be installed. If this jumper is installed, the ACT jumper must not be installed because the two jumpers are mutually exclusive.

6.0 Electrical Interface

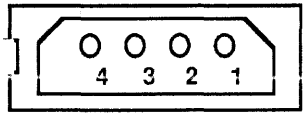
6.1 Power Connectors

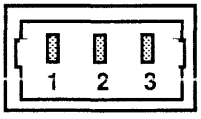
The CP3024 has a 4-pin DC power connector (J3) mounted on the PCB. The recommended mating connector is AMP part number 1-480424-0 utilizing AMP pins (part number 350078-4 or equivalent). DC power may also be supplied to the drive through a 3 pin connector (J5). The recommended mating connector is Molex part number 39-01-0033 utilizing Molex pins (part number 39-00-0031 or equivalent). For location of J3 and J5, see Figure 2.

Power is to be supplied at either J3 or J5, but not both.

6.2 Power Connector Pin Description

J3		J5	
1	+12V	1	+5V
2	GND	2	+12V
3	GND	3	GND
4	+5V		





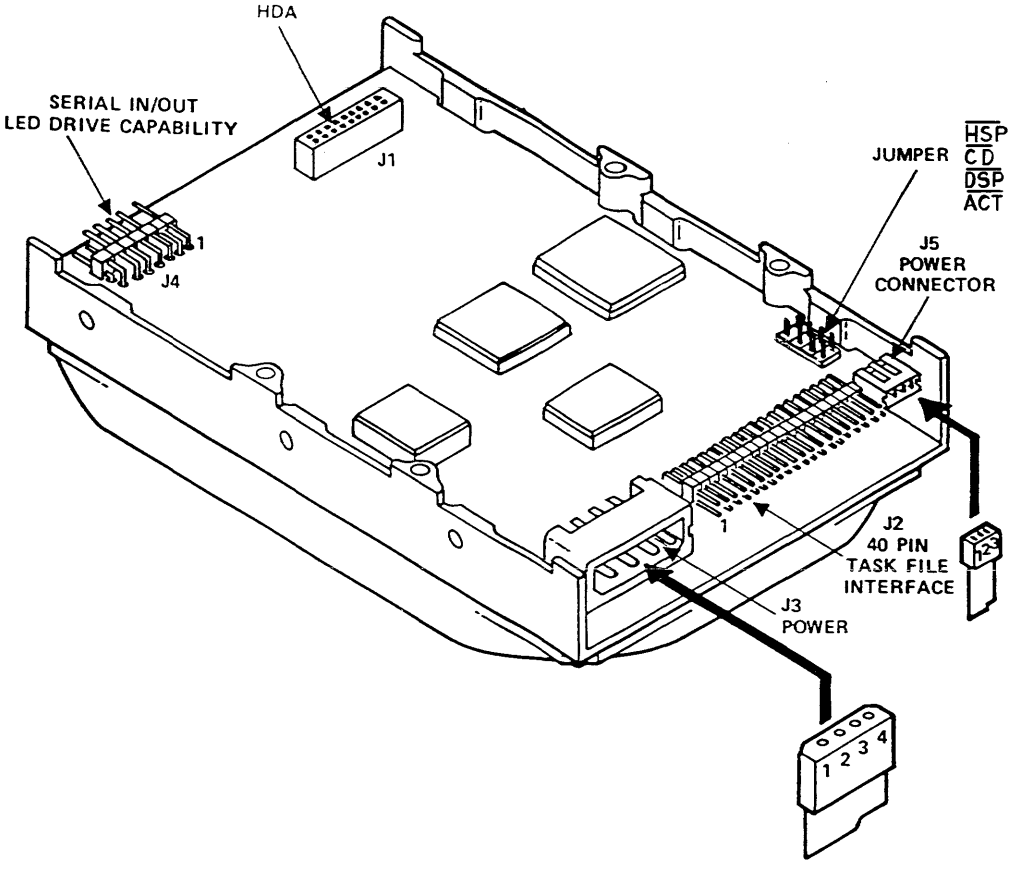


Figure 2. Connectors and Jumpers

6.3 Task File Interface Connector

The CP3024 has a 40-pin Task File Interface connector (J2) mounted on the printed circuit board. The recommended mating connector is Molex part number 10-91-2401 or equivalent. Two drives may be daisy chained together at this connector. Maximum cable length is two feet. For location of J2, see Figure 2.

6.4 Diagnostic Routines

The microprocessor performs diagnostics upon application of power. If an error is detected, the CP3024 will not come ready.

7.0 Recommended Mounting Configuration

The CP3024 drive is designed to be used in applications where the unit may experience shock and vibrations at greater levels than larger and heavier disk drives.

7.1 Shock Tolerance Features

The design features which allow greater shock tolerance are the use of rugged heads and media, a dedicated landing zone, closed loop servo positioning, and specially designed motor and actuator assemblies.

7.2 Mechanically Isolated Mounting Points

Ten base mounting points are provided to the customer. The drive is mounted using 6-32 screws; 1/8" maximum insertion for the sides, and 1/4" maximum insertion for the bottom. The system integrator should allow ventilation to the drive to ensure reliable drive operation over the operating temperature range. The drive may be mounted in any attitude.

For additional vibration isolation, an external suspension system may be used. For location of mounting holes, see Figure 1.

8.0 Electrical Description

8.1 Signal Levels

All signal levels are TTL compatible. A logic "1" is greater than 2.0 volts. A logic "0" is from 0.00 volts to .70 volts. The drive capability of each of the inbound signals is described below.

8.2 Signal Conventions

The interface between the drive adapter and the drive is called the Host Interface. The set of registers in the I/O space of the Host is known as the Task File.

All signals on the Host Interface shall have the prefix HOST. All negatively active signals shall be further prefixed with a "-" designation. All positive active signals shall be prefixed with a "+" designation. Signals whose source are the Host, are said to be "outbound" and those whose source is the drive, are said to be "inbound".

8.3 Pin Descriptions

The following table describes all of the pins on the Task File Interface:

Pin Number	Signal	Pin Number	Signal
01	- HOST RESET	02	GND
03	+ HOST DATA 7	04	+ HOST DATA 8
05	+ HOST DATA 6	06	+ HOST DATA 9
07	+ HOST DATA 5	08	+ HOST DATA 10
09	+ HOST DATA 4	10	+ HOST DATA 11
11	+ HOST DATA 3	12	+ HOST DATA 12
13	+ HOST DATA 2	14	+ HOST DATA 13
15	+ HOST DATA 1	16	+ HOST DATA 14
17	+ HOST DATA 0	18	+ HOST DATA 15
19	GND	20	KEY
21	RESERVED	22	GND
23	- HOST IOW	24	GND
25	- HOST IOR	26	GND
27	RESERVED	28	+ HOST ALE
29	RESERVED	30	GND
31	+ HOST IRQ14	32	+ HOST IO16
33	+ HOST ADDR 1	34	- HOST PDIAG
35	+ HOST ADDR 0	36	+ HOST ADDR 2
37	- HOST CSO	38	- HOST CS1
39	- HOST SLV/ACT	40	GND

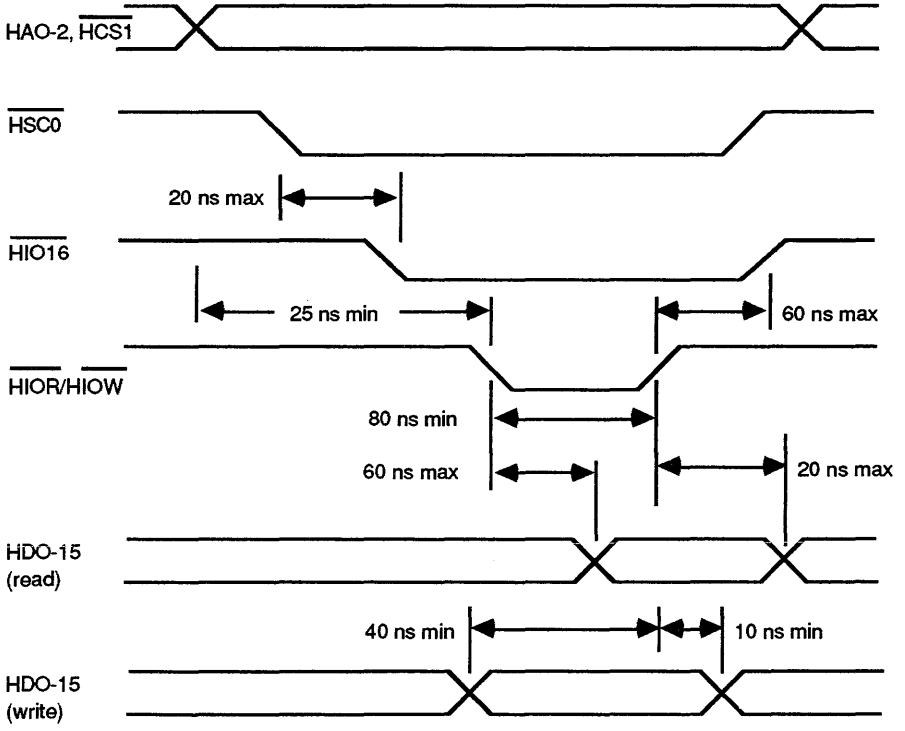
Signal Name	Direction	Pin	Description
- HOST RESET	O	01	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	O	02	Ground between the drive and the Host.
+HOST DATA 0-15	I/O	03-18	16-bit bi-directional data bus between the host and the drive. The lower 8 bits, HD0 - HD7, are used for register and ECC access. All 16 bits are used for data transfers. These are tri-state lines with 24 mA drive capability.
GND	O	19	Ground between the drive and the Host.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
RESERVED	O	21	
GND	O	22	Ground between the drive and the host.
- HOST IOW	O	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data register of the drive.
GND	O	24	Ground between the drive and the host.
- HOST IOR	O	25	Read strobe which, when low, enables data from a register or the data register of the drive onto the host data bus HD0 through HD15. The rising edge of - HOST IOR latches data from the drive at the host.
GND	O	26	Ground between the drive and the host.

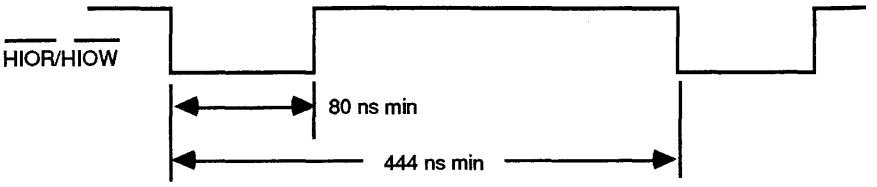
Signal Name	Direction	Pin	Description
RESERVED	O	27,29	
+HOST ALE	O	28	Host Address Latch Enable. A signal used to qualify the address lines. This signal is presently not used by the drive.
GND	O	30	Ground between drive and host.
+HOST IRQ14	I	31	Interrupt to the Host system, enabled only when the drive is selected, and the host activates the - IEN bit in the Digital Output register. When the - IEN bit is inactive, or the drive is not selected, this output is in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 8 mA drive capacity.
- HOST IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is a tri-state line with 24 mA drive capacity.
- HOST PDIAG	I	34	Passed diagnostic. Output by the drive if it is strapped in the slave mode (C/D not jumpered). Input to the drive if it is strapped in the master mode (C/D jumpered). This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is a tri state line with 24 mA drive capability.
+HOST A0, A1, A2	O	35, 33,36	Bit binary coded address used to select the individual registers in the task file.

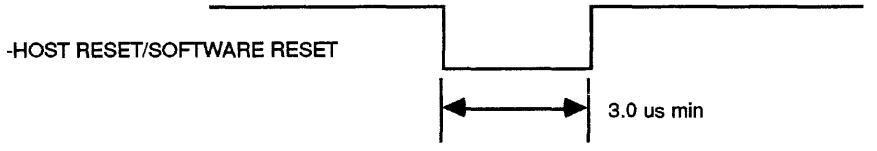
Signal Name	Direction	Pin	Description
- HOST CS0	O	37	Chip select decoded from the host address bus. Used to select some of the Host accessible registers.
- HOST CS1	O	38	Chip select decoded from the Host address bus. Used to select three of the registers in the Task File.
- HOST SLV/ACT	I	39	Signal from the drive used either to drive an active LED whenever the disk is being accessed or as an indication of a second drive present. (See the Customer Options section for further information.) When jumpered as - ACTIVE, this signal is active low when the drive is busy and has a drive capability of 20 mA. When jumpered as - SLAVE PRESENT signal, it is an indication of the presence of a second drive when low. In this state, it has a drive capability of 10 mA open drain.
GND	O	40	Ground between the drive and the host.

9.0 Timing Requirements

There are two principle activities on the Host Interface: data transfers and register transfers. The timing for both follow:




HIOR/HIOW
80 ns min
444 ns min


-HOST RESET/SOFTWARE RESET
3.0 us min

10.0 Host Address Decoding

The Host addresses the drive using programmed I/O. This method requires that

1) the desired register address be placed on the three Host address lines HA2 - HA0,

2) a proper chip select is asserted, and

3) a read or write strobe (-HOST IOR/-HOST IOW) is given to the chip.

The Host generates two independent chip selects on the interface. The high order chip select, -HOST CS1, is used to access register 3F6 or 3F7. The low order chip select, - HOST CS0, is used to address registers 1F0 - 1F7.

The Host data bus 15-8 is only enabled when IO16 Enable is active, and the Host is addressing the data register for transferring data, and not the ECC bytes (which are only transferred if the operation is a read or write long).

The following I/O map defines all of the register addresses and functions for these I/O locations.

[1] Addr	- CS0	- CS1	HA2	HA1	HA0	Read Function	Write Function
	1	1	x	x	x	No Operation	No Operation
	0	0	x	x	x	Invalid Address	Invalid Address
	1	0	0	x	x	High Impedance	Not Used
	1	0	1	0	x	High Impedance	Not Used
1F0	0	1	0	0	0	Data Register	Data Register
1F1	0	1	0	0	1	Error Register	Write Precomp Reg
1F2	0	1	0	1	0	Sector Count	Sector Count
1F3	0	1	0	1	1	Sector Number	Sector Number
1F4	0	1	1	0	0	Cylinder Low	Cylinder Low
1F5	0	1	1	0	1	Cylinder High	Cylinder High
1F6	0	1	1	1	0	SDH Register	SDH Register
1F7	0	1	1	1	1	Status Register	Command Register
3F6	1	0	1	1	0	Alt.Status Reg.	Dig Output Reg.
3F7	1	0	1	1	1	Drive Addr. Reg.	Not Used

x = don't care

[1] *These I/O port addresses are listed for programmer reference. They are a function of I/O decoding in the Host Adapter, such as the Conner AT Adapter Card shown in Appendix A. These I/O addresses are required for compatibility with typical AT BIOS.*

11.0 Register Description

In the following register descriptions, unused write bits should be treated as "don't cares", and unused read bits should be read as zeroes.

11.1 Data Register

- HOST CS0, Address 0, [Read/Write]

The data register is the register through which all data is passed on read and write commands. It is also the register to which the sector table is transferred during format commands and the data associated with the identify command is transferred. All transfers are high speed 16 bit I/O operations except for ECC bytes transferred during read/write long commands. These bytes are slower 8 bit operations that occur after the transfer of the data.

Data is stored on the disk with the Least Significant Byte first, then the Most significant byte for each word. This is important to remember when testing the ECC circuitry.

11.2 Error Register

- HOST CS0, Address 1, [Read Only]

This error register contains status from the last command executed by the drive. The contents of this register are only valid when the error bit (ER) is set in the Status register, unless the drive has just powered up or completed execution of its internal diagnostic. In this case the register contains a status code.

The error bits in the register are defined below.

Bit	7	6	5	4	3	2	1	0
	BBK	UNC	---	IDNF	---	ABRT	TKO	---

BBK: Indicates that a bad block mark was detected in the requested sector's ID field. A bad block is not created in the factory, but only when requested in the format command.

UNC: Indicates that a non-correctable data error has been encountered.

IDNF: Indicates that the requested sector's ID field could not be found.

ABRT: Indicates that the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.

TK0: Indicates that track 0 has not been found during a recalibrate command.

- - - : Not used. These bits are reset to zero.

11.3 Write Precomp Register

- HOST CS0, Address 1, [Write Only]

A register previously used to set write precompensation, that is present but is used only for enabling or disabling Look Ahead Read's.

11.4 Sector Count

- HOST CS0, Address 2, [Read/Write]

The sector count defines the number of sectors of data to be read or written. If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read such that the register contains the number of sectors left to access in the event of an error in a multi-sector operation. The contents of this register define the number of sectors per track when executing an initialize drive parameters command. This register is also used in the power commands (section 12.8) to provide the power down time-out parameter and status.

11.5 Sector Number

- HOST CS0, Address 3, [Read/Write]

This register contains the starting sector number for any disk access. At the completion of each sector, and at the end of the command this register is updated to reflect the last sector read correctly, or the sector on which an error occurred. During multiple sector transfers, this register is updated to point at the next sector to be read/written if the previous sector's operation was successful.

11.6 Cylinder Low

- HOST CS0, Address 4, [Read/Write]

The cylinder low register contains the low order 8 bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

11.7 Cylinder High

- HOST CS0, Address 5, [Read/Write]

The cylinder high register contains the two high order bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

11.8 SDH Register

- HOST CS0, Address 6, [Read/Write]

This register contains the drive and head numbers, as defined below:

Bit	7	6	5	4	3	2	1	0
	RSVD	0	1	DRV	HEAD	HEAD	HEAD	HEAD

DRV: Is the binary encoded drive select number. When this bit is reset, the master drive is selected, and when this bit is set, the slave drive is selected.

HEAD: Is the four-bit binary encoded head select number.

RSVD: This bit is used by the Host.

At the completion of each sector, and at the end of the command, this register is updated to reflect the currently selected head.

11.9 Status Register

- HOST CS0, Address 7 [Read Only]

This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the busy bit is active, no other bits are valid. The Host reading this register when an interrupt is pending is considered to be the interrupt acknowledge, and any pending interrupt is therefore cleared whenever this register is read.

The bits in this register are defined below:

Bit	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

BSY: Is the busy bit, which is activated whenever the drive has access to the Task File registers, and the Host is locked out from accessing the Task File. This bit is activated under the following circumstances:

1) At activation of the HOST RESET pin in the interface, or at activation of the software bit in the digital output register.

2) Immediately upon Host write of the command register with a read, read long, read buffer, seek recall, initialize drive parameters, verify,identify, or diagnostic command.

3) Immediately following transfer of 512 bytes of data after Host write of the command register with a write, format track, or write buffer command, or

4) 512 bytes of data and the four ECC bytes after a Host write of the command register with a write long command. When BSY is active, any Host read of a Task File register is inhibited and the Status register is read instead.

DRDY: The drive ready indication. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be inactive at power up and remain inactive until the drive is up to speed and ready to accept a command.

DWF: The drive write fault bit. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current write fault status. DRQ is the data request bit, which indicates that the drive is ready for transfer of a word or a byte of data between the Host and the Data register.

DSC: The drive seek complete line. It is an indication that the actuator is on track. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be inactive at power up and remain inactive until the drive is up to speed and ready to accept a command.

DRQ: The data request bit, which indicates that the drive is ready for transfer of a word or byte of data between the Host and the Data register.

CORR: The corrected data bit, which is active when a correctable data error has been encountered and the data has been corrected. This condition will not terminate a multi-sector read operation.

IDX: The index bit which is active once per disk revolution.

ERR: The error bit, which indicates that the previous command ended in some type of error. The other bits in the Status register, and the bits in the error register will have additional information as to the cause of the error.

11.10 Command Register

- HOST CS0, Address 7, [Write Only]

The eight-bit code written to this register passes to the drive the command from the Host. Command execution begins immediately after this register is written. A list of executable commands with the command codes and necessary parameters for each command follows.

Command Name	Command Code	Parameters Used			
		SC	SN	CY	SDH
Recalibrate	0 0 0 1 X X X X	N	N	N	D
Read Sector(s)	0 0 1 0 0 0 L R	Y	Y	Y	Y
Write Sector(s)	0 0 1 1 0 0 L R	Y	Y	Y	Y
Read Ver Sector(s)	0 1 0 0 0 0 0 R	Y	Y	Y	Y
Format Track	0 1 0 1 0 0 0 0	N	N	Y	Y
Seek	0 1 1 1 X X X X	N	N	Y	Y
Execute Drive Diagnostics	1 0 0 1 0 0 0 0	N	N	N	D
Initiator Drive Parameters	1 0 0 1 0 0 0 1	N	N	N	Y
Read Multiple	1 1 0 0 0 1 0 0	Y	Y	Y	Y
Write Multiple	1 1 0 0 0 1 0 1	Y	Y	Y	Y
Set Multiple	1 1 0 0 0 1 1 0	Y	N	N	D
Power Commands	1 1 1 0 0 P P P	Y	N	N	D
Read Sector Buffer	1 1 1 0 0 1 0 0	N	N	N	D
Write Sector Buffer	1 1 1 0 1 0 0 0	N	N	N	D
Identify Drive	1 1 1 0 1 1 0 0	N	N	N	D
Cache On/Off	1 1 1 0 1 1 1 1	N	N	N	D

Command Codes:

L: The long bit. If 1, read/write long commands are executed. If 0, normal read/write commands are performed.

R: The retry bit. 0 = retries are enabled. 1 = retries are disabled. Retries that may be enabled/disabled are those on ECC and data errors. When retries are disabled at the start of a command, they are always automatically enabled at the end of the command.

P: A valid bit for power commands EO-E3 and E5-E6

X: Don't care.

Parameters Used:

SC: The sector count register.

SN: The sector number register.

CY: The cylinder registers.

SDH: The drive/head register.

Y: The register contains a valid parameter for this command. For the drive/head register, Y means that both the drive and head parameters are used.

D: Only the drive parameter is valid and not the head parameter.

N: The register does not contain a valid parameter for this command.

For the command decode, the "1's" and "0's" are important. Failure to comply will result in an Aborted Command response or misinterpretation of the command.

11.11 Alternate Status Register

- HOST CS1, Address 6, [Read Only]

This register contains the same information as the Status Register in the Task File. The only difference being that reading this register does not imply interrupt acknowledge to reset a pending interrupt.

Bit	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

See the description of the Status register for definitions of the bits in this register.

11.12 Digital Output Register

- HOST CS1, Address 6, [Write Only]

This register contains two control bits as follows:

Bit	7	6	5	4	3	2	1	0
	---	---	---	---	---	SRST	- IEN	---

- **IEN:** The enable bit for this disk drive interrupt to the Host. When this bit is active and the drive is selected, the Host interrupt (-HOST IRQ14) is enabled, through a tri-state buffer

to the Host. When this bit is inactive, or the drive is not selected the -HOST IRQ14 pin will be in a high impedance state, regardless of the presence or absence of a pending interrupt.

SRST: Is the Host software reset bit. The drive is held reset when this bit is active, and enabled when this bit is inactive. If two drives are daisy chained on the interface, this bit will reset both drives simultaneously.

- - - : These bits are not used.

11.13 Drive Address Register

- HOST CS1, Address 7, [Read Only]

This register loops back the drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

Bit	7	6	5	4	3	2	1	0
	RSVD	- WTG	- HS3	- HS2	- HS1	- HS0	- DS1	- DS0

RSVD: Reserved and undriven by the drive. When the Host reads the drive address register, this bit must be in a high impedance state.

-WTG: The write gate bit, active when writing to the disk drive.

-HS3 through -HS0: The one's complement of the binary coded address of the currently selected head. For example, if -HS3 through -HS0 are 1 1 0 0, respectively, head 3 is selected. -HS3 is the most significant bit. -DS1 is the drive select bit for drive 1, and should be active when drive 1 is selected and active. -DS0 is the drive select bit for drive 0, and should be active when drive 0 is selected and active. It is important to note that Bit 7 is not driven for compatibility with the floppy drive address space. If your system is different, you may have to drive this bit when this register is read.

12.0 Command Description

All commands are decoded from the command register. The Host interface is programmed by the Host computer to perform commands and will return status to the Host at command completion. When two drives are daisy chained on the interface, commands are written in parallel to both drives. Only the selected drive will execute the command, except for the diagnostic command. In that case, both drives execute the command and the slave drive reports its status to the master via the -HOST PDIAG signal.

Drives are selected by the DRV bit in the drive/head register and by a jumper, on the drive designating it as either a master or slave. See the Section 5.7 on Customer Options. When the DRV bit is reset, the master drive is selected. When the DRV bit is set, the slave drive is selected. When drives are daisy chained, one must be jumpered as the master and one as the slave. When a single drive is attached to the interface, it must be jumpered as the master. Throughout this document, drive selection always refers to the state of the DRV bit and position of the master/slave jumper.

To issue a command, load the pertinent registers in the Task File, activate the interrupt enable bit, -IEN in the digital output register, and then write the command code to the command register. Execution begins as soon as the command register is written.

12.1 Recalibrate - 10

This command will move the read/write heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY and executes a seek to cylinder zero. The drive then waits for the seek to complete before updating status, resetting BSY and generating an interrupt. If the drive cannot reach cylinder 0, the error bit is set in the Status register and

the track 0 bit set in the error register. An aborted command response will be given if the drive is not spinning or is not on track. Upon successful completion of the command, the Task File registers will be as follows:

Error Register	00
Sector Count	Unchanged
Sector Number	Unchanged
Cylinder Low	00
Cylinder High	00
SDH	Unchanged

12.2 Read Sector(s) - 2X

This command will read from 1 to 256 sectors as specified in the Task File beginning at the specified sector (sector count equal to 0 requests 256 sectors).

When the command register is written, the drive sets the BSY bit and begins execution of the command. An aborted command is set if bits 2 and 3 are not equal to zero. An ID Not Found error is returned if incorrect task file parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data field is read into the sector buffer, error bits are set if an error was encountered, the DRQ bit is set, and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector.

Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector reads set DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector, and the drive is ready for the data to be read by the Host. DRQ is reset and BSY is set immediately when the Host empties the sector buffer.

If an error occurs during a multiple sector read, the read will terminate at the sector where the error occurs. The Task File registers will contain the cylinder, head, and sector number of the sector where the error occurs. The Host may then read the Task File to determine what error has occurred, and on which sector. If the error was either a correctable data error or an non-correctable data error, the flawed data is loaded into the sector buffer. The read does not terminate if the error was a correctable data error. If no error is detected, the cylinder, head, and sector registers are updated to point to the next sequential sector.

A read long may be executed by setting the long bit in command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine there has been any type of data error. Data bytes are 16 bit transfers and ECC bytes are 8 bit transfers.

12.3 Write Sector(s) - 3X

This command will write from 1 to 256 sectors as specified in the Task File beginning at the specified sector (sector count equal to 0 requests 256 sectors).

When the command register is written, the drive waits for the Host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive sets BSY and begins command execution.

If bits 2 and 3 are on, the command terminates with aborted command. An ID Not Found error is returned if incorrect task file parameters are passed.

If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes.

Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector writes set DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is reset and BSY is set immediately when the Host fills the sector buffer.

If an error occurs during a multiple sector write, it will terminate at the sector where the error occurs. The Task File indicates the location of the sector where the error occurred. The Host may then read the Task File to determine what error has occurred, and on which sector. If no error is detected, the cylinder, head, and sector registers are updated to point at the next sequential sector.

A write long may be executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer. The drive will not generate the ECC bytes itself for the write long command. Data byte transfers are 16 bits, ECC bytes are 8 bit transfers.

12.4 Verify Sectors - 4X

This command works exactly the same as the Read Sectors command except that no data is transferred. Up to 256 sectors will be read into the sector buffer and ECC bytes verified, beginning at the location specified by the task file.

When each sector has been verified, the Task File is updated but no data request or interrupt is set to indicate that the sector has been verified. When all sectors have been verified, an interrupt is generated to indicate that all sectors have been transferred. A value of 00 in the sector count register indicates that 256 sectors are to be verified.

Read look-aheads are enabled for this command.

12.5 Format Track - 5X

The purpose of the format command is to provide a means by which a defective sector may either be marked bad or reassigned.

This command has been used on other drives to do the low level formatting job of putting the header and creating the data fields for all tracks on the drive. It is not necessary to execute a format command prior to operating the drive on the Host PC because the drive is a hard sectored drive and all required low level formatting is done during the factory certification of the drive.

Conner supports the format command only to allow any sectors that become defective to be handled in a fashion required by different operating systems. It should be noted that the format command operates on one logical track at a time and that all sectors on that track are filled with zeroes.

There are two methods provided to handle defective sectors: mark the sector bad, or reassign the sector. When a sector is marked bad, the ID field of the sector is updated to indicate a bad block. Any time that sector is accessed thereafter, the drive will return bad block status in the error register. The second method, Assign, allows a spare sector on the drive to be used to replace the specified sector. Following this operation, the drive performance will be degraded slightly when the sector is accessed due to the drive automatically seeking to the new sector.

It is also possible to format a bad block good, and unassign an alternate. When a sector is unassigned, the spare sector that was used as the alternate cannot be reclaimed. It is therefore not correct to write a diagnostic that assigns and then unassigns alternates on a large scale, because the spare sectors will be lost.

The command is like a write command, i.e., the task file is written, the command register is written to begin the command, and the drive responds by activating Data Request in the status register. This indicates a request for 1 sectors (512 bytes) worth of data that is used to describe the operations to be performed on each sector of the track specified by the Task File. After the data is written to the Data Register, the drive analyzes the information for each sector and performs the requested action to each sector. When the command is complete, the drive raises Interrupt Request with ending status in the Task File.

The data in the sector buffer must conform to a specified format. There must be one word (two bytes) for each sector. The words must be contiguous and begin at the start of the sector.

Unlike some drives where the order of the words is used to determine the interleave, with the CP3024 the order of the words is not significant because the drive's interleave cannot

be changed. The most significant byte of each word must contain the sector number. The least significant byte must contain a descriptor byte that indicates what is to be done to each sector.

There are four possible descriptor bytes:

00_h	format sector good
80_h	format sector bad
40_h	assign this sector to an alternate location
20_h	unassign the alternate location for this sector

The drive will return an ID Not Found under the following conditions:

1) If there is a missing word for any sector on the track.
2) If the words are not contiguous from the start of the sector.
3) If there is more than one word per sector.
4) If the task file calls for an illegal cylinder and/or head register.

A utility program to handle defective sectors should provide some interface to obtain the defective sectors. The program should build a 512 byte block with a word for each sector for the track.

These words must be in the first contiguous words of the block. The most significant byte of each block should contain the sector number. Then the defective sectors descriptor byte should be set to either 80_h or 40_h depending on whether or not the sector is to be formatted bad or reassigned. All the remaining sectors should have a descriptor byte of 00, which says to format the sector good. Once the data byte block is

created, the format command can be executed by interfacing it to the BIOS.

Again, it is important to remember that all data on the track is lost. The drive formats to the logical track that is the power on reset default or the values issued by the last initialize drive parameters command.

12.6 Seek - 7X

This command initiates a seek to the track and selects the head specified in the Task File. The drive need not be formatted for a seek to execute properly.

When the command is issued, the drive sets BSY in the Status register, initiates the seek, resets BSY, and generates an interrupt. Only the cylinder register is valid for this command. The drive does not wait for the seek to complete before returning the interrupt. Seek complete will be set upon completion of the command. If a new command is issued to a drive while a seek is being executed, the drive will wait, with BSY active, for the seek to complete before executing the new command.

No checks are made on the validity of the Sector number in the Task File. The Error bit in the Status register and the ID Not Found bit in the Error register of the Task File will be set if an illegal cylinder number is passed.

12.7 Execute Drive Diagnostic - 90

This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests shall only be executed upon receipt of this command.

The drive sets BSY immediately upon receipt of the command. If the drive is a master, C/D jumpered, the drive performs the

diagnostic tests and saves the results. It then checks to see if a slave drive is present and waits up to 5 seconds for the slave to complete its diagnostics. If the slave successfully completes its diagnostics, it asserts -HOST PDIAG.

If the slave does not successfully complete its diagnostics, it sets the error register as follows. The master drive resets BSY, and generates an interrupt. The value in the error register should be viewed as a unique 8 bit code and not as the single bit flags defined previously. The interface registers are set to initial values except for the error register if error.

The table below details the codes in the error register and a corresponding explanation:

Error Code	Description
01	no error detected
03	sector buffer error
8x	slave drive failed [1]

[1] *If the slave drive fails diagnostics, the master drive shall "OR" 80h with its own status and load that code into the error register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive shall set bit 7 of the Error Register in the Task File to 0.*

12.8 Initialize Drive Parameters - 91

This command enables the host to set the head switch and cylinder increment points for multiple sector operations. The drive only activates translate mode if the sector count register contains 17 at the issuance of this command.

In the translate mode, the logical head, sector numbers, and cylinder number in the Task File will be translated to their native physical values as part of execution of the command. The sector head, and cylinder values in the Task File are not checked for validity by this command, therefore if they are invalid, no error will be reported until an illegal access is made by some other command.

Cylinder head increments on subsequent commands will occur after access of the maximum sector and maximum head specified by this command.

At power-up, the drive will default to translate mode, 17 sectors per track, 4 heads, and 615 cylinders. Upon receipt of the command, the drive sets BSY, saves the parameters, resets BSY, and generates an interrupt. To specify maximum heads, write 1 less than the maximum, e.g. write 4 for a 5 head drive. To specify maximum sectors, specify the actual number of sectors, e.g. 17 for a maximum of 17 sectors/track.

12.9 Read Multiple Command - C4

The read multiple command is identical to the read sectors operation but several sectors are transferred to the Host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block count on each sector. Long transfers are not permitted. The block count, which is the number of sectors to be transferred as block, is programmed by the set multiple mode command which must be executed prior to the read multiple command.

When the read multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block

transfer. The partial block transfer will be for N sectors, where

N = (sector count) modulo (block count)

If the read multiple command is attempted before the set multiple mode command has been executed or when read multiple commands are disabled, the read multiple operation will be rejected with an aborted command error.

Disk errors encountered during read multiple commands will be reported at the beginning of the block or partial block transfer, but DRQ will be set and the transfer will take place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks will only be transferred if the error was a correctable data error. All other errors will cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block. Read look-aheads are not active for this command.

12.10 Write Multiple Command - C5

The write multiple command performs similarly to the write sectors command except that the controller sets BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Several sectors are transferred to the Host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block, not on each sector. There is no IRQ prior to the first block transfer.

The block count, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command, which must be executed prior to the write multiple command. When the write multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested.

If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

N = (sector count) modulo (block count)

If the write multiple command is attempted before the set multiple mode command has been executed or when write multiple commands are disabled, the write multiple operation will be rejected with an aborted command error.

All disk errors encountered during write multiple commands will be reported after the attempted disk write of the block or partial block is transferred. The write operation will end with the sector in error, even if it was in the middle of a block. Subsequent blocks will not be transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

12.11 Set Multiple Mode - C6

This command enables the controller to perform read and write multiple operations and establishes the block count for these commands. Prior to command issuance, the sector count register should be loaded with the number of sectors per block. Block sizes supported are 1, 2, 4, 8, and 16.

Upon receipt of the command, the controller sets BSY and looks at the sector count register contents. If the register contents are valid and supported block count is supplied, that value is loaded for all subsequent read and write multiple commands and execution of these commands is enabled. Any unsupported block count in the register will result in an aborted command error and read and write multiple commands being disabled. If the sector count register contains 0 when the command is issued, read and write multiple commands will be disabled.

Once the appropriate action has been taken, the controller resets BSY and generates an interrupt. At power-up, or after a hardware or software reset, the default mode is read and write multiple disabled.

12.12 Power Commands - Ex

There are four power modes of operation for the drive, Read/Write, Idle, Standby, and Sleep Mode. They are explained below with the commands required to make them work.

Read/Write Mode: All drive circuitry is on.

Idle Mode: The drive is spinning but Read/Write circuitry is only turned on around each sector pulse.

Standby Mode: The drive is spun down and most analog circuitry is disabled, but the drive will accept commands from the interface.

Sleep Mode: All circuitry except the interface logic and the microprocessor circuitry is disabled. The microprocessor is stopped. The drive will only respond to the interface if it is issued a software or hardware reset. The host may read the interface Task File registers.

Commands E_h through E3, E5, and E6 constitute the power commands. The following table describes these commands:

COMMAND	DRIVE ACTION
$E0_h$	The drive enters STANDBY MODE immediately. To put a drive in Standby Mode, it is only necessary to write command E0 to the command register, $1F7_h$. This will cause the drive to spin down.
$E1_h$	The drive enters IDLE MODE immediately. To put a drive in Idle Mode, write command E1 to the command register, $1F7_h$. This will cause the drive to spin up if it is not spinning and have no effect if it is already spinning.
$E2_h$	The drive enters STANDBY MODE immediately. If the Sector Count register is non-zero then the Auto Power-Down feature is enabled and will take effect when the drive returns to IDLE MODE. If the Sector Count register is zero, then the Auto Power Down feature is disabled. To use this command, write the number of seconds, modulo 5 to the sector count register, $1F2_h$, and $E2_h$ to the command register, $1F7_h$. For example, to set an 80 second timeout write 10_h to $1F2_h$ and $E2_h$ to the command register at $1F7_h$. This will cause the drive to spin down immediately. It will not spin up until the next command that requires spin. After spinning up it will spin down after 80 seconds if no command is issued to the drive. The minimum time that the drive will accept is $0C_h$ or 60 seconds. For any value less than that, the drive will force 60 seconds.
$E3_h$	The drive enters the IDLE MODE immediately. If Sector Count register is non-zero, then the Auto Power-Down feature is enabled and will take effect immediately. If the Sector Count register is zero, then the Auto Power- Down feature is disabled. This works exactly as the Enable/Disable Auto Timeout Standby except that the drive will spin up if not spinning and remain spinning if already spinning.

COMMAND	DRIVE ACTION
$E5_h$	Read Power Mode Status. When command $E5_h$ is written to the command register, $1F7_h$, the drive will put FF_h in the sector count register, $1F2_h$ if it is in the idle mode, i.e. spinning or 00 in that register if it is not spinning, i.e. not spinning or spinning up.
$E6_h$	The drive enters the SLEEP MODE. When command $E6_h$ is written to the command register, $1F7_h$, the drive will spin down and turn itself off. It will not respond to the interface after that until it receives either an interface software or hardware reset after which it will spin up and be ready to accept commands. In this mode, the host may only read the interface task file registers.

All of the power commands, except command $E6_h$, will execute immediately and return the ending interrupt after the spin up/down sequence is initiated. Note that if the drive is already spinning (IDLE MODE) and a spin up command is issued from the host, the spin up sequence is not initiated. Similarly, if the drive is in the STANDBY MODE and the host issues a spin down command, the spin down sequence is not initiated. Return of the ending interrupt does not mean that the drive has fully transitioned to the desired operating mode. The sleep command is the exception. In command $E6_h$, the drive is spun down and when it is stopped, the drive returns the ending interrupt and the SLEEP MODE begins.

When enabling the Auto Power-Down feature, the value in the Sector Count register specifies the number of 5 second increments for the timeout value. If the drive does not receive a command within the specified time, the drive will enter the STANDBY MODE. The minimum timeout value is 60 seconds which means the smallest value for the Sector Count register is 12 when enabling the Auto Power-Down feature. If a number between 1 and 11 inclusive is specified in the Sector Count register, a value of 12 is used. The maximum allowable timeout value is 1100 seconds, or 18.3 minutes, resulting in a

maximum Sector Count register value of 220. If a number greater than 220 is specified, a value of 220 is used.

Assertion of Host Reset will only affect the current state of the SLEEP MODE. If the drive is in SLEEP MODE and Host Reset is asserted, the drive wakes up into STANDBY MODE. Note that the drive will not return to the state it was in when the host issued the sleep command.

The default power-on condition of the drive is IDLE MODE.

12.13 Read Buffer - E4

The read buffer command allows the Host to read the current contents of the drive's sector buffer. Only the command register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a read operation, set DRQ, reset BSY, and generate an interrupt. The Host may then read up to 512 bytes of data from the buffer.

12.14 Write Buffer - E8

The write buffer command allows the Host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the command register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a write operation set DRQ, and reset BSY. The Host may then write up to 512 bytes of data to the buffer.

12.15 Identify Drive - EC

The identify command allows the Host to receive parameter information from the drive. When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The Host may then read the information out of the sector buffer.

The parameter words in the buffer are arranged as follows:

- all reserved bits or words should be zeroes
- all numbers are given in hexadecimal format right justified
- all reserved words are zero

Word 00	A constant 0A5A
Word 01	Number of fixed cylinders
Word 02	Number of removable cylinders
Word 03	Number of heads
Word 04	Number of unformatted bytes/physical track
Word 05	Number of unformatted bytes/sector
Word 06	Number of physical sectors/track
Word 07	Number of bytes in the intersector gaps
Word 08	Number of bytes in the sync fields
Word 09	0000
Word 10-19	Serial number
Word 20	Controller type 0003 dual ported multiple sector buffer with LOOK AHEAD READs
Word 21	Controller buffer size in 512 byte increments
Word 22	Number of ECC bytes passed on read/write long commands
Word 23-26	Controller firmware revision
Word 27-46	Model Number
Word 47	Number of sectors/interrupt (0 = does not support > 1)
Word 48	Double word transfer flag (0 = not capable, 1 = capable)
Word 49-255	Reserved

12.16 Cache On/Off - EF

This command provides capability to enable or disable the LOOK AHEAD READ capability. "AA_h" in the write precomp register enables LOOK AHEAD READs. Any other value in the write precomp register will result in an aborted command error. The default state on power up or reset is LOOK AHEAD READ enabled. "55_h" disables LOOK AHEAD READs.

13.0 Operations Description

This section describes operations that span several of the commands that were covered in the preceding sections.

13.1 Reset

A RESET condition will set the drive busy, allowing the drive to perform the proper initialization required for normal operation.

A RESET condition can be generated in four ways. There are two hardware resets, one from the Host (- HOST RESET) and one from the drive power sense circuitry. These are set high when the system and the drive respectively acknowledge good power. The other two resets are software generated. The Host can write to the digital output register and set the reset bit. The Host software reset condition will persist until the reset bit is written to a zero. The drive microprocessor can set reset through a write to a register. The drive processor reset is valid for one cycle and like all other resets, is OR'ed together to generate the signals that initialize the hardware.

Once the reset has been removed and the drive has been re-enabled, with BSY still active, the drive will perform any necessary hardware initialization, clear any previously

programmed drive parameters and revert to the defaults, load the Task File registers with their initial values, and then reset BSY. No interrupt is generated when initialization is complete.

The initial values (hex) for the Task File registers are as follows:

Error Register	01
Sector Count	01
Sector Number	01
Cylinder Low	00
Cylinder High	00
Drive/Head Register	00

13.2 Busy Operation

The latch holding "busy" is set in a number of ways. A RESET condition described above is one way. Another method occurs when the Host issues a command. For a read type command, the register is clocked busy on the Host write of the command register. The disk controller and microprocessor prepare the data to return and set the drive not busy to allow the Host access of the data requested.

On a write type command, the command is issued, setting the IO16 enable and Data Request. But, Busy is not set until the data to be written is put into the RAM buffer. This is accomplished by setting the Busy flip flop on the condition of the buffer becoming full in write mode and not being the last transfer. Write type commands include Write Sector(s), Format, and Write Sector Buffer.

In addition, the drive microprocessor has the ability to set/reset the Busy flip flop. This is the only method by which the Busy latch can be cleared. This means that the only way a drive can

respond properly to a command is for the drive microprocessor to be active. When Busy is active, the drive has read and write access to the Task File registers. The Host can only read the Status Register and Alternate Status Register of the Task File. Any attempted "Host" read of a Task File register while Busy is active results in reading the Status register.

When Busy is inactive, the Host has read and write access to all Task File registers.

13.3 Data Retry Algorithm

When an ECC error is detected in the data field during a read operation, the following retry algorithm is used:

Step 1	read retry
Step 2	read retry
Step 3	read retry
Step 4	apply ECC to Step 3
Step 5	read retry with +65 uin offset
Step 6	apply ECC to Step 5
Step 7	read retry
Step 8	apply ECC to Step 7
Step 9	read retry with - 65 uin offset
Step 10	apply ECC to step 9
Step 11	read retry
Step 12	read retry
Step 13	read retry
Step 14	read retry
Step 15	read retry
Step 16	read retry

In the event of a hard error, steps 1-16 are repeated eight times for a total of 128 retries. Allowing 17 msec for each read retry and 75 msec for each ECC correction, this is a total time of 4.0 seconds (17 msec * 12 * 8 + 75 msec * 4 * 8 = 4032 msec) to

return a non-recoverable error condition to the host. With the exception of disabling retries (i.e. retry count = 0), the retry count of 128 is currently not changeable.

When the Read/Write heads are switched or a seek is completed, the drive will attempt an off track read when less than 200 uins from the center of the track. If this attempt is successful, 17 msecs of latency is saved and seek performance of the drive will exceed the specification. When this attempt is not successful, the drive will read the sector on the next pass as in a normal read operation (100 uins) and the seek specification is met.

13.4 Header Retry Algorithm

When an ECC error is detected while reading the header field, 20 read retries are attempted before a header error is returned to the host. If a header is successfully read before the 20 retries are completed, then the header retry counter is reset and the data field is processed. For a hard error in the header field, the total amount of time for 20 retries is 0.34 seconds (17 msec * 20 = 340 msec). Header retries can not be disabled from the interface, nor can the header retry count be changed.

14.0 Error Reporting

In general, errors are detected in the following fashion by the drive microprocessor. At the start of the execution of the command, the command register is checked for conditions that would lead to an aborted command. Then the operation is attempted. Any subsequent error terminates the command at the point that it is discovered. The errors that are valid for each command are summarized in the following matrix. Any subsequent error terminates the command at the point that it is discovered.

The following abbreviations are used in the matrix, where a V means the error type is valid for this command:

V means error type is valid for this command:	
BBK	bad block detected
UNC	non-correctable data error
IDNF	requested ID not found
ABRT	aborted command error
TKO	track 0 not found error
DRDY	disk drive not ready detected
DWF	disk drive write fault detected
DSC	disk drive seek complete not
CORR	detected corrected data error
ERR	error bit in the status register

	BBK	UNC	IDNF	ABRT	TKO	DRDY	DWF	DSC	CORR	ERR
Recalibrate				V	V	V	V	V		V
Read Sector	V	V	V	V		V	V	V	V	V
Read Long	V		V	V		V	V	V		V
Write Sector	V		V	V		V	V	V		V
Write Long	V		V	V		V	V	V		V
Read Verify	V	V	V	V		V	V	V	V	V
Format Track			V	V		V	V	V		V
Seek			V	V		V	V	V		V
Execute Drive Diagnostics				V						V
Initiator Drive Parameters				V						V
Read Multiple	V	V	V	V		V	V	V	V	V
Write Multiple	V		V	V		V	V	V		V
Set Multiple				V						V
Read Buffer				V						V
Write Buffer				V						V
Identify Drive				V						V
Cache On/Off				V						V

The following errors are valid upon issuing an invalid command code:

	BBK	UNC	IDNF	ABRT	TKO	DRDY	DWF	DSC	CORR	ERR
Invalid Command Code					V					V

Appendix: Evaluation Adapter Board

Introduction

In order to facilitate evaluation and aid those manufacturers interested in quickly getting the CP3024 drive running, Conner Peripherals has developed an adapter board to be used in conjunction with the drive on an AT or equivalent system. The drive requires no special driver program as it works with the existing AT BIOS or equivalent. It is hoped that the interface will be incorporated into the motherboard of the AT device or on some other multi-function adapter. The artwork and Bill of Materials are available upon request.

Description

The AT Task File Interface is a set of registers that allows execution of a set of commands via the Host Computer BIOS. The CP3024 drive implements the Task File on the drive. The adapter board buffers the drive from the Host and does the address decode.

The adapter card decodes the host I/O addresses IF0-1F7 and 3F6- 3F7. These addresses are set aside for disk drive use in the AT BIOS. The drive will respond to the commands issued by the BIOS.

The floppy drive also responds to address 3F7, bit 7. The adapter card does not drive this bit.

For CP3024, always jumper E4.

Requirements

The following are required to run the drive:

- Host adapter board
- CP3024 drive
- 40 pin flat cable

Installation of the Drive and Adapter Card

1. Remove power to the computer.

2. If another hard disk controller is installed, it is necessary to prevent it from responding to the addresses 1F0-7 and 3F6-7. It is also necessary to ensure that the controller is electrically disconnected or tri-stated from IRQ14 of the motherboard bus. This may be done either by removing the board, by electrically disconnecting the signals from the interface, or by setting the jumpers of the board to disable the hard disk controller.

3. Insert the board into any available card slot.

4. Configure the host adaptor for the correct configuration of your computer BIOS.

Jumpers	
E1	Always not installed
E2	Always installed
E3	Always not installed
E4	Always installed

5. Connect power to the CP3024.

6. Run the DOS F disk program to establish DOS partitions.

   NOTE: DOS 3.2 and below have limitations of 32 megabytes unless a software utility is used to overcome this.

7. Run the DOS format program by typing "Format C:/S". The volume may be named with the addition of the "/V". The format will be completed and the system transferred if the "/V" option was used. The system will ask for a volume name.

8. Files can then be copied to the C drive from the floppy.

9. When the system is rebooted, the system should boot from the hard drive (Drive C) if the floppy is removed.

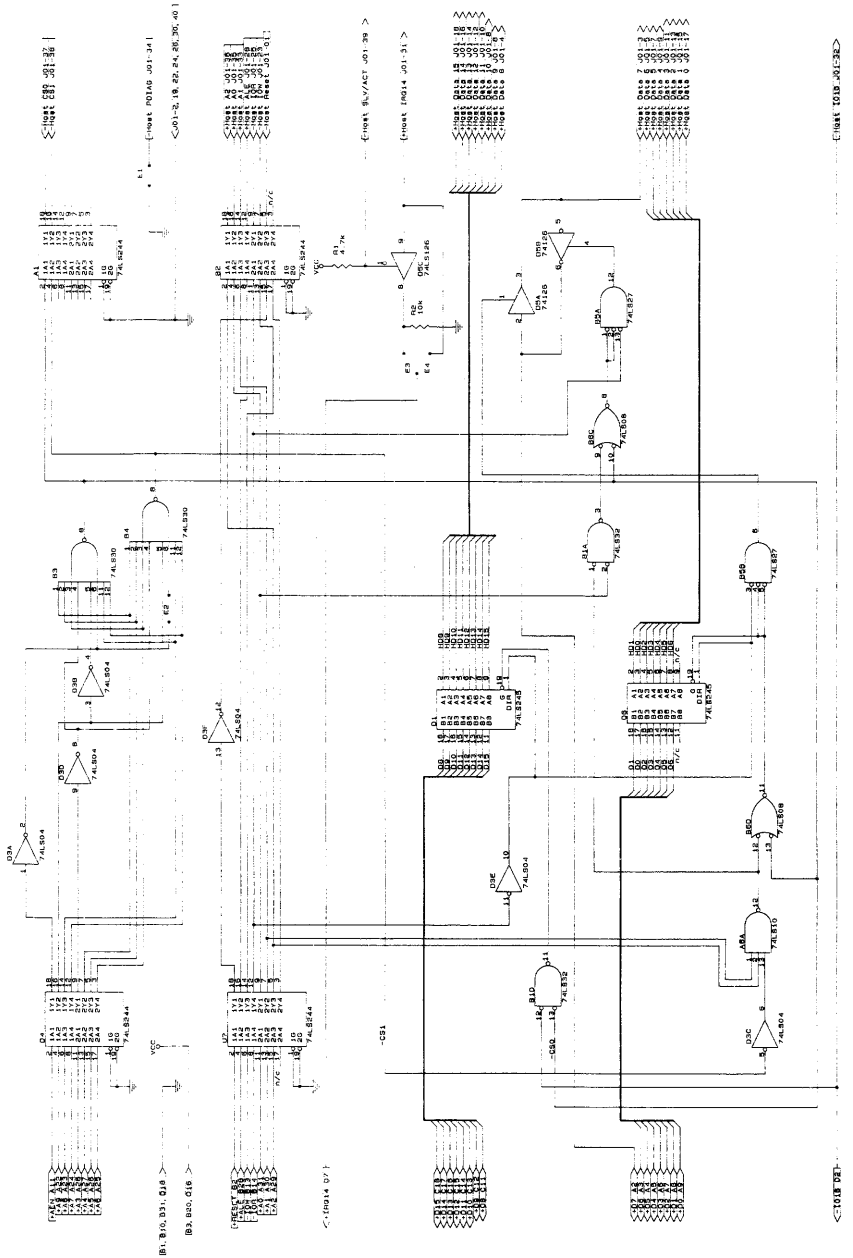


Figure A-1 AT Adapter Schematic

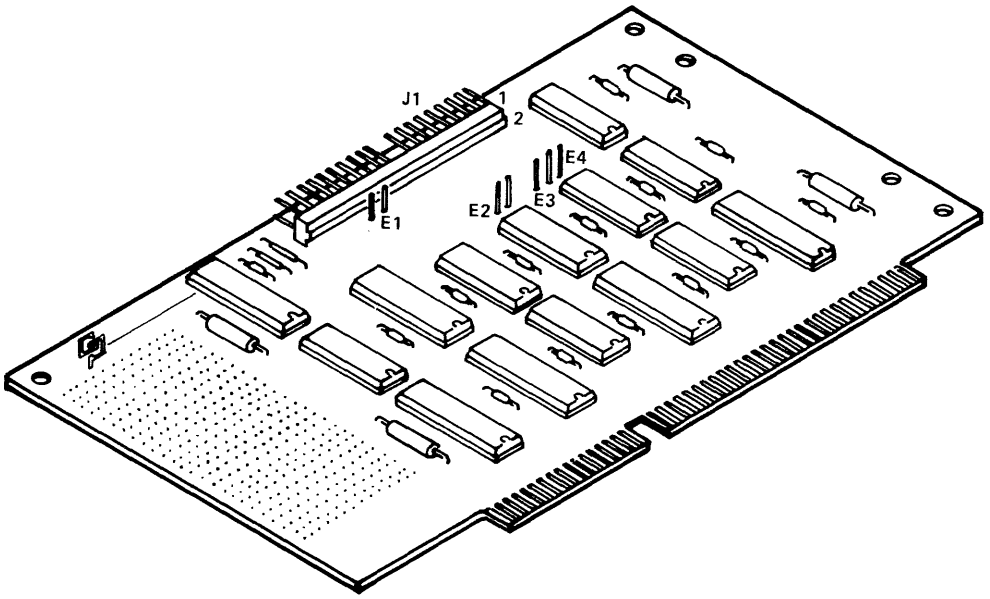


Figure A-2 AT Adapter Card Layout

System Board I/O							
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	N/C	B01	GND	C01	N/C	D01	N/C
A02	D7	B02	RST DRV	C02	N/C	D02	- IO16
A03	D6	B03	+5V	C03	N/C	D03	N/C
A04	D5	B04	N/C	C04	N/C	D04	N/C
A05	D4	B05	- 5V	C05	N/C	D05	N/C
A06	D3	B06	N/C	C06	N/C	D06	N/C
A07	D2	B07	- 12V	C07	N/C	D07	IRQ14
A08	D1	B08	N/C	C08	N/C	D08	N/C
A09	D0	B09	+12V	C09	N/C	D09	N/C
A10	N/C	B10	GND	C10	N/C	D10	N/C
A11	AEN	B11	N/C	C11	D8	D11	N/C
A12	N/C	B12	N/C	C12	D9	D12	N/C
A13	N/C	B13	- IOW	C13	D10	D13	N/C
A14	N/C	B14	- IOR	C14	D11	D14	N/C
A15	N/C	B15	N/C	C15	D12	D15	N/C
A16	N/C	B16	N/C	C16	D13	D16	+5V
A17	N/C	B17	N/C	C17	D14	D17	N/C
A18	N/C	B18	N/C	C18	D15	D18	GND
A19	N/C	B19	N/C				
A20	N/C	B20	N/C				
A21	N/C	B21	N/C				
A22	A9	B22	N/C				
A23	A8	B23	N/C				
A24	A7	B24	N/C				
A25	A6	B25	N/C				
A26	A5	B26	N/C				
A27	A4	B27	N/C				
A28	A3	B28	BALE				
A29	A2	B29	+5V				
A30	A1	B30	N/C				
A31	A0	B31	GND				

Problems

If at power on, the drive spins up but is ignored by the system (indicated by the system taking a long time to boot), it is possible the IRQ14 is not becoming active. Check to make sure that the interrupt is isolated electrically from the original hard disk controller's IRQ13.

If at power on, the drive does not ever spin up or does not spin up until after the computer completes power on, it is possible that RESET is either continually active or is electrically connected to some other signal.

If when taking a directory it is inaccurate or does not change, it is possible that the adapter board is connected to bit 7 when address 3F7 is read.

If the computer completes its power on sequence before the drive is up completely and subsequently gets a 17xx error of some sort, and if a subsequent warm boot is successful, it is possible the BIOS is expecting a different status at power on before the system is ready. Either delay the power on sequence or change the BIOS to expect a 00 status before the drive become ready.

Care must be exercised with the routing of the power and signal cables. They should not be routed next to the drive PCB or other high frequency or large current switching signals. Improper drive operation can result from improper cable routing.